参考資料

TI Designs: TIDA-01568
アプリケーション・プロセッサ用の12mm×12mm、5レールの電源シーケンシングのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、アプリケーション・プロセッサ、または高性能の制御プラットフォーム用の、検証済みでコスト競合力のある電源シーケンシング・ソリューションを紹介します。このソリューションは5つの異なる電源レールをサポートし、最適化によりレイアウト面積は12mm×12mmです。また、このデザインは各種の入力コンデンサと、プロセッサの様々な要件に対応するため、遅延時間を調整でき、各レールの電圧レベルを個別に再構成可能です。

このリファレンス・デザインはTIのAM335xプロセッサとWiLink 8™モジュールWL1837MODを基礎として、高性能の制御プラットフォームを構築することで、スマート家電や自動化アプリケーションにおいてより多くの機能と優れた性能を実現します。

リソース

TIDA-01568	デザイン・フォルダ
TLV62568/9	プロダクト・フォルダ
LM3881	プロダクト・フォルダ
TLV803	プロダクト・フォルダ
AM3358	プロダクト・フォルダ
WL1837MOD	プロダクト・フォルダ

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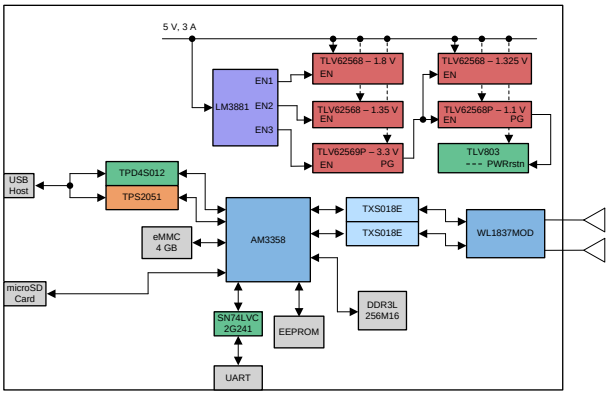
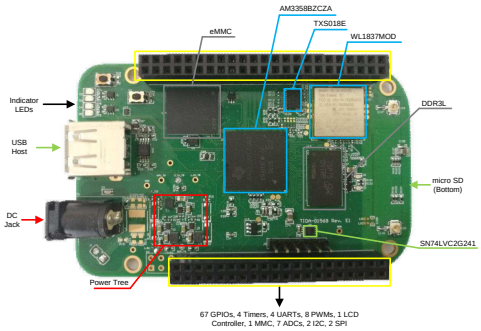


特長

- 検証済みの電源シーケンシング・ソリューション
- 遅延時間を構成可能なオプション
- さまざまな負荷状況において、制御外の電源オフに対しても正しい電源オン/オフ・シーケンスを実行
- 重負荷でも軽負荷でも電力ツリーの効率を維持(V_{IN}: 5V、I_{load}: 10mA)
  - 91%、3.3V
  - 84%、1.8V
  - 81%、1.35V
  - 81%、1.325V
  - 80%、1.1V
- 小さなレイアウト面積の電源: 12mm×12mm以下
- ARM® Cortex®-A8ベースのコアと3Dグラフィックによりユーザー・インターフェイスを拡張し、柔軟なペリフェラルを実現 - Sitara™AM335x
- 産業用デュアル・バンド、2×2 MIMO Wi-Fi®、Bluetooth®、Bluetooth Smartモジュール - WiLink WL183xMOD

アプリケーション

- 冷蔵庫
- 洗濯乾燥機
- 壁面型オーブン
- ロボット型掃除機
- ヒューマノイド(ヒト型ロボット)
- ヒューマン・マシン・インターフェイス(HMI)



1 System Description

Smart appliances offer new features and high performance that have been integrated into appliances gradually, such as voice recognition, wireless connectivity, advanced Human Machine Interface (HMI), advanced interaction, and so forth. Processors with high performance and wireless connectivity devices are widely used in smart appliance control platforms. TI's Sitara™ AM335x family and WiLink8™ family are ideal choices for control systems in smart appliance .

The processors or digital devices usually require different power supply voltages, mixed together on the board with the correct power sequence. Power supply voltages turned on with an incorrect power sequence can cause reliability problems such as characteristics degradation, inrush currents, and latch-up conditions. The challenge is how to design the power tree with correct sequencing without trading off factors such as power tree architect, efficiency, cost, size, and more.

This reference design provides a 5-rail multi-channel power sequencing solution. The small form factor of 12 mm × 12 mm is achieved by using the TLV62568/9, offering 1.5-MHz switching frequency in a small package of SOT-563. The correct power sequence is achieved by using the LM3881, offering three open-drain output flags with individual time delays to avoid latch conditions or large inrush currents that can affect the reliability of the system. This power sequencing solution also supports the uncontrolled power off by using a supervisor of the TLV803 to monitor the input voltage rail, while also generating the power reset signal to manage the power up and power down sequence.

The test report evaluates this power sequencing platform, powering the AM335x and WL1837MOD with all necessary components as a system control platform such as: 4GB eMMC, 256M × 16-Bit DDR3L, microSD™ Card, EEPROM, and USB host. The test result provides the details of the power up and power down sequence, and the typical characters of DC-DCs.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage range	3.3 V to 5.5 V
Input power	15 W
Output voltage rails	3.3 V / 2 A, 1.8 V / 1 A, 1.1 V / 1 A 1.35 V / 1 A, 1.325 V / 1 A
Voltage ripple	< 5% at 3.3 V, <5% at 1.8 V, <4% at 1.1 V, <5% at 1.35 V, <4% at 1.325 V
Power up/down Sequence	Meet requirements of the AM335x at "RTC Feature Disabled" mode and WL183xMOD's requirements
Efficiency at 5 V_{IN}	>95% at 3.3 V, >90% at 1.8 V, >87% at 1.1 V >89% at 1.35 V, >89% at 1.325 V
Efficiency at 10 mA, 5 V_{IN}	>91% at 3.3 V, >84% at 1.8 V, >80% at 1.1 V >81% at 1.35 V, >81% at 1.325 V
Specification of board	86 mm × 54 mm (12 mm × 12 mm for power part), 6 layer
Operating ambient	–40°C to 85°C

2 System Overview

2.1 Block Diagram

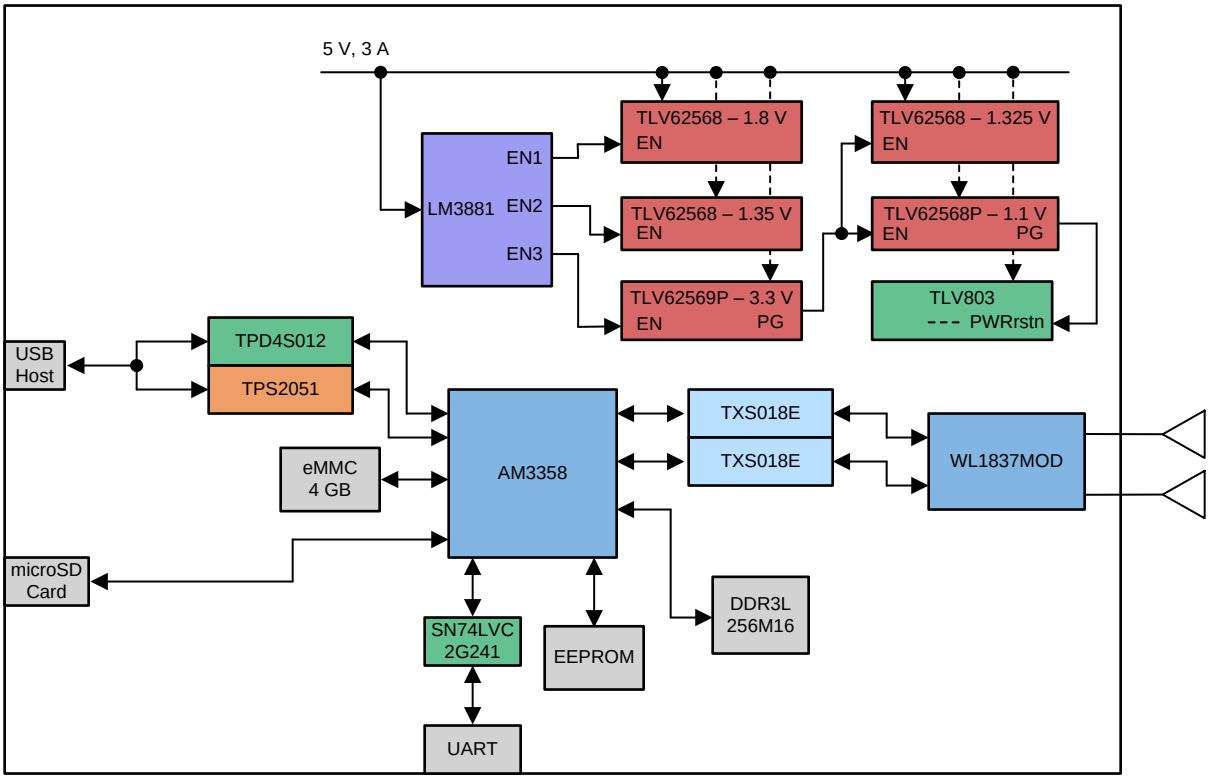


図 1. TIDA-01568 Block Diagram

2.2 Design Considerations

Before choosing or designing a power supply solution for application processors with a high level of complexity, the hardware engineer must understand the system power needs, then determine the architecture of the power tree to trade off efficiency, size, and cost.

2.2.1 Power Rails Requirements of the System

The considerations for power rails requirements consist of:

- Number of different power rails
- Load current of each rail
- Voltage rating
- Architecture of power tree

表 2 shows the basic power requirements of this system.

表 2. Basic Power Requirements

Sequence	Power Supply	Device	Nominal Rating	Max Current [mA]
4-up, 1-down	VDD_CORE	AM335x	1.1 V ± 4%	400
4-up, 1-down	VDD_MPU	AM335x	1.325 V ± 4%	1000
1-up, 4-down	VIO	WL1837MOD	1.62 ~ 1.95	< 400
1-up, 4-down	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDS_PLL_DDR, VDDS_PLL_MPU, VDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1, VDDS	AM335x	1.8 V ± 5%	590
3-up, 2-down	VDDA_USB0, VDDA_USB1, VDDSHVx	AM335x	3.3 V ± 5%	370
3-up, 2-down	VBAT	WL1837MOD	3.3 V	850
3-up, 2-down	V_NAND	NAND Flash	3.3 V	80
3-up, 2-down	Other Peripheral	Board	3.3 V	< 500
2-up, 3-down	VDDS_DDR, V_DDR3L	DDR3L	1.35	250

In this system, the processor device on the board is the AM3358BZCZA. The operating performance points (OPPs) have been configured for "Nitro", which means the VDD_MPU should be 1.325 V, enabling a 1-GHz speed grade. The recommended operating conditions are showed in Section 5.5 of the AM335x data sheet. The power consumption summary for each terminal is showed in Section 5.6 of the AM335x data sheet.

2.2.2 Power Sequencing Requirements of the System

Power sequencing requirements are another key consideration. The operation mode of this system has been set as RTC Feature Disable, the details of power sequencing requirements are shown in Figure 6-6 of AM335x data sheet. In this mode, consider the configuration for each pin related to RTC functionality when designing the schematic. The use case scenarios are provided in the AM335x_Schematic_Checklist.

図 2 shows the power sequence requirements of the AM335x for this system.

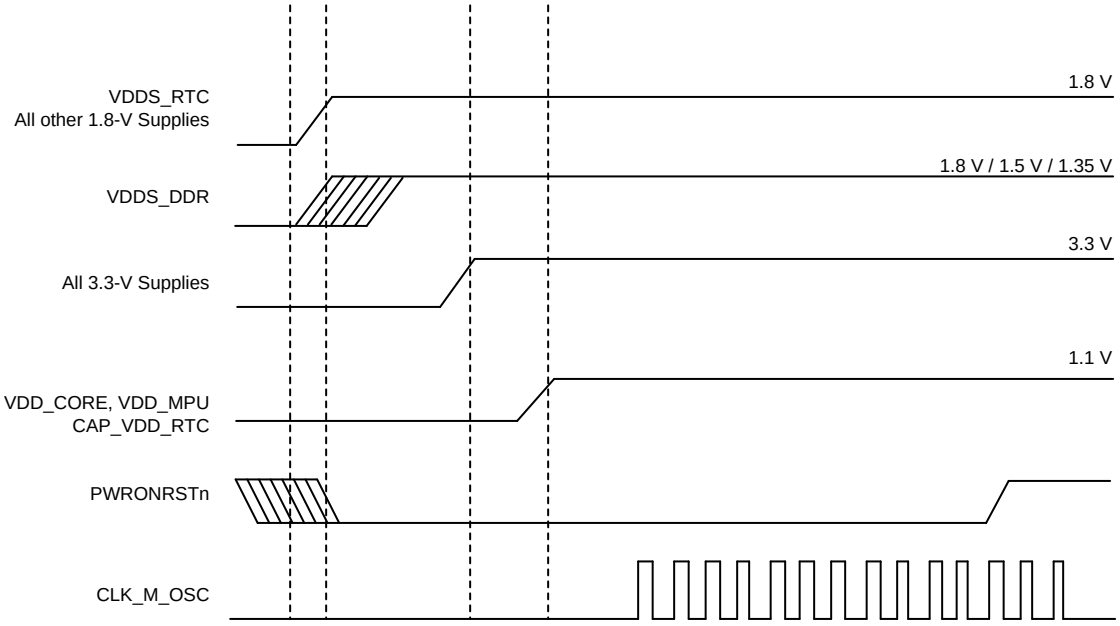


図 2. Power Supply Sequencing for AM335x with RTC Feature Disabled

The requirements for the power-up sequencing:

1. VDDS_RTC and all other 1.8-V supplies ramp up.
2. VDD_DDR, which has been set at 1.35 V, ramp up at second order.
3. All 3.3-V supplies ramp up at third order.
4. VDD_CORE at 1.1 V and VDD_MPU at 1.325 V ramp up after the 3.3-V rail goes high and at fourth order.
5. PWRONRSTn ramps up after all other rails go high.

The requirements for the power-down sequencing:

1. The PWRONRSTn input terminal should be taken low, which stops all internal clocks before the power supplies are turned off. All other external clocks to the device should be shut off.
2. The preferred method to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that was ramped up first should be the last one to be ramped down. This ensures there are no spurious current paths during the power-down sequence. The VDDS power supply must ramp down after all 3.3-V VDDSHVx [1-6] power supplies.
3. If it is desired to ramp down VDDS and VDDSHVx[1-6] simultaneously, it should always be ensured that the difference between VDDS and VDDSHVx[1-6] during the entire power-down sequence is < 2 V. Any violation of this could cause reliability risks for the device. Further, TI recommends maintaining VDDS ≥ 1.5 V, as all the other supplies fully ramp down to minimize in-rush currents.
4. If none of the VDDSHVx [1-6] power supplies are configured as 3.3 V, the VDDS power supply may ramp down along with the VDDSHVx [1-6] supplies, or after all the VDDSHVx [1-6] supplies have ramped down. TI recommends maintaining VDDS ≥ 1.5 V, as all the other supplies fully ramp down to minimize in-rush currents.

The VBAT and VIO for the WL183xMOD do not have a strict requirement on which can come up first. However, there are strict requirements for the Enable and Clock power sequences, which are outlined on Section 5.22.2 of the WL18x7MOD data sheet .

2.2.3 Uncontrolled Power Off

Uncontrolled power off is a situation when the power supply is removed unexpectedly, meaning the power supply rails' discharge time depends on the input capacitor and load current. The corresponding situation is controlled power off, which means the power off is controlled by software, achieved by connecting the processor's power management pin to the power sequencing controller's enable pin.

In an uncontrolled power-off situation, the discharging time is short and may cause the power-down sequence to be out of order. The most efficient method is to use a supervisor to monitor the input voltage, and generate the sudden flag indicating power off occurred.

In this design, the supervisor monitors the input voltage rail. When the input voltage rail ramps down, the output of supervisor -- POWERONRSTn goes low, which disables the main oscillator, reduces the load current, and increases the discharge time.

2.2.4 12-V Input Voltage Rail

The architecture of the power tree in this design is also scalable for a 12-V input power supply. 図 3 and show this input voltage rails.

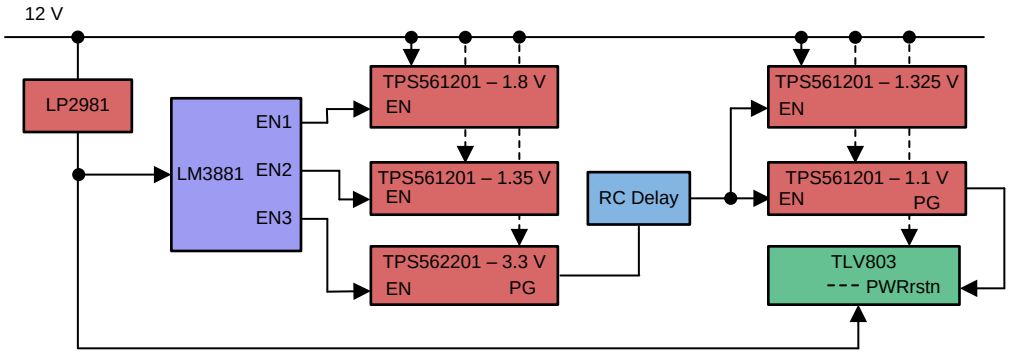


図 3. Power Sequencing Platform Diagram at 12-V Input Voltage Rail

An extra LDO and RC delay circuit should be added in the new architecture of the power tree with the 12-V input voltage rail. The LDO provides power for the sequencer, and the supervisor monitors the LDO's output voltage, which represents the input voltage rail's change.

2.3 Highlighted Products

For more information on each of the devices listed below, see their respective product folders at www.ti.com.

2.3.1 TLV62568/9

This reference design selected the TLV62568 with a 1-A output current and the TLV62569P with a 2-A output current.

The TLV62568/9 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device typically operates at a 1.5-MHz frequency pulse width modulation (PWM), at moderate to heavy load currents. Based on the VIN/VOUT ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

図 4 shows the functional block diagram of the TLV62568, and as a reference diagram for the TLV62569.

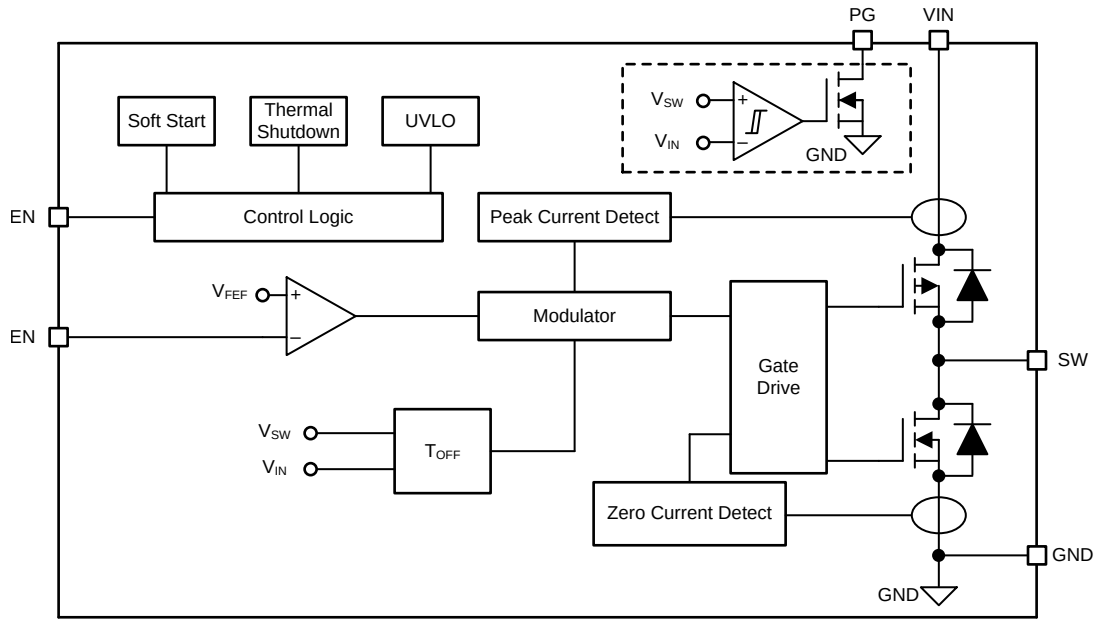


図 4. TLV62568 Functional Block Diagram

Features:

- Up to 95% Efficiency
- Low R DS(ON) Switches 150 mΩ / 100 mΩ
- 2.5-V to 5.5-V Input Voltage Range
- Adjustable Output Voltage from 0.6 V to VIN
- Power Save Mode for Light Load Efficiency
- 100% Duty Cycle for Lowest Dropout
- 35-µA Operating Quiescent Current
- 1.5-MHz Switching Frequency
- Power Good Output
- Over Current Protection
- Internal Soft Startup
- Thermal Shutdown Protection
- Available in SOT Package
- Pin-to-Pin Compatible with TLV62569

2.3.2 LM3881

The LM3881 Simple Power Sequencer provides a simple solution for sequencing multiple rails in a controlled manner. An established clock signal facilitates control of the power up and power down of three open-drain FET output flags. These flags permit a connection to the shutdown or enable pins of the linear regulators or switching regulators to control the operation of the power supplies. This allows the design of a complete power system without the concern of large inrush currents or latch-up conditions that can occur during an uncontrolled startup. An invert (INV) pin reverses the logic of the output flags. This pin should be tied to a logic output high or low, and not be allowed to remain an open circuit. The following sections assume that the INV pin is held low such that the flag output is active high.

図 5 shows the functional block diagram of the LM3881.

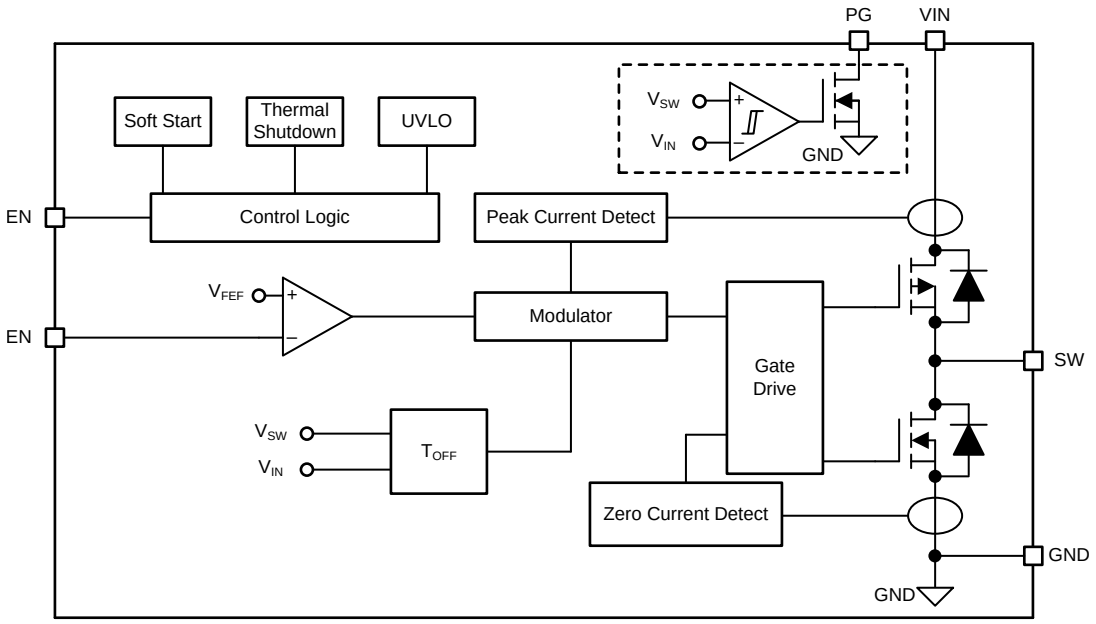


図 5. LM38881 Functional Block Diagram

Features:

- Easy Method to Sequence Rails
- Power-Up and Power-Down Control
- Tiny Footprint
- Low Quiescent Current of 80 µA
- Input Voltage Range of 2.7 V to 5.5 V
- Output Invert Feature
- Timing Controlled by Small Value External Capacitor

2.3.3 TLV803

The TLV803 family of supervisory circuits provides circuit initialization and timing supervision. The TLV853 and TLV863 are both functionally equivalent to the TLV803. These devices output a logic low when VDD drops below the negative-going threshold voltage (VIT–). The output, RESET, remains low for approximately 200 ms after the VDD voltage exceeds the positive-going threshold voltage (VIT– + Vhys). These devices are designed to ignore fast transients on the VDD pin.

図 6 shows the functional block diagram of the TLV803.

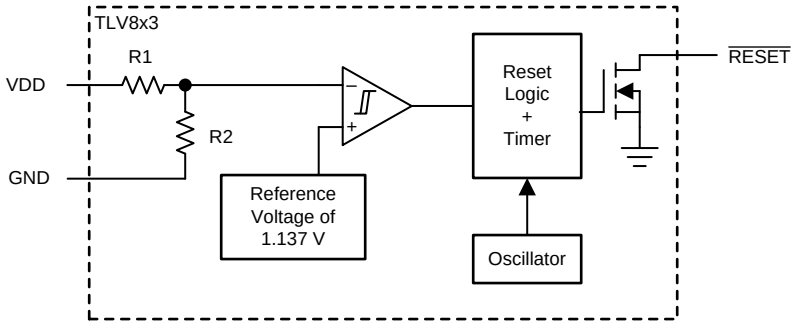


図 6. TLV803 Functional Block Diagram

Features:

- 3-Pin SOT23 Package
- Supply Current: 9 µA (Typical)
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V
- Power-On Reset Generator with Fixed Delay Time of 200 ms
- Temperature Range: –40°C to +125°C
- Open-Drain, RESET Output

2.3.4 AM335x

The AM335x microprocessors, based on the ARM Cortex-A8 processor, are enhanced with image, graphics processing, peripherals, and industrial interface options such as EtherCAT and PROFIBUS. The devices support high-level operating systems (HLOS). Linux® and Android™ are available free of charge from TI.

The microprocessor unit (MPU) subsystem is based on the ARM Cortex-A8 processor and the PowerVR SGX™ Graphics Accelerator subsystem provides 3D graphics acceleration to support display and gaming effects.

The PRU-ICSS is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, and others. Additionally, the programmable nature of the PRU-ICSS, along with its access to pins, events, and all system-on-chip (SoC) resources, provides flexibility in implementing fast, real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of SoC.

図 7 shows the functional block diagram of the AM335x.

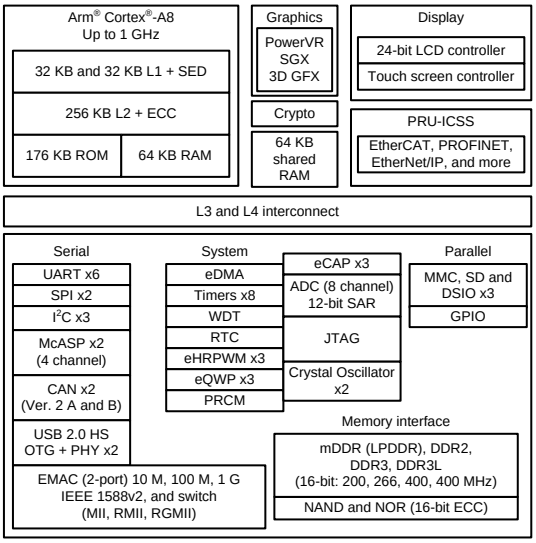


図 7. AM335x Functional Block Diagram

2.3.5 WL1837MOD

The certified WiLink 8 module from TI offers high throughput and extended range, along with Wi-Fi and Bluetooth coexistence (WL1837MOD only) in a power-optimized design. The WL18x7MOD is a Wi-Fi, dual-band, 2.4- and 5-GHz module solution with two antennas supporting Industrial temperature grade. The device is FCC, IC, ETSI/CE, and TELEC certified for AP (with DFS support) and client. TI offers drivers for high-level operating systems, such as Linux and Android. Additional drivers, such as WinCE and RTOS, which includes QNX, Nucleus, ThreadX, and FreeRTOS, are supported through third parties.

図 8 shows the functional block diagram of the WL1837MOD.

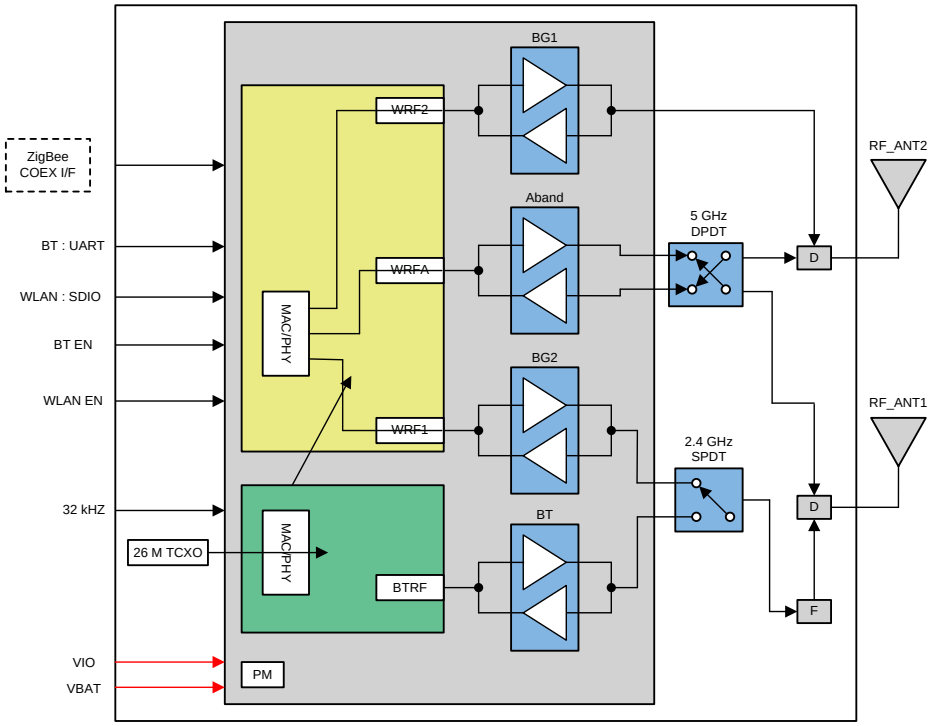


図 8. WL1837MOD Functional Block Diagram

2.4 System Design Theory

2.4.1 Power Tree Architecture

This design provides an efficient power tree architecture, as shown in 図 9. The input voltage rail of 5 V is configured as the power supply for each part; power-up sequence and power-down sequence are divided into 5 orders, as shown in 2.2.2. The power sequence controller is achieved by a sequencer and a supervisor. The sequence order of VDD_MPU and VDD_CORE is achieved by leveraging the 3.3-V converter's power good signal.

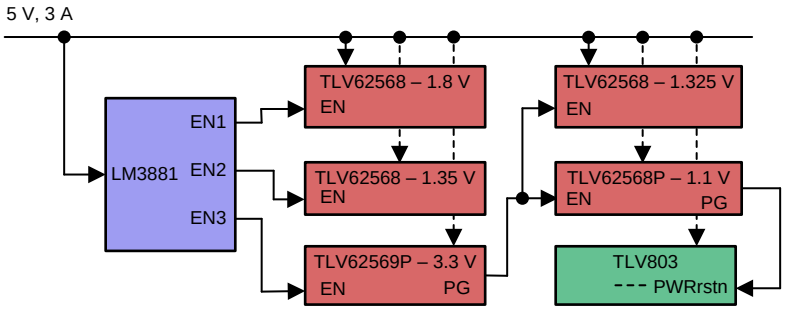


図 9. Power Sequencing Platform Diagram

2.4.2 Power Sequencing Solution

The TLV62568 and TLV62569 are chosen as the converters in this power tree, and the TLV62568P and TLV62569P are the versions with the power good feature. The LM3881 is chosen as the sequencer in this power tree, and the TLV803 is chosen as the supervisor. 図 10 shows the schematic of this power sequencing solution.

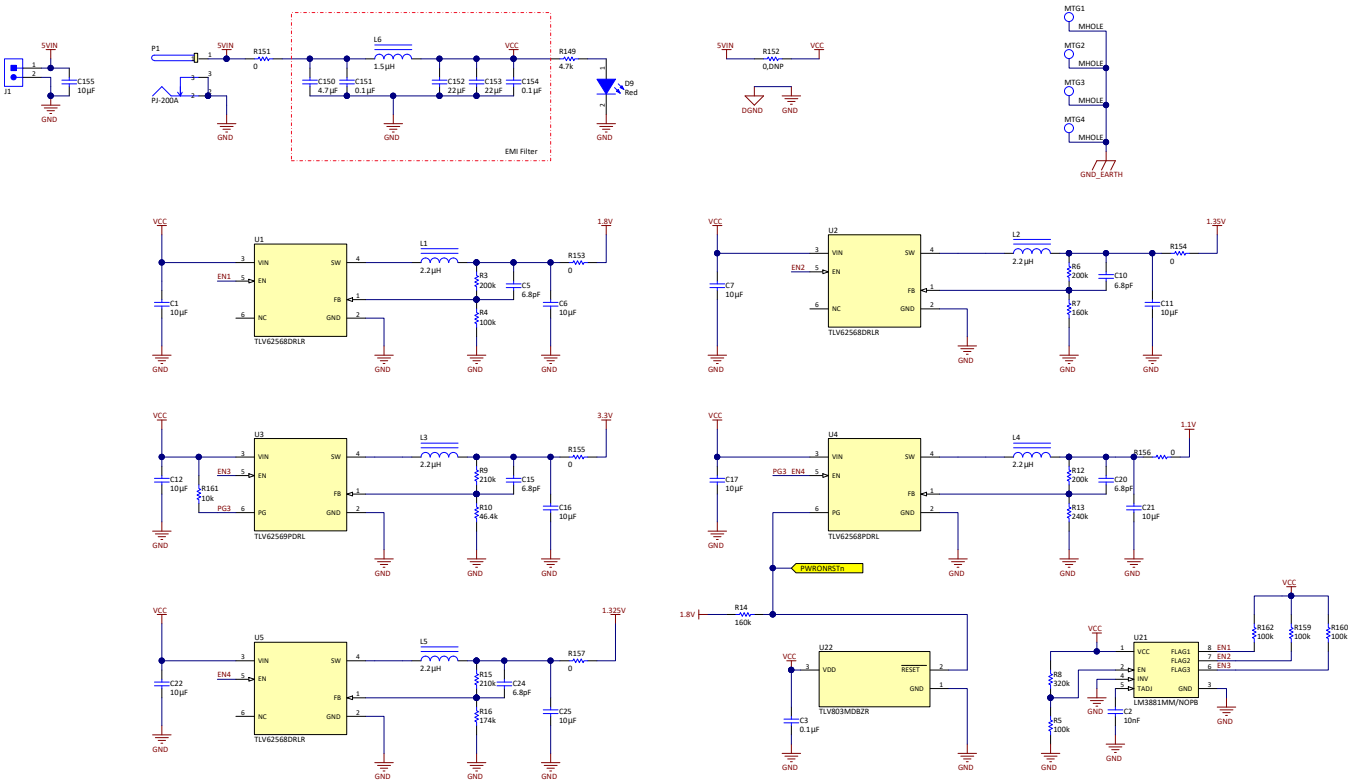


図 10. Power Sequencing Circuit

2.4.2.1 Design Steps for DC-DCs

Select the circuit topology. The cost, space, and efficiency are key concerns in home appliance design, so select a Buck topology. Use a synchronous converter with integrated FET and high switching frequency to reduce the bill of material cost and size.

Then, select the TLV62568/9. The TLV62568/9 is a high efficiency synchronous converter in a SOT563 package, and typically operates at a 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load, the device automatically enters Power Save Mode (PSM) to maintain high efficiency.

Next, set the output voltage, which is adjusted by the resistor divider, as shown in 式 1. A reference design example is for a 1.8-V power supply, when sizing R4, to achieve low current consumption and acceptable noise sensitivity, to use a maximum of 200 kΩ for R4. Larger currents through R4 improve noise sensitivity and output voltage accuracy, but increase current consumption. In this design, 100 kΩ is selected for R4.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_2}{R_4}\right) = 0.6\ V \times \left(1 + \frac{R_2}{R_4}\right) \quad (1)$$

A feed forward capacitor, C5 of 6.8 pF, is recommended for improving the loop bandwidth to make a fast transient response.

The inductor and output capacitor together provide a low-pass filter. The inductor peak-to-peak ripple current, peak current, and the RMS current are calculated using 式 2, 式 3, and 式 4.

$$II_{p-p} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times F_{SW}} \quad (2)$$

$$II_{peak} = I_O + \frac{II_{p-p}}{2} \quad (3)$$

$$I_{LO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (4)$$

The inductor saturation current rating must be greater than the calculated peak current, and the RMS or heating current rating must be greater than the calculated RMS current. Use 1.5 MHz for f_{SW}. Ensure the chosen inductor is rated for the peak current of 式 3 and the RMS current of 式 4.

For this design, the inductor used is the DFE252010F-2R2M=P2 (2.2 µH), with a peak current rating of 3.3 A and RMS current rating of 2.3 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TLV62568 is intended for use with ceramic or other low-ESR capacitors. Use 式 5 to determine the required RMS current rating for the output capacitor.

$$I_{LO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (5)$$

For this design, a Murata 10-µF output capacitor is used.

2.4.2.2 Design Steps for the Sequencer

Select the suitable sequencer offering 3 power up and power down sequencing orders in regard to the power tree architecture. Cost, space, and ease-of-use are the key concerns for the sequencer.

In this design, the LM3881 provides a simple solution for sequencing multiple rails in a controlled manner. A small external timing capacitor (C2) establishes the clock waveform; the relationship between the capacitor and the clock period is typically 120 µs/nF. In this design, a 10-nF capacitor is used, which means the clock period is 1.2 ms. The delay time between the 3 flags is 8 clock cycles, which means the interval time between power rails is 9.6 ms.

A resistor divider can also be used to enable the LM3881, based on exceeding a certain VCC supply voltage threshold. The supply voltage for which EN is asserted is given in 式 6.

$$VCC_{ENABLE} = 1.22\ V \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - 7\ \mu A \times \left(R_{EN1} \| R_{EN2}\right) \quad (6)$$

By tuning the capacitor, the delay time can be adjusted for a different discharge time. By tuning the VCC supply voltage threshold, the moment when the sequencer works also can be adjusted for a different discharge time.

2.4.2.3 Design Steps for the Supervisor

The TLV803 is chosen as the supervisor in this design. The LM803M's reset pin is connected to a 1.1-V converter's power good pin, which ensures the reset signal ramps up after all the power rails go high.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Connector Configuration of TIDA-01568

shows the top view of the PCB and connector configuration for this reference design, which features:

- A two-terminal input for power supply (J1): This pin is used to connect the input DC supply. The positive and negative terminals are also shown in .
- A six-pin connector for UART (J2): Three of the pins are used for external UART communication with a host machine. This interface is usually used for monitoring booting information during Linux software development.
- System Reset (S1): This switch is used to reset the processors.
- Boot Mode Configuration (S2): This switch is used to change boot mode between two modes. The usual operation is to change boot from the on-board flash to an external microSD card.
- Expansion headers (P8,P9): These two headers lead out the processors' available GPIOs and on-chip resources, which can be used for expand functions, including 67 GPIOs, 4 timers, 4 UARTs, 8 PWMs, 1 24-bit LCD controller, 1 MMC, 7 ADCs, 2 I2Cs, and 2 SPIs.
- PFC Antenna: These two terminals are used for installing 2.4G / 5G PFC antennas in UFL/IPEX-1 type.

表 3. Expansion Headers – P8

DGND	1	2	DGND
GPIO1_6	3	4	GPIO1_7
GPIO1_2	5	6	GPIO1_3
GPIO2_2 TIMER4	7	8	GPIO2_3 TIMER7
GPIO2_5 TIMER5	9	10	GPIO2_4 TIMER6
GPIO1_13 LCD_DATA18	11	12	GPIO1_12 LCD_DATA19
GPIO0_23 EHRPWM2B LCD_DATA22	13	14	GPIO0_26 LCD_DATA21
GPIO1_15 LCD_DATA16	15	16	GPIO1_14 LCD_DATA17
GPIO0_27 LCD_DATA20	17	18	GPIO2_1
GPIO0_22 EHRPWM2A LCD_DATA23	19	20	GPIO1_31 MMC1_CMD
GPIO1_30 MMC1_CLK	21	22	GPIO1_5 MMC1_DAT5
GPIO1_4 MMC1_DAT4	23	24	GPIO1_1 MMC1_DAT1
GPIO1_0 MMC1_DAT0	25	26	GPIO1_29
GPIO2_22 LCD_VSYNC	27	28	GPIO2_24 LCD_PCLK
GPIO2_23 LCD_HSYNC	29	30	GPIO2_25 LCD_DE
GPIO0_10 LCD_DATA14 UART5_CTSN+	31	32	GPIO0_11 LCD_DATA15 UART5_RTSN
GPIO0_9 LCD_DATA13 UART4_RTSN	33	34	GPIO2_17 LCD_DATA11 EHRPWM1B UART3_RTSN
GPIO0_8 LCD_DATA12 UART4_CTSN	35	36	GPIO2_16 LCD_DATA10 EHRPWM1A UART3_CTSN
GPIO2_14 LCD_DATA8 UART5_TXD+	37	38	GPIO2_13 LCD_DATA9 UART5_RXD+
GPIO2_12 LCD_DATA6	39	40	GPIO2_11 LCD_DATA7
GPIO2_10 LCD_DATA4	41	42	GPIO2_9 LCD_DATA5
GPIO2_8 LCD_DATA2	43	44	GPIO2_7 LCD_DATA3
GPIO2_6 LCD_DATA0 EHRPWM2A	45	46	GPIO2_5 LCD_DATA1 EHRPWM2B

表 4. Expansion Headers – P9

DGND	1	2	DGND
3.3V	3	4	3.3V
5.0V	5	6	5.0V
5.0V	7	8	5.0V
EXTINTn	9	10	SYS_RESETn
GPIO0_30 UART4_RXD	11	12	GPIO1_28
GPIO0_31 UART4_TXD	13	14	GPIO1_18 EHRPWM1A
GPIO1_16	15	16	GPIO1_19 EHRPWM1B
GPIO0_5 I2C1_SCL SPI1_CS0	17	18	GPIO0_4 I2C1_SDA SPI1_D1
GPIO0_13 I2C2_SCL UART1_RTSn SPI1_CS1	19	20	GPIO0_12 I2C2_SDA UART1_CTSn SPI1_CS0
I2C2_SCL SPI0_D0 GPIO0_3 UART2_TXD EHRPWM0B	21	22	SPI0_SCLK GPIO0_2 UART2_RXD EHRPWM0A I2C2_SDA
GPIO1_17	23	24	GPIO0_15 UART1_TXD I2C1_SCL
GPIO3_21	25	26	GPIO0_14 UART1_RXD I2C2_SDA
GPIO3_19	27	28	GPIO3_17 SPI1_CS0 ECAPPWM2
GPIO3_15 SPI1_D0 EHRPWM0B	29	30	GPIO3_16 SPI1_D1
GPIO3_14 SPI1_SCLK EHRPWM0A	31	32	VDD_ADC
AIN6	33	34	GNDA_ADC
AIN4	35	36	AIN5
AIN2	37	38	AIN3
AIN0	39	40	AIN1
GPIO0_20	41	42	GPIO0_7 ECAPPWM0 SPI1_CS1
DGND	43	44	DGND
DGND	45	46	DGND

3.1.1.2 Procedure for Board Bring-up and Testing

Follow this procedure for board bring-up and testing:

1. Configure the developing environment; for details, refer to the Processor SDK Getting Started Guide.
2. After setting the correct configuration, modify the processor SDK by installing patch files for this reference design.
3. Connect the board to the host machine through a UART to USB cable; configure the UART debug tools (super terminal, tera term, and so forth) with the correct serial port. Insert a microSD card containing an image of the modified Linux operating system.
4. Power on the board on the voltage supply input with a 5-V DC.

3.1.2 Software

3.1.2.1 Description of Environment Implementation

This section describes the details of developing an environment implemented during the Linux operation system bringing up, listed in 表 5.

表 5. Development Environment Description

Environment Components	Description
Ubuntu 16.04.3	Linux host's version (the LTS version is preferred)
Processor-SDK-Linux-AM335x 04_02_00_09	The version of published SDK used in this design, patch files are compatible with this version
Code Composer Studio 7.2.0	Using as the add-on debug tool for AM335x
u-boot_tida_01568.patch	A patch file for boot loader to support this design
linux_tida_01568_without_wifi.patch	A patch file for Linux kernel to support this design, no WIFI driver support
linux_tida_01568_with_wifi.patch	A patch file for Linux kernel to support this design, WIFI driver support

3.1.2.2 How to Customize the Processor SDK for This Reference Design

An operating system is necessary in most applications to manage hardware and software resources, while the released kernel carries rich features or low-level drivers that may not fit the user's hardware. For this reference design, run the fit kernel on board by applying a patch to processor SDK. 図 11 shows the instructions used for this process.

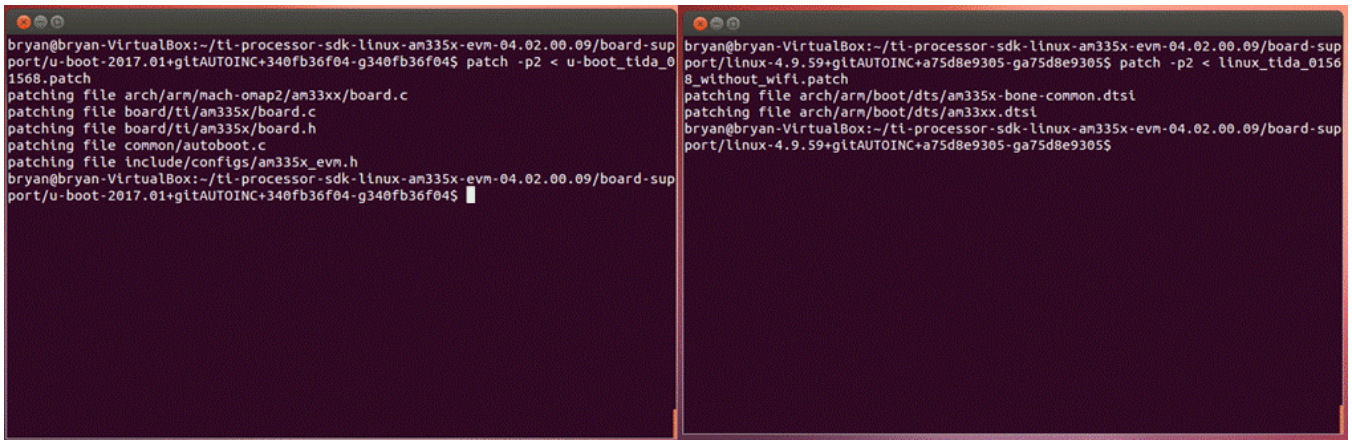


図 11. How to Apply a Patch to the Processor SDK

Comparing to the AM335x EVM or Beagle Bone family, the differences in hardware are:

- The EEPROM on this board does not contain the information of board ID.
- This board does not support the internal RTC.
- This board does not support the PMIC IC for power management.

The brief principle of modified codes behind the patch files:

1. U-Boot: Disable the board detect function and enforce the return value for "am335x-boneblack".
2. U-Boot: Disable the I2C communication with PMIC.
3. U-Boot: Disable the RTC related function.
4. U-Boot: Disable the "BOOTCOUNT_LIMIT" configuration during auto booting.

5. Kernel: Remove the RTC node, PMIC node and related codes in device tree (DTS file).
6. Kernel: Disable the "RTC Real Time Clocking" configuration.
7. Kernel: Add WL1837MOD driver configuration.

3.1.3 Software Bring-up Tips

1. Before developing the software, ensure the hardware is working correctly: consequent CCCC's should print on the screen when the SD card is not inserted.
2. Code Composer Studio is a tool used for tracking the instructions executed during bringing up the software. The terminal of P2 on the bottom of the board is a JTAG header to connect the emulator. The System.map file is a symbol table, which is a look-up between symbol names and their addresses in memory. Combining the symbol table and memory data lets the user track the process of how the software is running.

3.2 Testing and Results

3.2.1 Test Setup

The test performs the power-up and power-down sequencing, with a DC source and a switch that simulate the situation when removing the DC power. 図 12 shows the test setup.

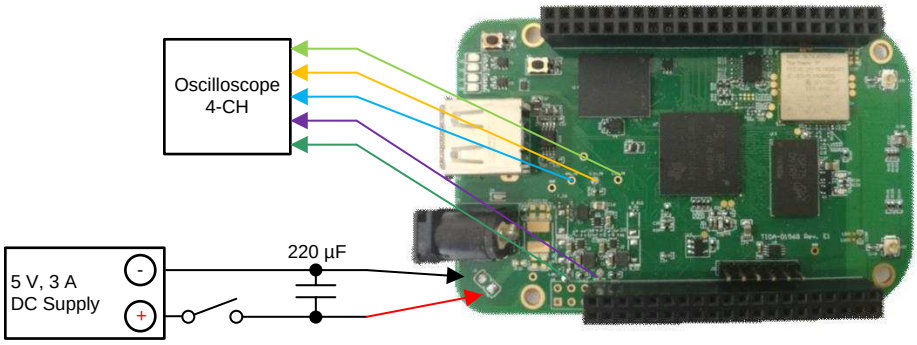


図 12. Power Sequencing Test Setup

3.2.2 Test Results

3.2.2.1 Power-Up and Power-Down Sequence Test

The following waveforms show the power-up and power-down sequence provided by this power solution that meet the requirements of the AM335x. The test environment is as below:

1. The input capacitor is 220 µF.
2. The status of the board is: Linux running with Wi-Fi enabled.
3. The style of the power down directly removes the DC power through the switch.

図 13 shows the power sequences of the input voltage rail and 1.8-V, 3.3-V, and 1.35-V rails.

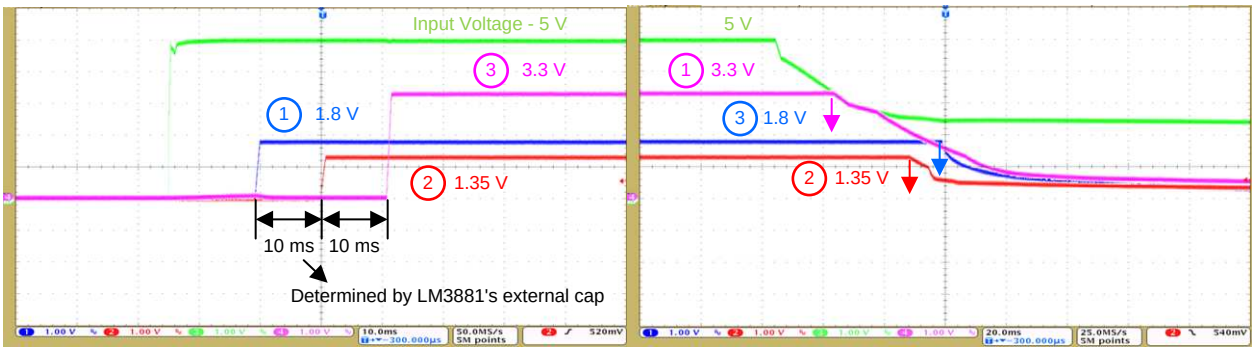


図 13. Power Sequence for 5-Vin,1.8-V, 3.3-V, and 1.35-V Rails

For the power-up sequencing, the 1.8-V, 1.35-V, and 3.3-V rails power turn on sequentially after the input voltage rail turns on. For the power-down sequencing, the 3.3-V, 1.35-V, and 1.8-V rails turn off sequentially in the precise reverse order after the input voltage rail turns off. The delay time between the different power rails is approximately 10 ms, which can be adjusted by changing the external capacitor of the LM3881MM.

図 14 shows the power sequences of the 3.3-V, 1.8-V, 1.35-V, and 1.1-V rails.

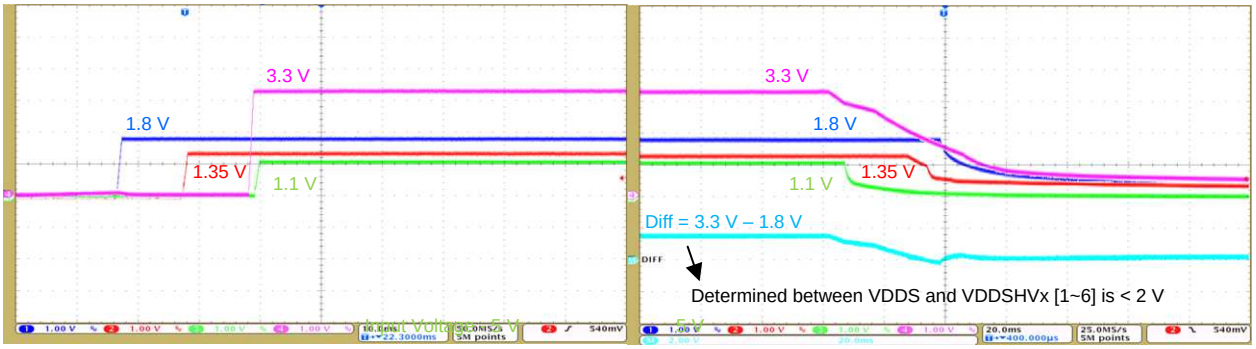


図 14. Power Sequence for 3.3-V, 1.8-V, 1.35-V, and 1.1-V Rails

For the power-up sequencing, the 1.8-V, 1.35-V, and 3.3-V rails power turn on sequentially after the input voltage rail turns on. For the power-down sequencing, the 3.3-V, 1.35-V, and 1.8-V rails turn off sequentially in the precise reverse order after the input voltage rail turns off. The difference between VDDS and VDDSHVx[1-6] during the entire power down sequence is < 2 V.

図 15 shows the power sequences of the 5-Vin, 1.8-V, 3.3-V, and PWRONRSTn rails.

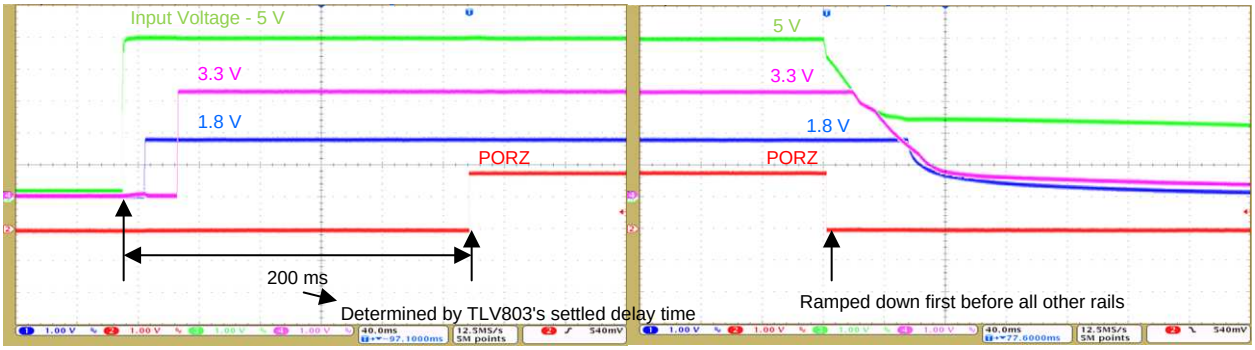


図 15. Power Sequence for 5-Vin, 1.8-V, 3.3-V, and PWRONRSTn Rails

For the power-up sequencing, the 1.8-V, 3.3-V, and PWRONRSTn rails turn on sequentially after the input voltage rail turns on, and the PWRONRSTn rail turns on after all the other rails are ON. For the power-down sequencing, the PWRONRSTn rail ramps down first before all other rails turn off, and the other rails ramp down sequentially. The delay time between PWRONRSTn and input voltage rail is 200 ms, which depends on the fixed delay time of the supervisor for the TLV803.

図 16 shows the power sequences of the 1.8-V, 3.3-V, 1.1-V, and 1.325-V rails.

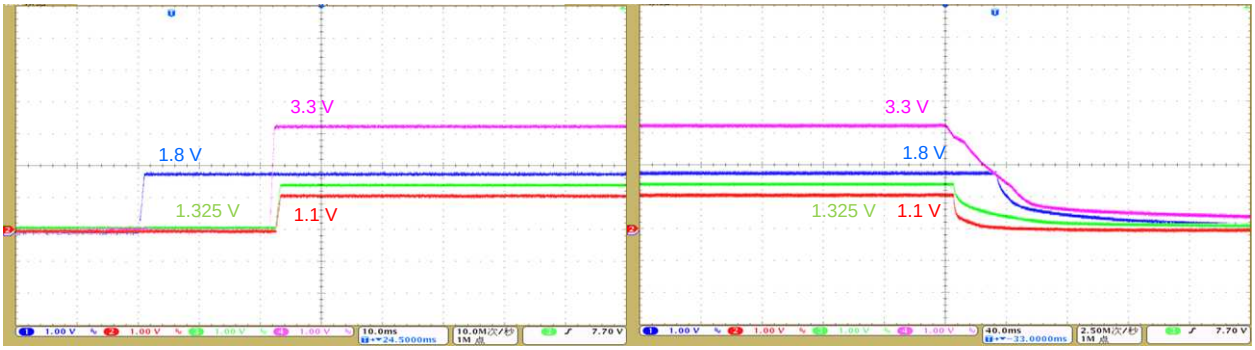


図 16. Power Sequence for 1.8-V, 3.3-V, 1.1-V, and 1.325-V Rails

For the power-up sequencing, the 1.8-V, 3.3-V, 1.1-V, and 1.325-V rails turn on sequentially, and the 1.325-V and 1.1-V rails ramp up at the same time. For the power-down sequencing, the 1.8-V, 3.3-V, 1.1-V, and 1.325-V rails ramp down sequentially, and the 1.325-V and 1.1-V rails ramp down at the same time.

3.2.2.2 Typical Characteristics of DC-DCs

図 17 shows the efficiency of the 5 voltage rails with 5-V DC supply.

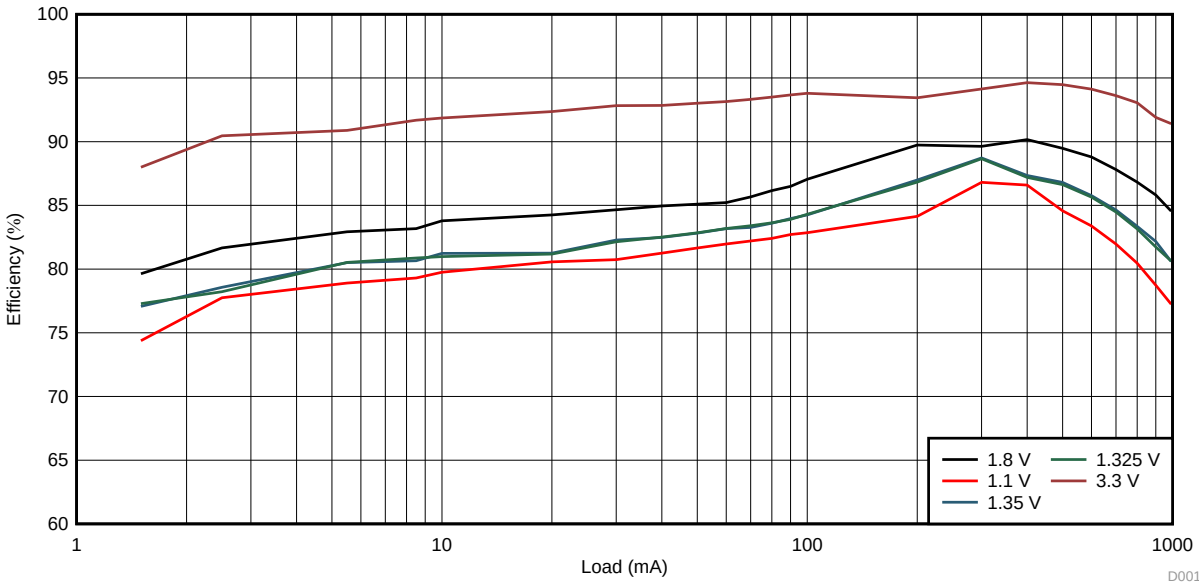


図 17. Efficiency of 5 Voltage Rails

To test the efficiency, four multimeters are used: two are set up as voltmeters to measure the input and output voltages, and two are set up as ammeters to measure the input and output currents. In addition, an electronic load is used to achieve different currents.

表 6, 表 7, 表 8, 表 9, and 表 10 list the details of the efficiency curves shown in 図 17.

表 6. Efficiency of 1.8-V Rail

V_{IN}(V)	I_{IN}(mA)	V_{OUT}(V)	I_{OUT}(V)	η(%)
4.972	4.55	1.807	10.49	83.79
4.949	8.52	1.806	19.67	84.25
4.924	12.97	1.804	29.97	84.66
4.899	17.28	1.802	39.91	84.95
4.876	21.38	1.802	49.23	85.10
4.85	25.95	1.802	59.52	85.22
4.823	30.66	1.802	70.3	85.67
4.798	34.91	1.801	80.13	86.16
4.773	39.31	1.796	90.36	86.49
4.749	43.53	1.796	100.2	87.05
4.491	88.58	1.789	199.55	89.74
4.911	121.1	1.785	298.65	89.64
4.883	160.1	1.78	396	90.16
4.85	206.68	1.775	505.3	89.48
4.822	245.64	1.77	594.23	88.80
4.786	295.55	1.765	703.75	87.81
4.754	339.95	1.76	797.25	86.82
4.718	388.68	1.756	896.17	85.82
4.718	440.6	1.75	1003	84.44

表 7. Efficiency of 1.1-V Rail

V_{IN}(V)	I_{IN}(mA)	V_{OUT}(V)	I_{OUT}(V)	η(%)
5.02	2.74	1.0883	10.08	79.75
5	5.52	1.09	20.4	80.57
4.988	8.22	1.09	30.37	80.74
4.974	10.73	1.089	39.82	81.25
4.958	13.53	1.087	50.39	81.65
4.942	16.23	1.086	60.54	81.97
4.927	18.95	1.085	70.74	82.21
4.913	21.36	1.084	79.78	82.41
4.896	24.24	1.083	90.64	82.71
4.881	26.99	1.082	100.88	82.86
4.715	55.97	1.073	206.93	84.14
4.574	80.63	1.0688	299.54	86.81
4.395	111.8	1.064	399.9	86.59
4.944	126.74	1.0595	500.17	84.57
4.924	154.4	1.055	600.9	83.39
4.904	182.63	1.05	699.15	81.97
4.881	213.6	1.046	802	80.46
4.858	245.66	1.04	903.47	78.73
4.834	278.5	1.036	1002	77.11

表 8. Efficiency of 3.3-V Rail

V_{IN}(V)	I_{IN}(mA)	V_{OUT}(V)	I_{OUT}(V)	η(%)
4.968	7.6	3.319	10.45	91.86
4.93	14.18	3.318	19.46	92.36
4.885	21.9	3.317	29.94	92.83
4.846	28.69	3.314	38.95	92.84
4.8	36.67	3.313	49.42	93.02
4.753	44.79	3.31	59.91	93.15
4.712	51.88	3.31	68.92	93.32
4.663	60.28	3.31	79.4	93.50
4.613	68.85	3.31	89.88	93.67
4.57	76.37	3.31	98.9	93.80
4.898	143.46	3.296	199.21	93.44
4.84	216.12	3.2866	299.6	94.13
4.78	289.16	3.2823	398.51	94.63
4.715	367.1	3.2778	498.89	94.48
4.643	448.84	3.2736	599.17	94.12
4.565	534.06	3.2695	698.05	93.61
4.472	626.51	3.2655	798.38	93.05
4.276	746	3.262	898.72	91.90
4.18	853.2	3.2585	1000	91.37

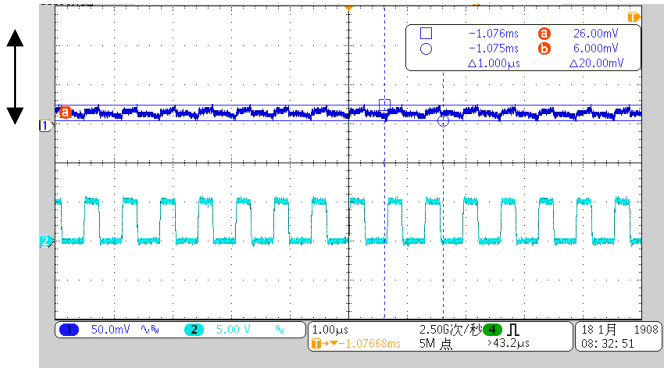
表 9. Efficiency of 1.35-V Rail

V_{IN}(V)	I_{IN}(mA)	V_{OUT}(V)	I_{OUT}(V)	η(%)
4.992	3.57	1.353	10.7	81.23
4.974	6.66	1.356	19.85	81.25
4.955	10	1.3545	30.1	82.28
4.935	13.51	1.3531	40.64	82.48
4.917	16.59	1.352	49.97	82.82
4.898	20	1.3512	60.3	83.17
4.879	23.21	1.351	69.8	83.27
4.859	26.7	1.35	80.34	83.60
4.839	30.31	1.348	91.36	83.97
4.823	32.97	1.347	99.46	84.25
4.63	66.54	1.34	200	86.99
4.432	101.27	1.3344	298.44	88.73
4.923	122.96	1.3296	397.66	87.35
4.9	155.16	1.325	498.08	86.80
4.873	191.27	1.3196	605.8	85.77
4.848	225.04	1.315	702.2	84.64
4.823	260.34	1.31	798.94	83.35
4.793	300	1.305	905.32	82.16
4.764	340.2	1.3	1003	80.45

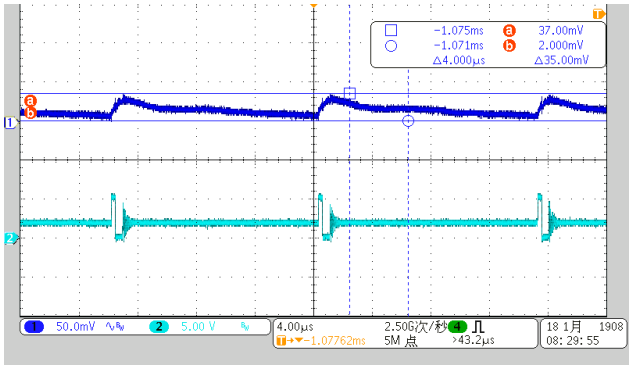
表 10. Efficiency of 1.325-V Rail

V_{IN}(V)	I_{IN}(mA)	V_{OUT}(V)	I_{OUT}(V)	η(%)
4.993	3.42	1.322	10.46	80.98
4.976	6.38	1.325	19.45	81.18
4.956	9.73	1.323	29.94	82.14
4.94	12.63	1.322	38.94	82.51
4.921	16	1.32	49.42	82.85
4.9	19.4	1.32	59.91	83.19
4.88	22.81	1.3187	70.4	83.40
4.865	25.72	1.318	79.4	83.63
4.846	29.1	1.3165	89.87	83.90
4.826	32.44	1.3146	100.4	84.31
4.64	64.65	1.3075	199.2	86.82
4.44	99.14	1.3027	299.59	88.66
4.924	120.48	1.298	398.5	87.19
4.9	152	1.2933	498.9	86.63
4.877	184.85	1.2886	599.2	85.65
4.852	218.66	1.284	698	84.48
4.825	254.5	1.279	798.37	83.16
4.798	291.96	1.274	898.7	81.73
4.769	330.6	1.2696	1000	80.53

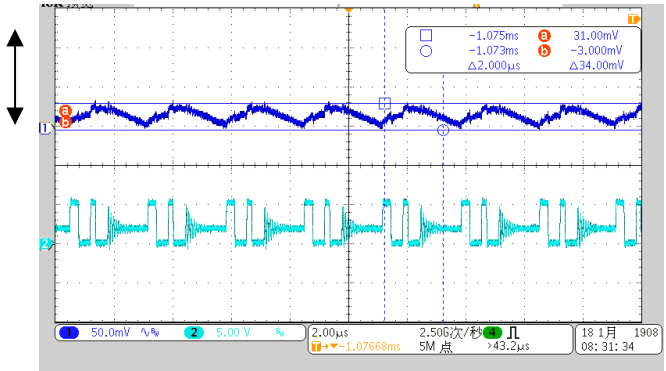
図 18 shows the output voltage ripple of the 1.8-V rails at 4 different loads.



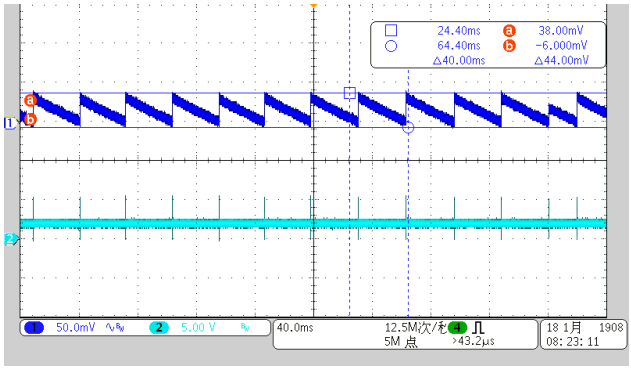
Ripple at 1 A



Ripple at 10 mA



Ripple at 0.1 A



Ripple at No Load

図 18. Output Voltage Ripple of 1.8 V at 4 Different Output Load

The output voltage ripple remains below 30 mVpp under a full load (1 A), light load (10 mA), 100mA and no load. This test result has a large margin, comparing the 5% requirement. The device automatically enters PSM to improve efficiency at light load when the inductor current becomes discontinuous. In PSM, the converter reduces switching frequency and minimizes current consumption.

The other power supply rails' ripple are similar to the 1.8-V rail, refer to the TLV62568/9's data sheet for more details.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at .

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at .

4.3 PCB Layout Recommendations

4.3.1 PCB Layout Guidelines

The board's PCB is set up for 6 layers; the 1, 3, 4, and 6 layers are signal layers, the 2 layer is a GND layer, and the 5 layer is a power layer. The PCB layers are shown in 図 19 through 図 24.

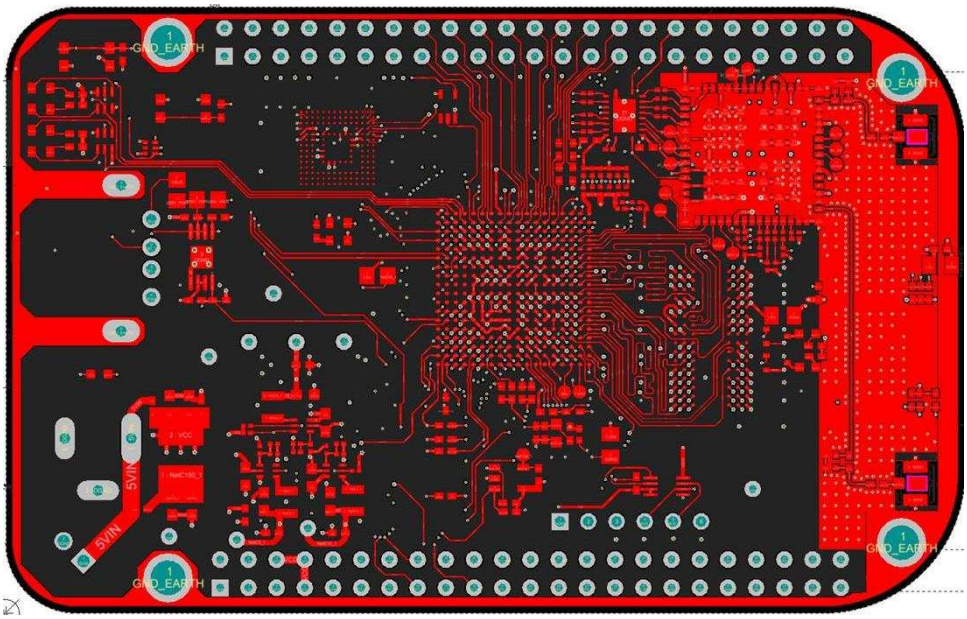


図 19. Top Layer of TIDA-01568

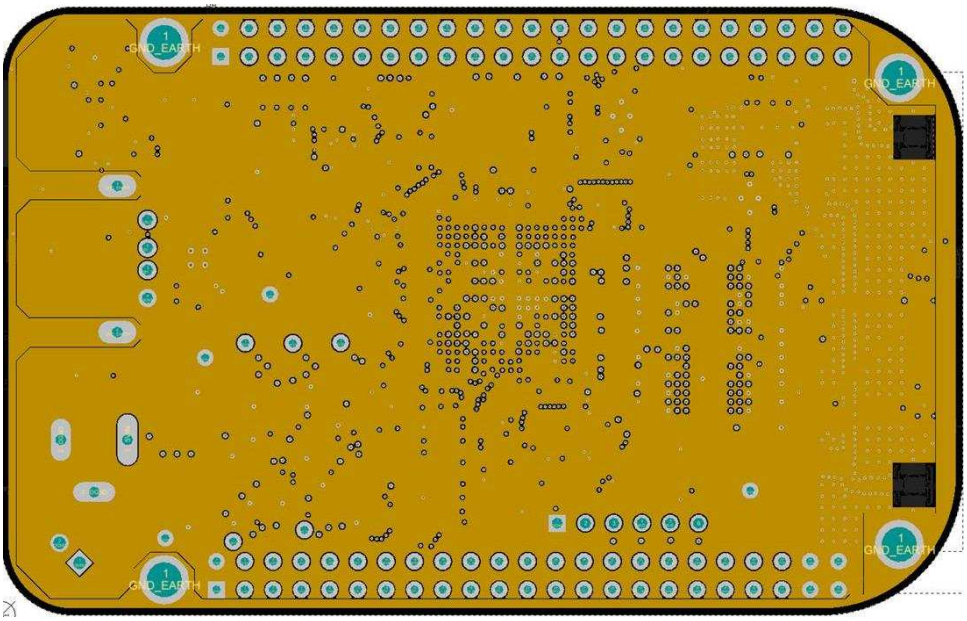


図 20. Layer 2 of TIDA-01568

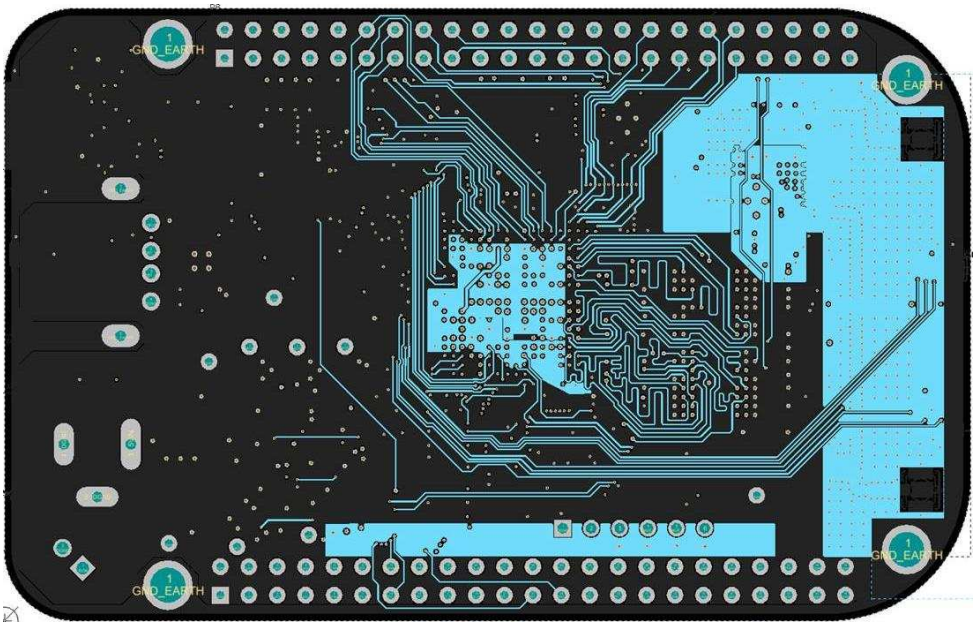


図 21. Layer 3 of TIDA-01568

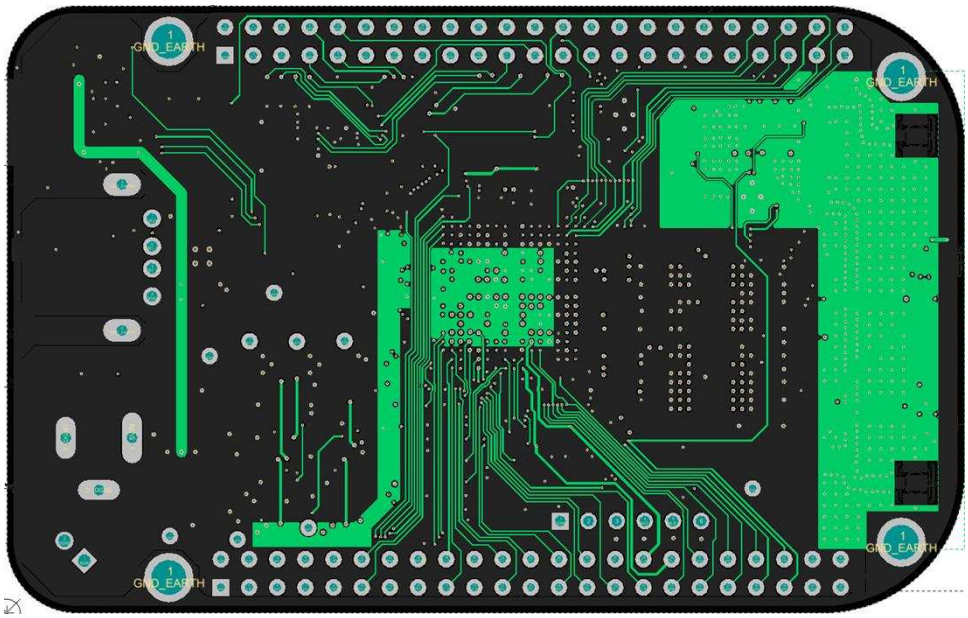


図 22. Layer 4 of TIDA-01568

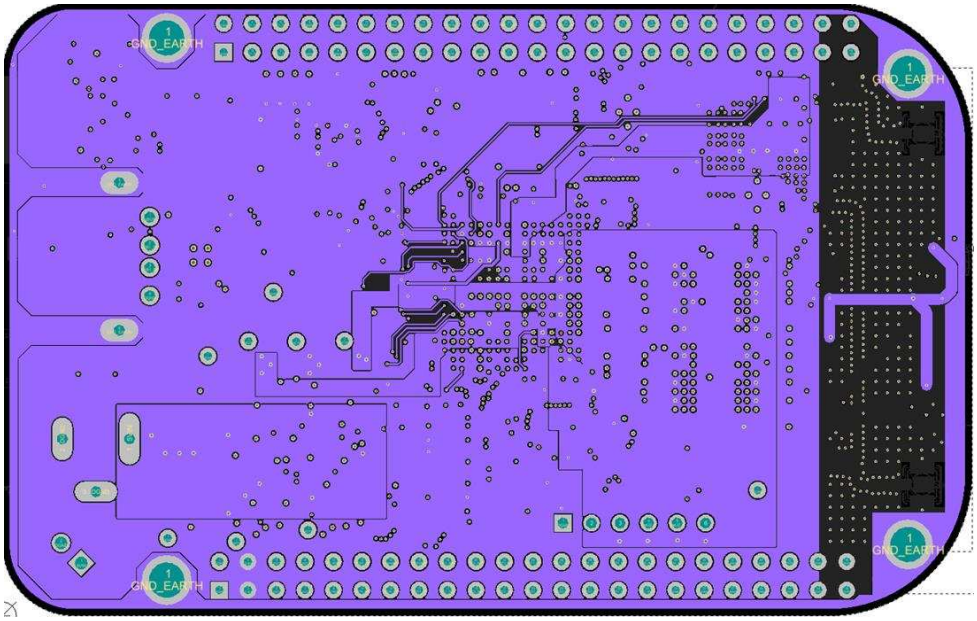


図 23. Layer 5 of TIDA-01568

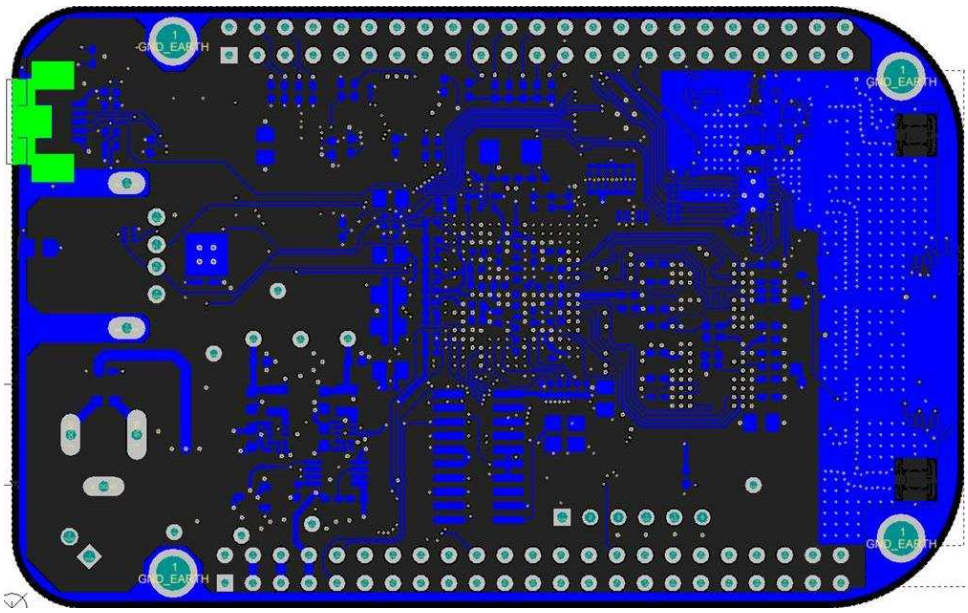


図 24. Bottom Layer of TIDA-01568

During the layout for DC-DC, coupling between different loops should be avoided. Place the input capacitor as close as possible to the device. The noise sensitive loop should be separated with high di/dt loops, so that the feedback trace should be put as far as possible from components and traces with high di/dt. Another key concern is the ground plane: it should be as large as possible to reduce noise sensitivity and improve thermal dissipation.

Another concern during layout is for the WL183xMOD: keep the proximity of ground vias close to the pad. There should be 4 vias per pad, and a complete ground pattern under the module for better thermal performance. In this design, the GND pour is added on layer 3 and layer 4 under the module.

During the layout for the antenna, use a 50-Ω impedance match on the trace to the antenna, and 50-Ω traces for the PCB layout. RF traces must have via stitching on the ground plane beside the RF trace on both sides. RF traces must have constant impedance (microstrip transmission line). RF trace bends must be gradual, with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners. The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.

For more details on WiLink layout, refer to the WL1837MODCOM8I WLAN MIMO and BT Module EVB for TI Sitara Platform User's Guide.

4.3.2 Layout Prints

To download the layer plots, see the design files at .

4.4 Altium Project

To download the Altium project files, see the design files at .

4.5 Gerber Files

To download the Gerber files, see the design files at .

4.6 Assembly Drawings

To download the assembly drawings, see the design files at .

5 Software Files

To download the software files, see the design files at .

6 Related Documentation

1. Discreat Power Solution for AM437x*SLVUAB1A*

6.1 商標

7 Terminology (Optional)

8 About the Author

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