参考資料

デザイン・ガイド：TIDA-01040
大電流アプリケーション用バッテリ・テスタのリファレンス・デザイン

概要

リチウムイオン・バッテリの構成と電気的テストには、正確な電圧および電流制御、一般には指定の温度範囲にわたって±0.05%以内の精度が必要です。このリファレンス・デザインでは、8V～16Vの入力(バス)電圧と、0V～5Vの出力負荷(バッテリ)電圧に対応できる大電流(最大50A)のバッテリ・テスタ・アプリケーション用ソリューションを提案します。このデザインでは、TIの統合マルチフェーズ双方向コントローラのLM5170を、TIの高精度データ・コンバータおよび計装アンプと組み合わせ、0.01%フルスケールの充電および放電精度を実現しています。バッテリ容量を最大化し、バッテリ構成にかかる時間を最小化するため、このデザインでは高精度の定電流(CC)および定電圧(CV)較正ループと、単純化されたインターフェイスを使用しています。主要な設計理論をすべて説明し、部品の選択プロセスや最適化についての指針も示しています。また、回路図、基板レイアウト、ハードウェア・テスト、結果も公開しています。

リソース

TIDA-01040	デザイン・フォルダ
LM5170-Q1、LM2664、TPS709	プロダクト・フォルダ
LM5118	プロダクト・フォルダ
INA188	プロダクト・フォルダ
DAC80004	プロダクト・フォルダ
ADS131A04	プロダクト・フォルダ
TLV07、OPA2227、OPA827、THS4561、LM6142	プロダクト・フォルダ

TI E2E™ Community

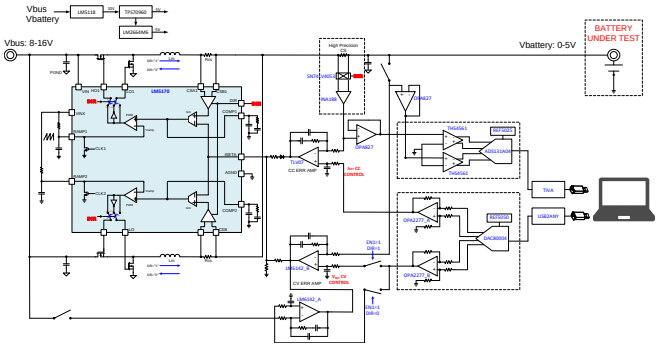
E2E™エキスパートに質問

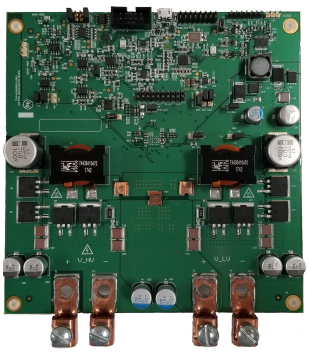
特長

- 較正制御付きのバッテリ・テスト・サブシステムは、0.01%フルスケールの電流制御精度を実現
- 最大 50A のアプリケーションを 8V ～ 16V の入力電圧（バス）と 0V ～ 4.5V（最大 5V）の出力負荷（バッテリ）でサポート
- LM5170 双方向昇降圧コントローラ
- DAC80004 によりプログラム可能な高精度基準電圧
- ADS131A04 24ビット・デルタ-シグマによる電圧および電流監視
- 使いやすい制御インターフェイス

アプリケーション

- バッテリ・テスト機器





1 System Description

Demand for Li-Ion batteries continues to grow at an exponential pace. Battery formation and testing is an important manufacturing step to maximize battery life and storage capacity requiring multiple charge and discharge cycles. During these cycles, battery current and voltage must be precisely controlled. The TIDA-01040 reference design provides an easy-to-design solution utilizing high accuracy constant current (CC) and constant voltage (CV) calibration loops to achieve up to 0.01% full scale charge and discharge current control accuracy. This solution supports charge and discharge rates of up to 50 A and provides a high-precision DAC and ADC to regulate and monitor the battery voltage and current . Furthermore, the flexible solution provides an option for additional higher current and multi-phase applications.

1.1 Li-Ion Formation

The Li-Ion battery manufacturing process includes electrode production, stack and jelly-roll construction, cell assembly and end-of-line conditioning. 図 1 shows a simplified Li-Ion battery manufacturing process. Formation and testing at the end-of-line conditioning step are the process bottlenecks, limiting throughput. To maximize battery life, quality and performance, battery test equipment must possess accurate voltage and current control, often better than ±0.05%, over the specified temperature range.

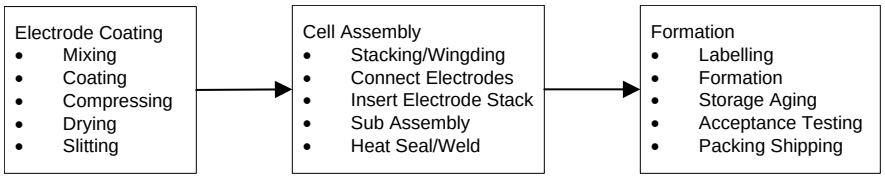


図 1. Simplified Li-Ion Battery Manufacturing Process

Some battery test equipment has adopted linear regulators to easily meet the accuracy requirements of formation and testing of batteries used in portable equipment, while compromising on efficiency. On larger batteries, this approach will have challenges with heat management and efficiency. Switching regulators have been widely used in battery test equipment for their better performance in efficiency and heating management.

1.2 Li-Ion Battery Formation Profile

図 2 shows the typical Li-Ion battery formation profile which is similar to the battery charging profile. This process can be divided into three phases: initial process, CC, and CV. At first, a small *initial* charge of around 10% of the full-charge current is applied. This prevents the cell from overheating until such a time that it is able to accept the full current of the constant-current phase. In reality, this phase is rarely needed because most modern mobile devices are designed to shut down while there is still some charge left because deep discharge, like overcharging, can damage the cell.

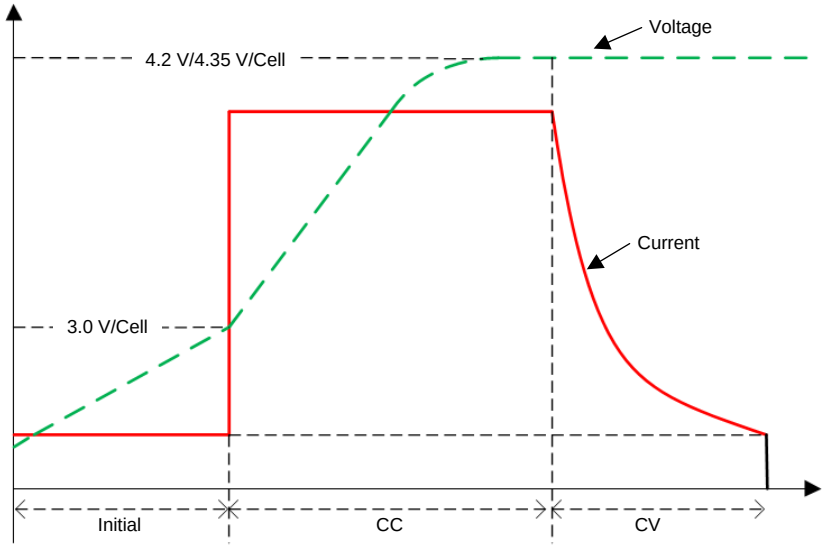


図 2. Regular Li-Ion Battery Formation Profile

Then, the battery is typically charged at a CC of 0.5 A. (typical) or less until the battery voltage reaches 4.1 or 4.2 V (depending on the exact electrochemistry). When the battery voltage reaches 4.1 or 4.2 V (typical), the charger switches to a *constant voltage* phase to eliminate overcharging. Superior battery test equipment manages the transition from CC to CV smoothly to ensure maximum capacity is reached without risking damage to the battery. At higher charge current, the transition between CC and CV occurs earlier, because the cell voltage is higher due to the voltage drop across the internal resistance of the cell, and therefore the CV voltage is reached sooner.

1.3 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
$V_{battery\_min}$	0 V	Battery-port minimum operating voltage
$V_{battery\_normal}$	4.2 V	Battery-port normal operating voltage
$V_{battery\_max}$	5 V	Battery-port maximum operating voltage
V_{bus_min}	8 V	Bus-port minimum operating voltage
V_{bus_normal}	12 V	Bus-port normal operating voltage
V_{bus_max}	16 V	Bus-port normal operating voltage
F_{SW}	100 kHz	Switching frequency
I_{max}	25 A	Maximum DC current per phase, bidirectional
I_{Total_max}	50 A	Total maximum DC current at battery-port
Current control accuracy	0.01%	Full-scale current control accuracy for charge and discharge

2 System Overview

2.1 Block Diagram

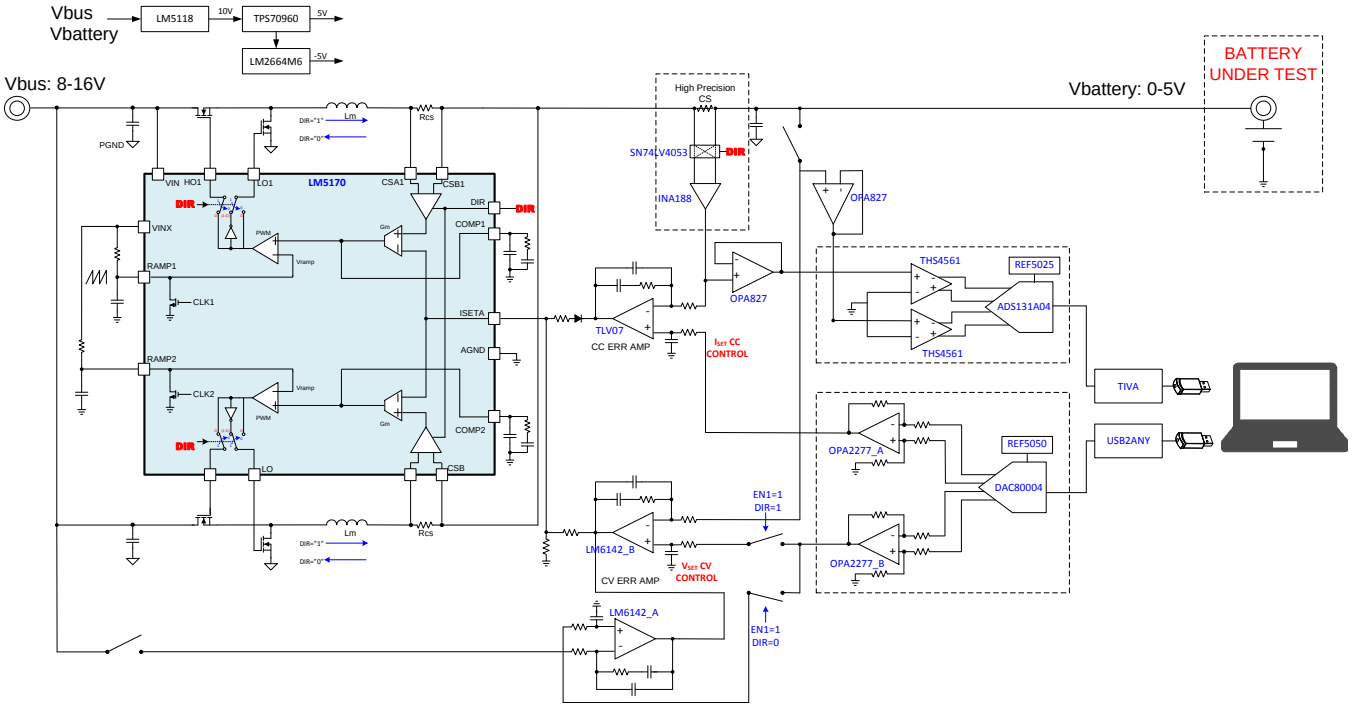


図 3. TIDA-01040 Block Diagram

In this reference design, LM5170 is a buck-boost controller which charges or discharges the battery depending on the "DIR" setting. The high precision current sense amplifier monitors the charging or discharging current. SN74LV4053 is a 2-channel CMOS analog multiplexer/demultiplexer which converts the bidirectional signal into a single directional signal. The INA188 device is high-precision instrumentation amplifier which amplifies the cross voltage of the high-precision current sensor with low noise. TLV07 is an error amplifier that compares the current with the reference control signal. LM6142 is a two-channel error amplifier which compares the battery voltage or bus voltage with the reference control signal. "EN1" and "DIR" signals enable the calibration of the bus voltage in boost mode or the battery voltage in buck mode. Two OPA827 devices operate as buffers between the main control system and data acquisition system. THS4561 is a differential amplifier which converts the single ended measurement signals to differential signals. ADS131A04 is a four-channel, 24-bit delta-sigma ADC which monitors the current and voltage of the battery. DAC80004 is a four-channel, 16-bit high precision DAC that provides reference control signals to the CC and CV control with a two-channel amplifier OPA2277. There is also an onboard TIVA processor that communicates between the ADS131A04 device and the PC. The USB2ANY interface adaptor communicates between the DAC80004 device and the PC.

2.2 Highlighted Products

2.2.1 LM5170-Q1 Multiphase Bidirectional Current Controller

The LM5170-Q1 device is a dual-channel, bidirectional, multiphase controller that supports high-current battery test applications up to 200 A using eight phases. It can regulate the average current flowing between the high- and low-voltage ports in the direction designated by the DIR input signal.

Other important features include:

- 5-A peak half-bridge gate drivers which enables the ability to drive high currents
- Programmable oscillator frequency which allows the user to choose the FET switching frequency
- MOSFET failure detect at start-up and circuit breaker control which provides security to the system

2.2.2 INA828 Precision Instrumentation Amplifier

The INA828 device is a precision instrumentation amplifier with integrated resistor networks for sensing and data acquisition systems. This device measures and amplifies a differential voltage that represents output current which acts as feedback to regulate current. The INA828 device uses super-beta input transistors which allows for lower input bias current and current noise while also improving input offset voltage and offset drift.

Other important features include:

- Gain drift: 50 ppm/ºC (G > 1) which limits the variation of calibration at high temperatures
- Bandwidth: 2 MHz (G = 1), 260 kHz (G = 100) which allows for fast transients
- Inputs protected up to ±40 V which provides protection to the device
- Power-supply rejection: 100 dB, minimum (G = 1) which limits the noise observed on the signal chain

Alternatives:

The INA828 device offers lower noise than its predecessor, the INA188 device, but has a narrower bandwidth than the INA821. The INA828 device is pin-to-pin compatible with the SOIC package of the INA188 device.

表 2. INA828 Alternatives

	INA828	INA821	INA188	INA819
Quiescent current	0.6 mA	0.6 mA	1.4 mA	350 µA
Noise density at 1 kHz	7 nV/√Hz	7 nV/√Hz	12 nV/√Hz	8 nV/√Hz
Gain error (±)	0.15%	0.15%	0.50%	0.005%
Bandwidth at G = 1	2 MHz	4.7 MHz	0.6 MHz	2 MHz

2.2.3 DAC80004 16-bit DAC With 1 LSB INL/DNL

The DAC80004 device is low-power, quad-channel, 16-bit digital-to-analog (DAC) converter. Hexadecimal values are written to the DAC using a computer which produces voltages at two channels. These voltages set the battery voltage charge and discharge rate. The four channels of the DAC80004 are used for the generation of high accuracy, user-defined voltage references.

Other important features include:

- True 16-bit performance: 1 LSB INL/DNL (maximum) which ensures accurate references for current and voltage
- Output buffer with rail-to-rail operation which provides clean references for current and voltage
- 50 MHz, 4- or 3-wire SPI-compatible which allows for simplified user interface

Alternatives:

The DAC80508 device is an eight channel DAC from the same family as the DAC80004.

表 3. DAC80004 Alternatives

	DAC80004	DAC80508
INL/DNL	1 LSB (maximum)	1 LSB (maximum)
# of channels	4	8
Glitch energy	1 nV-s	4 nV-s

2.2.4 ADS131A04 24-bit, 128-kSPS, 4-Channel, Simultaneous-Sampling Delta-Sigma ADC

The ADS131A04 device uses four channels to simultaneously and continuously sample voltage or current measurements. The ADC is the front-end of the battery tester and interface with a computer to display voltage and current values in TI's EvaluaTIon software. The ADS131A04 device is well equipped for measuring current and voltage signals due to it being a simultaneous sampling 4-channel converter, with a flexible SPI and data integrity to check and correct single-bit errors during data transmission.

Other important features include:

- Single-channel accuracy: Better than 0.01% at 10,000:1 dynamic range which enables high accuracy data acquisition
- Effective resolution: 20.6 bits at 8 kSPS which allows for high accuracy data acquisition
- Low-drift internal voltage reference: 6 ppm/ºC which limits the effects that temperature has on the data acquisition
- Multiple SPI data modes which allows for a simplified user interface

Alternatives:

The ADS131E08 and ADS131E04 devices, predecessors to the ADS131A04, have a lower data rate but implement integrated buffer amplifiers.

表 4. ADS131A04 Alternatives

	ADS131A04	ADS131E08	ADS131E04
Data rates (maximum)	128 kSPS	64 kSPS	64 kSPS
# of Channels	4	8	4
SNR	115 dB	107 dB	107 dB

2.2.5 Other Highlighted Products

In addition to the key products highlighted in the previous sections, this reference design also showcases the following TI devices:

- OPA2277 precision op amp; DAC driver buffer
- OPA827 precision op amp; ADC current and voltage measurement buffers
- TPS709 LDO regulators; 5-V DAQ and control power rails
- TLV07 36-V precision, rail-to-rail output, op amp; CC control amplifier
- THS4561 low-power, 70-MHz, high-supply range, fully differential amplifier; differential signal input for ADC
- LM2664 switched capacitor voltage converter; –5-V power rail
- LM7705 low-noise negative bias generator; –0.2 power rail
- LM5118 non-synchronous buck-boost controller; 10-V power rail
- LM6142 rail-to-rail I/O op amp; CV control amplifier
- SN74LVC1G04 single inverter; boost control logic
- SN74LV1T32 2-input positive OR gate; boost control logic
- SN74LV1T00 2-input positive NAND gate; buck control logic

2.3 System Design Theory

2.3.1 Constant Current Control Design

For CC control, a high precision current sensor with low inductance and temperature coefficient is necessary. The WSL2726 and WSLP2726 serial resistors are welded constructions of power metal strips which are ideal for current sensing with 1% tolerance, maximum 75 ppm/°C temperature coefficient, 0.5-nH to 5-nH inductance and less than 20-dB element TCR. See *WSL2726* and *WSLP2726* for detailed parameters.

A mux is used to manage the bidirectional current when charging or discharging. This design uses the SN74LV4053A, a triple 2-channel analog multiplexer/demultiplexer.

The next stage of the CC control loop chain is a zero-drift instrumentation amplifier INA188. This stage amplifies the current signal across the current sensor with low noise and low output impedance.

For the instrumentation amplifier, the common-mode voltage affects the input and output range limitation. The *Vcm vs Vout Calculator for Instrumentation Amplifier* design tool enables designers to easily determine the input common-mode and output swing limitations of the chosen instrumentation amplifier to ensure dynamic range and minimize prototyping time.

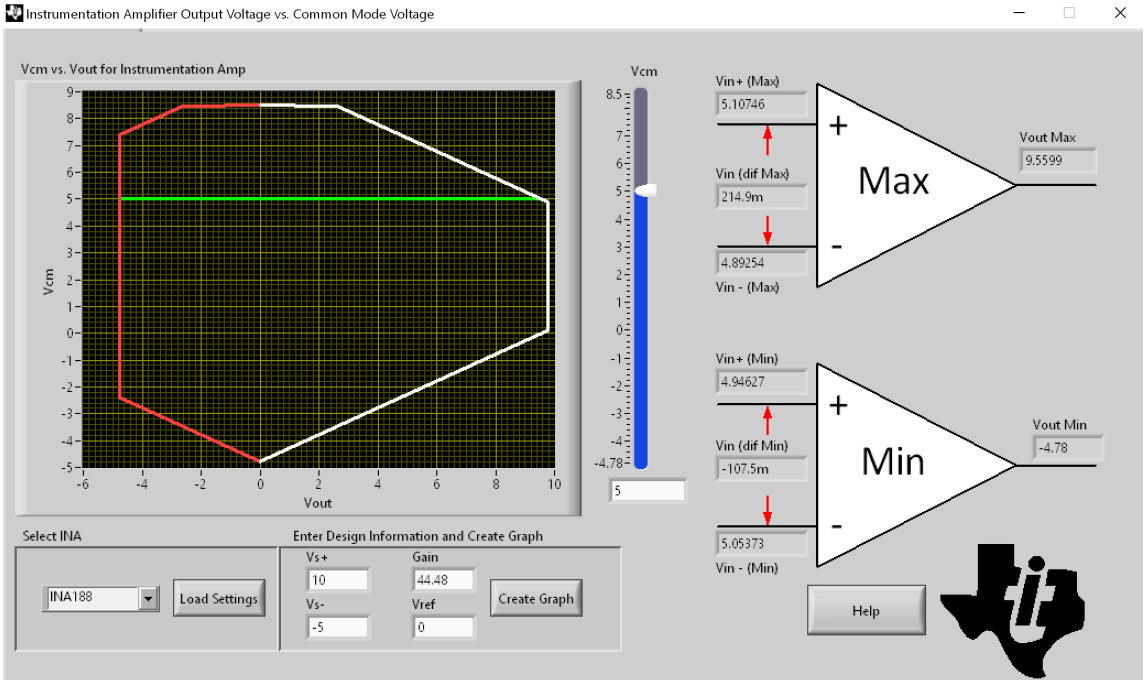


図 4. Vcm vs Vout Calculator for INA188

図 4 highlights the calculation results of the INA188 input and output range for this reference design. In this case, the maximum common mode voltage is the same as the maximum voltage on the battery side, so its maximum value is 5 V. When the INA188 is powered by 10 V and –5 V, and the gain is configured at 44.48, the calculation results show the input range is from –107.5 mV to 214.9 mV. It fits within the current signal range (±50 A × 1 mΩ = ±50 mV).

The CC control loop needs a high-precision error amplifier to calibrate to the target signal. TLV07 is a low-noise, precision operational amplifier whose maximum offset voltage is less than ±100 µV and has a 1-MHz bandwidth.

Due to the high current of this application, the high temperature will have an effect on the performance of this board. The input offset voltage drift is a key parameter to consider when choosing the amplifier. The input offset voltage drift of the TLV07 device is only 0.9 µV/°C. The maximum input offset voltage at 125°C is: 0.9 µV × 125 = 112.5 µV. In the worst-case 50-A application, this input offset voltage will cause an error of 112.5 µV / (50 A × 0.001 × 44.48) × 100% = 0.005058% on the control loop. This error is less than the 0.01% demanded accuracy, so the TLV07 device is a suitable amplifier.

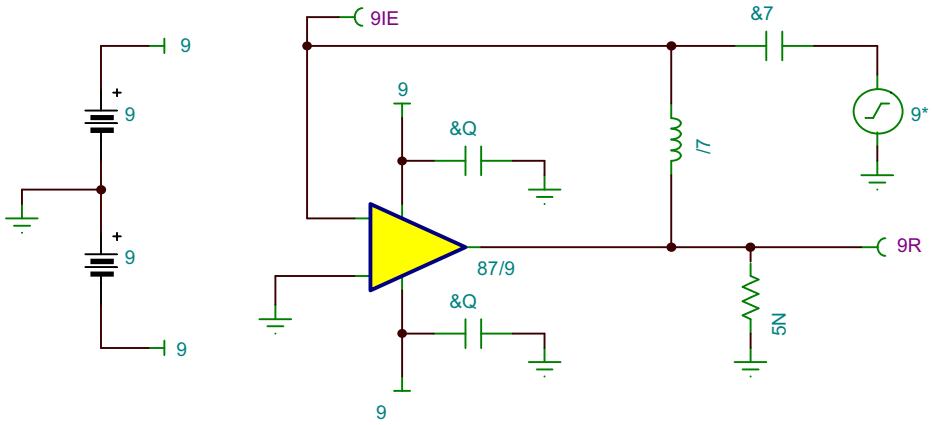


図 5. TLV07 TINA-TI Stability Schematic

図 5 highlights the schematic used to test the stability of the TLV07 device. The TINA-TI schematic in 図 5 features a 1TF capacitor and 1TH inductor for simulation purposes. This is used to break the feedback loop as the capacitor will be an open at DC while the inductor is a short. At high frequencies, the inductor will be an open and the capacitor will be a short. The load the TLV07 device experiences at the next stage of the system was also added on the right side of the schematic. This allows for the proper simulation of the stability of the circuit.

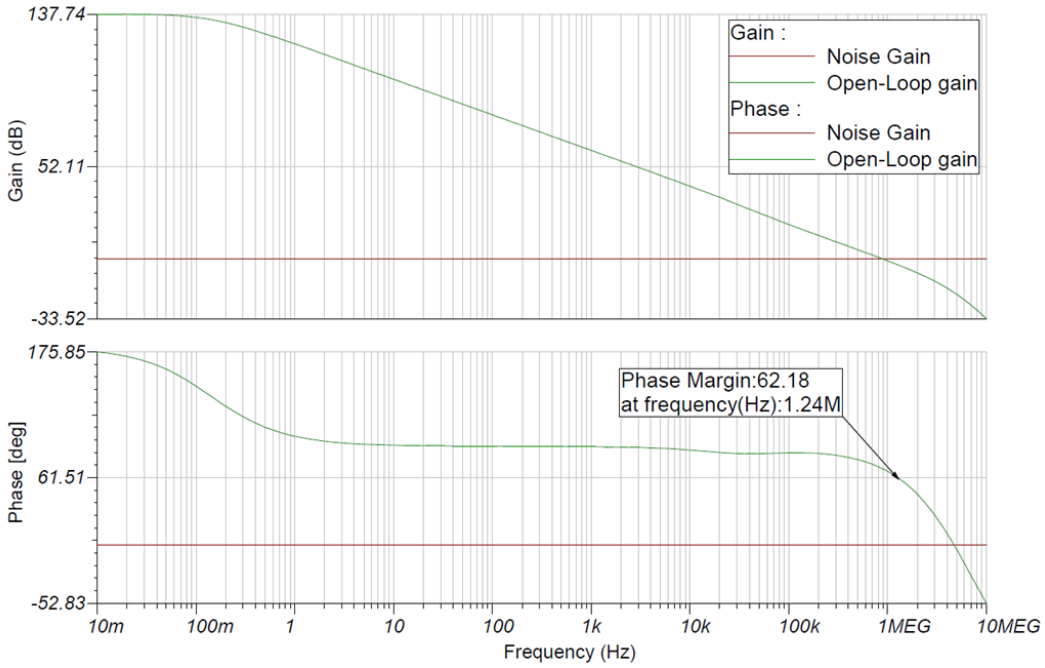


図 6. TLV07 TINA-TI Stability Simulation Results

図 6 highlights the results from the TLV07 stability simulation including a phase margin of > 62°, which implies stability. It is also important to consider the rate of closure between the loop gain and loaded open-loop gain curves. The loaded open-loop gain curve is decreasing at –20 dB per decade at the point of intersection with the noise gain curve. The noise gain curve is flat, meaning it is at 0 dB per decade. The rate of closure is thus 20 dB per decade. For a circuit to be considered stable, the rate of closure has to be less than 40 dB per decade. For more information about amplifier stability, see *TI's Precision Labs - Op Amps*.

To verify the power stage and control stability, this reference design has adopted SIMetrix®/SIMPLIS® to build simulation modes to verify the control performance.

図 7 shows the CC control simulation schematic. To keep the system working in CC control mode, V4 provides a DC voltage for D4 to conduct all the time. ISET1 and ISET2 capture the differential voltage across the current sense resistor, E1 is an ideal differential amplifier to output a single-ended signal, R16 and C19 create a low pass filter, and X6 is the error amplifier used to calibrate the current signal to the reference signal.

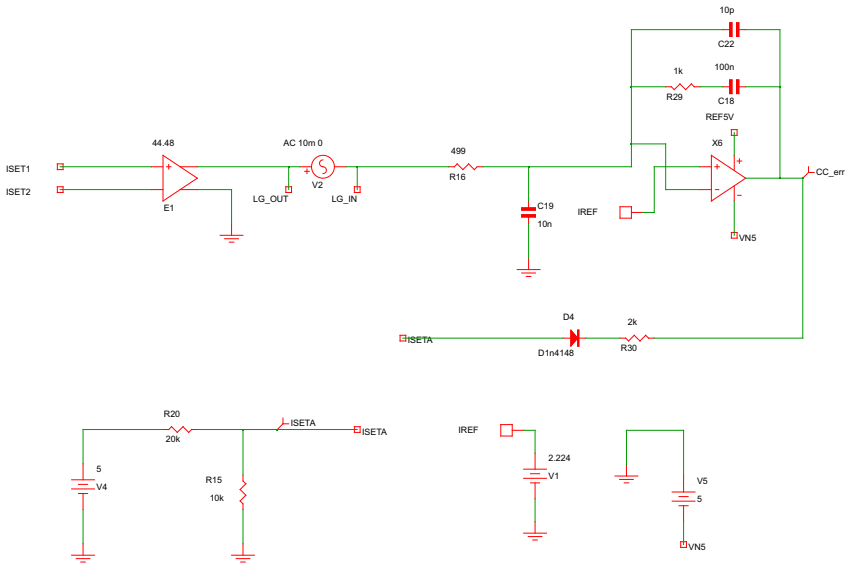


図 7. Constant Current Control Simulation Schematic

図 8 shows the transient simulation result. The "ISETA" pin is clamped to 1.67 V by V4 after power on. With the increase of current, the output of error amplifier X6 decreases, and the CC control circuit takes the control of the system. The final steady current is 50 A, in line with design parameters.

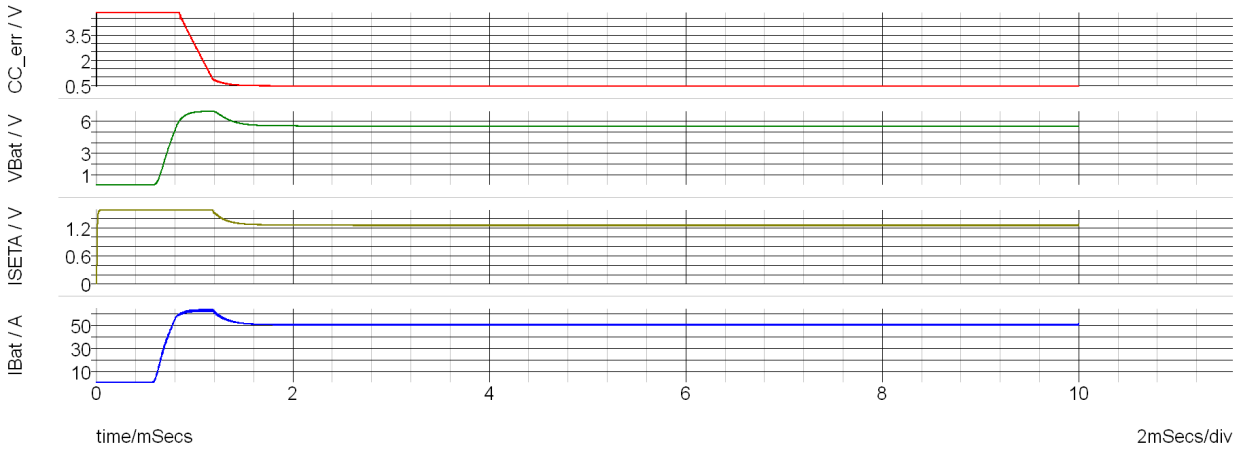


図 8. Constant Current Control Transient Simulation Results

図 9 shows the small signal performance of this CC control subsystem. The gain crossover frequency is 22.15 kHz, and the phase margin is 69.57° which means this control circuit is stable and can provide enough bandwidth.

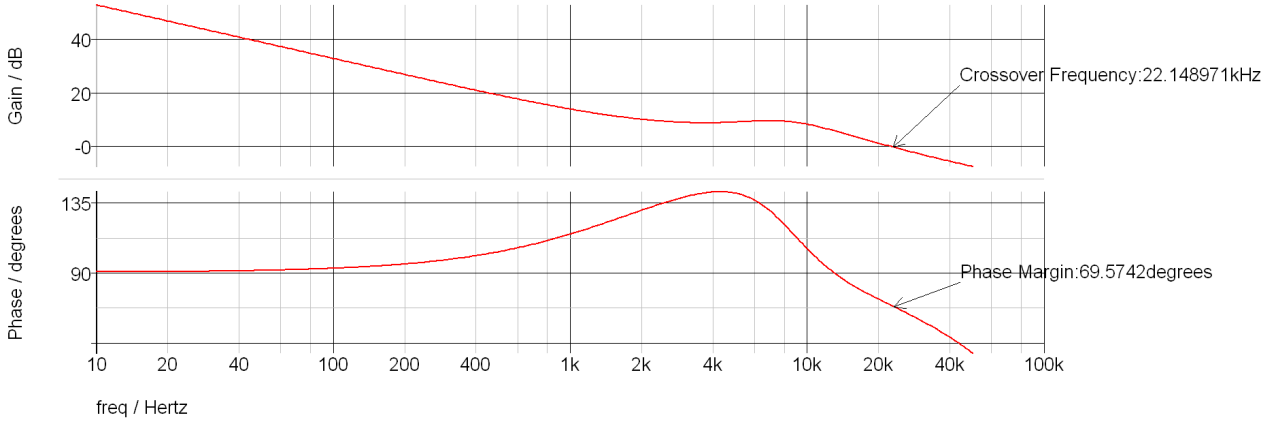


図 9. CC Small Signal Simulation Results

2.3.2 Constant Voltage Control Design

For CV control, the bus voltage at boost mode needs to be monitored, so logic control is used to enable the bus side at boost mode or battery side at buck mode. The buck-boost controller uses the "DIR" command pin to set the work mode. This reference design uses the SN74LV1T00 and SN74LV1T32 devices to enable the different voltage sides.

The LM6142 device is dual high-speed and low-power amplifier that is used for calibrating the battery or bus voltage with the reference control signal. The input offset drift is 3 µV/°C. At the worst case, 5-V output voltage and 125°C, this drift will case 3 µV × 125 / (5 V × 26.7 / 31.12) × 100% = 0.008741157% accuracy error, which can meet the demand of 0.01% accuracy.

For CV control simulation, remove the current control subsystem. 図 10 shows the CV control schematic. R20 and R15 determine the maximum DC current of the system, C12, R2, C20, R19, and C13 consist of a type III compensator to provide enough bandwidth and phase margin. See *Demystifying Type II and Type III Compensators Using Opamp and OTA for DC/DC Converters* for design theory details.

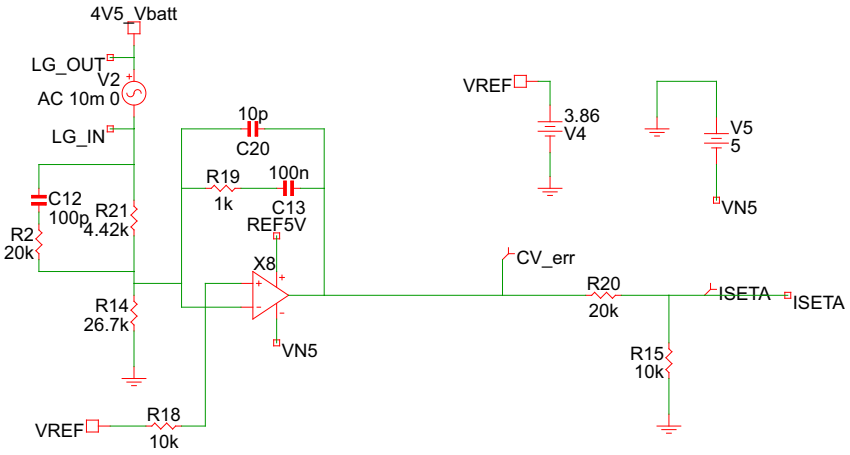


図 10. Constant Voltage Control Simulation Schematic

図 11 shows the transient performance of this subsystem. The final battery voltage is controlled by the reference voltage, as expected.

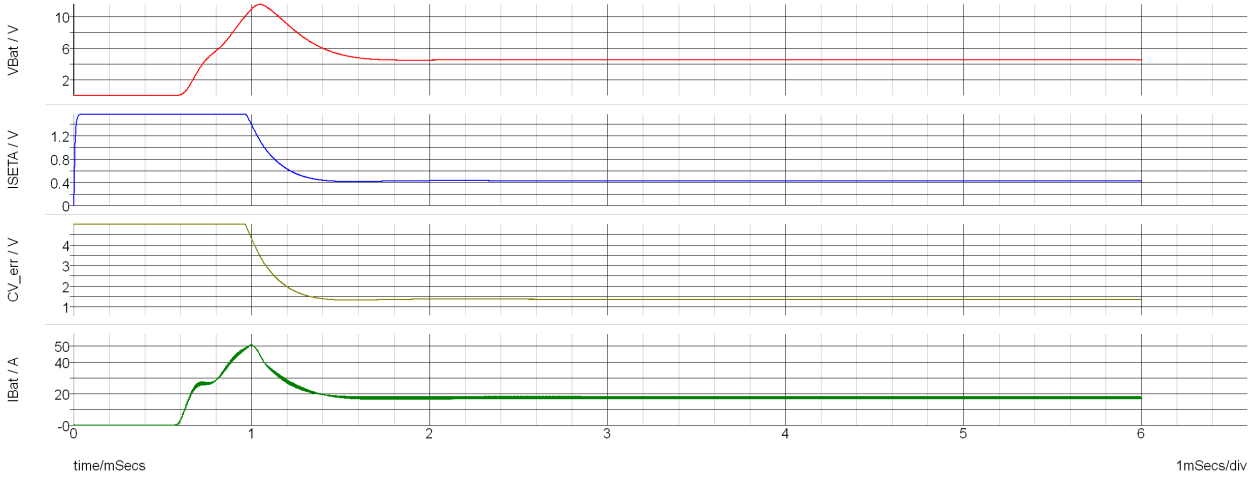


図 11. Constant Voltage Control Transient Simulation Results

図 12 and 図 13 show the steady state and small signal performance under CV control. The gain crossover frequency is 1.01 kHz, and the phase margin is 79.22°, which means the CV control loop is steady.

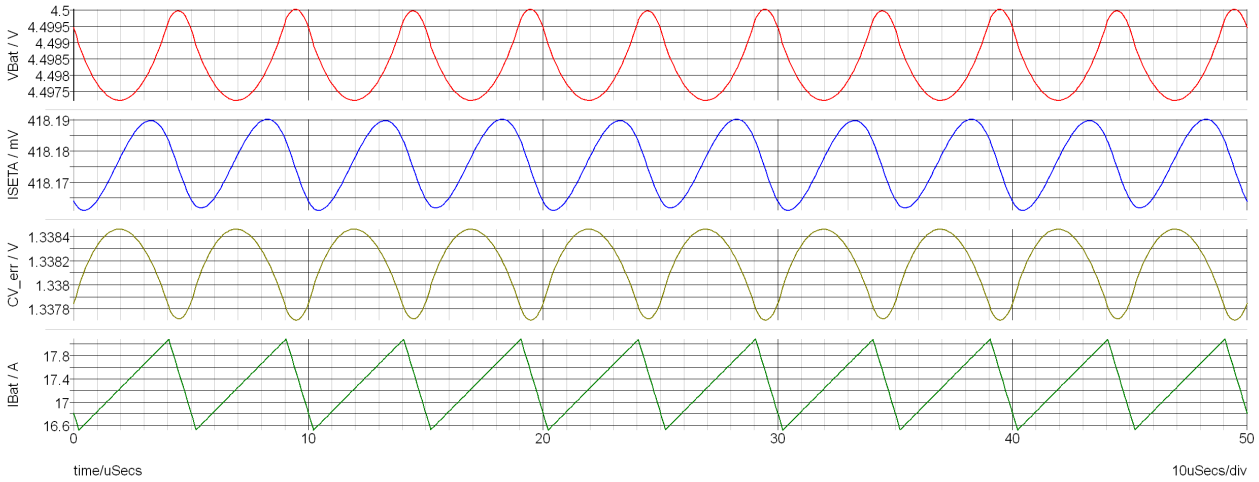


図 12. CV Steady State Simulation Results

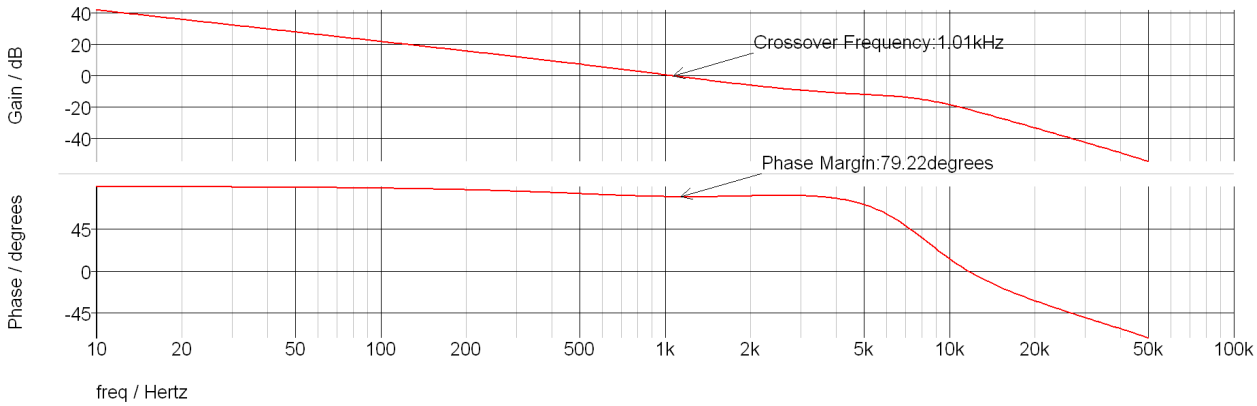


図 13. CV Small Signal Simulation Results

2.3.3 System Simulation

図 14 shows the whole system simulation schematic. CC control and CV control are connected together with R20, R15, D4 and R30. A battery is simulated with the R12Load and C14.

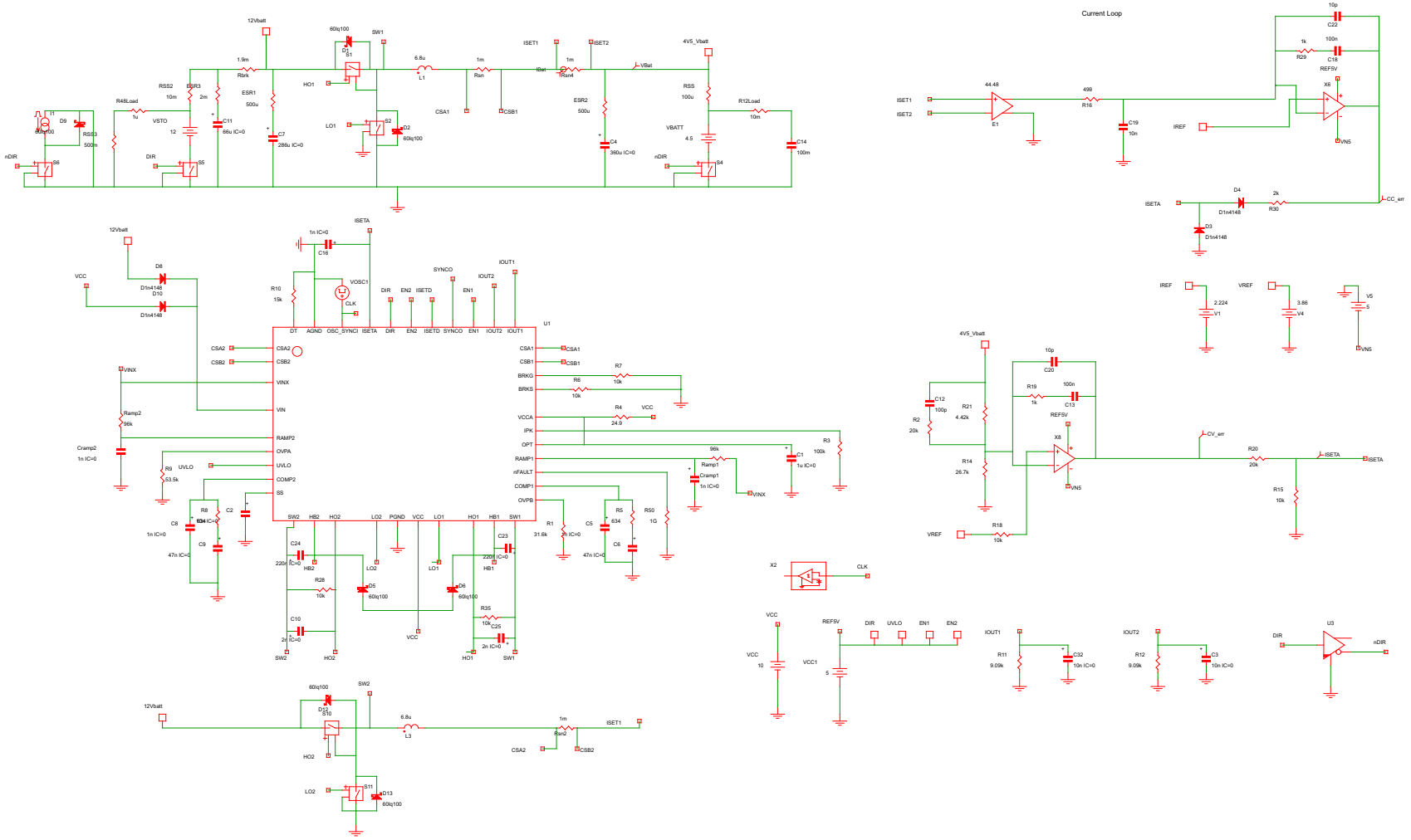


図 14. TIDA01040 System Simulation Schematic

図 15 shows the transient performance of this system. After power on, due to the low voltage at this time, the CV loop outputs high voltage. It provides enough DC voltage for D4 to conduct, and the CC control loop starts taking control of the whole system at about 2 ms. The current keeps a constant 50 A and the battery voltage increases with time. At about 9 ms, the battery voltage reaches near 4.5 V. After this time, the CV control error amplifier decreases the output voltage and it gets the control of the system. The battery current then decreases and the battery voltage keeps steady after the switch from CC control to CV control.

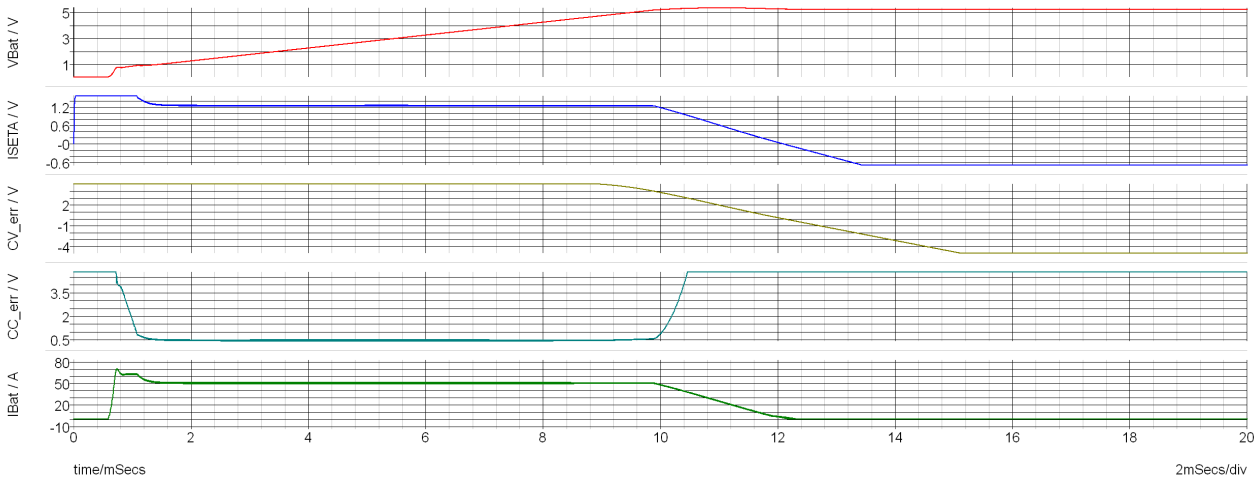


図 15. TIDA01040 System Transient Simulation Results

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Design

3.1.1 Power Bias

図 16 shows the power bias subsystem which supports power for the whole system whether in charge or discharge mode. LM5170 needs a bias voltage of about 10 V, and the amplifiers need ±5 V to calibrate the control signal. The LM5118 device is a wide input, current mode nonsynchronous buck-boost controller which connects to the high- or low-voltage side manually depending on the mode. This is able to provide 10 V for the LM5170 device, LDOs, and switched capacitor voltage converter. In this reference design, U3 and U4 are used to provide isolated 5.0 V to the control subsystem and DAQ subsystem.

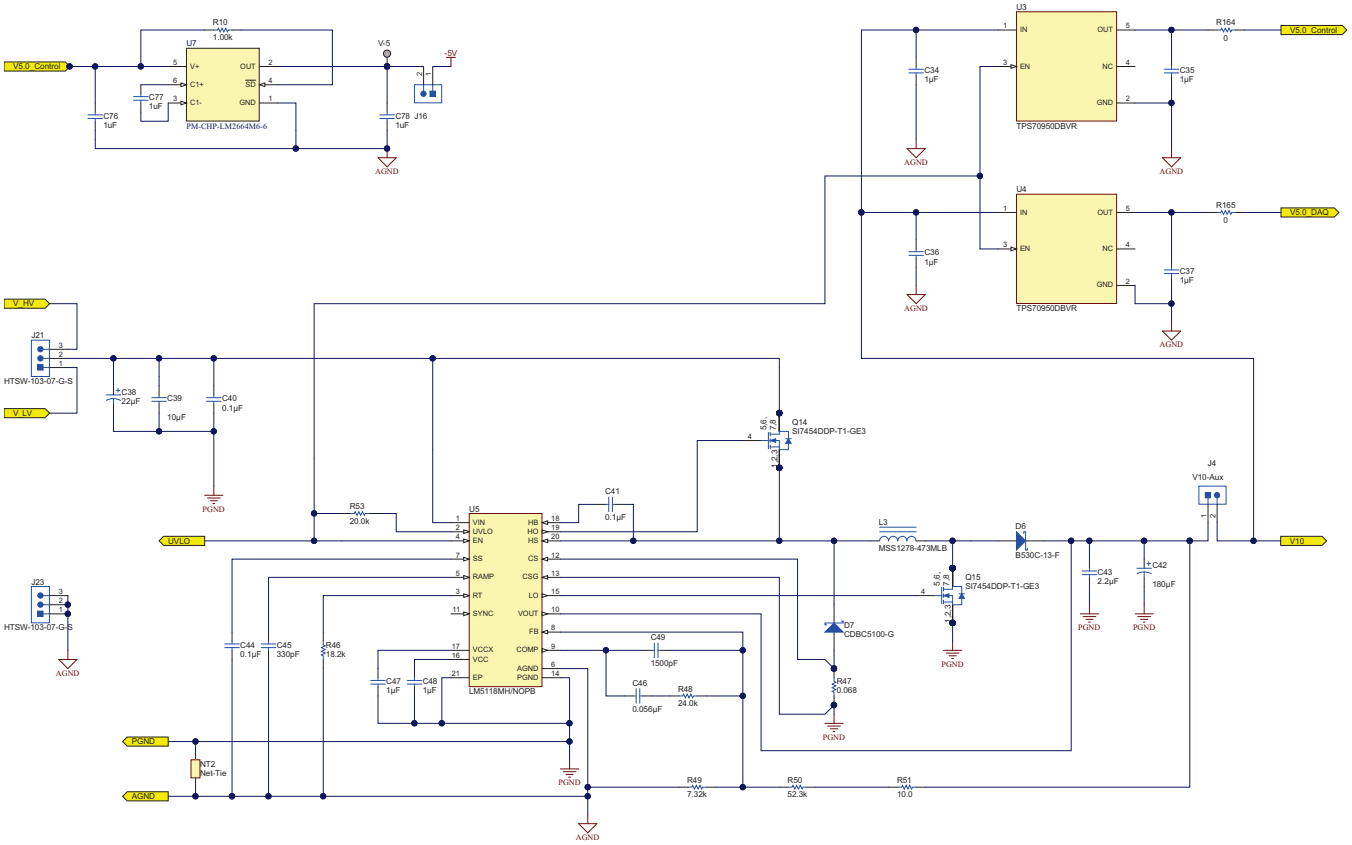


図 16. Power Bias Subsystem

3.1.2 Main Power Convert Stage

図 17 shows the power stage. The power stage can be set to buck or boost mode using the LM5170 device. The two same power stages were connected in parallel to work in higher current applications, as with the parallel MOSFETs. R21, R16, and R22 are high-power current sensing resistors whose temperature coefficients are ±75 ppm/°C. R21 and R22 are used to monitor the current per channel to balance the safety current, while R16 was used to detect the total two phase current to the CC control loop and ADC. The parallel input and output capacitors provide low ESR with enough capacitance. The detailed design guide is found in *LM5170-Q1 Multiphase Bidirectional Current Controller*. This proposed solution can support higher power or current by employing larger inductors, high power MOSFETs, and smaller current sense resistors.

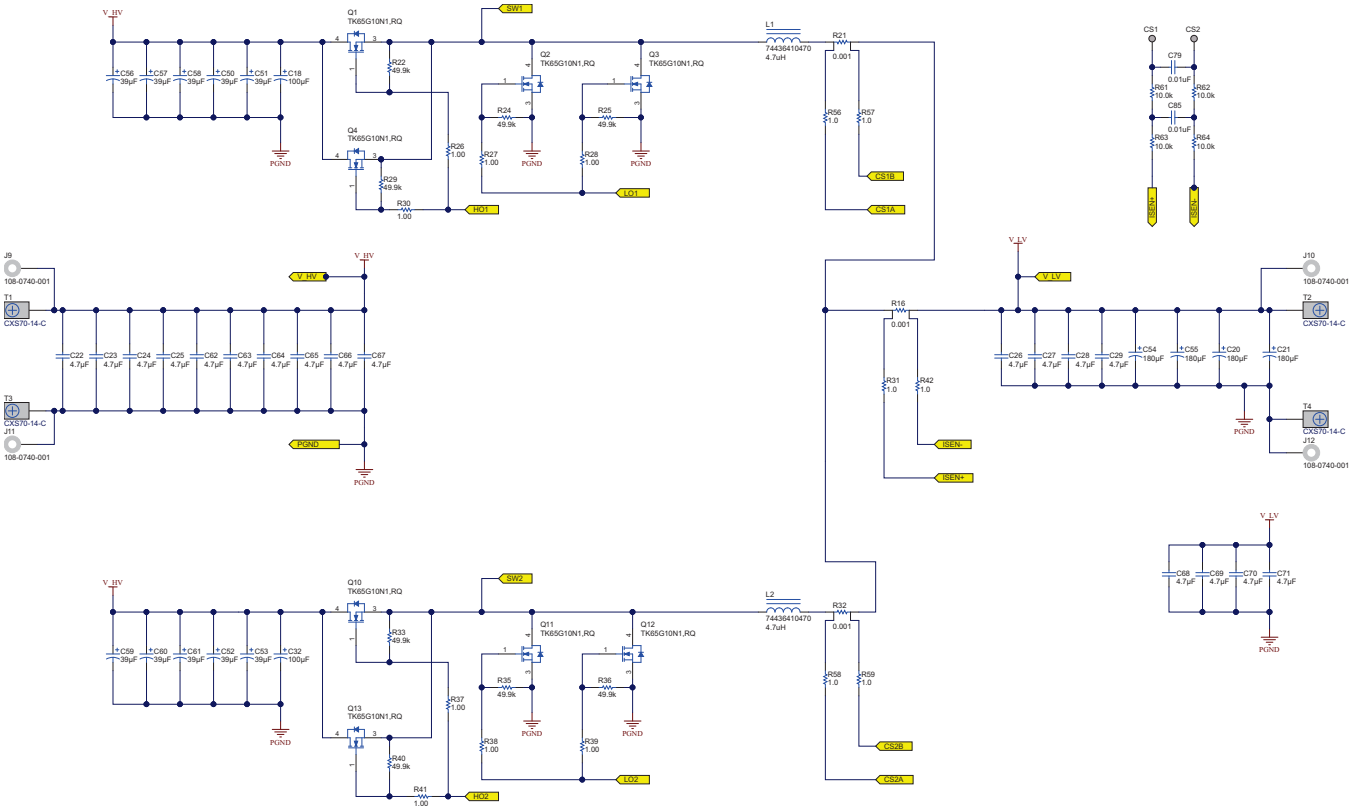


図 17. Main Power Convert Stage Subsystem

3.1.3 LM5170 Subsystem

図 18 shows the LM5170 control schematic. See the *LM5170-Q1 EVM User Guide* and *LM5170-Q1 Multiphase Bidirectional Current Controller Data Sheet* for the detailed design guide. The DIR pin can be used to choose either buck or boost mode. The FB pin delivers the control signal from the CC and CV control loops to the LM5170 device. The SYNCOUT pin, OPT pin, and SYNCIN pin can be used for further multiphase applications.

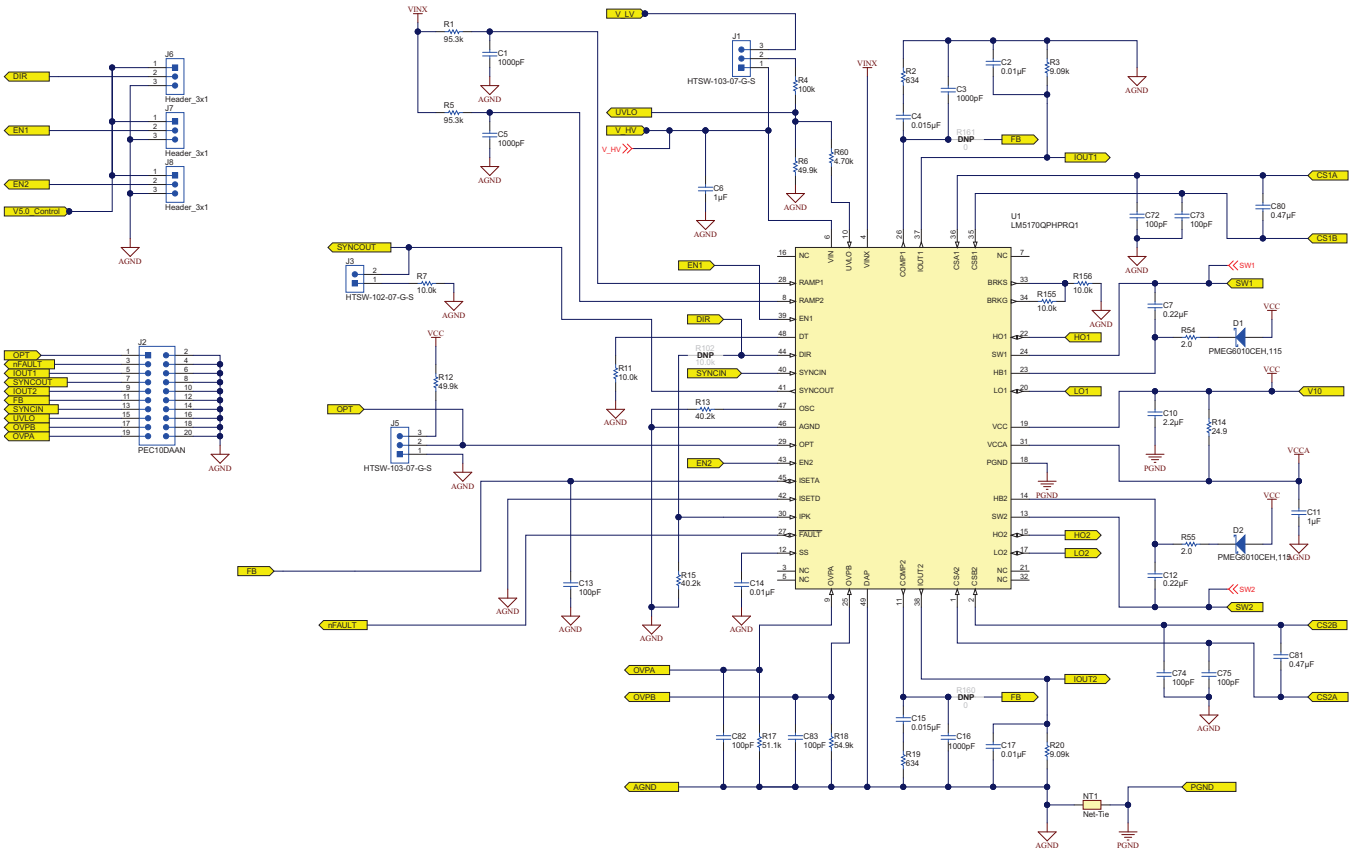


図 18. LM5170 Subsystem

3.1.4 CC Calibration Subsystem

図 19 shows the CC calibration subsystem. The SN74LV4053 device converts the bidirectional current to one direction to be used in the CC control loop. When the DIR pin is high, the whole system works in buck mode. The current flows from "ISEN+" to "1-COM" to "1Y1" to "INA188" to "2Y1" to "2-COM" to "ISEN–". Otherwise in boost mode, the current flows from "ISEN–" to "2-COM" to "2Y0" to "INA188" to "1Y0" to "1-COM" to "ISEN+". INA188 is a zero-drift, rail-to-rail-out instrumentation amplifier, that converts the voltage from the current sensing resistor to a proper value. The gain of the CC control loop is (1 + 2 × 25 kΩ / R70) = 44.48. R71 and C110 form a low-pass filter which can filter significant switching noise from the MOSFETs. The output signal from the filter is compared with the current reference signal through an error amplifier with compensation. At power up, the battery voltage is very low. The CV calibration loop outputs a high voltage to the FB pin. At this time, D3 starts to conduct and the CC calibration loop takes control of the whole system.

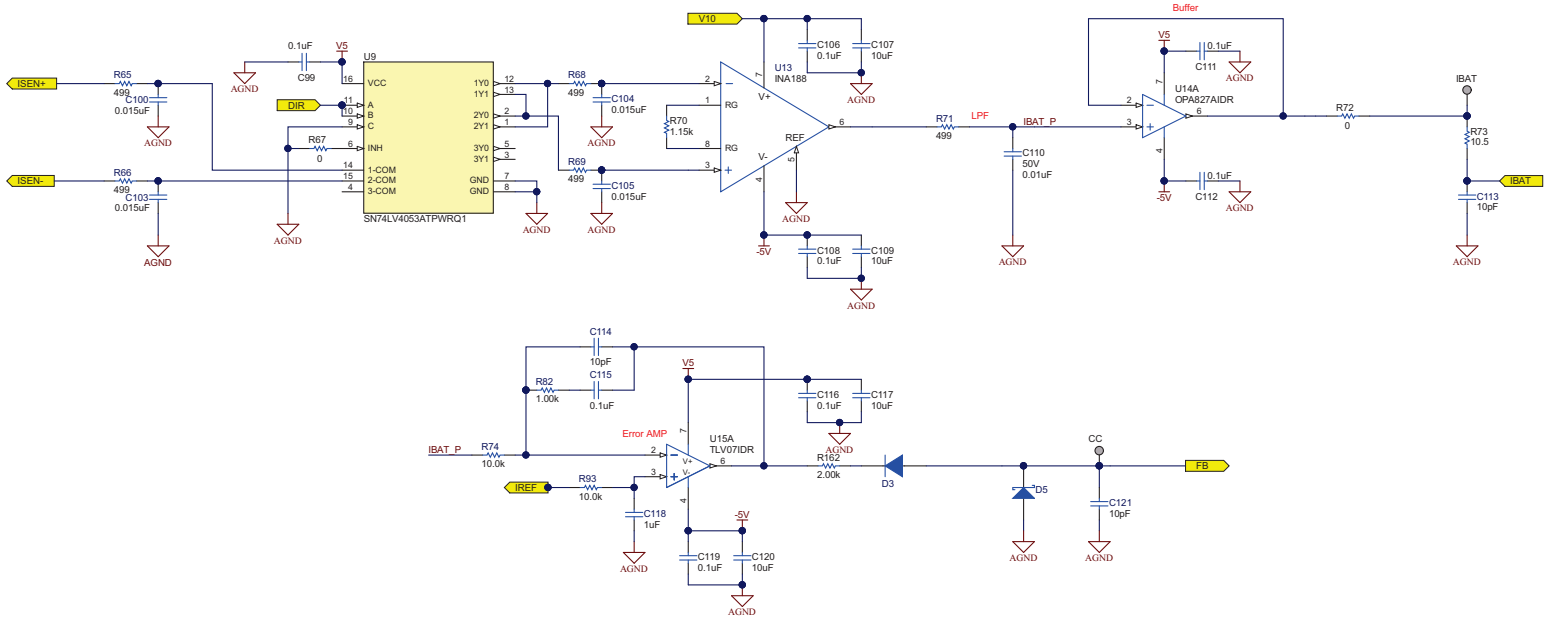


図 19. CC Calibration Subsystem

3.1.5 CV Calibration Subsystem

図 20 shows the battery-side CV calibration subsystem. It needs to monitor the battery side in buck mode and the bus side in boost mode. The logic components U10, U11, and U12 are controlled by the EN1 and DIR signal from the LM5170 device. U2 is a dual-channel high-speed rail-to-rail amplifier which acts as an error amplifier to calibrate the terminal voltage to the reference voltage. When the system works in buck mode, with the increase of the battery voltage, the CV calibration loop starts taking control of the whole system to keep the battery voltage equal to the VREF voltage. Q16 is opened by the startup command (EN and DIR), which allows the VREF signal to rise up slowly. Adjust R84 and C90 values to set the REF ramp up rate which affects the inrush current after power on.

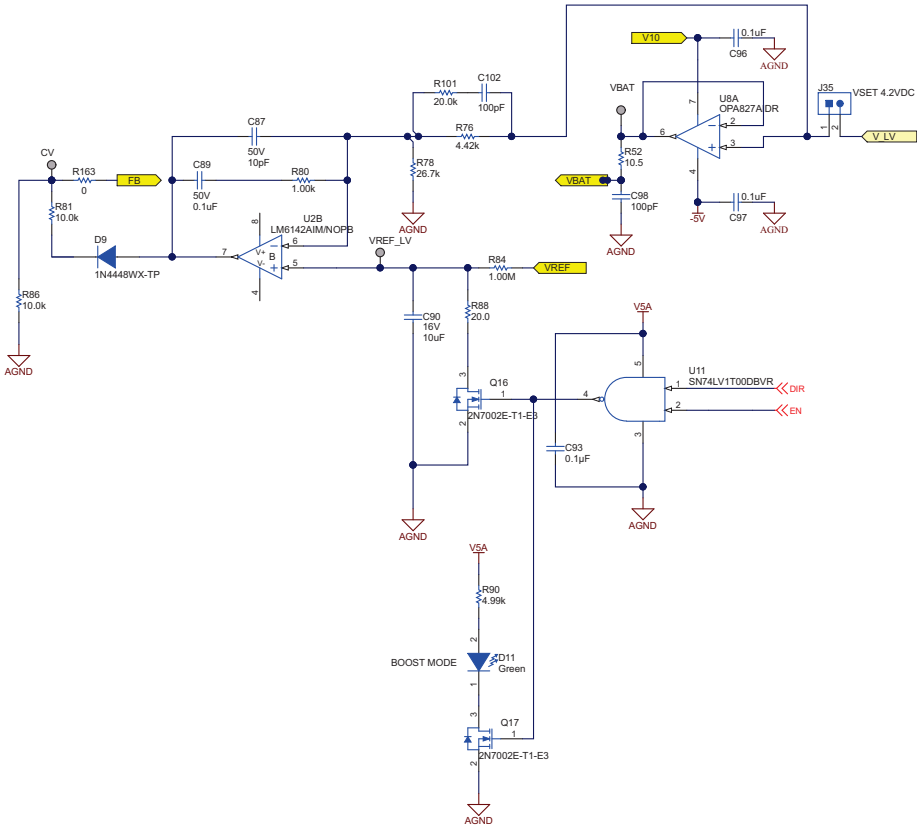


図 20. CV Calibration Subsystem

図 21 shows the system soft start waveform with R84 = 1 MΩ, C90 = 10 µF, and the current setting = 10 A. This result shows that the reference voltage ramps up slowly causing the "ISETA" signal to ramp up slowly as well. This soft start circuit has sharply decreased the inrush current at power on.

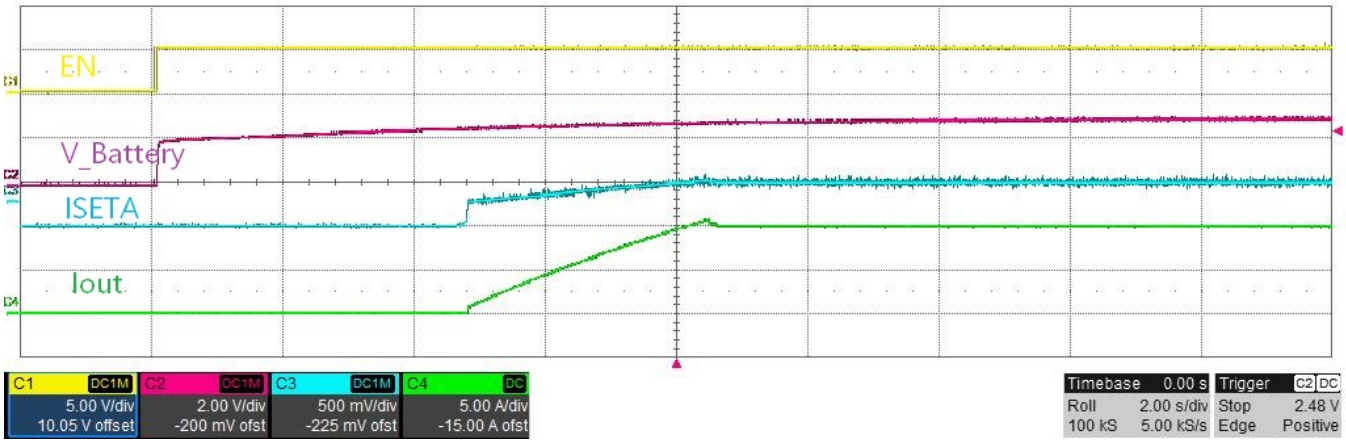


図 21. Soft Start Waveform

There is another software method to achieve this soft start performance: increasing the voltage reference signal slowly at power on instead of giving the final reference voltage immediately.

3.1.6 DAC Subsystem

図 22 shows the DAC subsystem, which provides the reference signals for the CC and CV calibration subsystem. The DAC80004 device is a high-accuracy, low power 16-bit DAC. It can be controlled through the USB2ANY interface. The REF5050 device has great noise performance which provides a 5-V reference voltage for DAC. The OPA2277 device is a high-precision, low-noise amplifier which works as a buffer and changes the output range of the DAC subsystem.

In this schematic, all four channels are connected to the amplifiers to be used to calibrate the offset voltage of the amplifier to achieve better calibration performance. In real applications, only two channels can be used to provide voltage and current reference control signals.

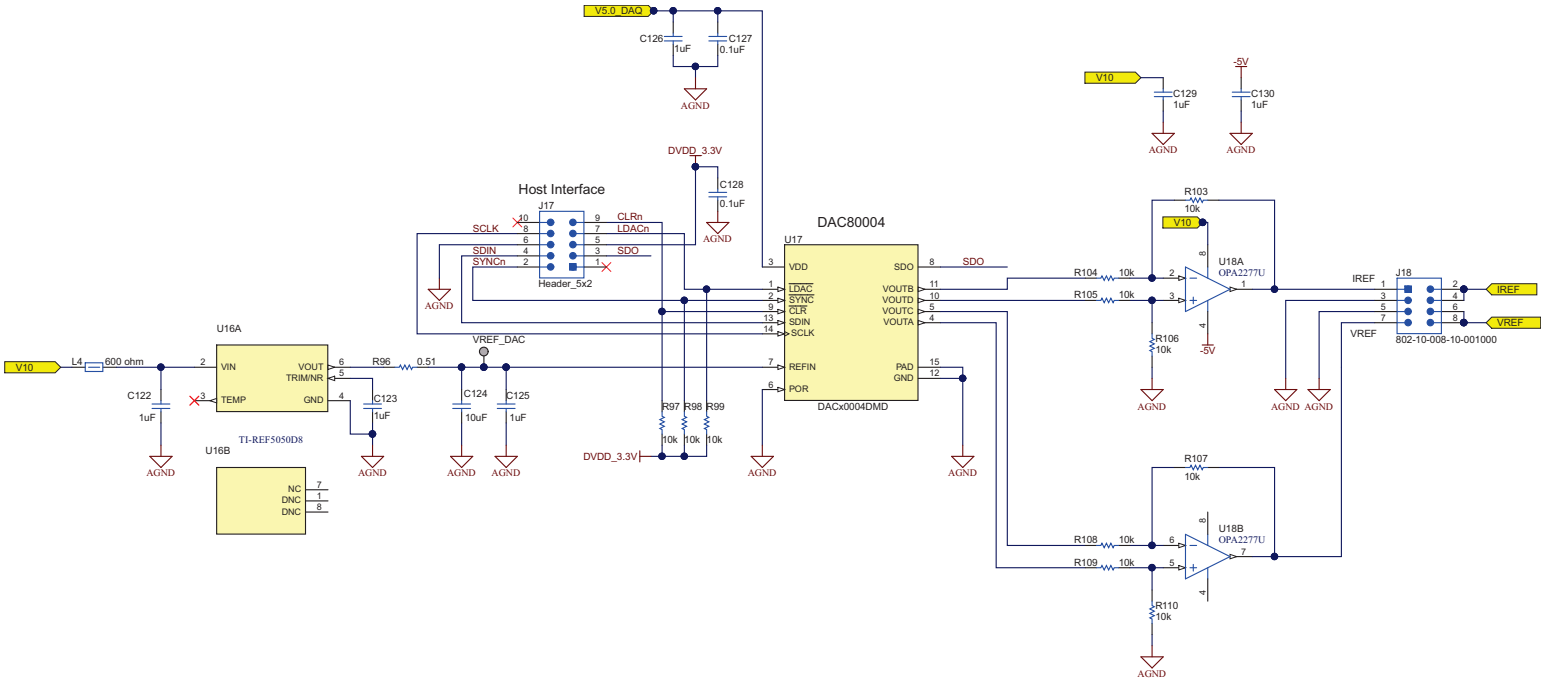


図 22. DAC Subsystem

3.1.7 DAQ Subsystem

図 23 shows the DAQ subsystem that consists of the ADS131A04, THS4561, and REF5025 devices. The THS4561 device can convert the single-ended signal of the battery current and voltage to differential signals and provide suitable gain to drive the ADC. The ADS131A04 device is a 24-bit, 128-kSPS delta-sigma ADC that allows battery parameters to be viewed in the GUI. It uses an onboard MCU, TIVA4, to communicate with the GUI.

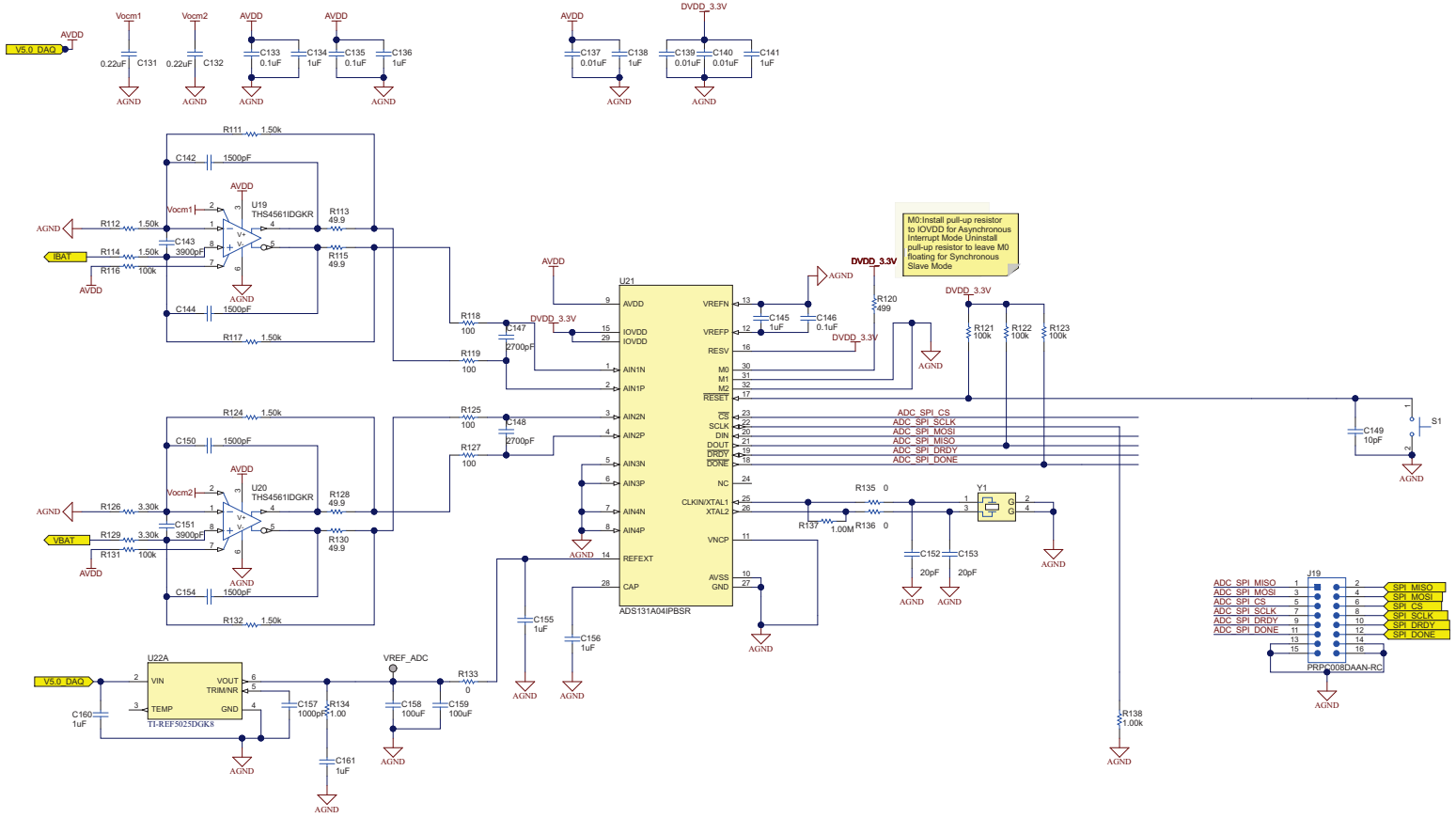


図 23. DAQ Subsystem

図 24 shows how the full driver-ADC subsystem stability simulations are performed.

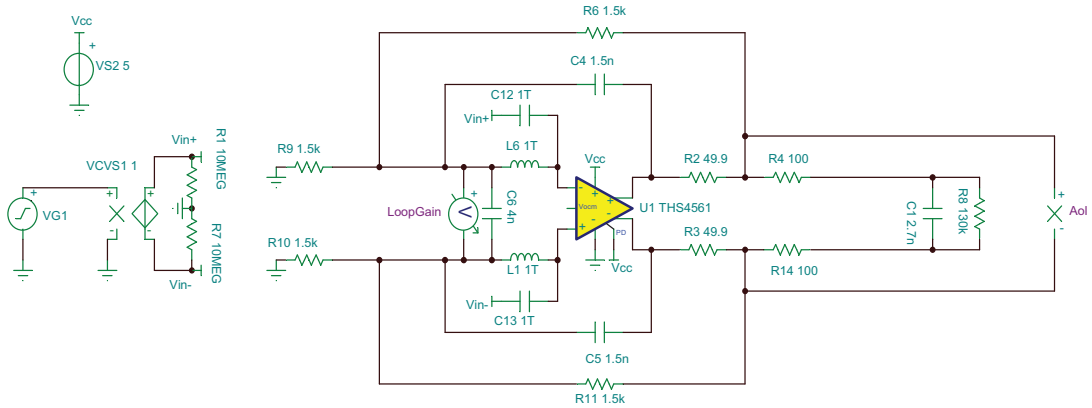


図 24. THS4561 Stability Simulation Schematic

図 25 shows the simulation results of the THS4561 stability. It shows that the crossover frequency is about 9.58 MHz, and the phase margin is about 42.46°. These are indications of a stable circuit. To learn more about amplifier stability, see *TI's Precision Labs - Op Amps*.

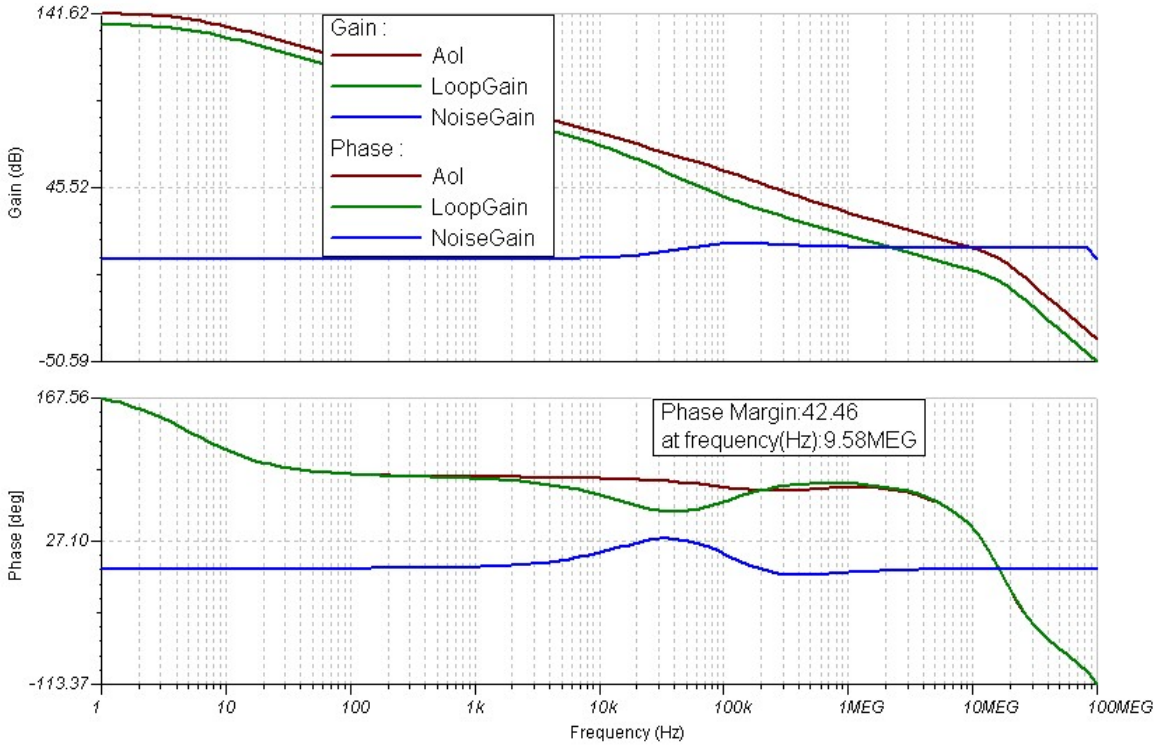


図 25. THS4561 Stability Simulation Results

Transient response simulations are also completed for the THS4561 and INA188 stage to further ensure the proper functionality of this stage. 図 26 shows the output of a 50-mV peak-to-peak, 1-kHz square wave that is put into the circuit. 図 27 displays the results of the transient response of this analog front end stage. As seen, the output is a 2.2-V square wave, which corresponds to the expected gain of 44.48. There is no oscillation present on the output so this stage is considered stable.

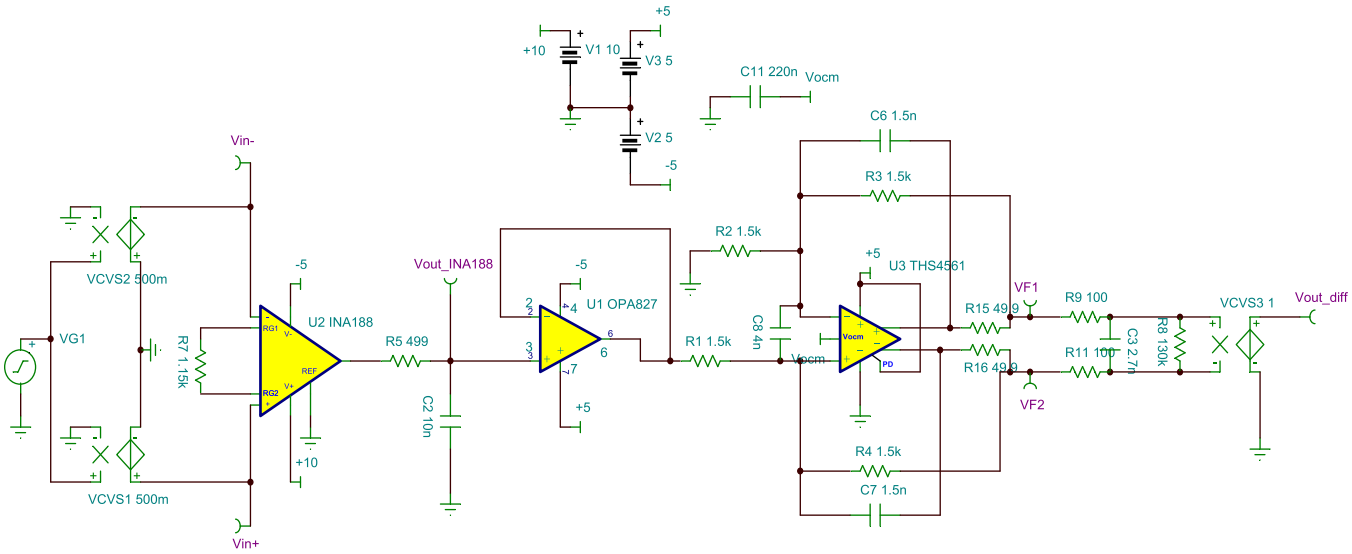


図 26. TIDA-01040 AFE Transient Schematic

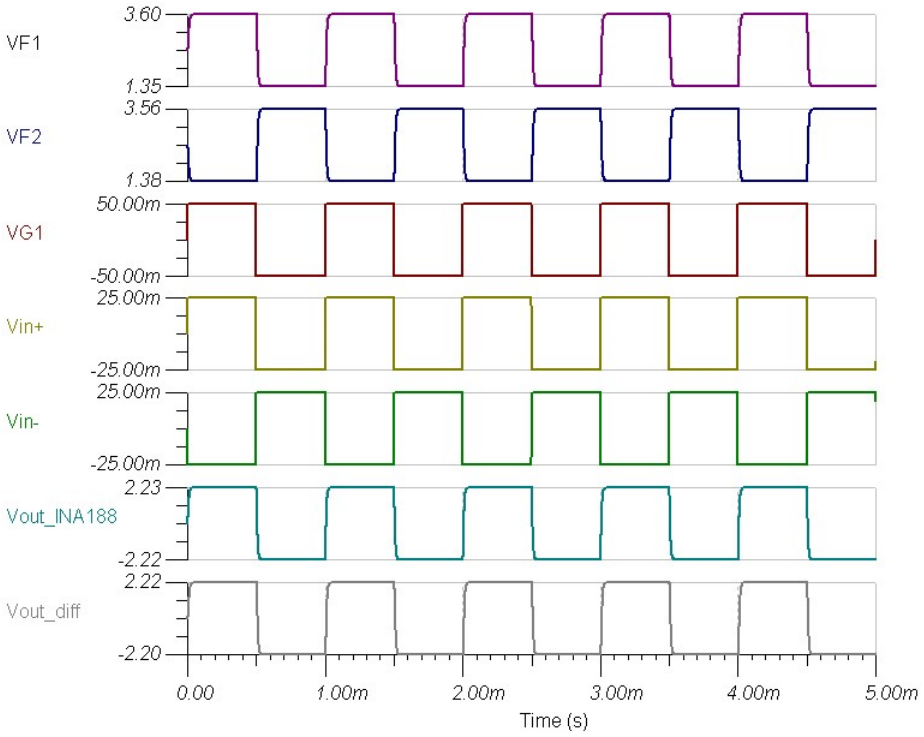


図 27. TIDA-01040 AFE Transient Results

3.2 Software Design

3.2.1 DAC

This reference design uses the USB2ANY interface adapter to communicate with the DAC80004 device to generate a reference signal for current and voltage control. First, open the *USB2ANY Explorer*, click *Select Interface* to choose the SPI, then click the *3.3V ON* button. Click the SPI tab above the Activity Logging section. If the SPI tab does not appear, click around the words "Activity Logging" as sometimes the tabs are hidden. Configure the GUI parameters as shown in 図 28.

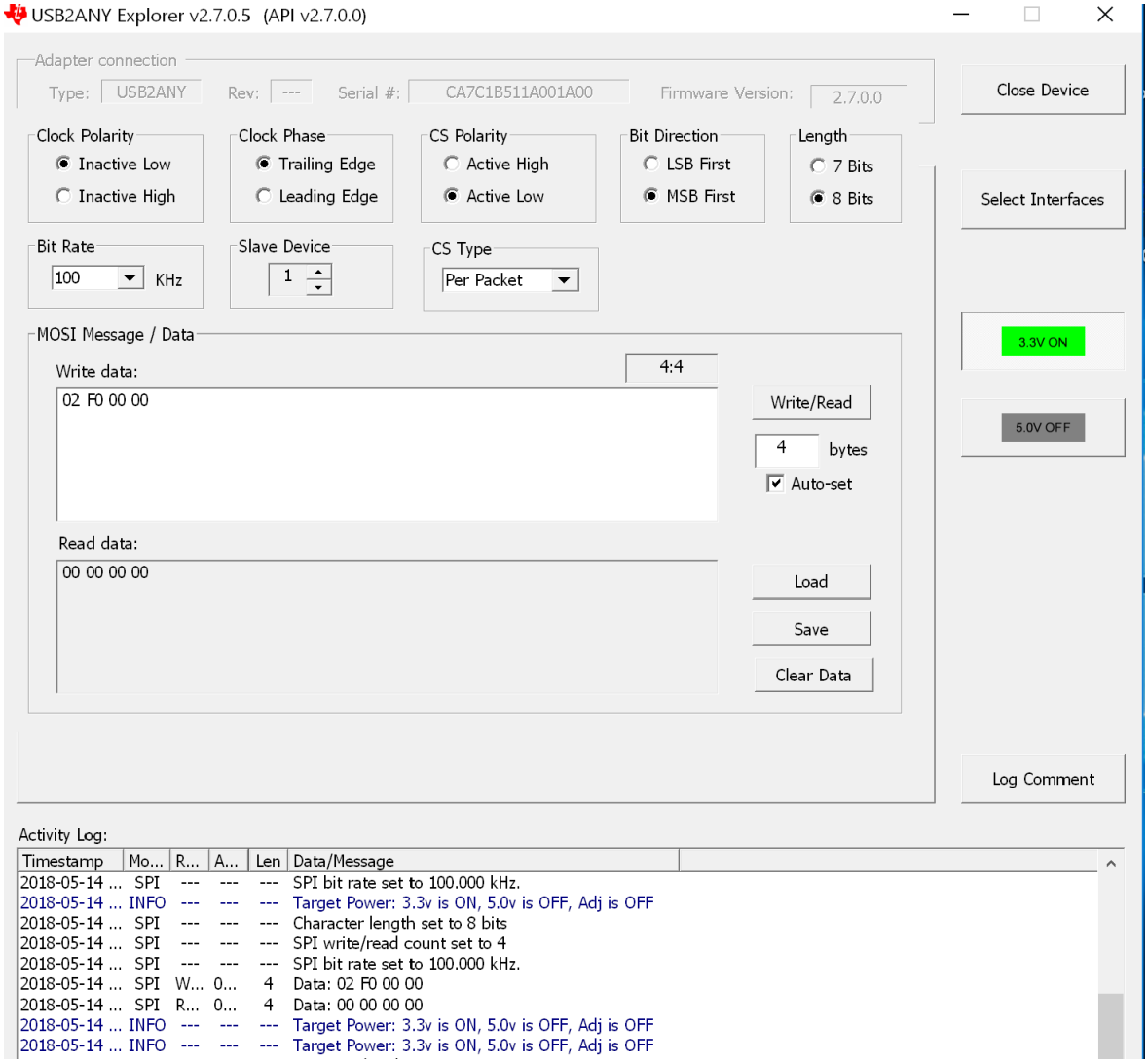


図 28. USB2ANY Configuration

The DAC80004 commands are found in the *DACx0004, Quad 16-,14-,12-Bit, 1 LSB INL, Buffered, Voltage-Output Digital-to-Analog Converters Data Sheet*.

3.2.2 ADC

In this reference design, the *Delta-Sigma ADC Evaluation Software* is used to communicate with the ADS131A04 device. See the *Delta-Sigma ADC EvaluaTIon Software User's Manual* and *ADS131A04 Evaluation Module User's Guide* for detailed information.

After launching this software, click the *Scripts* menu, then click *Predefined* and choose *Basic startup with Datarate @ 8kSPS* as 図 29 shows. Finally, click the *Run* button at the right side of the window.

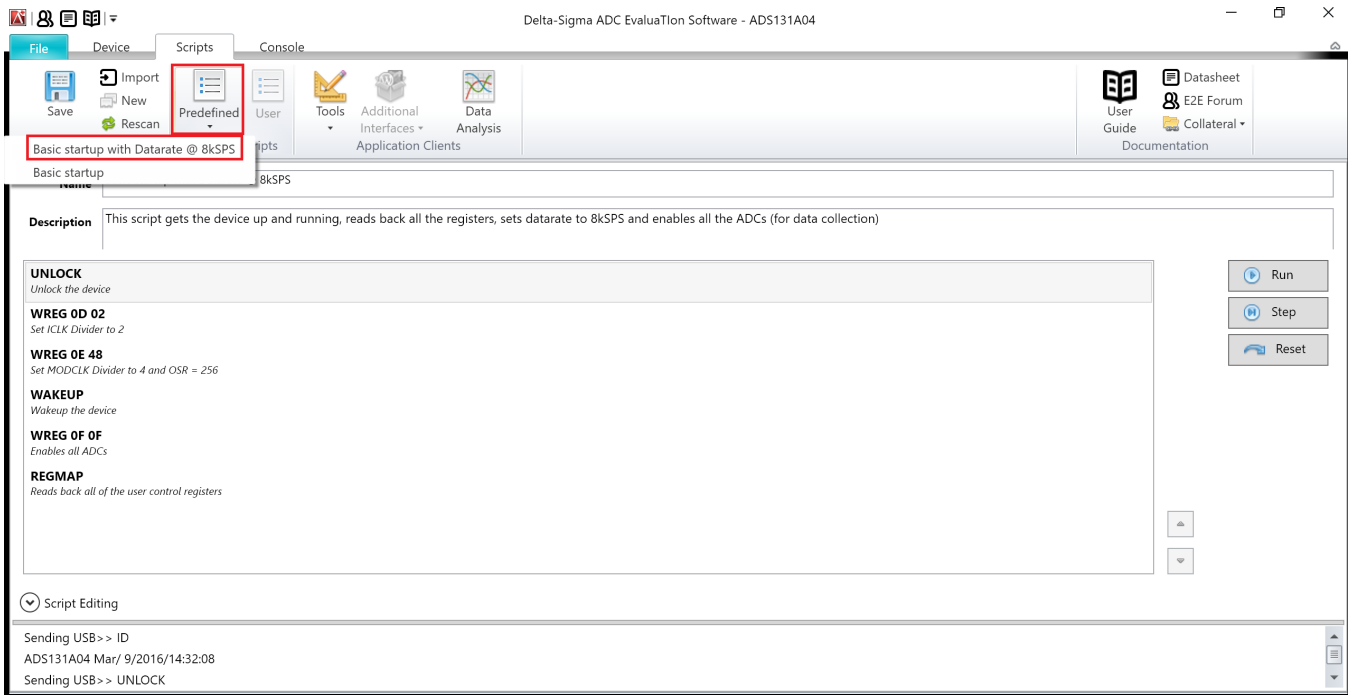


図 29. ADC GUI Setting

The second step is to set the register of the ADC. 図 30 shows the setting with an external reference voltage. It also can modify clock settings and OSR settings.

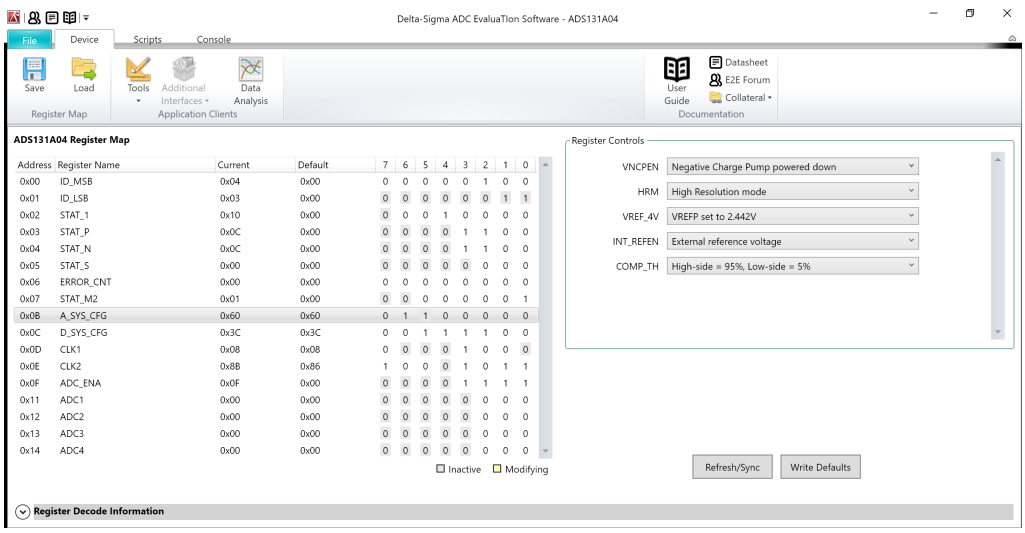


図 30. ADC Register Setting

After setting the GUI and registers, the software can now capture the data: click the *Data Analysis* menu, choose "ADC0" and "ADC1", change the *Clock* and *VRef (V)*, then click the *Collect Data* button as 図 31 shows.

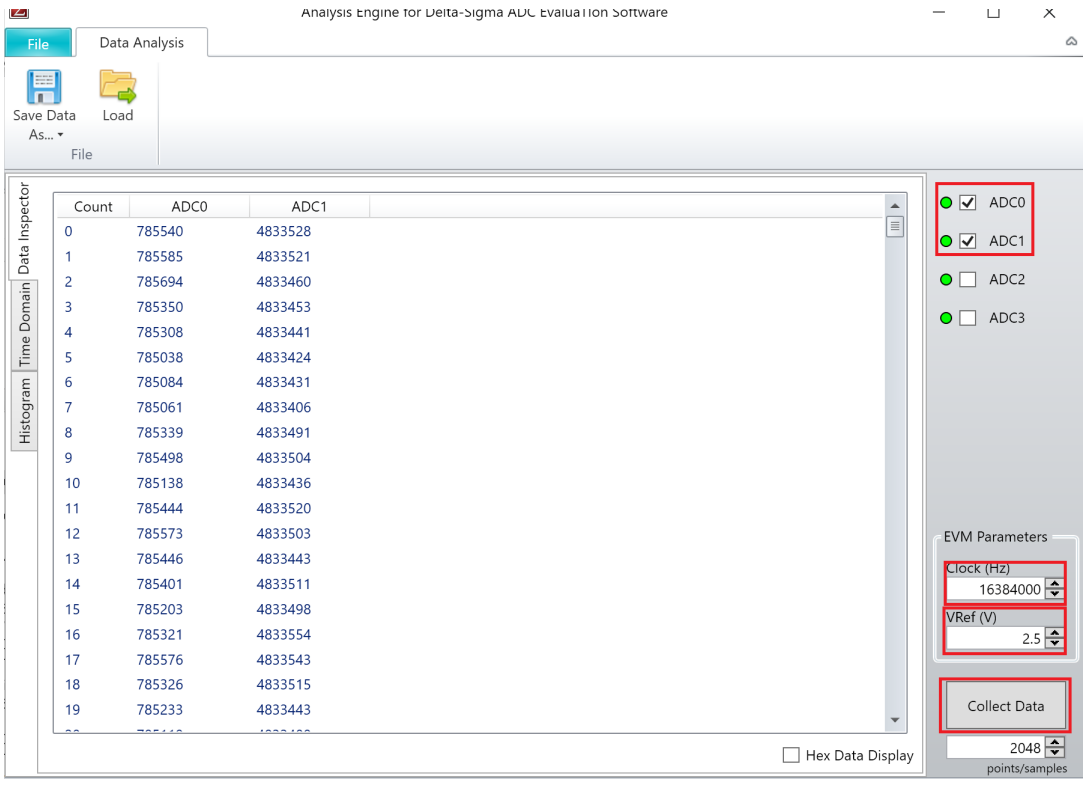


図 31. ADC GUI Collect Data

The raw data is shown on the GUI, but the mean value of current and voltage is needed.

図 32 illustrates the GUI when the *Histogram* menu at the left corner is clicked.

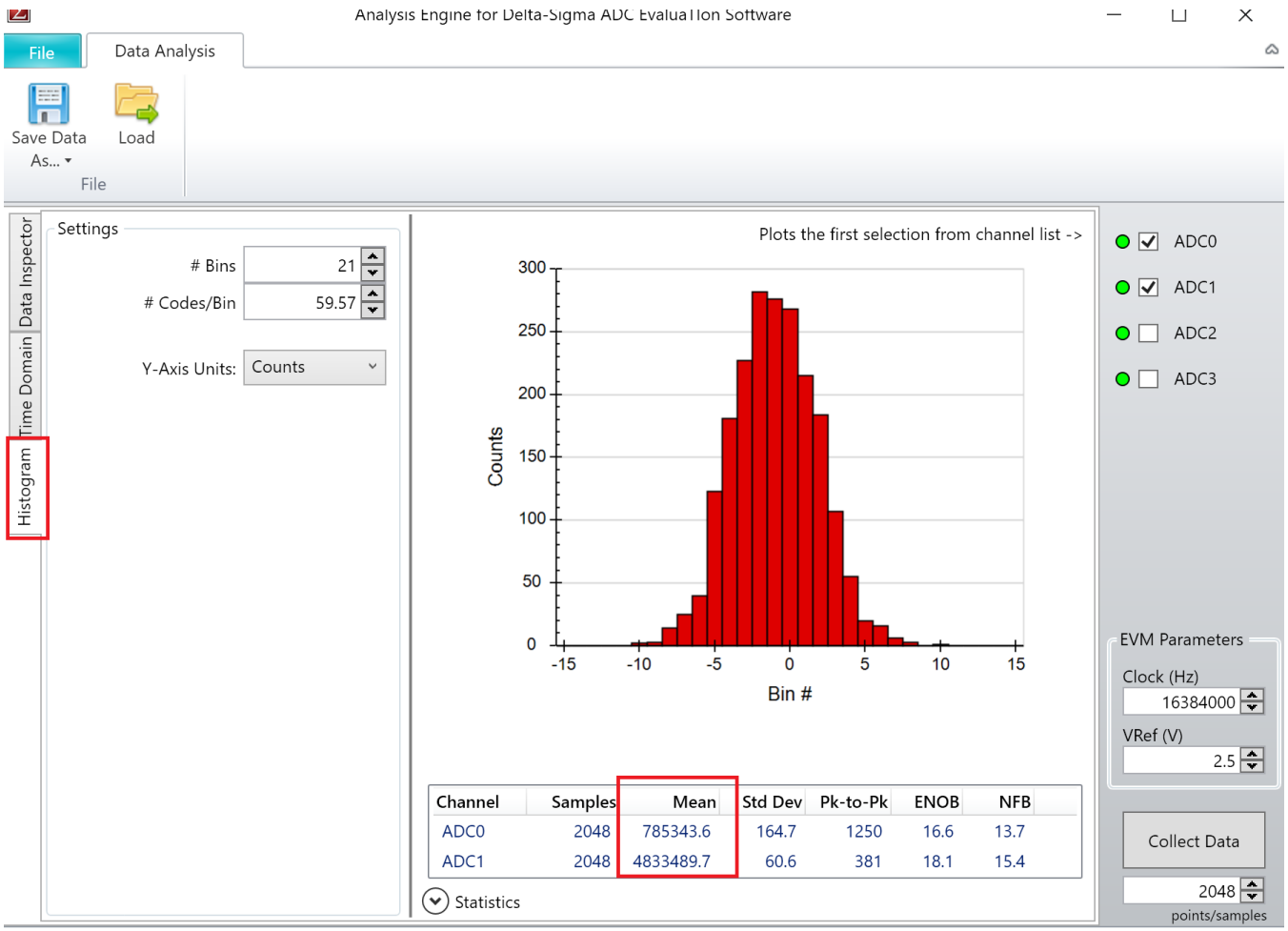


図 32. ADC GUI Data Analysis

図 32 shows the mean value on the bottom after analysis, but this is the full scale format. Divide by 8388607 (DEC of 0X7FFFFF), and multiply by "VRef", then the real current and voltage signal is obtained as 式 1 and 式 2 show. This example was tested under CC control: the control current is 5 A, the battery voltage is 3.1 V.

$$ADC_{current} = \frac{ADC0_{Mean}}{8388607} \times V_{Ref} = \frac{785343.6}{8388607} \times 2.5 \quad V = 234.05 \quad mV \tag{1}$$

$$ADC_{voltage} = \frac{ADC1_{Mean}}{8388607} \times V_{Ref} = \frac{4833489.7}{8388607} \times 2.5 \quad V = 1.4405 \quad V \tag{2}$$

The expected value of channel 0 should be (Iset × Rcs × Gain_INA188 × Gain_ADC0) = 5 A × 1 mΩ × 44.48 × 1 = 222.4 mV, and the expected value of channel 1 should be (Vset × Gain_ADC1) = 3.1 V × (1.5 k/3.30 k) = 1.4091 V. Those values are close to the mean value from the histograms. Due to the offset and noise of the components, refer to 3.3.3.4 to calibrate the ADC. The result is a more accurate value.

3.3 Testing and Results

3.3.1 Getting Started Hardware

This section gives brief information to set up and run the board. 図 33 shows the sections of the board.

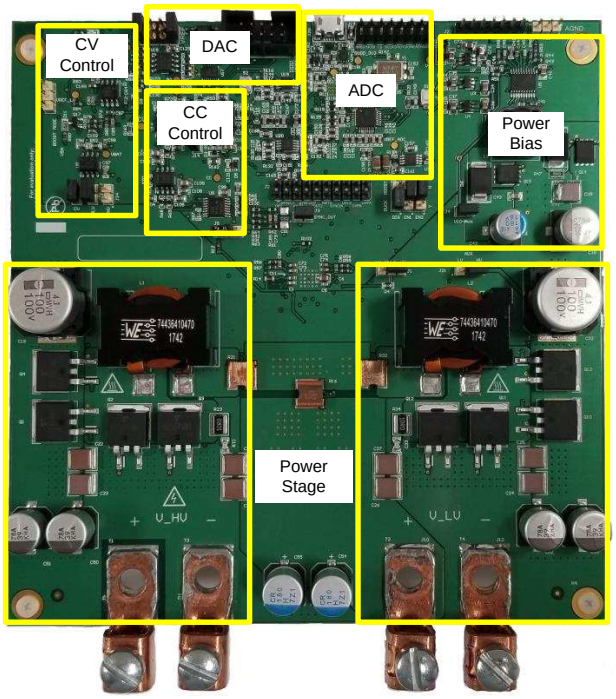


図 33. TIDA-01040 Hardware

This system has some configuration options. 表 5 highlights the purpose of each jumper as well as the default configurations.

表 5. Jumper Configuration

HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J1	UVLO	(1,2)	Enable from V_HV	Y
		(2,3)	Enable from V_LV	
J3	SYNCOUT	(1,2)	Clock output for multiphase configuration	Y
J4	V10-Aux	(1,2)	Auxiliay power	Y
J5	OPT	(1,2)	Multiphase configuration	
		(2,3)	No Multiphase configuration	Y
J6	DIR	(1,2)	BUCK mode	Y
		(2,3)	BOOST mode	
J7	EN1	(1,2)	Onboard CH-1 enable	
		(2,3)	Onboard CH-1 disable	Y
J8	EN2	(1,2)	Onboard CH-2 enable	
		(2,3)	Onboard CH-2 disable	Y
J14	V5	(1,2)	Enable power supply for CC control	Y
J18	IREF/VREF	(1,2),(7,8)	Enable DAC output signal for CC/CV control loop	Y
J34	V_HV	(1,2)	Enable CV control for bus voltage(V_HV)	N
J35	V_LV	(1,2)	Enable CV control for battery voltage(V_LV)	Y
J37	V5A	(1,2)	Enable power supply for CV control	Y

3.3.2 Test Setup

The test setup for a bidirectional charge and discharge converter requires a different setup for current and voltage control loop tests. 図 34 shows a block diagram of the hardware setup for the TIDA-01040 current control loop test.

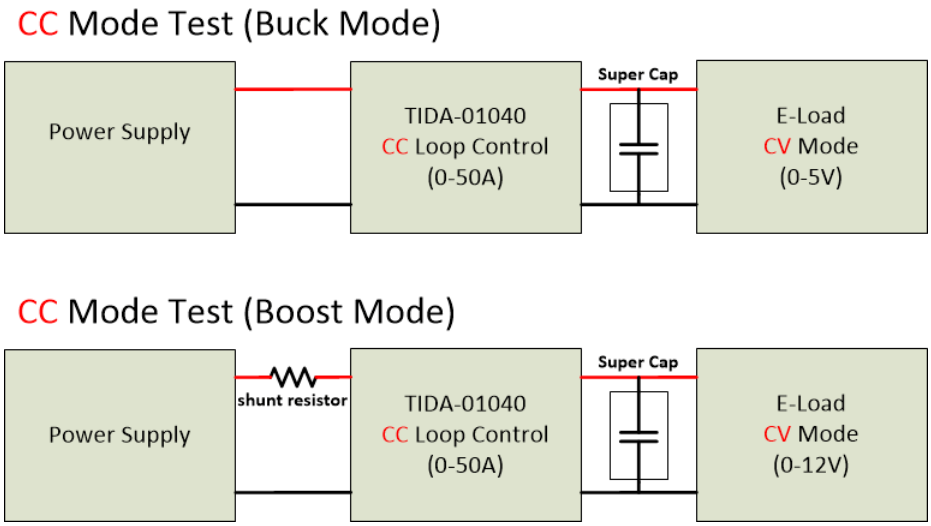


図 34. Current Control Test Block Diagram

The power supply must be able to provide enough power in both charge and discharge mode. Configure the TIDA-01040 board to BUCK or BOOST mode through the "DIR" header (J6). Then set current and voltage control signals to control loop. Configure the electronic load to operate in CV mode whose value should be smaller than the voltage set by the DAC. The CV control loop will give enough forward voltage for D3, and the system can work in CC mode. The super capacitor is required to clamp the output voltage and simulate the battery performance.

The reason for connecting a shunt resistor in BOOST mode is for monitoring the current flow out from the battery (discharging current). In BUCK mode, it is easy to read the current flow into battery (charging current) on the electronic load.

図 35 shows the block diagram of the hardware setup for the TIDA-01040 voltage control loop test.

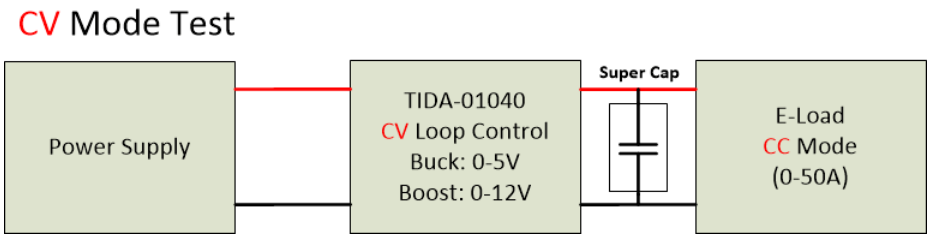


図 35. Voltage Control Test Block Diagram

When testing the CV control performance, configure the system to work in CV mode. Configure the electronic load to operate in CC mode with a value smaller than the current value set by DAC.

3.3.3 Test Results

3.3.3.1 Current Control Accuracy

The current accuracy depends on the current sensing resistor, the gain, offset, and drift of the current amplifier, INA188, and TLV07 devices. These parameters vary from device to device. To achieve good current control accuracy, the total gain and the offset of the designed circuit must be calibrated. Because high temperature effects the drift of some device in the system, the relationship between the current control signal and the real output current is not linear. Three point data is used to calibrate the CC control considering the drift in a high current situation. In buck mode, the battery current is 5.479 A if the DAC current reference signal code is 3229(DEC). The battery current is 34.932 A if the DAC current reference signal code is 20522(DEC), and the battery current is 49.942 A if the DAC current reference signal code is 29360(DEC). From these three test results, the real gain and offset can be calculated as follows:

$$\text{Gain1} = \frac{(I_{out2} - I_{out1})}{(DAC_{code2} - DAC_{code1})} = \frac{34.932\ A - 5.479\ A}{20522 - 3229} = 0.001700225\ A \quad (3)$$

$$\text{Offset1} = I_{out1} - \text{Gain1} \times DAC_{code1} = 5.479\ A - 0.001700225\ A \times 3229 = -0.011026958\ A \quad (4)$$

$$\text{Gain2} = \frac{(I_{out3} - I_{out2})}{(DAC_{code3} - DAC_{code2})} = \frac{49.942\ A - 34.932\ A}{29360 - 20522} = 0.001704133\ A \quad (5)$$

$$\text{Offset2} = I_{out2} - \text{Gain2} \times DAC_{code2} = 34.932\ A - 0.001704133\ A \times 20522 = -0.091333333\ A \quad (6)$$

The current accuracy in boost mode can be calibrated with the same method. Using the gain and offset, the output current value can be determined and compared to the actual test output current.

図 36 shows the full scale (FS) CC control accuracy of this reference design at buck (high side is 12 V, low side is 1 V) and boost (low side is 2 V, high side is 10 V) mode conditions. The output is controlled within 0.01% in the whole range.

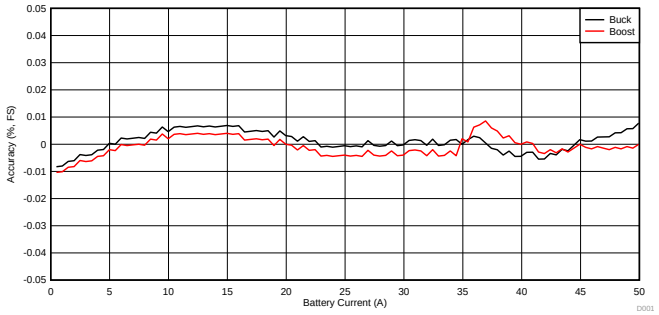


図 36. CC Control Accuracy

To know the whether a change in voltage has any effect on the CC control accuracy, 表 6 shows test current under different battery voltage and different current settings. The tested data shows that the voltage setting has very little effect on the current control.

表 6. CC Control with Different Battery Voltage

	I_{SET}				
$V_{Battery}$ (V)	10 A	20 A	30 A	40 A	50 A
0.5	9.976	19.966	29.96	39.958	49.968
1	9.976	19.966	29.96	39.958	49.968
1.5	9.976	19.966	29.96	39.958	49.968
2	9.976	19.966	29.96	39.958	49.97
2.5	9.976	19.966	29.96	39.958	49.97
3	9.976	19.966	29.96	39.958	49.97

表 6. CC Control with Different Battery Voltage (continued)

	I_{SET}				
$V_{Battery}$ (V)	10 A	20 A	30 A	40 A	50 A
3.5	9.976	19.966	29.96	39.958	49.972
4	9.976	19.966	29.96	39.958	49.972
4.5	9.976	19.966	29.96	39.958	49.972
5	9.976	19.966	29.96	39.958	49.973

3.3.3.2 Voltage Control Accuracy

The voltage control accuracy of this system depends on the gain offset, offset of the resistor division, and the LM6142 device. This also requires calibration to achieve good voltage control accuracy. Because the voltage control subsystem is far away from the main power stage, use a simplified two points calibration method to calibrate the gain as 式 7 and 式 8:

$$\text{Gain} = \frac{(V_{out2} - V_{out1})}{(DAC_{code2} - DAC_{code1})} = \frac{3996.49\ \text{mV} - 998.79\ \text{mV}}{44982 - 11245} = 0.088854966\ \text{mV} \quad (7)$$

$$\text{Offset} = V_{out1} - \text{Gain} \times DAC_{code1} = 998.79\ \text{mV} - 0.088854966\ \text{mV} \times 11245 = -0.3840967\ \text{mV} \quad (8)$$

After calibration, the calculated output voltage can be compared with the actual test output voltage. 図 37 shows the accuracy of CV control at buck mode (high side 12 V, output current 10 A).

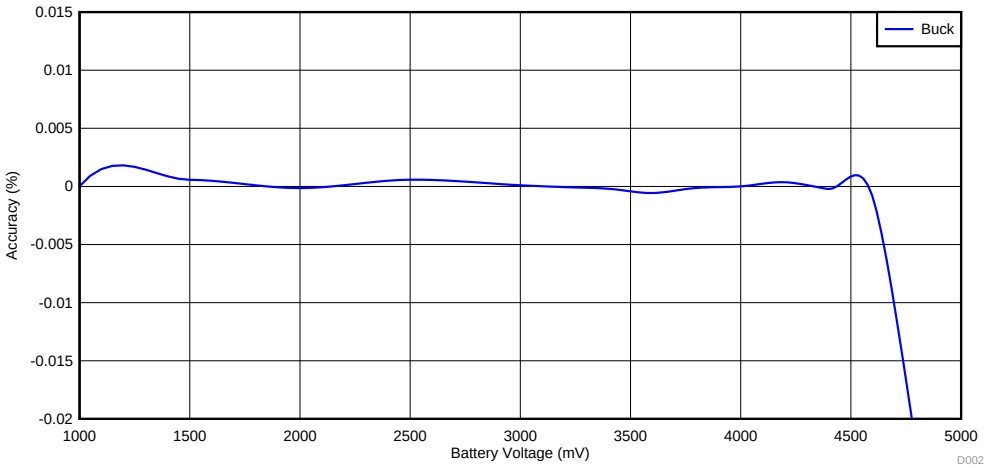


図 37. CV Control Accuracy

To determine whether the CV control accuracy will change with different current conditions, these conditions must be tested. 表 7 shows the different calibrated gain and offset values at different currents.

表 7. CV Control Calibration Under Different Current

CURRENT (A)	GAIN	OFFSET
10	0.089015028	–0.073989981
20	0.089012064	–1.840658624
30	0.089006136	–3.57399591
40	0.089001921	–5.484399232
50	0.088994807	–7.164402077

図 38 and 図 39 show the linear relationship between gain and offset with current.

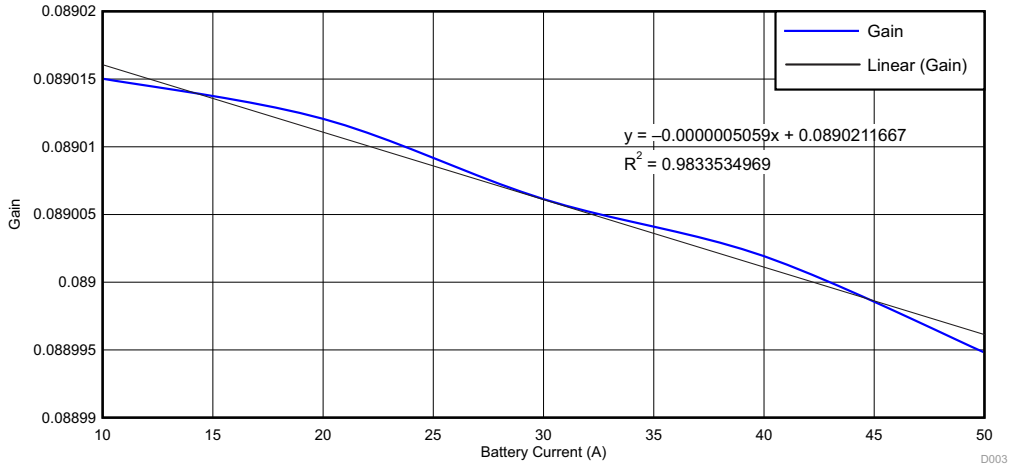


図 38. CV Calibration Gain vs Current

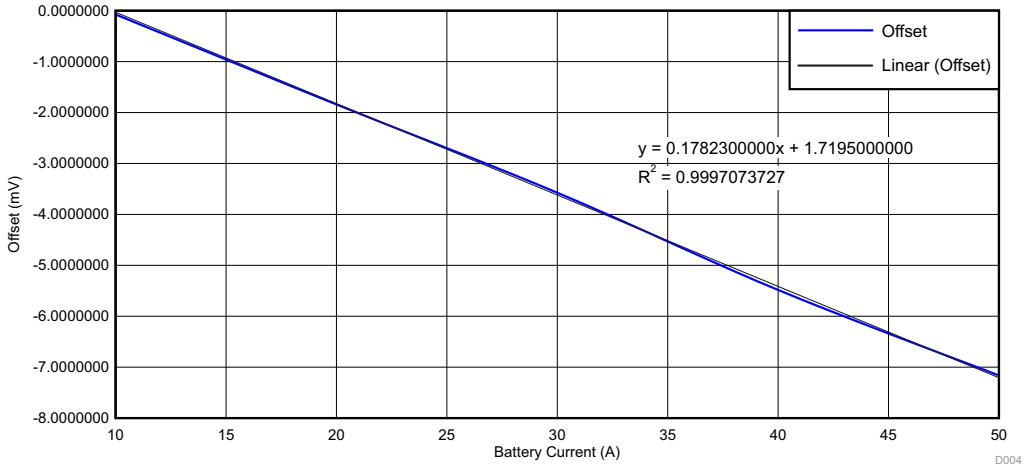


図 39. CV Calibration Offset vs Current

Use the equations in 図 38 and 図 39 to get the new gain and offset values under different currents. 表 8 shows some sample values.

表 8. CV Control Updated Calibration Under Different Current

CURRENT (A)	GAIN	OFFSET
10	0.089016108	–0.0628
20	0.089011049	–1.8451
30	0.08900599	–3.6274
40	0.089000931	–5.4097
50	0.088995872	–7.192

Using the updated gain and offset, obtain the updated CV control accuracy with different current as 図 40 shows. The results show the CV control can almost maintain 0.01% accuracy within the whole battery voltage range (1.0 V–4.5 V).

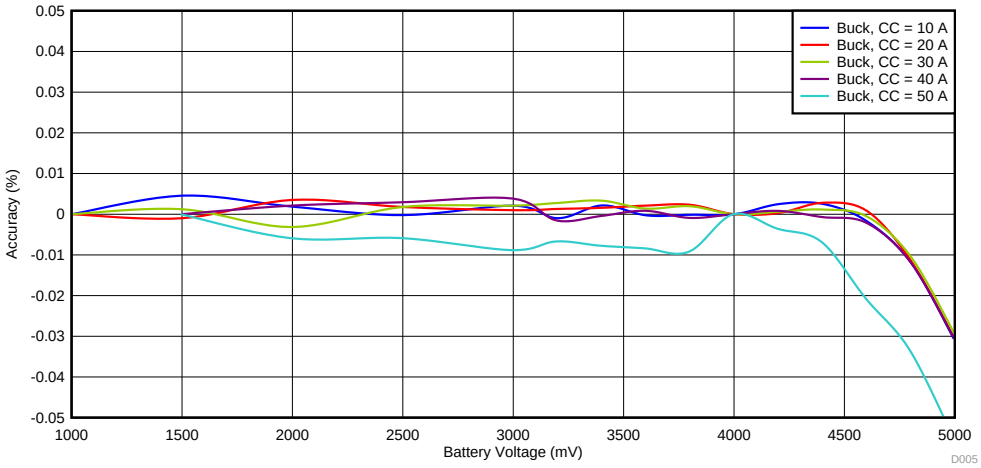


図 40. CV Control Accuracy With Different Current

3.3.3.3 CC, CV Transformation

The complete battery formation profile should include both the CC control and the CV control. It is critical to understand the performance of the system when transforming from CC mode to CV mode. 図 41 and 図 42 show the transformation under different current and different voltage settings.

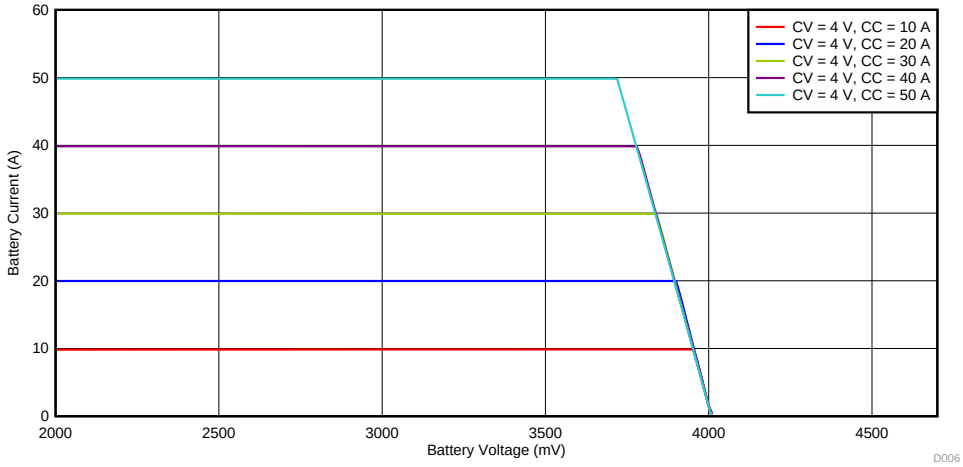


図 41. CC, CV Transformation Under Different Current Setting

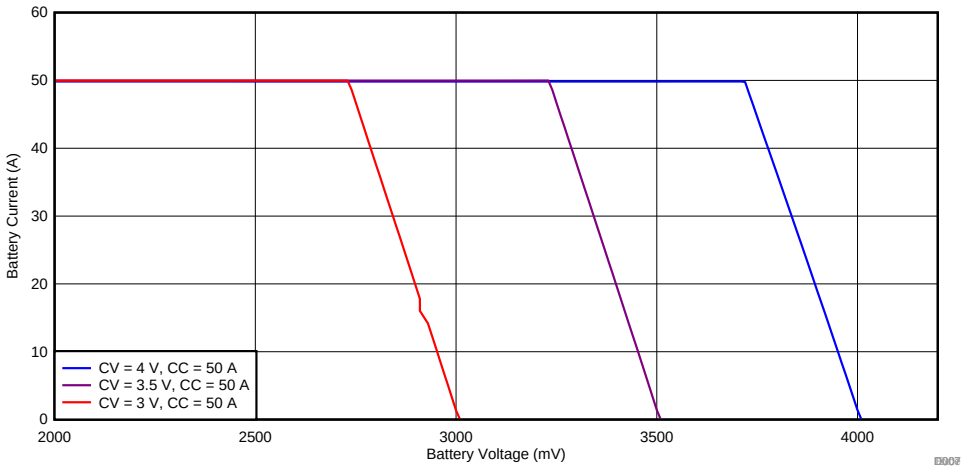


図 42. CC, CV Transformation Under Different Voltage Setting

In 図 41, with the increase in current setting, the CC control will start transforming to CV control at lower voltage. 図 42 shows that voltage setting has less effect on the switch from CC control to CV control.

3.3.3.4 ADC Calibration

Two channels are used to monitor the battery current and voltage. The accuracy of this data acquisition depends on the gain and offset of the THS4561 device and other components, so the output of the ADC should be calibrated. Use a similar method to calibrate those two channels as the previous current and voltage control loop:

ADC channel 1 calibration:

$$Gain1 = \frac{(I_{out2} - I_{out1})}{(ADC_{out2} - ADC_{out1})} = \frac{34.932\ A - 5.479\ A}{1565.7\ mV - 256.25\ mV} = 0.02249265\ A / mV \quad (9)$$

$$Offset1 = I_{out1} - Gain \times ADC_{out1} = 5.479\ A - 0.02249265\ A / mV \times 256.25\ mV = -0.284741456\ A \quad (10)$$

$$Gain2 = \frac{(I_{out3} - I_{out2})}{(ADC_{out3} - ADC_{out2})} = \frac{49.942\ A - 34.932\ A}{2231.4\ mV - 1565.7\ mV} = 0.022547694\ A / mV \quad (11)$$

$$Offset2 = I_{out2} - Gain \times ADC_{out2} = 34.932\ A - 0.0225476944\ A / mV \times 1565.7\ mV = -0.370924741\ A \quad (12)$$

ADC channel 2 calibration:

$$Gain = \frac{(V_{out2} - V_{out1})}{(ADC_{out2} - ADC_{out1})} = \frac{4005.8\ mV - 1002.5\ mV}{1822.3\ mV - 460.5\ mV} = 2.205389925 \quad (13)$$

$$Offset = V_{out1} - Gain \times ADC_{out1} = 1002.5\ mV - 2.205389225 \times 460.5\ mV = -13.08206051\ mV \quad (14)$$

図 43 and 図 44 show the accuracy of this data acquisition after calibration.

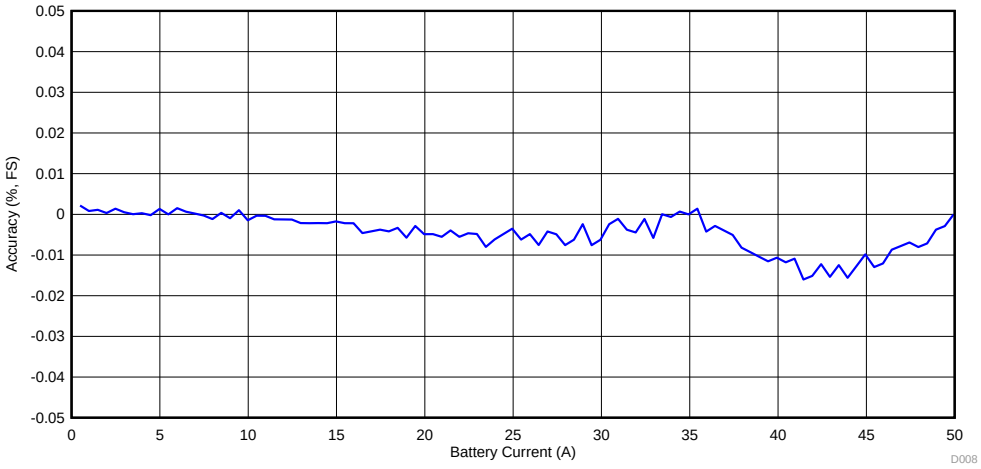


図 43. ADC Current Acquisition Accuracy

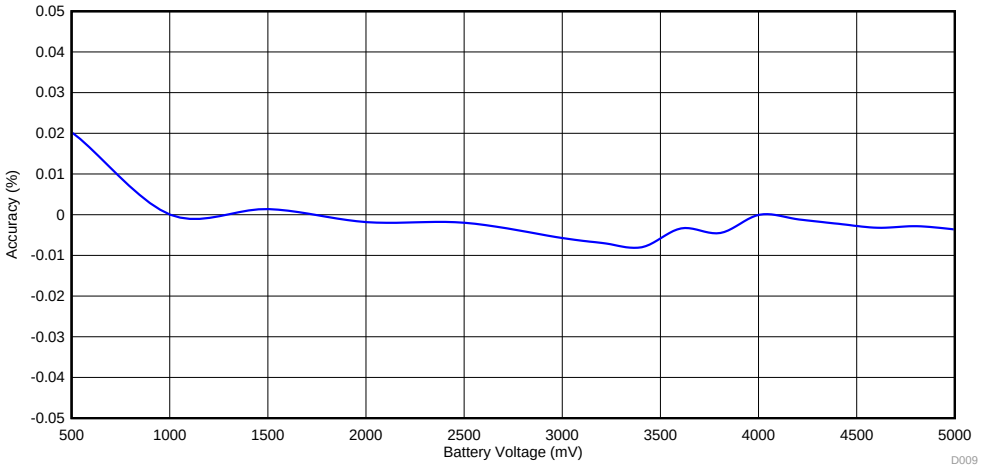


図 44. ADC Voltage Acquisition Accuracy

The results show the ADC current acquisition accuracy is excellent. Although the ADC voltage acquisition accuracy is not good in the low voltage range, battery tester applications usually are more concerned with the accuracy in the high-voltage range. In battery tester applications, engineers can refer to 3.3.3.1 and 3.3.3.2 to set the DAC to control the current and voltage after calibration. Then engineers can refer to 3.3.3.4 to get the real output current and voltage after calibration and adjust the DAC value to get the better performance.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01040.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01040.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01040.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01040.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01040.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01040.

4.7 Simulation Results

To download the simulation results, see the design files at TIDA-01040.

5 Software Files

To download the software files, see the design files at TIDA-01040.

6 Related Documentation

1. Texas Instruments, *LM5170-Q1 Multiphase Bidirectional Current Controller Data Sheet*
2. Texas Instruments, *LM2664 Switched Capacitor Voltage Converter Data Sheet*
3. Texas Instruments, *TPS709 150-mA, 30-V, 1-μA IQ Voltage Regulators with Enable Data Sheet*
4. Texas Instruments, *LM5118 Wide Voltage Range Buck-Boost Controller Data Sheet*
5. Texas Instruments, *INA188 Precision, Zero-Drift, Rail-to-Rail Out, High-Voltage Instrumentation Amplifier Data Sheet*
6. Texas Instruments, *DACx0004, Quad 16-,14-,12-Bit, 1 LSB INL, Buffered, Voltage-Output Digital-to-Analog Converters Data Sheet*
7. Texas Instruments, *ADS131A0x 2- or 4-Chan, 24-Bit, 128-kSPS, Simultaneous-Sampling, Delta-Sigma ADC Data Sheet*
8. Texas Instruments, *TLV07 36-V Precision, Rail-to-Rail Output Operational Amplifier Data Sheet*
9. Texas Instruments, *OPAx22x High Precision, Low Noise Operational Amplifiers Data Sheet*
10. Texas Instruments, *OPA827 Low-Noise, High-Precision, JFET-Input Operational Amplifier Data Sheet*
11. Texas Instruments, THS4561 Low-Power, High Supply Range, 70-MHz, Fully Differential Amplifier Data Sheet
12. Texas Instruments, *LM6142/LM6144 17 MHz Rail-to-Rail Input-Output Operational Amplifiers*

13. Texas Instruments, *PMP15038 Test Results Technical Reference*

6.1 商標

7 About the Author

Sean Zhou is an application engineer at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Sean has earned his master of science in electrical engineering (MSEE) degree from the Soochow University in Suzhou, China.

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8 Acknowledgement

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (September 2018) から **Revision B** に変更 **Page**

- *LM5170-Q1 Multiphase Bidirectional Current Controller* section. 変更 5
- *LM5118*, *TLV07*, *LM6142*, and *OPA2277* sections. 削除 5
- Updated *INA828 Precision Instrumentation Amplifier* section. 5
- Updated *DAC80004 16-bit DAC With 1 LSB INL/DNL* section. 6
- Updated *ADS131A04 24-bit, 128-kSPS, 4-Channel, Simultaneous-Sampling Delta-Sigma ADC* section. 6
- Updated *Other Highlighted Products* section. 7

2018年6月発行のものから更新 **Page**

- 'CC, CV' to 'constant current (CC) and constant voltage (CV)' 変更 2
- wording in 1.1 変更 2
- '0.5 C' to '0.5 A' 変更 3
- wording throughout 2 変更 4
- wording throughout 3 変更 17
- information in 表 5 変更 31
- 8 追加 42

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