参考資料

TI Designs: TIDA-01536
シングル・チャネル、絶縁、3線式電流ループ・トランスミッタのリファレンス・デザイン

概要

このリファレンス・デザインで紹介するシングル・チャネル、入力絶縁、3線式の電流ループ・トランスミッタは、24V電源で動作し、0mA～20mAの電流範囲を出力します。このデザインには、回路の目標を達成するため、高精度のデジタル/アナログ・コンバータ(DAC)と内部基準電圧、、統合された3線式電流ループ・トランスミッタ、デジタル・アイソレータが搭載されています。保護回路が内蔵されており、IEC61000-4テストに合格します。

リソース

TIDA-01536	すべてのデザイン・ファイル
XTR111	プロダクト・フォルダ
DAC8551	プロダクト・フォルダ
ISO7340C	プロダクト・フォルダ
REF5050	プロダクト・フォルダ

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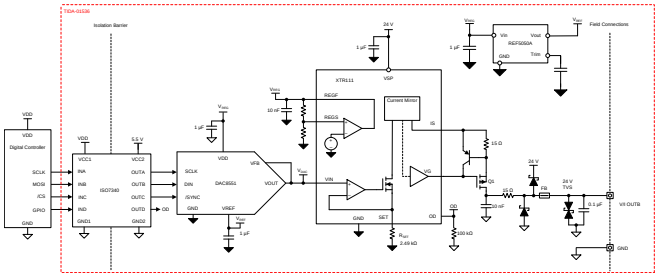
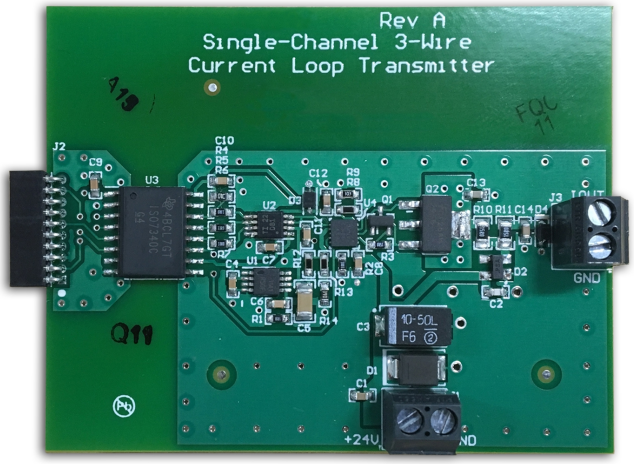
特長

- ファクトリ・オートメーションや制御向けのアナログ出力
- 0mA～20mAの電流出力
- 16ビット分解能
- IEC61000-4過渡に対する保護
- 3線式SPI入力

アプリケーション

- ファクトリ・オートメーション/制御
- ビルディング・オートメーション





TIDUB12 翻訳版 — 最新の英語版資料 http://www-s.ti.com/sc/techlit/TIDUB12

1 System Description

This reference design accepts a nominal single-supply voltage of 24 V, and produces current sources with ranges commonly used in factory automation and control applications. The 16-bit current output achieves less than 0.15% full-scale range (FSR) of total unadjusted error (TUE) at room temperature, and less than 0.033% FSR after calibration. Protective circuitry is included that allows the system to pass the ICE61000-4 tests. The transmitter operates from 7 V to 40 V, but must be provided with enough voltage to drive the load plus compliance voltage.

1.1 Key System Specifications

表 1. Comparison of Design Goals, Simulated, and Measured Performance

Specifications	Goals	Calculated	Measured
Input voltage to drive 1kΩ load	24V	24V	24V
Total unadjusted error (TUE)	±0.15 %FSR	±0.116 %FSR	0.14 %FSR
Calibrated output error	±0.033 %FSR	±0.005 %FSR	0.025 %FSR

2 System Overview

2.1 Block Diagram

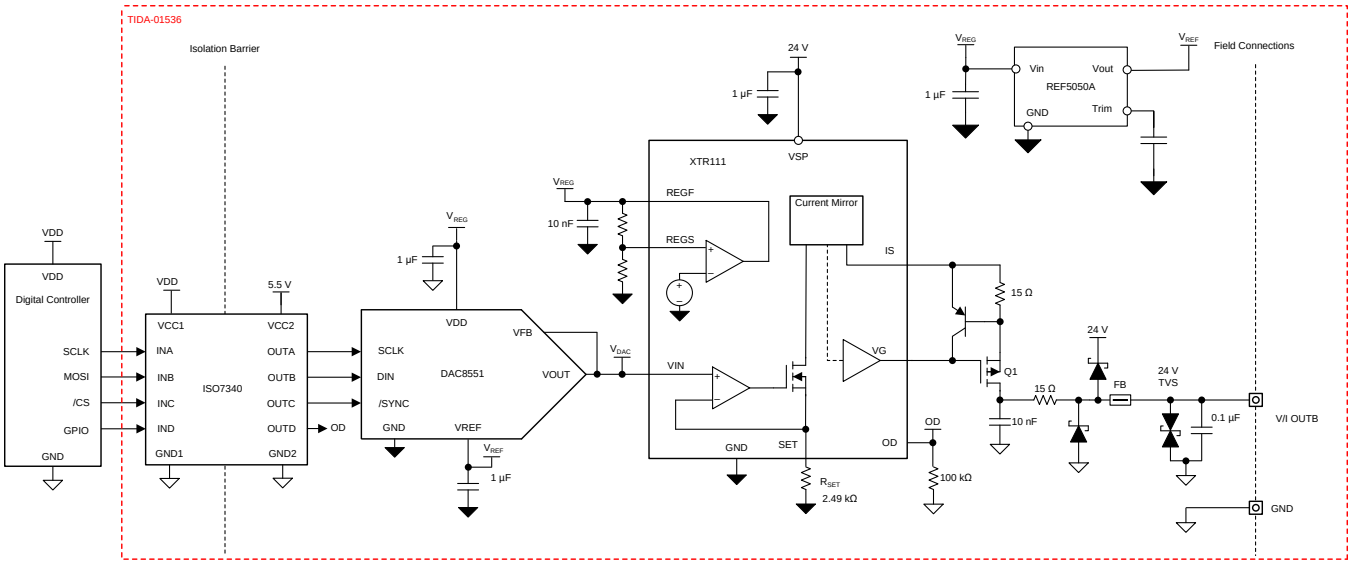


図 1. Block Diagram

2.2 Design Considerations

The design requirements are as follows:

- Supply voltage: 7 V to 40 V
- Input: 3-wire SPI
- Resolution: 16 bits
- Current output: 0 mA to 20 mA
- Accuracy: 0.15% FSR
- Circuit protection: Protected against IEC61000-4 transients.

The analog output circuitry for this isolated 3-wire current loop transmitter is designed with a 16-bit DAC and a dedicated industrial current loop output driver. The integrated output driver includes all of the required circuitry to take a low-voltage DAC output and create the high-side current source required for 3-wire current loop transmitter outputs. The integrated output driver also includes a voltage regulator that is used to power the DAC, digital isolator, and the reference voltage. Digital isolation for the SPI and GPIO control signals is accomplished using a 4-channel digital isolator. This design can be used in analog output modules or to create an input-isolated 3-wire sensor transmitter. The output current transfer function of the transmitter is shown in Equation 1.

$$I_{OUT}\,(mA) = 10 \times \left(\frac{V_{DAC}}{R_{SET}}\right) \tag{1}$$

2.2.1 Calculated IOUT Accuracy

The IOUT circuit performance is based on the specifications of the DAC8551, XTR111, and the RSET gain setting resistor. The typical dc performance specifications of the DAC8551 are listed in 表 2.

表 2. Typical DAC8551 Performance Specifications

DAC8551 Specifications	Typical Value
Offset	2 mV
DNL	0.25 LSB
INL	3 LSB
Gain error	0.02 %FSR
VREF initial accuracy	0.1 %FSR

The zero-code error, full-scale error, and gain error are specified between codes 485 and 64741; therefore, the output range of the DAC spans from 0.04 V to 4.94 V. To achieve the current output of 0 mA to 20 mA, the passive components must be selected correctly according to 2.2.3. Using the input span and the specifications of the DAC8551, the total unadjusted error (TUE) of the DAC8551 is calculated as shown in Equation 2. A root sum of squares (RSS) is used to calculate the overall error from the independent error sources.

$$I_{TUE\_DAC}\,(\%FSR) = \left(\sqrt{\left(\frac{V_{OS}}{V_{Fullscale}}\right)^2 + \left(\frac{INL_{LSB}}{N_{BITS}}\right)^2 + \left(\frac{GAIN_{ERROR}\%}{100}\right)^2 + \left(\frac{V_{REF}Accuracy\%}{100}\right)^2}\right) \times 100\%$$

$$I_{TUE\_DAC}\,(\%FSR) = \left(\sqrt{\left(\frac{.002}{4.9}\right)^2 + \left(\frac{3}{2^{16}}\right)^2 + \left(\frac{0.02}{100}\right)^2 + \left(\frac{0.1}{100}\right)^2}\right) \times 100\% = 0.1099\%FSR \tag{2}$$

Apply a two-point line of best fit calibration to the design to remove the effects of gain and offset errors, and leave only the linearity errors of the DAC8551, as shown in Equation 3.

$$I_{CAL\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{INL_{LSB}}{N_{BITS}}\right)^2}\right) \times 100$$

$$I_{CAL\_DAC}(\%FSR) = \left(\sqrt{\left(\frac{3}{2^{16}}\right)^2}\right) \times 100 = 0.0046\%FSR \quad (3)$$

The XTR111 performance specifications, including the effects of the external R_{SET}, are listed in 表 3. Errors from V_{REF} form an offset error in the XTR111 circuit performance because V_{REF} is used to offset the DAC output voltage and is part of the XTR111 circuit transfer function. Although not done in this design, when using V_{REF} to shift the XTR111 output to 4 mA for a 0-V input, V_{REF} errors also add offset errors.

表 3. Typical XTR111 Circuit IOUT Performance Specifications

XTR111 Specification	Typical Values
Offset	0.002 %FSR
Nonlinearity	0.002 %FSR
Gain error	0.015 %FSR
RSET tolerance	0.03 %FSR

Using these specifications and the DAC8551 output range, the TUE of the XTR111 is calculated as shown in Equation 4. The calculations show that the R_{SET} resistor tolerance is the largest error source. Lower tolerance resistors can be used to decrease the total unadjusted error at the expense of increased system cost.

$$I_{TUE\_XTR}(\%FSR) = \sqrt{V_{OS}{}^2 + Nonlinearity^2 + Gain_{ERROR}{}^2 + R_{SET\_TOL}{}^2}$$

$$I_{TUE\_XTR}(\%FSR) = \sqrt{0.002^2 + 0.002^2 + 0.015^2 + 0.03^2} = 0.034\% \quad (4)$$

Apply a two-point calibration to the design to remove the effects of gain and offset errors, and leave only the linearity errors of the XTR111, as shown in Equation 5.

$$I_{CAL\_XTR}(\%FSR) = 0.002\% \quad (5)$$

Because the DAC error and the XTR error are uncorrelated, a probable full system TUE is calculated by taking the root of the sum of squares (RSS) of the individual errors from the DAC8551 and XTR111, as shown in Equation 6.

$$I_{TUE\_TOTAL}(\%FSR) = \sqrt{I_{TUE\_DAC}(\%FSR)^2 + I_{TUE\_XTR}(\%FSR)^2} = \sqrt{(0.1099\%)^2 + (0.036\%)^2} = 0.116\%FSR \quad (6)$$

The final calibrated results are shown in Equation 7.

$$I_{CAL\_TOTAL}(\%FSR) = \sqrt{I_{CAL\_DAC}(\%FSR)^2 + I_{CAL\_XTR}(\%FSR)^2} = \sqrt{(0.0046)^2 + (0.002)^2} = 0.00506\%FSR \quad (7)$$

These calculations can also be repeated for worst-case analysis by replacing the typical values in 表 2 with the maximum values from the data sheet.

2.2.2 3-Wire Current Loop Driver

The DAC output voltage (V_{DAC}) is converted to a high-side output current (I_{OUT}) with a two-stage high-side current source topology similar to the circuits shown in TIPD102 and TIPD153. The first stage sinks current through the external span setting resistor (R_{SET}) based on the transfer function shown in Equation 8.

$$I_{RSET}(mA) = \frac{V_{DAC}}{R_{SET}} \quad (8)$$

Then the high-side current mirror sources a current 10 times greater than the I_{RSET} current of the IS pin through Q1 to the load. The high-side current mirror gain results in the transfer function for the current loop driver shown in Equation 9.

$$I_{OUT}(mA) = 10 \times \left(\frac{V_{DAC}}{R_{SET}} \right) \quad (9)$$

2.2.3 Passive Component Selection

The R_{SET} resistor values are determined based on the desired output ranges and the V_{DAC} and V_{REF} voltages. Equation 9 is rearranged to calculate R_{SET} for the desired 20-mA, full-scale output range, as shown in Equation 10. The system is designed with a V_{DAC} voltage range of 0.04 V to 4.94 V to operate the DAC8551 in the specified linear output range from codes 485 to 64714.

$$R_{SET} = 10 \times \left(\frac{V_{DAC}}{I_{OUT}} \right) = 10 \times \left(\frac{4.94\ V}{0.020\ A} \right) = 2470\ \Omega \quad (10)$$

Based on availability of 0.1% tolerance components, R_{SET} is selected to be 2469 Ω using 2430-Ω and 39-Ω resistors in series to get as close as possible to the desired 2470 Ω. Lower unadjusted error is achieved by selecting a lower tolerance R_{SET} resistor to match the 0.015% typical gain error specification of the XTR111.

An offset shift circuit is also implemented to minimize the zero-code error by adding a 40-mV offset to R_{SET}, as shown in Equation 11 to solve for R_{OS}.

$$IOUT = 10 \times \left(\frac{V_{DAC}}{R_{SET}} \right) + 10 \times \left(\frac{V_{DAC} - V_{REF}}{R_{OS}} \right)$$

$$0\ mA = 10 \times \left(\frac{40\ mV}{2469} \right) + 10 \times \left(\frac{40\ mV - 5\ V}{306.2\ k\Omega} \right) \quad (11)$$

Because of the availability of 0.1% tolerance resistors, a value 309 kΩ is selected for R_{OS}, and results in an actual offset of 39.6 mV.

2.3 Highlighted Products

2.3.1 DAC—DAC8551

To meet the requirements of this design, use a 16-bit, rail-to-rail voltage-output DAC with an output range of 5 V. Select a DAC with gain, offset, and VREF errors that are lower than the total unadjusted goals of 0.15% FSR, and with linearity errors less than 0.1% to meet the calibrated error goals.

The DAC8551 meets the requirements of the design and offers strong dc performance with typical offset errors of 2 mV, gain errors of 0.02% FSR, and integral nonlinearity (INL) errors of ±3 LSB. The maximum differential nonlinearity (DNL) specification of ±1 least significant bits (LSB) provides fully monotonic operation.

2.3.2 Output Current Loop Driver—XTR111

The XTR111 is a precision single-channel, 3-wire, current loop output driver for industrial process and control applications. The output span is programmable to the popular output ranges of 0 mA to 20 mA, 0 mA to 24 mA, 4 mA to 20 mA and other similar ranges with a single external resistor. The XTR111 features strong dc performance with typical offset of 0.002% FSR and offset drift of 0.0002% FSR/°C. Typical gain errors of 0.015% FSR and linearity errors of 0.002% FSR make this a good choice given the accuracy goals in this design.

An open-drain error flag (EF) is available to monitor for errors on the output of the transmitter that prevent the output current from reaching the proper level. These errors include wire-break (open-circuit), too much output load impedance, or insufficient power-supply voltage. A digital output disable pin (OD) is available, and sets the XTR111 output to a high-impedance state.

The XTR111 also includes an internal regulator programmable from 3 V to 12 V. However, because of a poor accuracy of ±5% (max) with 30 ppm/°C, a more accurate voltage reference is required.

2.3.3 External MOSFET

The external MOSFET used in this design must have maximum drain-to-source (VDS) and gate-to-source (VGS) voltages that exceed the maximum voltages present in this design. The MOSFET must also have gate capacitances less than 500 pF, and a package that allows for proper power dissipation during the maximum output current and supply conditions. The NTD2955 is selected, with a maximum VDS voltage of 60 V and maximum VGS voltage of 20 V. The gate capacitance is 450 pF and the power dissipation is 55 W.

2.3.4 Digital Isolator—ISO7340C

The digital signals used to control the DAC and XTR111 must be isolated through a digital isolator to achieve isolation from the host controller. The ISO734XFC family of digital isolators supports data rates up to 25 MBPS with greater than 4 kVpk of galvanic isolation. The ISO7340C was selected based on the four, forward direction isolation channels required for the 3-wire SPI interface and the XTR111 OD signal.

2.3.5 Voltage Reference—REF5050A

The REF5050A has an initial accuracy of 0.1% (max) with 8-ppm/°C temperature drift, and can source or sink up to 10 mA at the VOUT pin.

2.3.6 Protection Component Selection

The protection scheme in this design, shown in 図 2, is intended to provide immunity to EMI/RFI interference and transient voltage disturbances as described in the IEC61000-4 tests. The IEC61000-4 transients have two components: a high-frequency component and a high-energy component. Therefore, the protection strategy focuses on attenuating the high-frequency transients and diverting the energy from the high-energy components away from the sensitive circuitry.

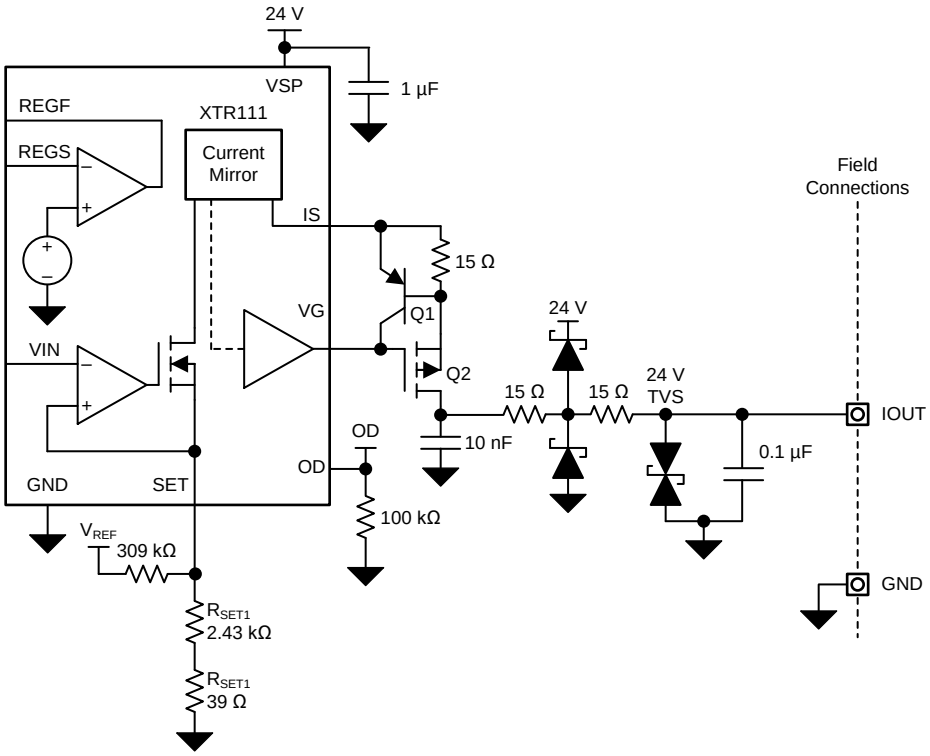


図 2. Output Protection Circuit

2.4 System Design Theory

2.4.1 Voltage Regulator and Reference

A voltage regulator is required to reduce the 24-V supply voltage to a lower voltage required for the DAC and digital isolator used in the design. In this design, a simple linear dropout regulator (LDO) that is included in the current loop driver is used to reduce the input supply voltage to 5.5 V. Additionally, a voltage reference is used to maintain an accurate and low drift 5 V for the DAC and the current loop driver references.

2.4.2 Isolation

Most analog output (AO) modules require isolation from the backplane and other AO modules. Input-isolated, 3-wire transmitters require a way to receive isolated data from the input sensor to control the output current. In both of these applications, the isolation is typically accomplished by isolating the digital signals between the host processor, controller, or input, and the DAC in the output transmitter circuitry. There are many topologies available to achieve the isolation, but galvanic (capacitive) isolation has many advantages over other topologies and is selected for this design. Input power supply isolation is also a consideration for current loop transmitter applications.

2.4.3 IEC61000-4 Immunity Testing

The industrial environment can be very dangerous for sensitive electronic components. Systems are therefore designed to be very robust and provide immunity to environmental hazards that may lead to electrical overstress or undesired performance.

Many transient signals or radiated emissions common in industrial applications can cause electrical overstress (EOS) damage or other disruptions to unprotected systems. IEC61000-4 is a test suite that simulates these transient and emission signals, and awards a certification to systems that prove to be immune. During each of the IEC61000-4 tests, the output of the equipment under test (EUT) is monitored for deviations or total failure. Results are assigned one of four class ratings for each test. The classes are listed and described in 表 4

表 4. IEC61000-4 Result Classes

Grade	Description
Class A	Normal performance within an error band specified by the manufacturer.
Class B	Temporary loss of function or degradation of performance that ceases after the disturbance is removed. The equipment under test recovers normal performance without operator interference.
Class C	Temporary loss of function or degradation of performance; correction of performance requires operator intervention.
Class D	Loss of function or degradation of performance that is not recoverable; permanent damage to hardware or software, or loss of data.

Full details of each of the IEC61000-4 tests are licensed by the IEC and must be purchased.

2.4.3.1 IEC61000-4-2: Electrostatic Discharge

The electrostatic discharge (ESD) immunity test emulates the electrostatic discharge of an operator directly onto an electrical component. To simulate this event, an ESD generator applies ESD pulses to the EUT either through air discharge or through vertical and horizontal coupling planes. Air discharge tests are conducted near any exposed I/O terminal. The ESD waveform is shown in 図 3

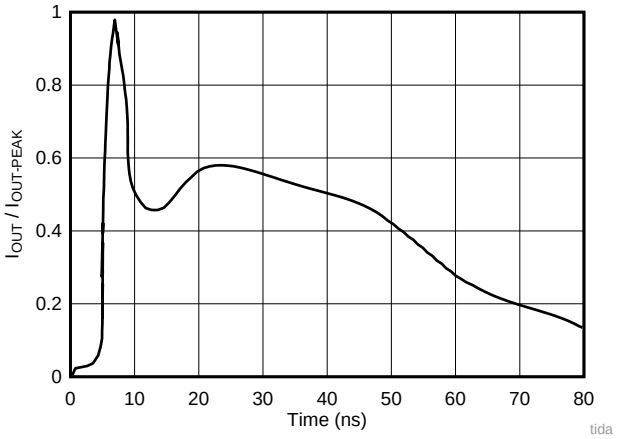


図 3. IEC61000-4 ESD Test Pulse

The ESD test pulse is pictured in 図 4. The ESD test pulse is a high-frequency transient with a pulse period of less than 100 ns. The pulse is a high-voltage signal, ranging from 4 kV to 15 kV, depending on the threat level appropriate for the EUT. The complete ESD test requires 10 sequential discharges of each positive and negative polarity for each test configuration.

2.4.3.2 IEC61000-4-3: Radiated Immunity

The radiated immunity (RI) test emulates exposure to high-frequency radiated emissions, such as radio devices or other emissions common in industrial processes. The frequency range and field strength of the radiated signals vary in this test based on the type of EUT. For this design, the tested frequency range was 80 MHz to 1 GHz, and the field strength was 20 V/m.

2.4.3.3 IEC61000-4-4: Electrically Fast Transient

The burst immunity, or electrically fast transient (EFT), emulates day-to-day switching transients from various sources in a typical industrial application space. The test is performed on power, signal, and earth wires, or a subset, depending on what is appropriate for the EUT. The IEC61000-4 EFT pulse is shown in 図 4

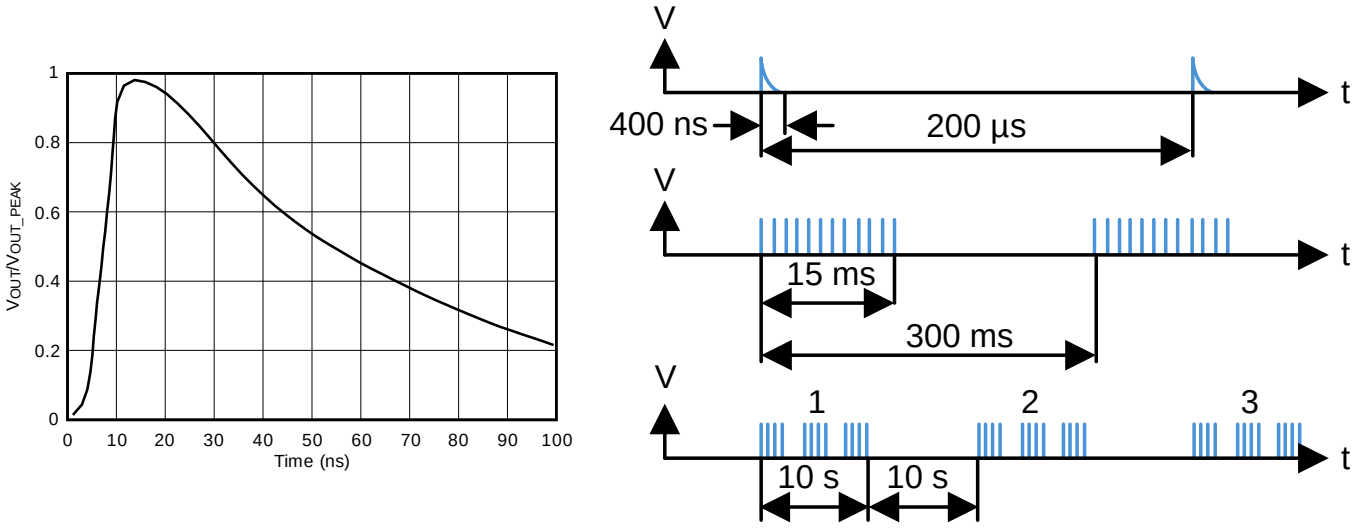


図 4. IEC61000-4 EFT Test Pulses

In this test, a burst generator produces a series of EFT bursts, each lasting 15 ms, with 300 ms between bursts. The pulse rate of each burst is approximately 5 kHz. A typical test exposes the EUT to 1 minute to 3 minutes of EFT bursts. Similar to the ESD test pulse, the EFT pulses are a high-frequency signal, but the magnitude of the EFT test pulse only ranges from 0.25 kV to 4 kV. Bursts of both positive and negative polarity are applied.

2.4.3.4 IEC61000-4-5: Surge

The surge test emulates power line surges that are produced from power switches and lightning. A surge of 1 kV with a source impedance of 42 Ω is used for this test.

2.4.3.5 IEC61000-4-6: Conducted Immunity

The conducted immunity (CI) test emulates exposure to conducted emissions. CI is tested over a frequency range of 150 kHz to 80 MHz at 10 V/m. This test measures the impact that conducted emissions have over the power-supply and signal lines.

2.4.3.6 Protection Circuitry

The IEC61000-4 transients have two main components: a high-frequency component and a high-energy component. These two properties can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

Attenuation is achieved through resistors and capacitors that attenuate high-frequency transients and also limit series current. Capacitors placed between the output terminals help attenuate transient energy from high frequency tests, such as electrostatic discharge (ESD) and electrically fast transients (EFT).

Diverting the large energy transients is accomplished using transient voltage suppressor (TVS) diodes and clamp-to-rail diodes. The protection scheme must limit the level of the voltage transients to a level less than the absolute maximum rating for the output driver. More information on the IEC61000-4 tests and the protection circuitry requirements can be obtained in TIPD153.

2.4.4 TVS Diode

A unidirectional TVS diode is used to divert energy from high-voltage transients away from the XTR111 and pass transistor (Q2). Select the TVS diode based on the working voltage, breakdown voltage, leakage current, and power rating. The working voltage specification defines the largest reverse voltage at which the diode is meant to be operated continuously without conducting. The working voltage is the voltage at the *knee* of the reverse breakdown curve where the diode begins to break down and exhibits some small leakage current. As the voltage increases above the working voltage, more current begins to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode is fully allowing current to flow. It is important to keep in mind that if large currents flow through the diode, the breakdown voltage rises.

Make sure that the diode breakdown voltage is low enough to protect all the components connected to the output pins and provide enough headroom to maintain protection as the breakdown voltage rises with large currents. In this design, keep the working voltage of the TVS diode at or above the upper limit of the allowed supply voltages because any higher voltage causes leakage through the diode. In this case, the CDSOD323-T24S diode is selected with a working voltage of 24 V, breakdown voltage of 26.7 V, and power rating of 500 W. An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in the breakdown region, some leakage current still flows through the diode. This leakage current affects system accuracy, and the leakage current varies over temperature. The diode selected for this design features 1-µA maximum leakage current at the working voltage.

2.4.5 Clamp-to-Rail Diodes

The clamp-to-rail diodes used in this design must maintain a low-enough forward voltage drop to keep the voltage for all components connected to the output pins within the absolute maximum ratings. The CD143A-SR70 clamp-to-rail diodes used in this design feature a forward voltage drop of 1.5 V when 1 A is flowing through the diodes. The diodes are connected between the output and GND and the positive supply, which means that the diodes clamp at 25.5 V and –1.5 V for transients with 1 A of current. Like the TVS diodes, Schottky diodes can contribute some leakage current on the voltage and current outputs based on the reverse leakage current specification. Reverse leakage current is usually specified at a specific reverse voltage. The diode used in this design has a reverse leakage current specification of 1 µA at 70-V reverse voltage.

2.4.6 Current Limit

An external current limit circuit is implemented using 15-Ω resistor R_{LIM}, and the Q1 BJT placed between the gate and source of the Q2 PMOS transistor. The current limit functions by limiting the gate-to-source voltage (Q2) that limits the output current. When the voltage drop across R_{LIM} exceeds the base-to-emitter voltage (VBE) of Q1, the current limit becomes active. Therefore the current limit is set to 43.3 mA using Equation 12.

$$R_{LIM} = \frac{V_{BE}}{I_{LIM}} = \frac{0.65\ V}{43.3\ mA} = 15\ \Omega \tag{12}$$

2.4.7 Passive Components

A parallel capacitor is used to attenuate transient signals that may remain after passing across the TVS diode. The capacitor chosen has a voltage rating of 100 V.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The design hardware consists of a single PCB that contains all the circuitry required for the current loop transmitter. To set the loop current, use an SM-USB-DIG connector as an SPI interface to control the DAC output from a USB port.

3.2 Testing and Results

3.2.1 Test Setup

The loop current transfer function and TUE is measured by connecting the output of the transmitter in series with an ammeter. The SM-USB-DIG connecter uses an SPI interface to sweep the DAC code and the current is measured at each code. The ESD, EFT, RI, CI, and surge testing are conducted according to the IEC61000-4 standard.

3.2.2 Test Results

The current output accuracy for this design is tested by sweeping the DAC code and measuring the current at each code. 図 5 shows the full transfer function of the current output for each DAC code. 図 6 shows the current output of only the first 1000 codes, and the error at codes near zero-scale as the DAC output approaches the ground rail.

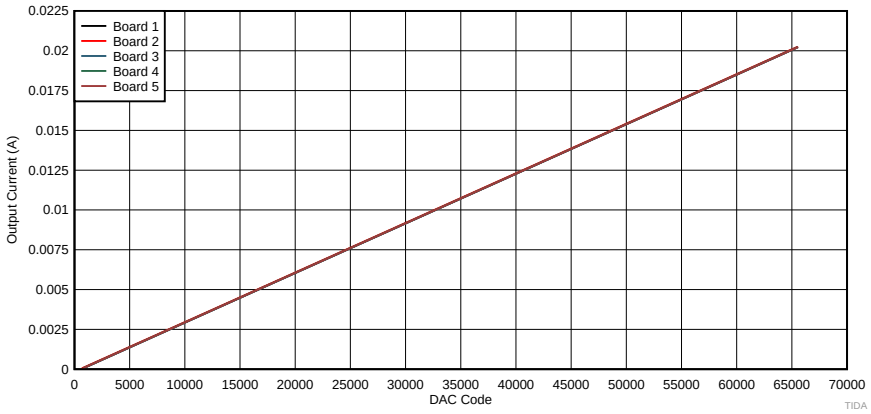


図 5. Output Current vs DAC Code (All Codes)

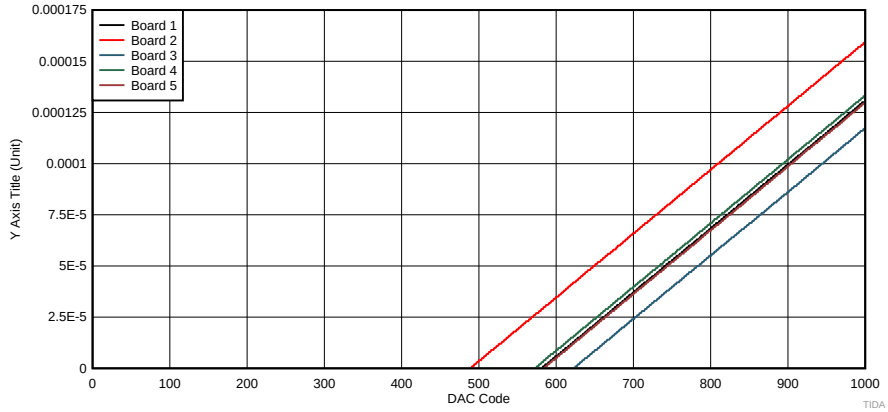


図 6. Output Current vs DAC Code (0 to 1000)

図 7 and 図 8 show the total unadjusted error before calibration in microamps and as a percentage of full-scale range. The total unadjusted error is calculated by comparing the measured transfer function to the ideal transfer function.

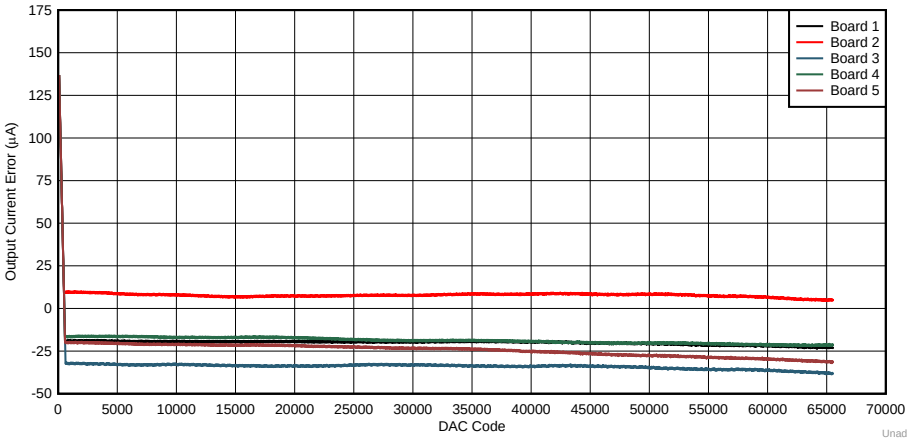


図 7. Total Unadjusted Error (µA)

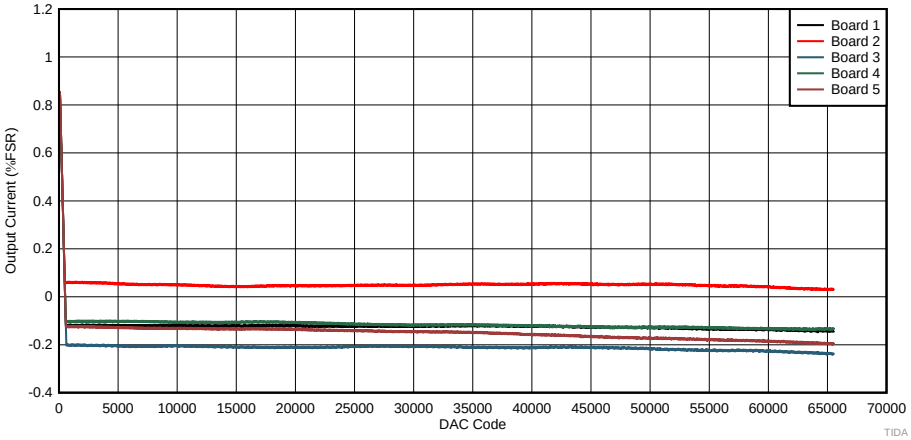


図 8. Total Unadjusted Error (%FSR)

図 9 and 図 10 show the error after calibration. By calibrating, the gain and offset error are corrected.

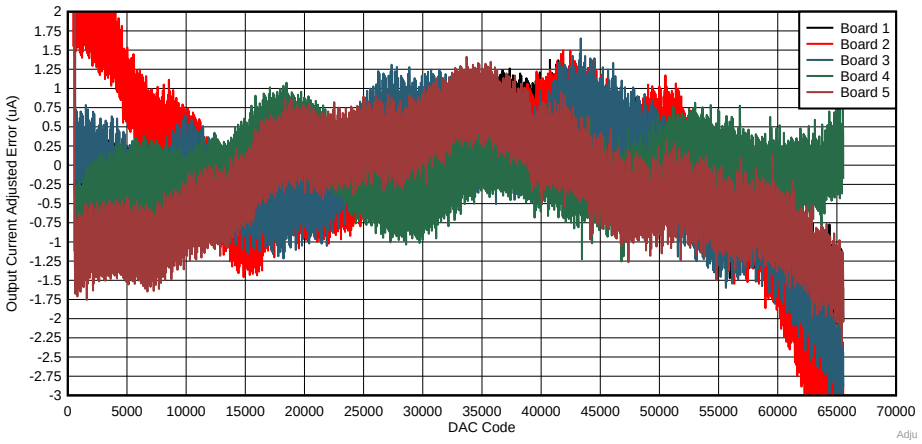


図 9. Adjusted Error (µA)

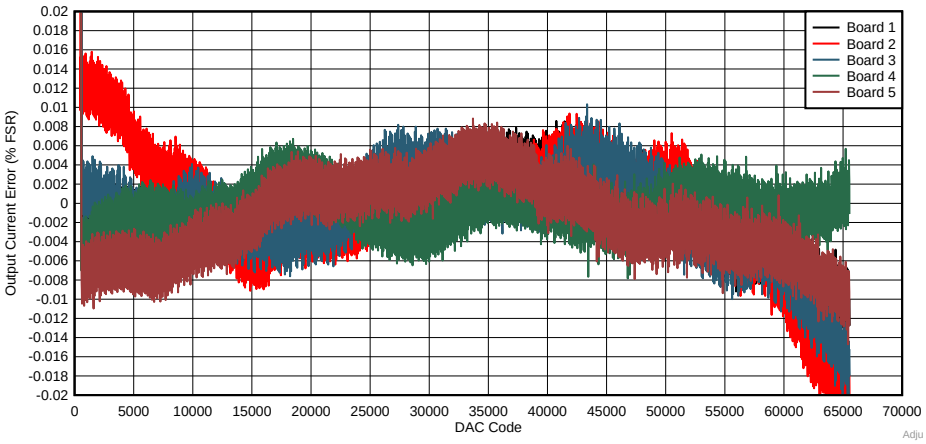


図 10. Adjusted Error (%FSR)

The ESD test requires a 15-kV air discharge, and 8-kV coupling plane discharge with horizontal and vertical orientations. The ESD strikes had little affect on the output current of the system. The result of the air discharge test is shown in 図 11, and the results for the coupling plane discharge are shown in 図 12. 表 5 shows the classification test result. Because the current output stayed with in the range of –0.15% FSR and 0.15% FSR, Class A results are achieved.

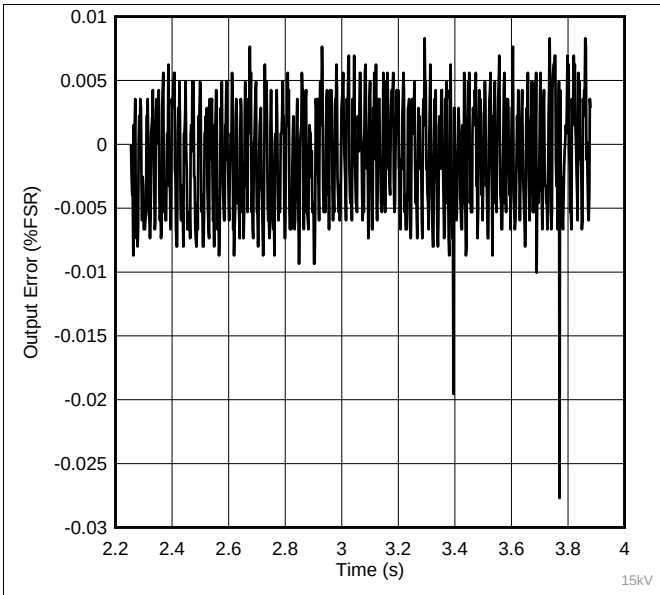


図 11. 15-kV ESD Air Discharge

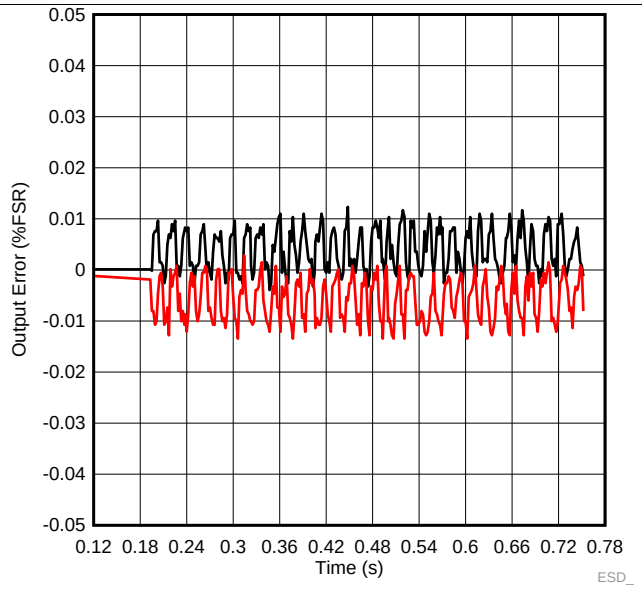


図 12. 8-kV ESD Vertical and Horizontal Coupling Plane Discharge

表 5. IEC61000-4-2: ESD Results

Orientation	Result	Class
Coupling plane discharge	PASS	A
Air discharge	PASS	A

Radiated immunity (RI) was also tested by exposing the system to 20-V/m electric field strength. 図 13 and 図 14 show the current output error during the RI test for horizontal and vertical antenna orientations, respectively. 表 6 summarizes the test results.

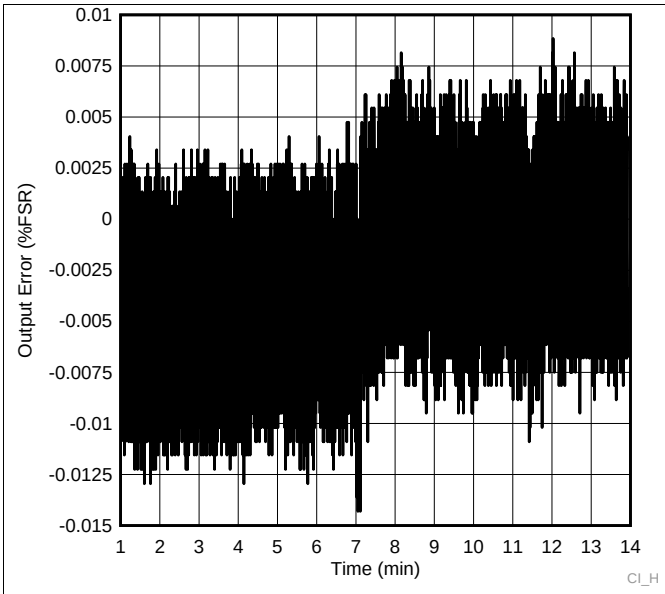


図 13. Radiated Immunity Horizontal

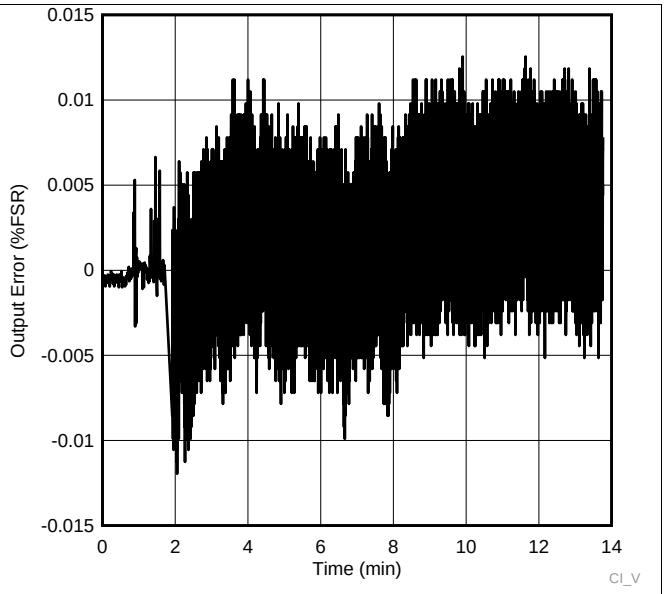


図 14. Radiated Immunity Vertical

表 6. IEC61000-4-3: Radiated Immunity Results

Orientation	Result	CLASS
Horizontal	PASS	A
Vertical	PASS	A

The EFT pulse had little effect on the output of the system. Both positive and negative EFT waveforms were tested. 表 7 shows the results in terms of classification.

表 7. IEC61000-4-4: EFT Results

Polarity	Result	Class
Positive	PASS	A
Negative	PASS	A

Conducted immunity (CI) testing led to some deviation in output current beyond the acceptable range for Class A. The CI was tested at 10 V/m. The output recovers without operator intervention so achieves class B. 図 15 shows the current output error during the CI testing.

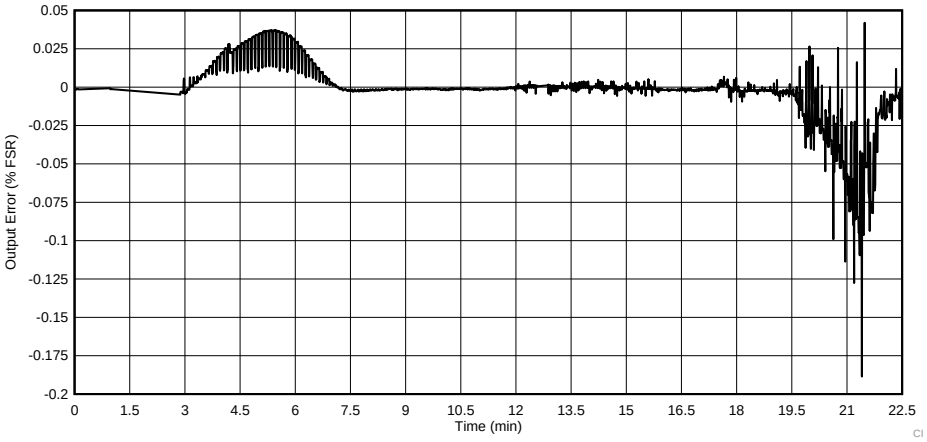


図 15. Conducted Immunity Testing

図 16 shows the surge results for the positive, negative, and line-to-line tests. 表 8 shows a summary of the results.

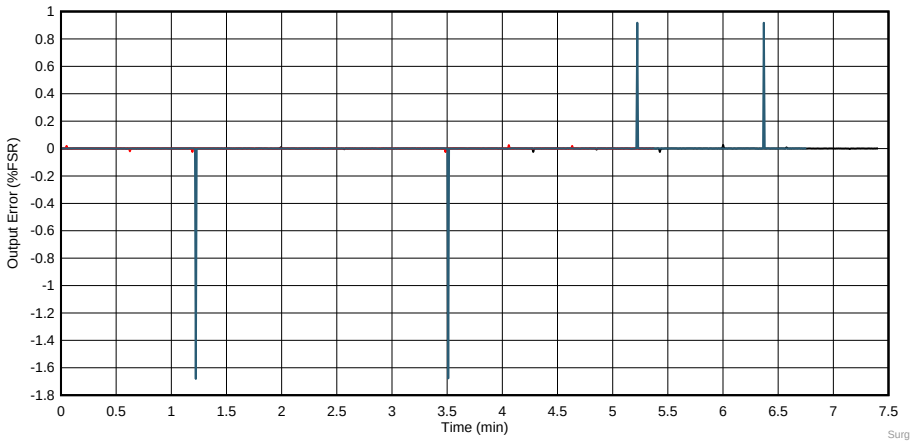


図 16. Surge Testing

表 8. IEC61000-4-5: Surge Testing

Test	Result	Class
Positive	PASS	A
Negative	PASS	A
L2L	PASS	B

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01536.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01536.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01536.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01536.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01536.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01536.

5 Software Files

To download the software files, see the design files at TIDA-01536.

6 Related Documentation

1. Texas Instruments, TIPD216: Quad-Channel Industrial Voltage and Current Output Driver Reference Design(EMC/EMI Tested)
2. Texas Instruments, TIPD153: Single-Channel Industrial Voltage and Current Output Driver, Isolated, EMC/EMI Tested Precision Design
3. International Electrotechnical Commission (2008). IEC Publication 61000-4-2 *Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test*.
4. International Electrotechnical Commission (2006). IEC Publication 61000-4-3 *Electromagnetic Compatibility (EMC) – Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test*.
5. International Electrotechnical Commission (2012). IEC Publication 61000-4-4 *Electromagnetic Compatibility (EMC) – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test*.
6. International Electrotechnical Commission (2012). IEC Publication 61000-4-5 *Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques - Surge immunity test*.
7. International Electrotechnical Commission (2008). IEC Publication 61000-4-6 *Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields*.

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