参考資料

TI Designs: TIDA-01566
ウェアラブルおよびIoT用の軽負荷高効率、低ノイズ電源のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、ウェアラブル、スマートウォッチ、スマートフォン、ヘッドセット、ヘッドフォン、イヤホン、組み込みカメラ・システムなど携帯型の個人用電子機器で使用される、高効率で低ノイズの電源レール用の超小型電源ソリューション(合計8.5mm^2)を紹介します。DC/DCコンバータの後に低ドロップアウト(LDO)リニア・レギュレータが配置され、LDOと同じ低ノイズの特性と、DC/DCコンバータの高効率を両立できます。無負荷時の合計入力電流(スイッチングI_Qとも呼ばれます)はわずか8μAで、LDOのみに基づいた設計よりも高い効率を維持できるとともに、出力ノイズは100μV近くで、DC/DCのみの設計よりもクリーンな電力を、敏感な負荷に供給できます。このデザイン・ガイドでは、LDOのみ、DC/DCのみ、DC/DCにLDOを結合したものの3種類のデザインについて、効率、I_Q、リップルなどの重要な性能特性を記載し、比較します。

リソース

TIDA-01566	デザイン・フォルダ
TPS62801	プロダクト・フォルダ
TPS7A10	プロダクト・フォルダ

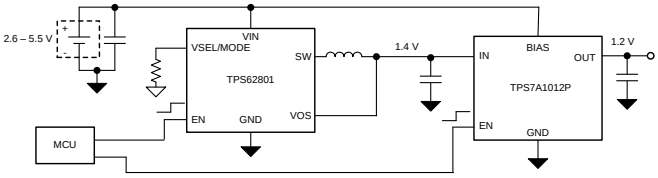
TI E2E™ Community　E2E™エキスパートに質問

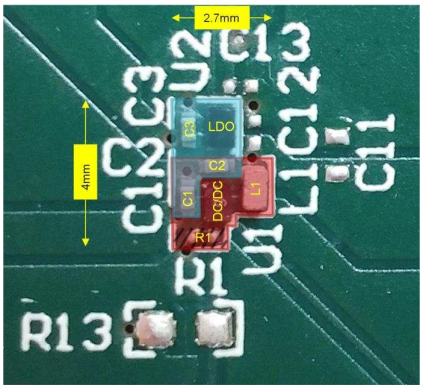
特長

- 面積8.5mm^2、高さ0.65mm未満のソリューション
- 無負荷時入力電流(スイッチングI_Q): 8μA
- 100μVに近い出力ノイズ(10Hz～100kHz)
- 最低0.5Vまで出力電圧を簡単に変更可能
- 1.2 V_{OUT}について入力電圧範囲2.6V～5.5V
- 出力電流300mAのLDO (DC/DC出力において1A)

アプリケーション

- ウェアラブル・フィットネスおよびアクティビティ・モニタ
- スマート・ウォッチ
- スマートフォン
- ヘッドセット、ヘッドホン、小型イヤホン
- 組み込みカメラ・システム





1 System Description

The TIDA-01566 optimizes both the TPS62801 DC/DC converter and the TPS7A10 LDO to produce an ultra-small, efficient, low noise 1.2-V supply from a single-cell, rechargeable lithium battery. The DC/DC operates in power save mode for maximum efficiency at light loads. In power save mode, it reduces the switching frequency to save power. This increases the output ripple, while decreasing the frequency of this ripple. Both the lower frequency and higher magnitude ripple may not be acceptable to some sensitive loads, such as sensors, data converters, global positioning system (GPS) receivers, wireless communication devices (for example, Bluetooth and Narrowband IoT (NB-IoT)), and so on.

To overcome the challenge of higher ripple, an LDO is added after the DC/DC. LDOs have a high power supply rejection ratio (PSRR) at the lower frequency power save mode of most DC/DC converters, and effectively attenuate the ripple to extremely low levels. The low current consumption (I_Q) of the TPS7A10 maintains high efficiency, even at light loads below 1 mA. This enables a lower standby current for portable systems and a corresponding fewer number of battery recharge cycles. Adding a DC/DC in front of an LDO also achieves a higher efficiency at higher loads, which eliminates thermal considerations that arise when using just an LDO at these high currents.

Both the TPS62801 and TPS7A10 come in ultra-small wafer-chip-scale packages (WCSP) for smallest solution size. The TPS62801 switches at up to 4 MHz, which decreases the size of its output filter. An 0201-size output capacitor and 0402-size inductor make an effective filter in this design.

While such a DC/DC plus LDO solution offers high performance, a DC/DC-only or LDO-only solution may be more appropriate for certain systems. Systems that tolerate higher ripple, such as microcontrollers (MCUs), may not require the LDO. Lowest current systems, such as the smallest standalone sensors, may not benefit much from the higher efficiency of an added DC/DC and would benefit more from the size savings of using just the LDO. The relative performance of all three architectures is shown and compared later in this document.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
TIDA-01566 Circuit	
Input voltage range	2.6 V to 5.5 V
DC/DC output voltage	1.4 V
DC/DC output current	0 A to 1 A
LDO output voltage	1.2 V
LDO output current	0 mA to 300 mA
No load input current (3.6 V_{IN})	8 µA
Efficiency (10-mA load, 3 V_{IN})	73%
Total RMS noise (10 Hz to 100 kHz, 300-mA load)	104.6 µV
DC/DC Only Circuit	
Input voltage range	1.8 V to 5.5 V
DC/DC output voltage	1.2 V
DC/DC output current (V_{IN} > 2.3 V)	0 A to 1 A
No load input current (3.6 V_{IN})	2.5 µA
Efficiency (10-mA load, 3 V_{IN})	84%
Total RMS noise (10 Hz to 100 kHz, 300-mA load)	241.9 µV
LDO Only Circuit	

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS
Input voltage range	2.6 V to 3.3 V
LDO output voltage	1.2 V
LDO output current	0 mA to 300 mA
No load input current (3 V_{IN})	6 µA
Efficiency (10-mA load, 3 V_{IN})	40%
Total RMS noise (10 Hz to 100 kHz, 300-mA load)	104.3 µV

2 System Overview

2.1 Block Diagram

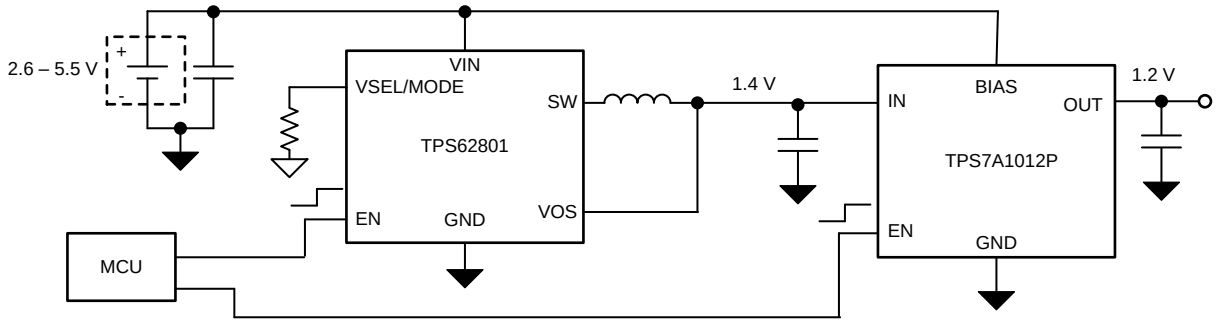


図 1. TIDA-01566 Block Diagram

2.2 Design Considerations

2.2.1 NMOS versus PMOS LDO

The choice of pass transistor type in the LDO determines the lowest possible input and output voltage. The TPS7A10 uses an NMOS pass transistor, optimized for the lowest output voltages, which provides lower dropout. For the TPS7A10, an external BIAS voltage is required to be at least 1.4 V above the 1.2-V output voltage. This sets the minimum input voltage of this reference design to 2.6 V.

Alternatively, an LDO with a PMOS pass transistor can be used for higher output voltages. For example, the TPS7A0518 supports a 1.8-V output voltage down to approximately 2.2 V_{IN}.

2.2.2 Passive Component Selection

This reference design uses the smallest possible passive components (capacitors and inductors) available. This includes 0201-sized (0603 metric) capacitors and a 0402-sized (1005 metric) inductor to optimize the design for smallest size. Using larger passive components increases the total solution size, but also allows more available components to be chosen. Generally, a larger inductor provides higher efficiency, through its lower DC resistance, while larger capacitors reduce the ripple and noise through their higher effective capacitance.

2.3 Highlighted Products

2.3.1 TPS62801 DC/DC

The TPS62801 is a tiny, step-down DC/DC converter optimized for small size and high efficiency portable applications, such as wearables. Its 0.35-mm pitch WCSP package and 4-MHz switching frequency support the smallest size solutions. It delivers up to 1 A of output current with a non-switching quiescent current (I_Q) of just 2.3 µA. The output voltage is adjustable through a single resistor, and a MODE pin is available for lowest noise requirements.

2.3.2 TPS7A10 LDO

The TPS7A10 is a family of low drop-out (LDO) linear regulators also optimized for small size and high efficiency applications. The TPS7A10 is packaged in a 0.4-mm pitch WCSP package. It delivers up to 300 mA of output current with an I_Q of just 6 µA. It provides a BIAS pin, which is ideal for high efficiency, post-DC/DC low noise operation. The output voltage is chosen through the choice of the exact device part number.

3 Hardware and Test Results

3.1 Hardware and Schematic

The TIDA-01566 is built on a dedicated printed circuit board (PCB) and optimized for the smallest solution size. See 図 2 for the schematic. Jumpers are available for enabling the DC/DC (JP2) and LDO (JP3) independently, as well as selecting the higher efficiency pulse frequency modulation (PFM) mode or the lower noise pulse width modulation (PWM) mode for the DC/DC (JP1).

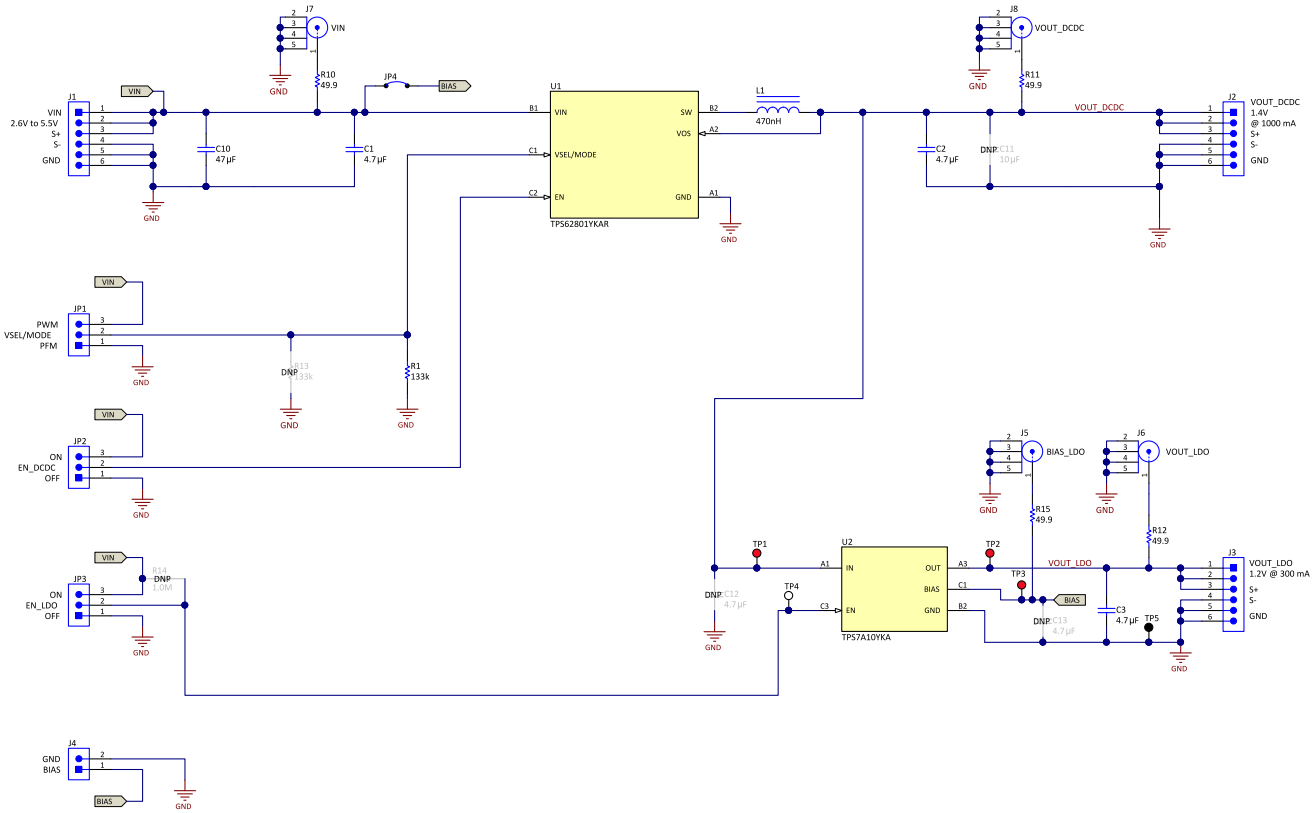


図 2. TIDA-01566 Schematic

3.2 Test Results

3.2.1 Test Setup

Three circuit configurations are measured and their performance presented: DC/DC + LDO (referred to as TIDA-01566), DC/DC only, and LDO only. The key performance data for each of the three circuits is compared at 3 V_{IN}, which each configuration supports.

3.2.2 Test Results

3.2.2.1 TIDA-01566 Circuit

Unless otherwise noted, this circuit configuration sets the DC/DC output voltage at 1.4 V and the LDO output voltage at 1.2 V.

3.2.2.1.1 Efficiency

図 3 shows the efficiency of the TIDA-01566 across various input voltages. The load is swept from 1 µA to 300 mA.

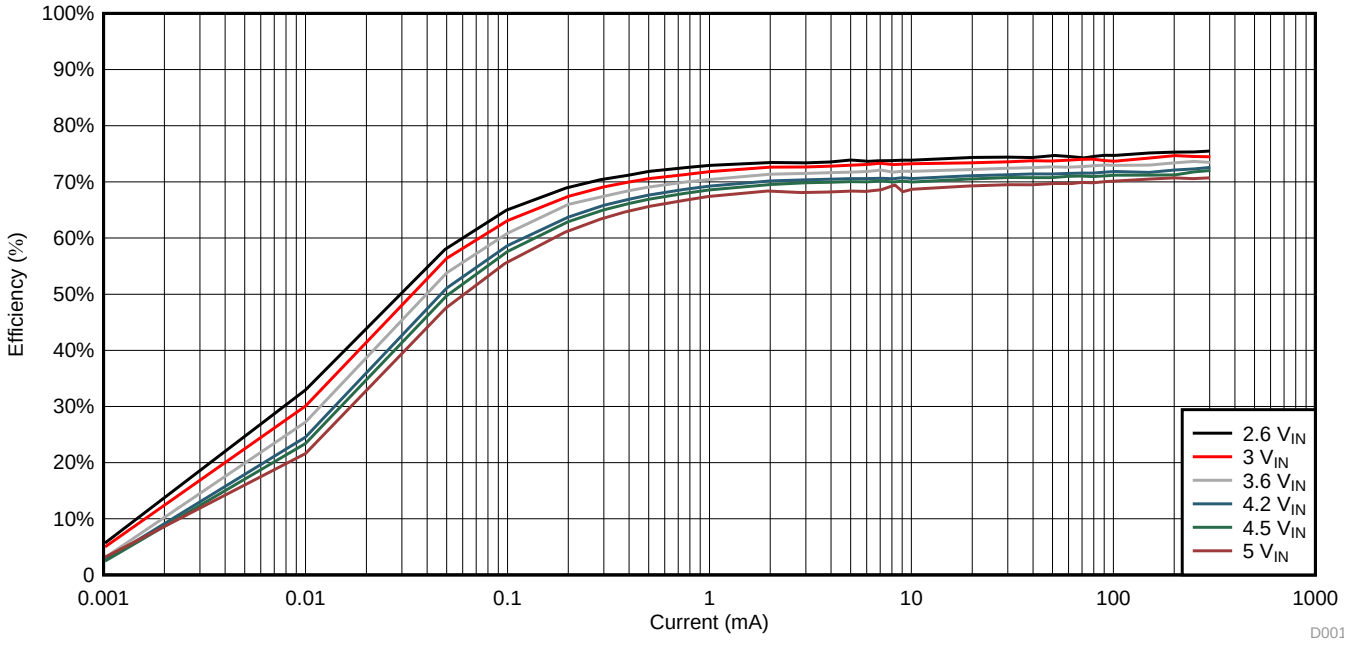


図 3. TIDA-01566 Efficiency

3.2.2.1.2 Output Ripple

図 4, 図 5, and 図 6 show the output ripple of the TIDA-01566 with a 3-V input voltage. 図 7, 図 8, and 図 9 show the output ripple of the TIDA-01566 with a 3.6-V input voltage.

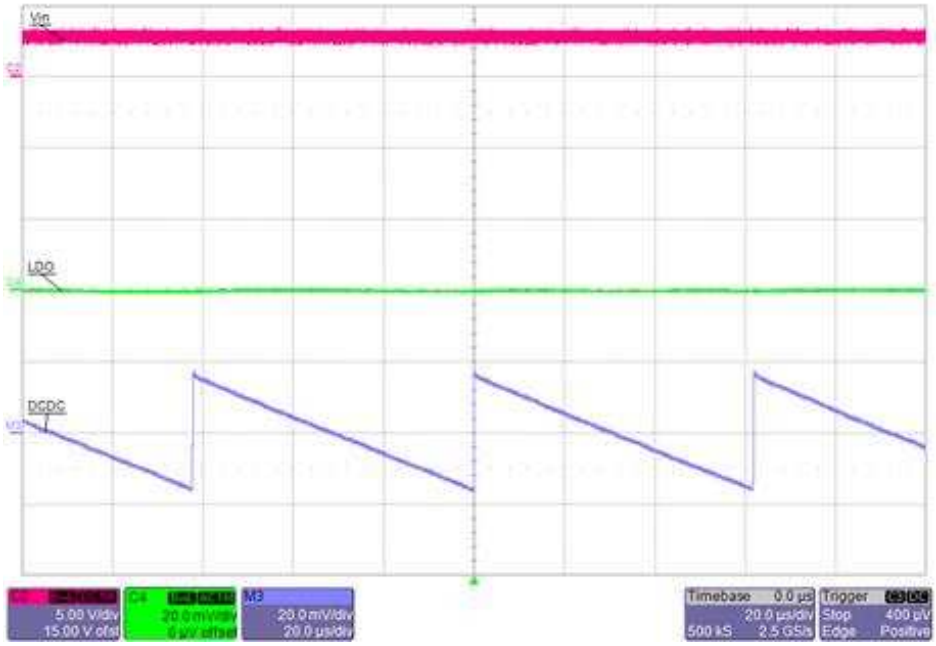


図 4. TIDA-01566 Output Ripple (V_{in} = 3 V, Load = 1 mA)

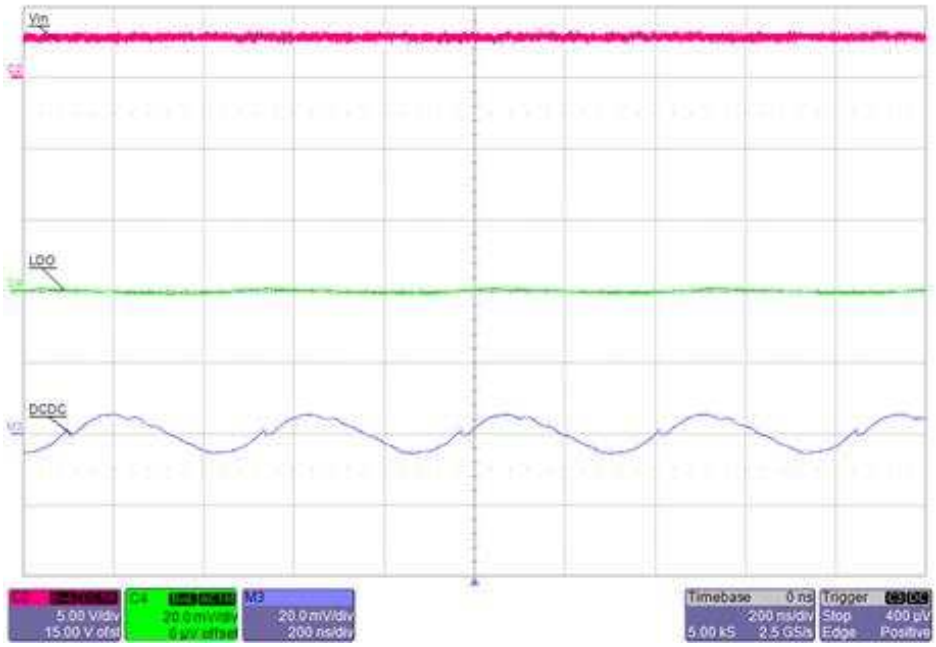


図 5. TIDA-01566 Output Ripple (V_{in} = 3 V, Load = 100 mA)

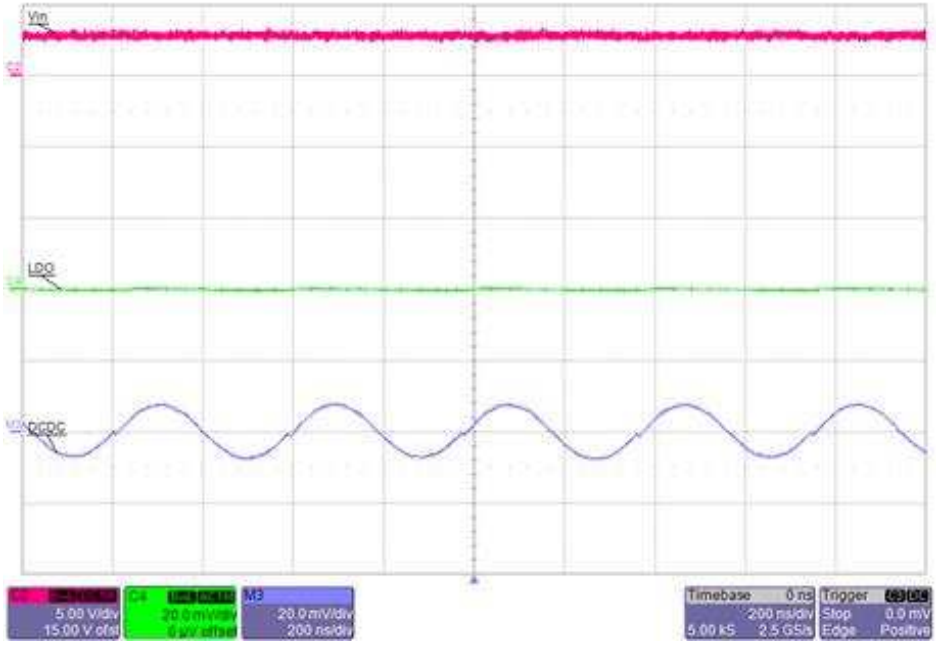


図 6. TIDA-01566 Output Ripple (V_{in} = 3 V, Load = 300 mA)

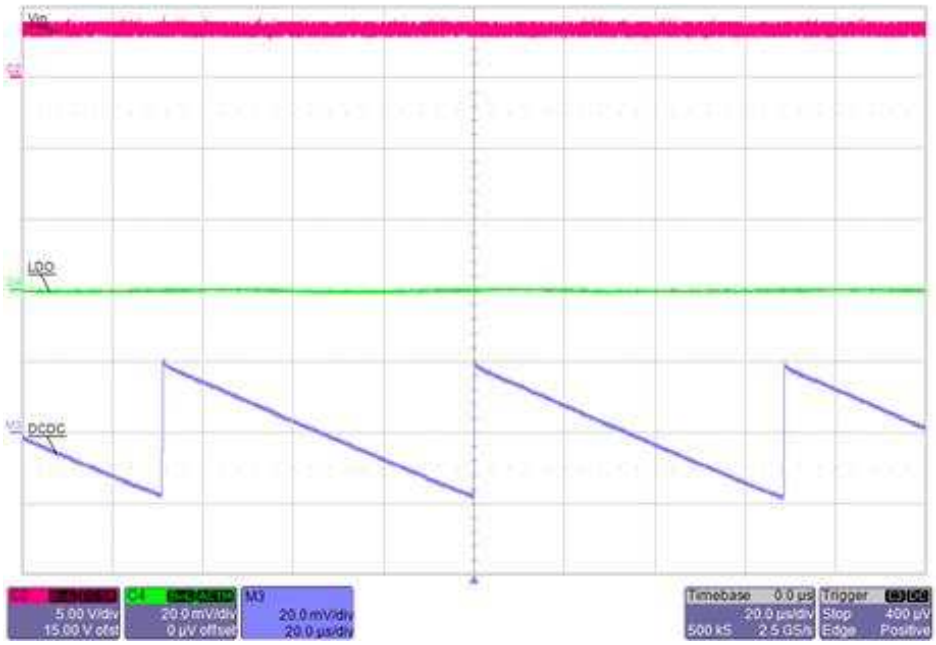


図 7. TIDA-01566 Output Ripple (V_{in} = 3.6 V, Load = 1 mA)

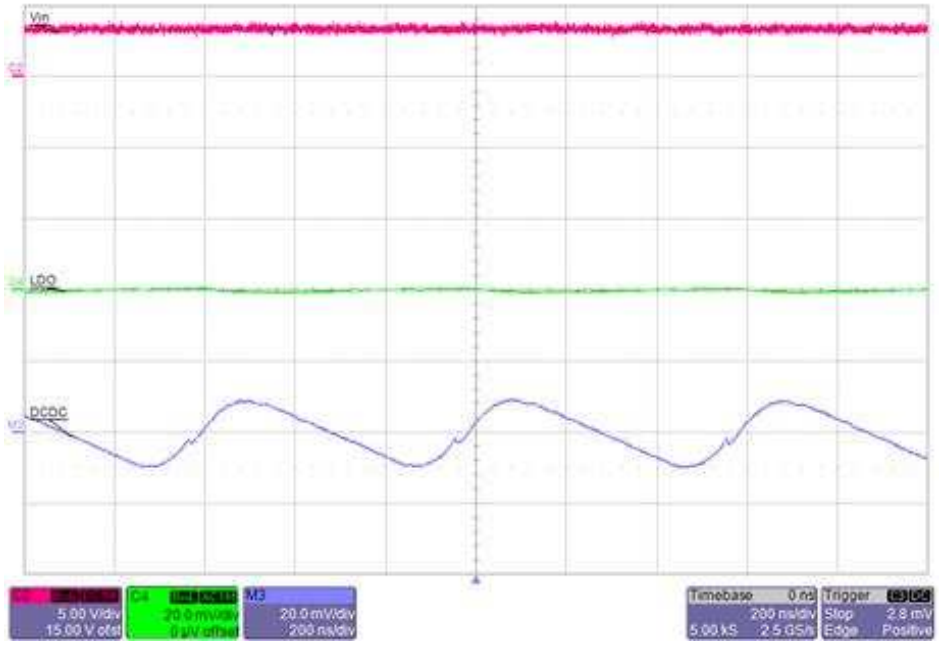


図 8. TIDA-01566 Output Ripple (V_{in} = 3.6 V, Load = 100 mA)

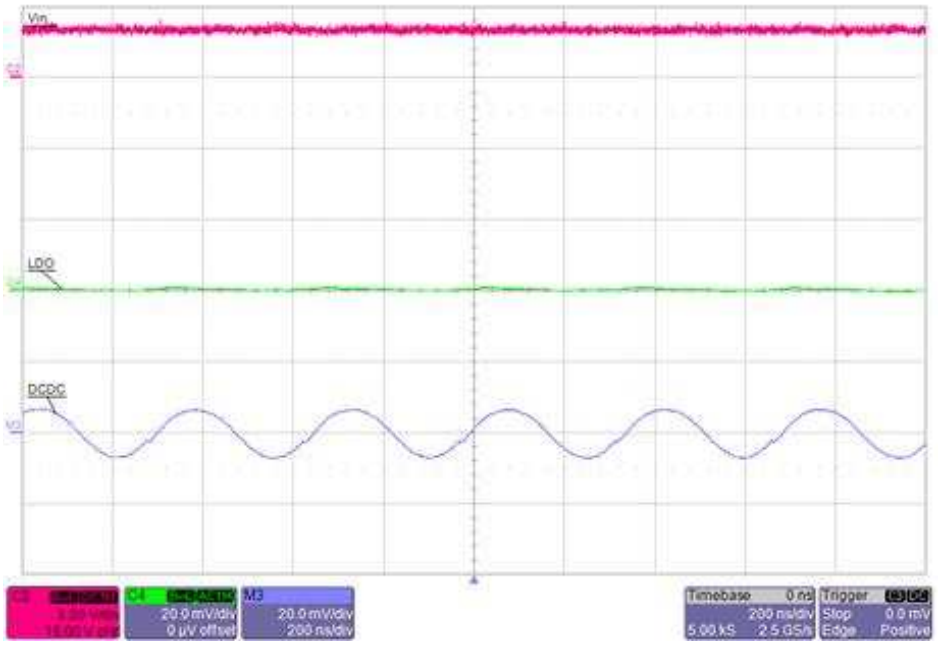


図 9. TIDA-01566 Output Ripple (V_{in} = 3.6 V, Load = 300 mA)

3.2.2.1.3 Noise Density

図 10 shows the noise density of the TIDA-01566 across multiple load currents.

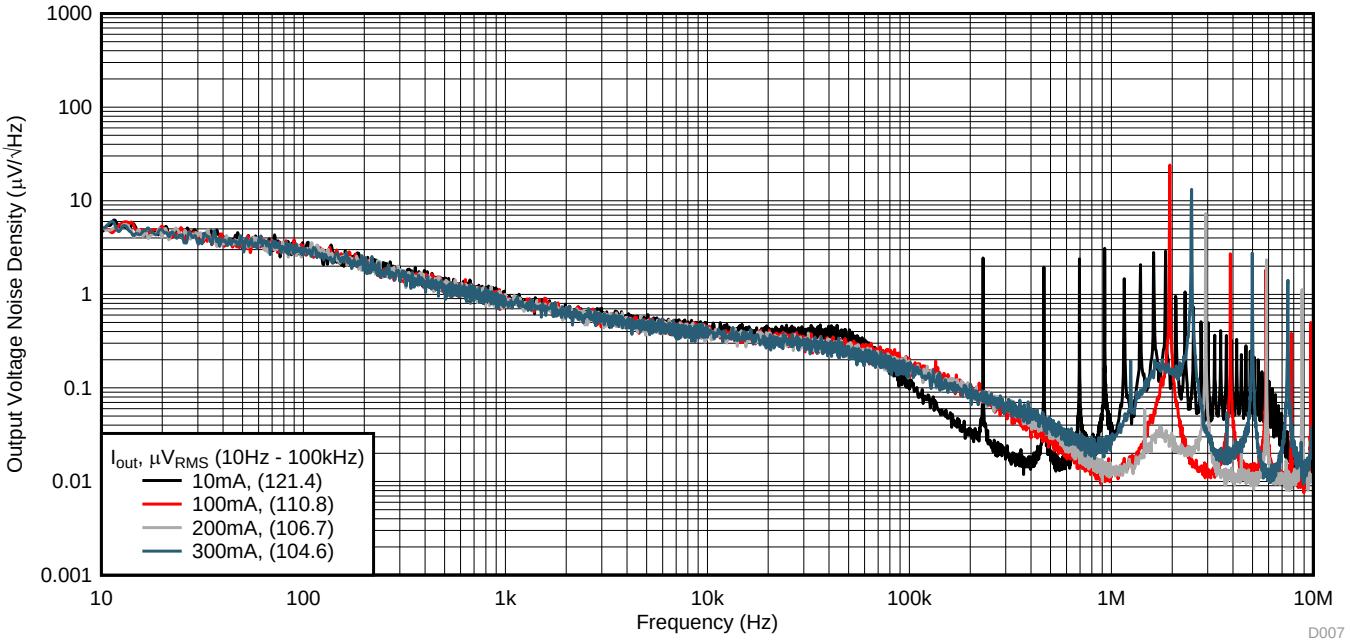


図 10. TIDA-01566 Noise Density (V_{in} = 3 V)

3.2.2.1.4 Transient Response

図 11 and 図 12 show the transient response of the TIDA-01566 to a 10-µA to 50-mA load step and to a 1-mA to 200-mA load step, respectively, both with a 3-V input voltage and 1-µsec rise and fall times. Transient response does not change significantly with changes in input voltage.

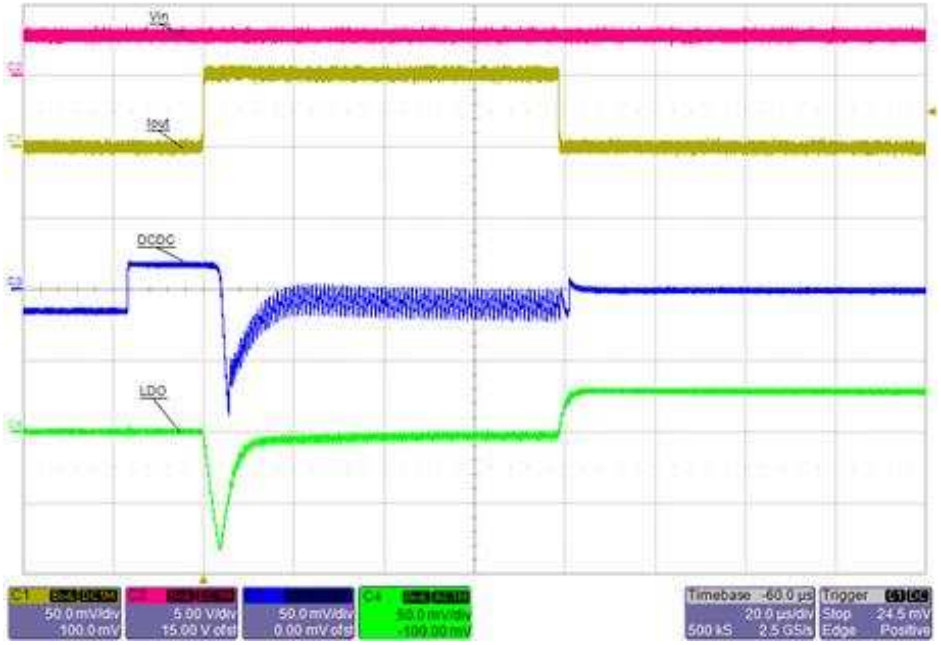


図 11. TIDA-01566 Load Transient Response (V_{in} = 3 V, 10-µA to 50-mA Load Step)

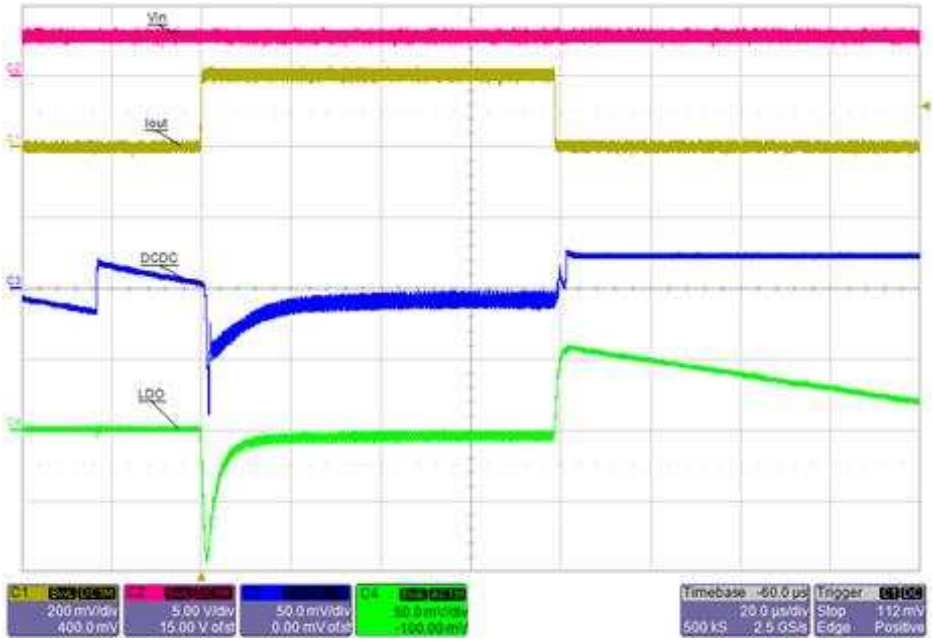


図 12. TIDA-01566 Load Transient Response (V_{in} = 3 V, 1-mA to 200-mA Load Step)

3.2.2.1.5 Thermal Performance

図 13 shows the thermal image of the TIDA-01566 with a 3-V input and 300-mA load current.

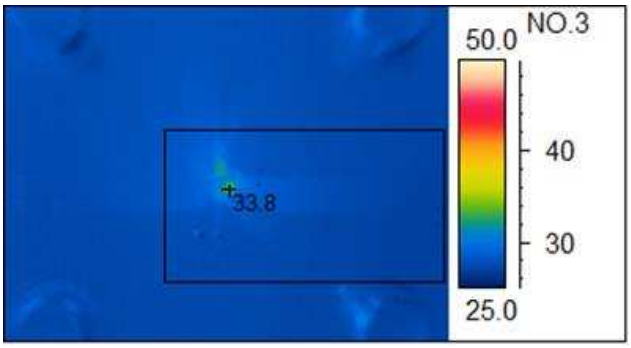


図 13. TIDA-01566 Thermal Performance (V_{IN} = 3 V, Load = 300 mA)

3.2.2.1.6 Start-Up and Shutdown

図 14 shows the start-up and shutdown of the TIDA-01566 with a 3-V input and 0-A load current.

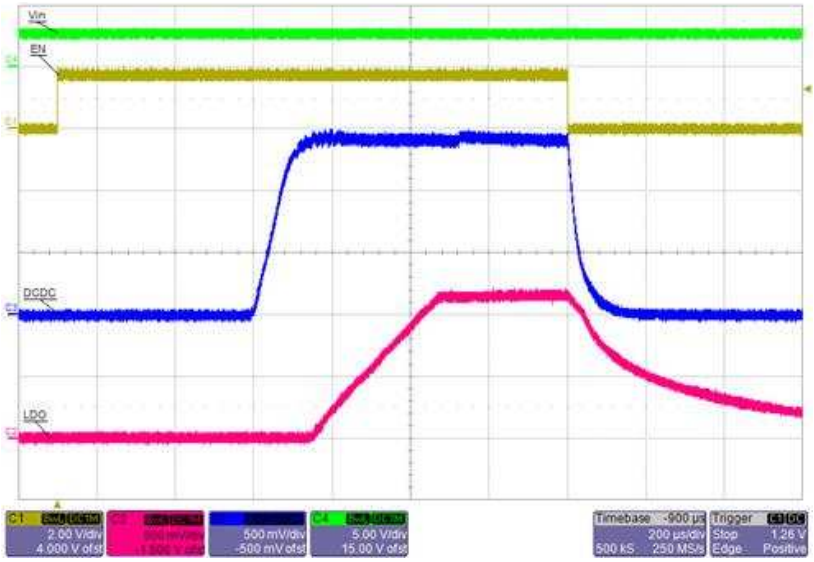


図 14. TIDA-01566 Start-Up and Shutdown (V_{IN} = 3 V, Load = 0 A)

3.2.2.2 TPS62801 (DC/DC) Circuit

This circuit configuration sets the DC/DC output voltage at 1.2 V, and does not use an LDO.

3.2.2.2.1 Efficiency

図 15 shows the efficiency of the TPS62801 across various input voltages. The load is swept from 1 µA to 1 A, with the exception of the forced PWM mode, which is swept from 1 mA to 1 A. Also, the load current is limited to 700 mA at a 1.8-V input voltage.

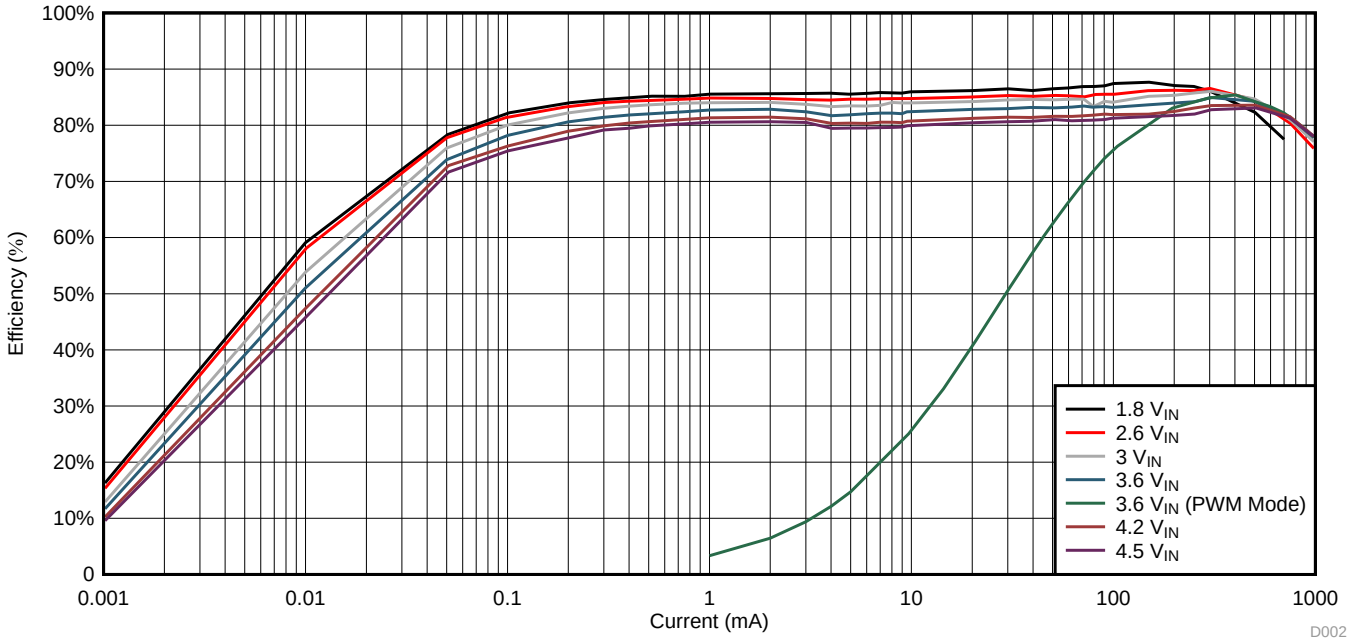


図 15. TPS62801 Efficiency

3.2.2.2.2 Output Ripple

図 16, 図 17, and 図 18 show the output ripple of the TPS62801 with a 3-V input voltage. 図 19, 図 20, and 図 21 show the output ripple of the TPS62801 with a 3.6-V input voltage.

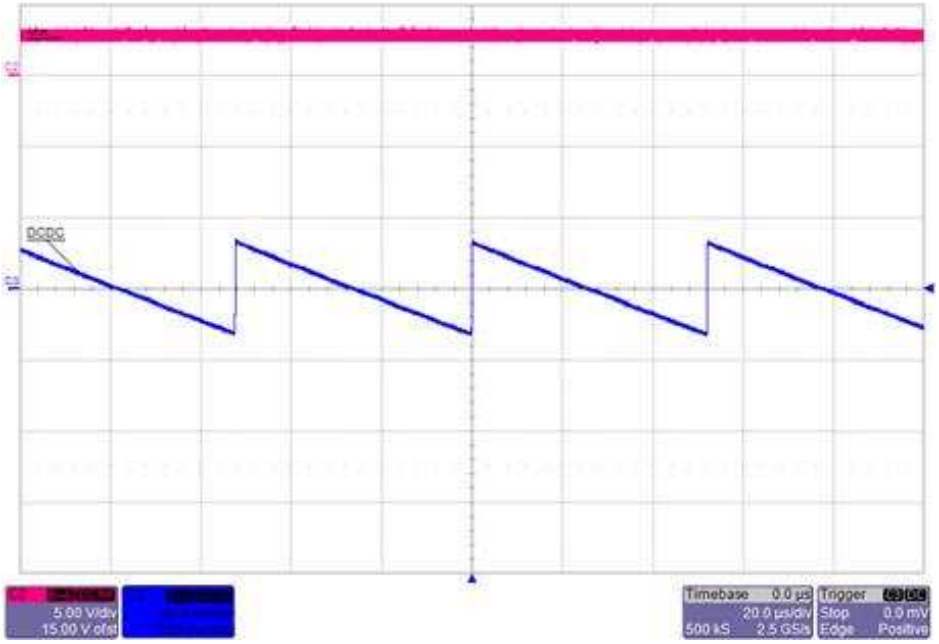


図 16. TPS62801 Output Ripple (V_{IN} = 3 V, Load = 1 mA)

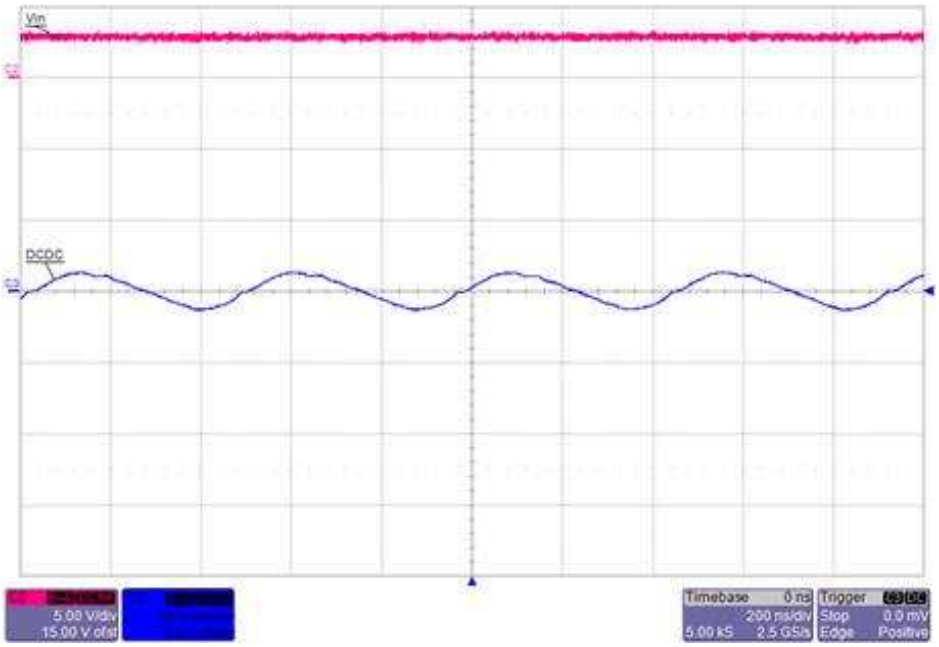


図 17. TPS62801 Output Ripple (V_{IN} = 3 V, Load = 100 mA)

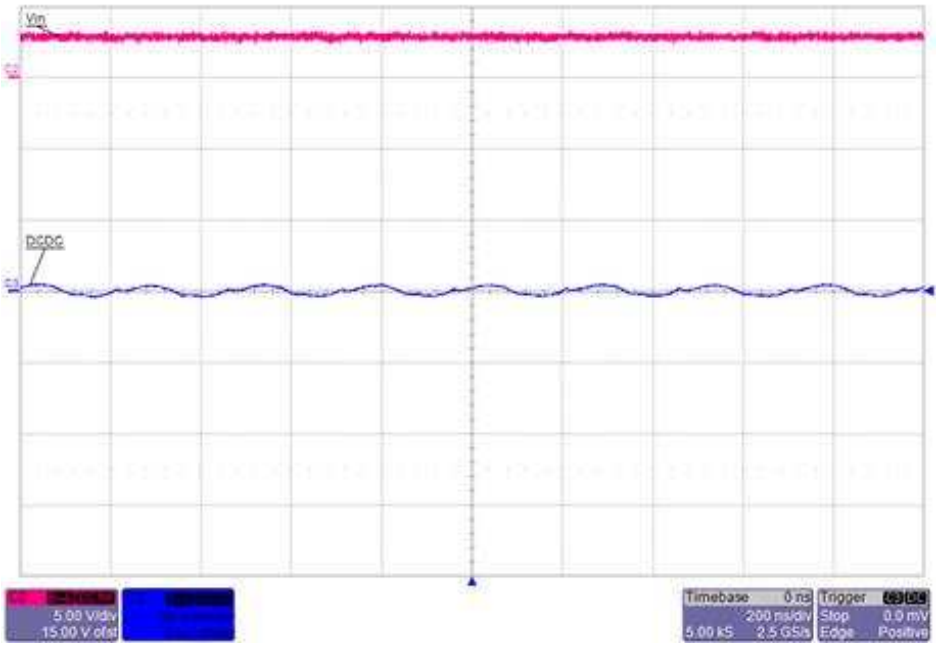


図 18. TPS62801 Output Ripple (V_{IN} = 3 V, Load = 300 mA)

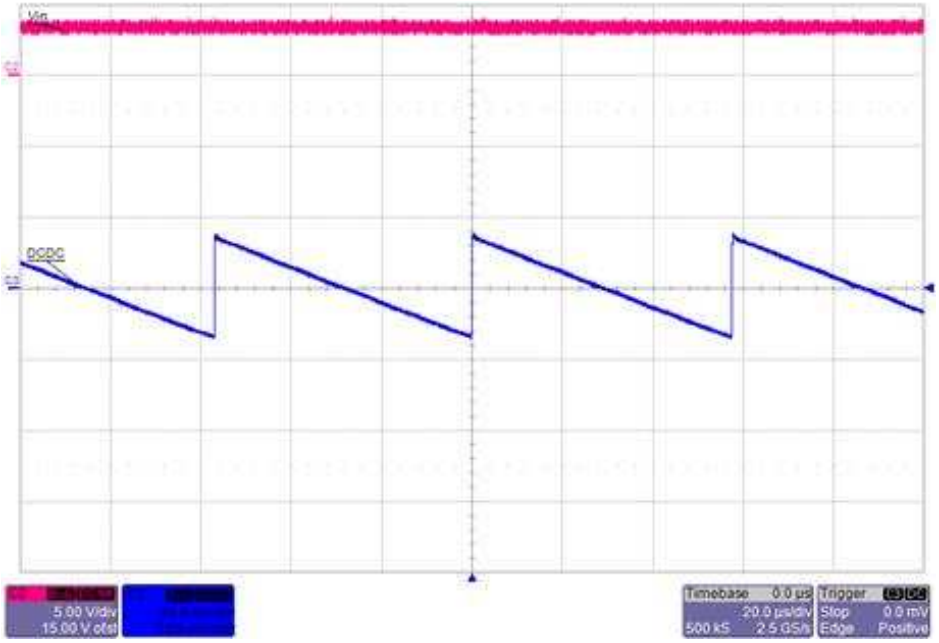


図 19. TPS62801 Output Ripple (V_{IN} = 3.6 V, Load = 1 mA)

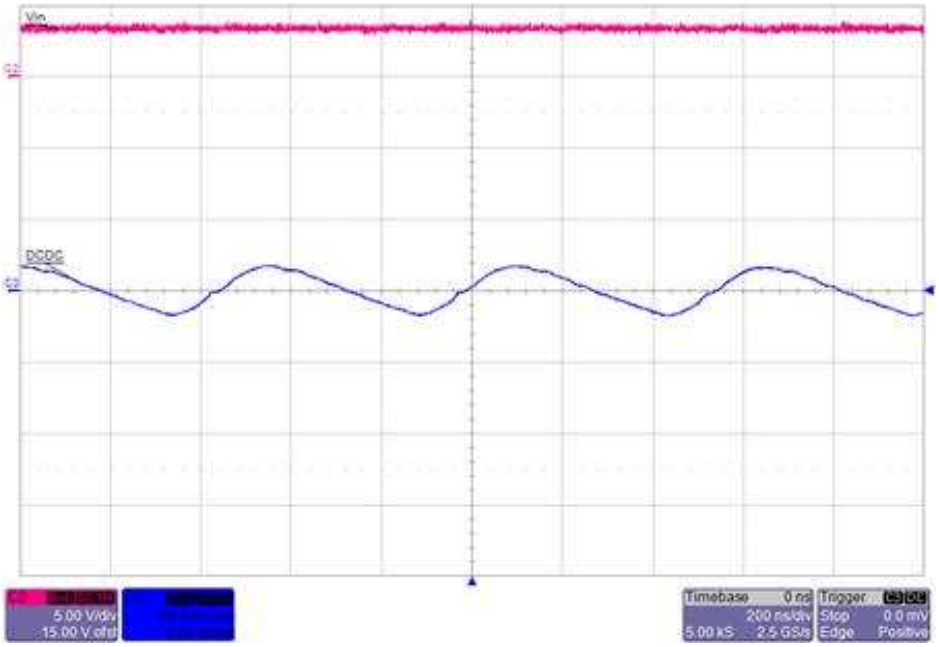


図 20. TPS62801 Output Ripple (V_{IN} = 3.6 V, Load = 100 mA)

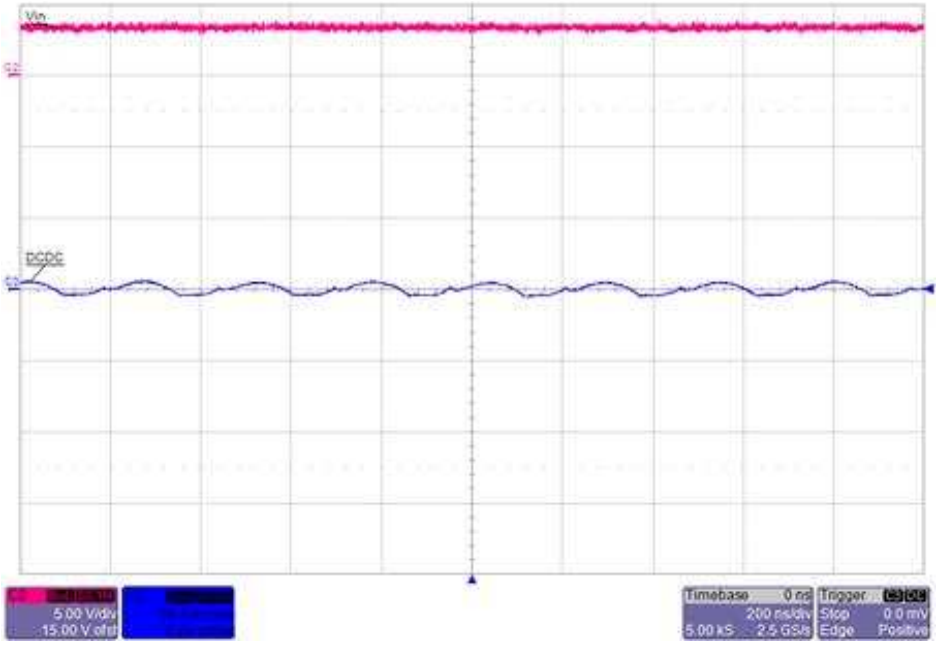


図 21. TPS62801 Output Ripple (V_{IN} = 3.6 V, Load = 300 mA)

3.2.2.2.3 Noise Density

図 31 shows the noise density of the TPS62801 across multiple load currents.

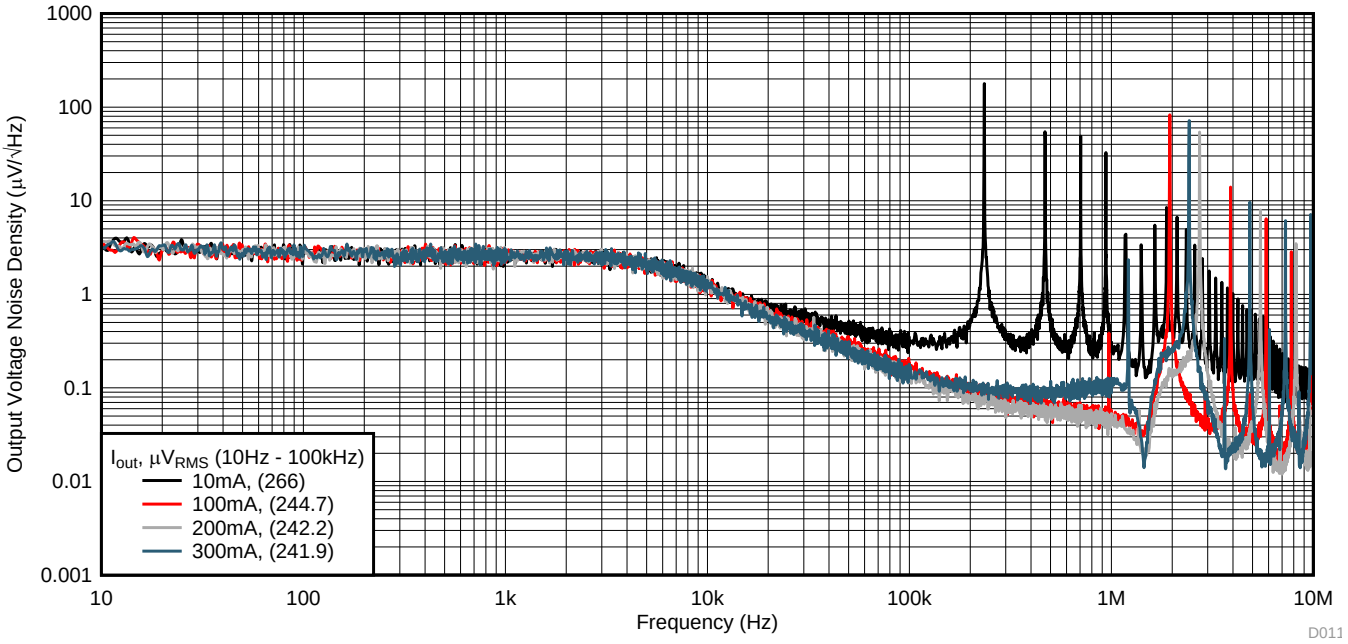


図 22. TPS62801 Noise Density (V_{in} = 3 V)

3.2.2.2.4 Transient Response

図 23 and 図 24 show the transient response of the TPS62801 to a 10-µA to 50-mA load step and to a 1-mA to 200-mA load step, respectively, both with a 3-V input voltage and 1-µsec rise and fall times. Transient response does not change significantly with changes in input voltage.

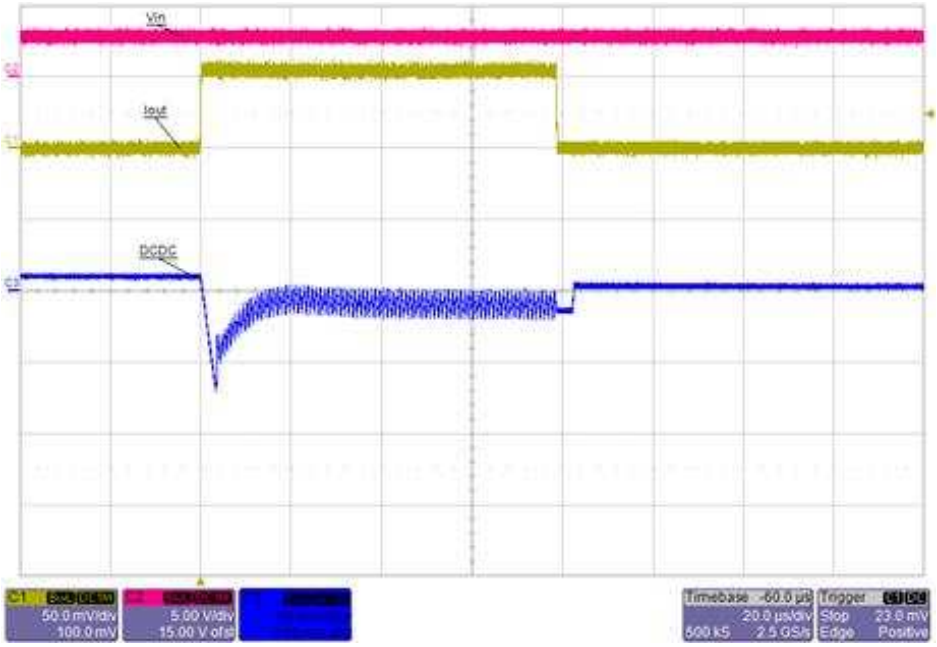


図 23. TPS62801 Load Transient Response (V_{IN} = 3 V, 10-µA to 50-mA Load Step)

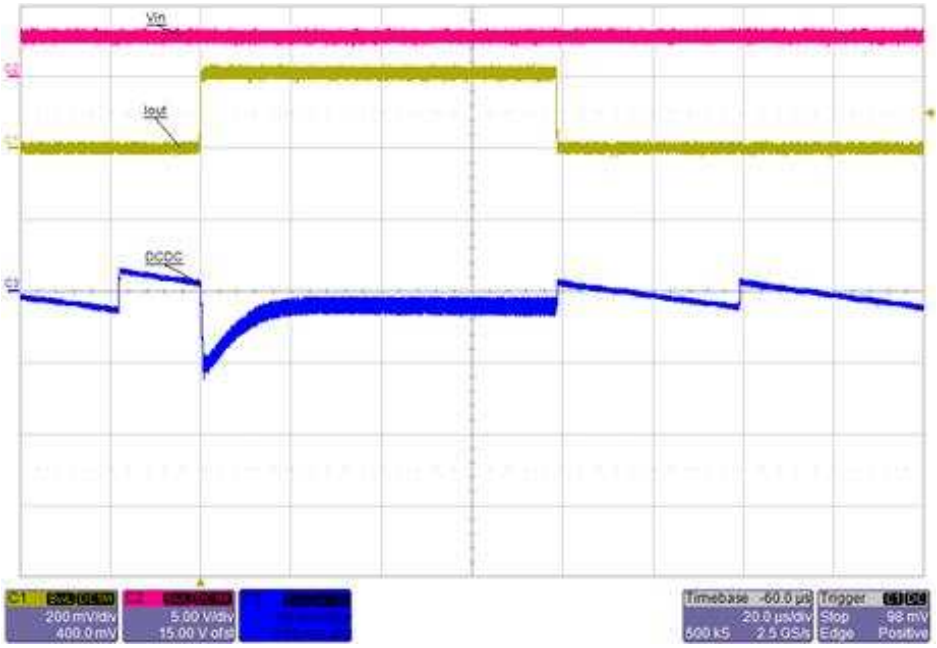


図 24. TPS62801 Load Transient Response (V_{IN} = 3 V, 1-mA to 200-mA Load Step)

3.2.2.2.5 Thermal Performance

図 25 shows the thermal image of the TPS62801 with a 3-V input and 300-mA load current.

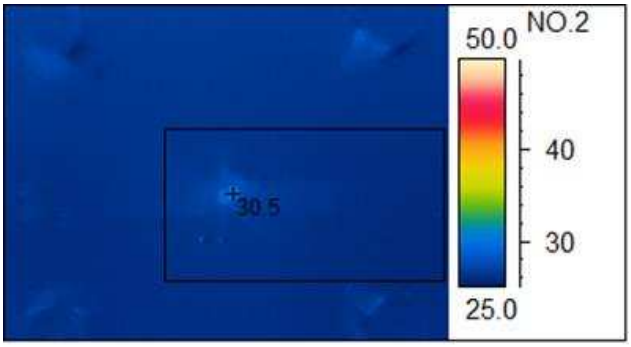


図 25. TPS62801 Thermal Performance (V_{IN} = 3 V, Load = 300 mA)

3.2.2.2.6 Start-Up and Shutdown

図 26 shows the start-up and shutdown of the TPS62801 with a 3-V input and 0-A load current.

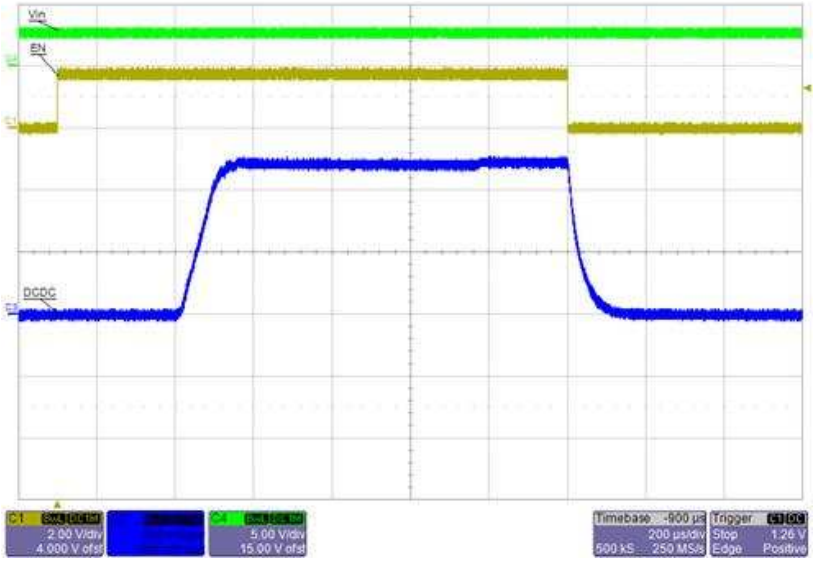


図 26. TPS62801 Start-Up and Shutdown (V_{IN} = 3 V, Load = 0 A)

3.2.2.3 TPS7A10 (LDO) Circuit

This circuit configuration sets the LDO output voltage at 1.2 V, and does not use a DC/DC.

3.2.2.3.1 Efficiency

図 27 shows the efficiency of the TPS7A10 with a 3-V input. The load is swept from 1 µA to 300 mA.

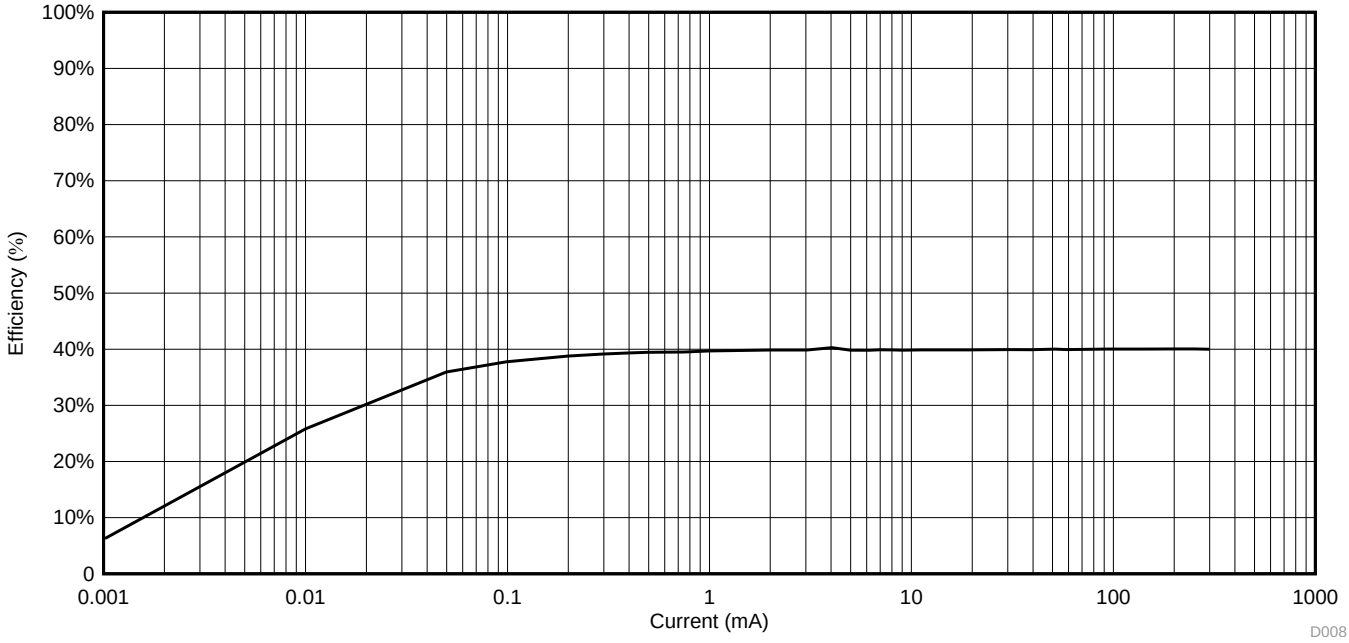


図 27. TPS7A10 Efficiency at V_{IN} = 3 V

3.2.2.3.2 Output Ripple

図 28, 図 29, and 図 30 show the output ripple of the TPS7A10 with a 3-V input voltage.

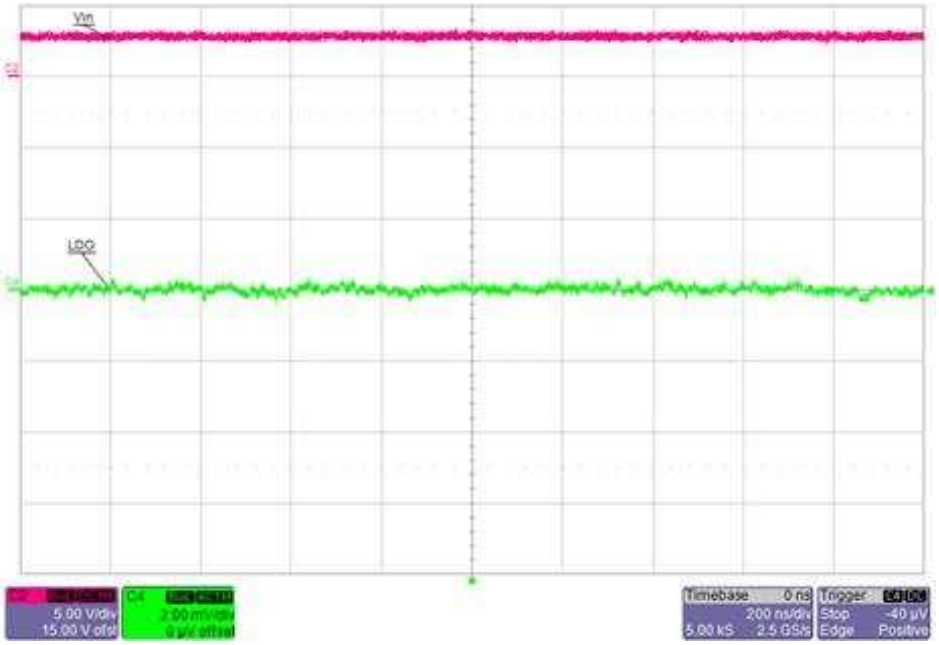


図 28. TPS7A10 Output Ripple (V_{IN} = 3 V, Load = 1 mA)

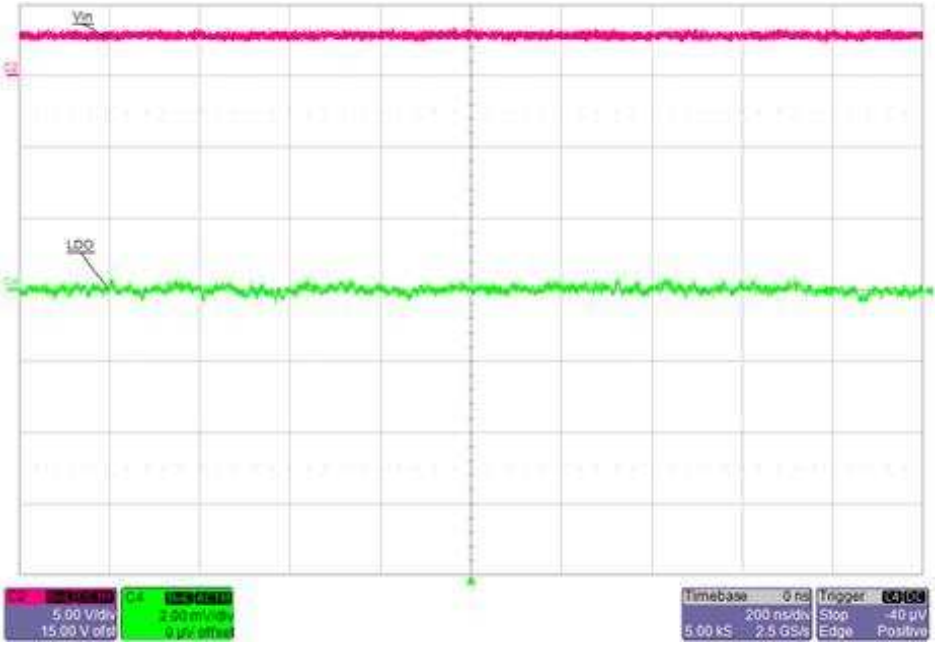


図 29. TPS7A10 Output Ripple (V_{IN} = 3 V, Load = 100 mA)

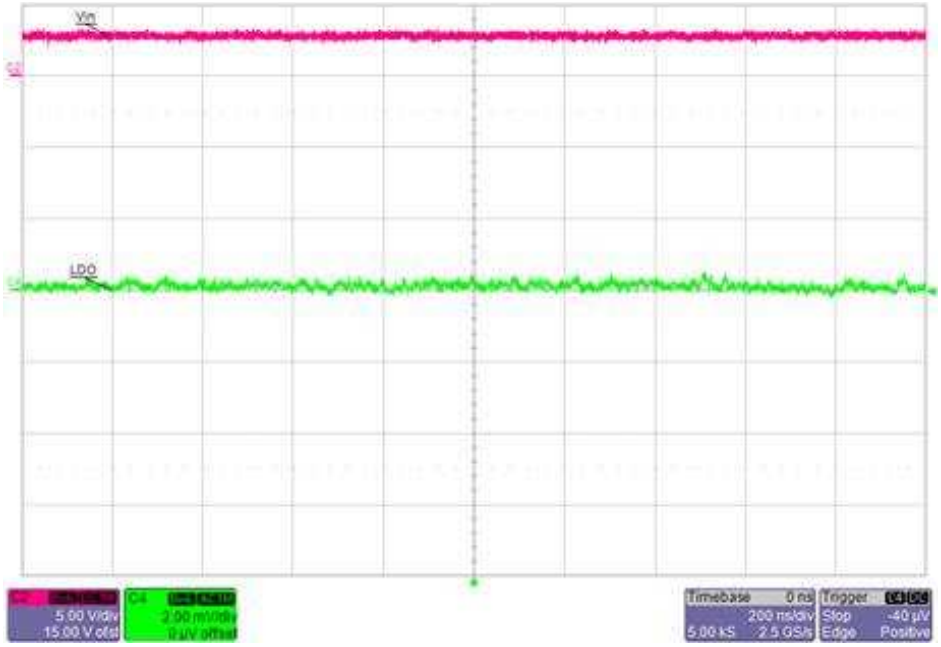


図 30. TPS7A10 Output Ripple (V_{IN} = 3 V, Load = 300 mA)

3.2.2.3.3 *Noise Density*

図 31 shows the noise density of the TPS7A10 across multiple load currents.

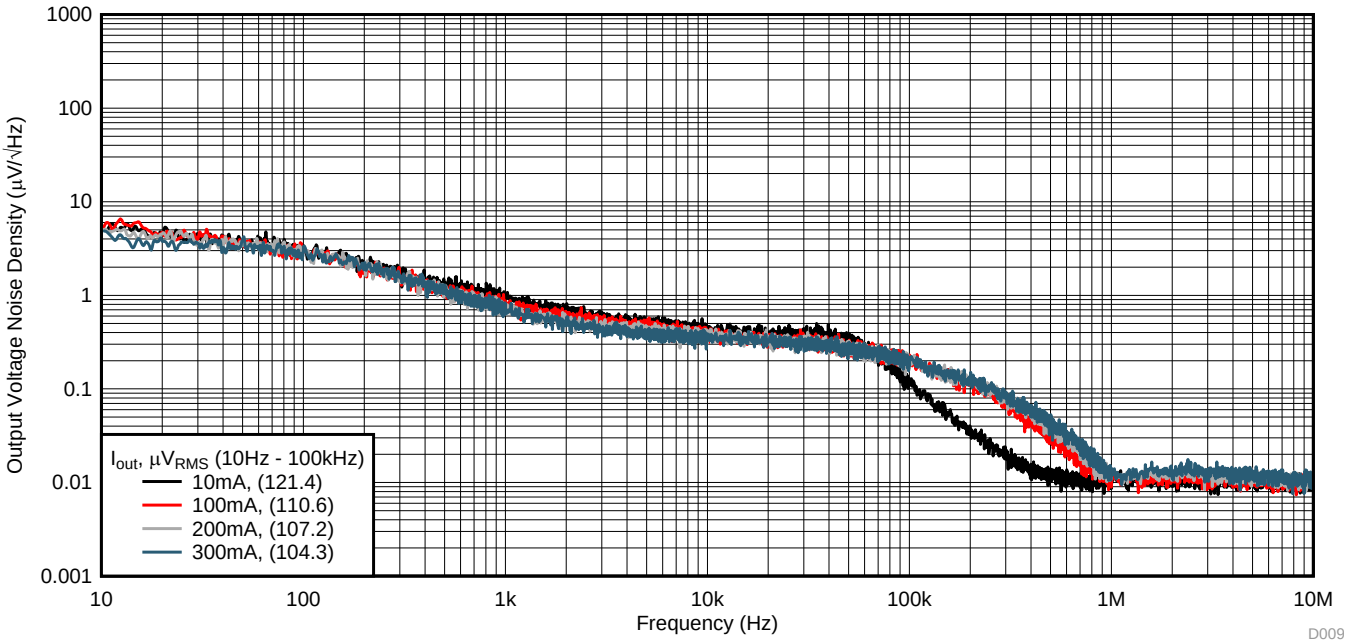


図 31. TPS7A10 Noise Density (V_{in} = 3 V)

3.2.2.3.4 Transient Response

図 32 and 図 33 show the transient response of the TPS7A10 to a 10-µA to 50-mA load step and to a 1-mA to 200- mA load step, respectively, both with a 3-V input voltage and 1-µsec rise and fall times. Transient response does not change significantly with changes in input voltage.

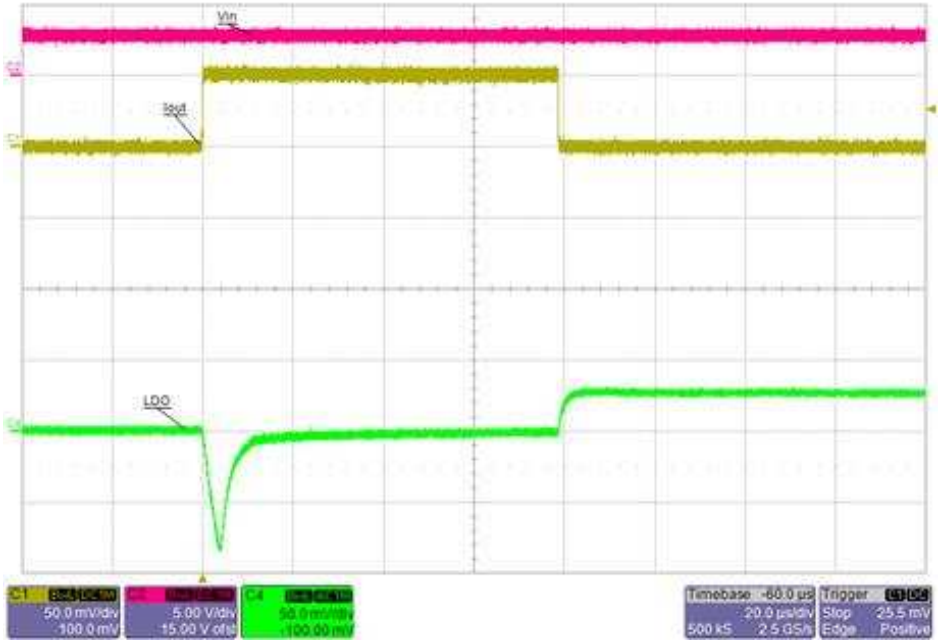


図 32. TPS7A10 Load Transient Response (V_{IN} = 3 V, 10-µA to 50-mA Load Step)

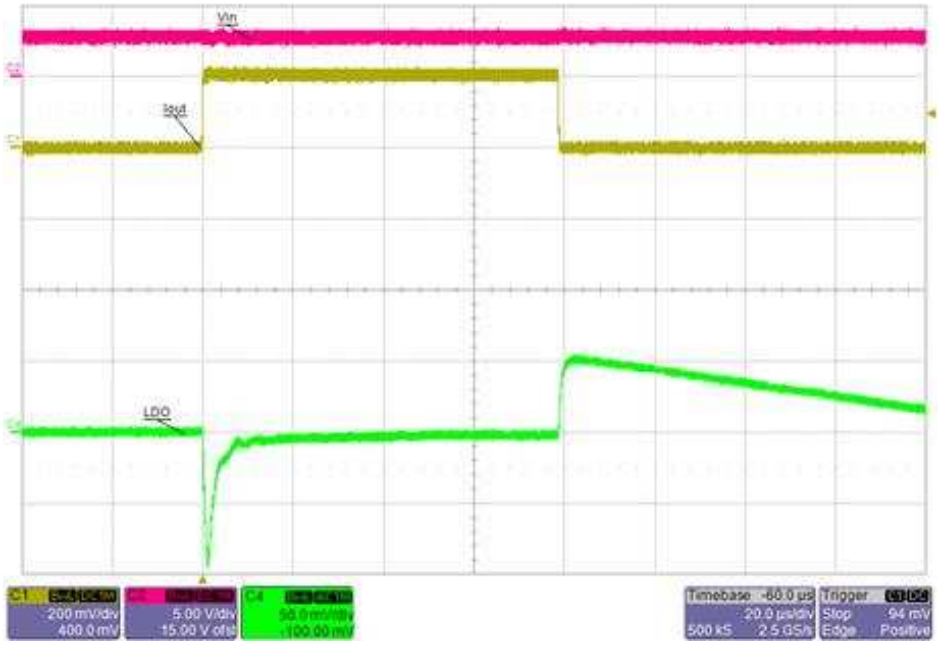


図 33. TPS7A10 Load Transient Response (V_{IN} = 3 V, 1-mA to 200-mA Load Step)

3.2.2.3.5 Thermal Performance

図 34 shows the thermal image of the TPS7A10 with a 3-V input and 300-mA load current.

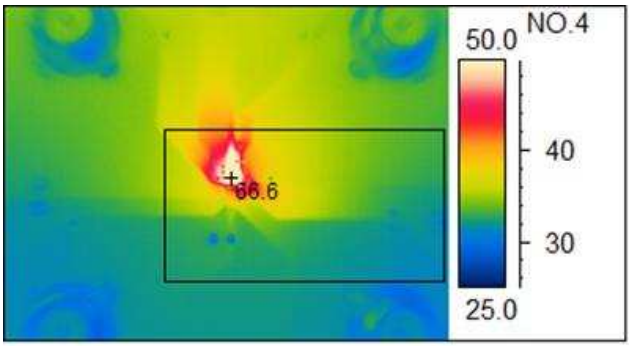


図 34. TPS7A10 Thermal Performance (V_{IN} = 3 V, Load = 300 mA)

3.2.2.3.6 Start-Up and Shutdown

図 35 shows the start-up and shutdown of the TPS7A10 with a 3-V input and 0-A load current.

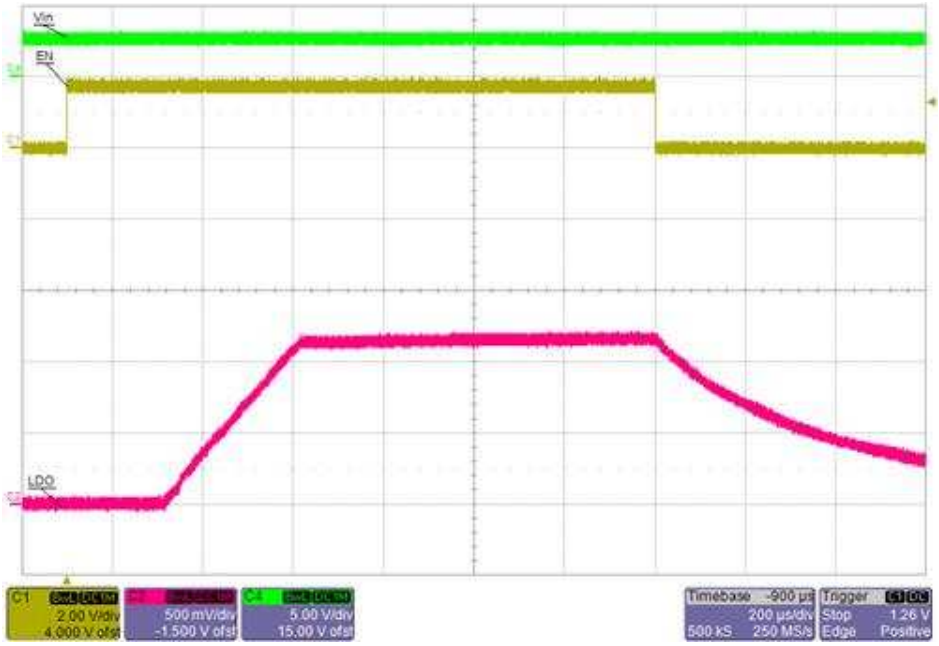


図 35. TPS7A10 Start-Up and Shutdown (V_{IN} = 3 V, Load = 0 A)

3.2.2.4 Circuit Comparison

This section compares the performance of each of the previous three configurations at a V_{IN} of 3 V.

3.2.2.4.1 Efficiency

図 36 shows the efficiency of the TIDA-01566 compared to the TPS62801 DC/DC converter and the TPS7A10 LDO, with a 3-V input voltage.

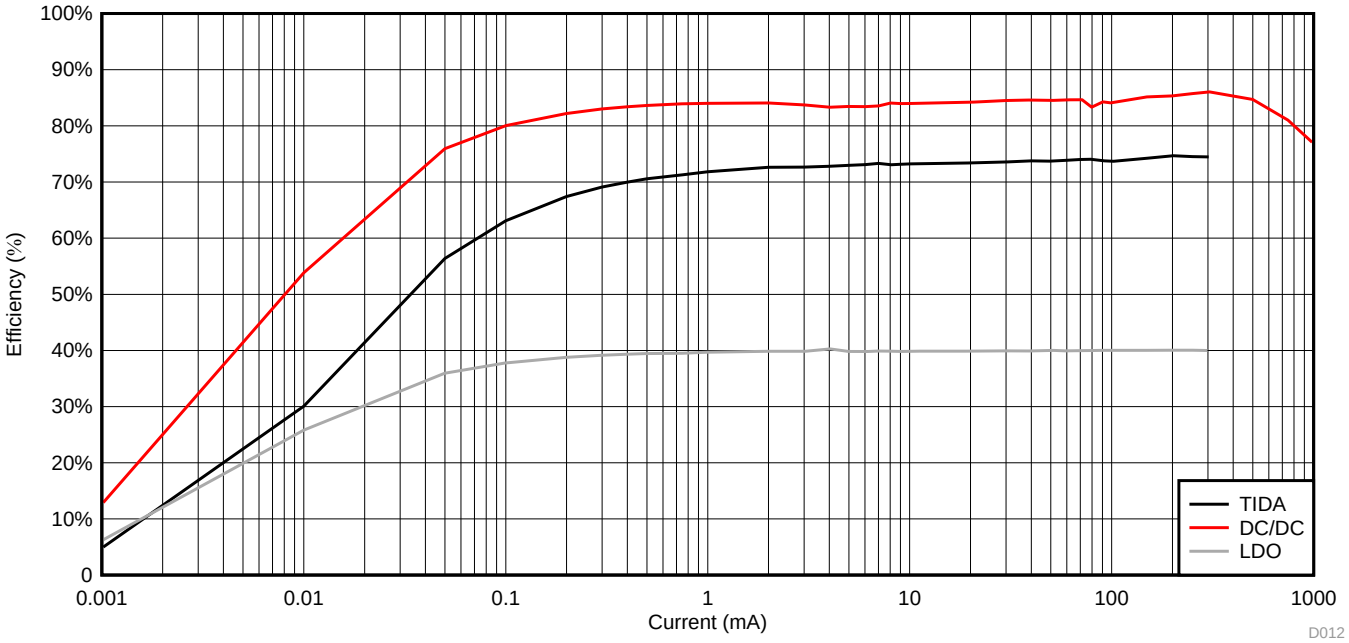


図 36. Efficiency Comparison (V_{IN} = 3 V)

3.2.2.4.2 Switching Quiescent Current (No-Load Input Current)

図 37 compares the no-load input current of each design over input voltage.

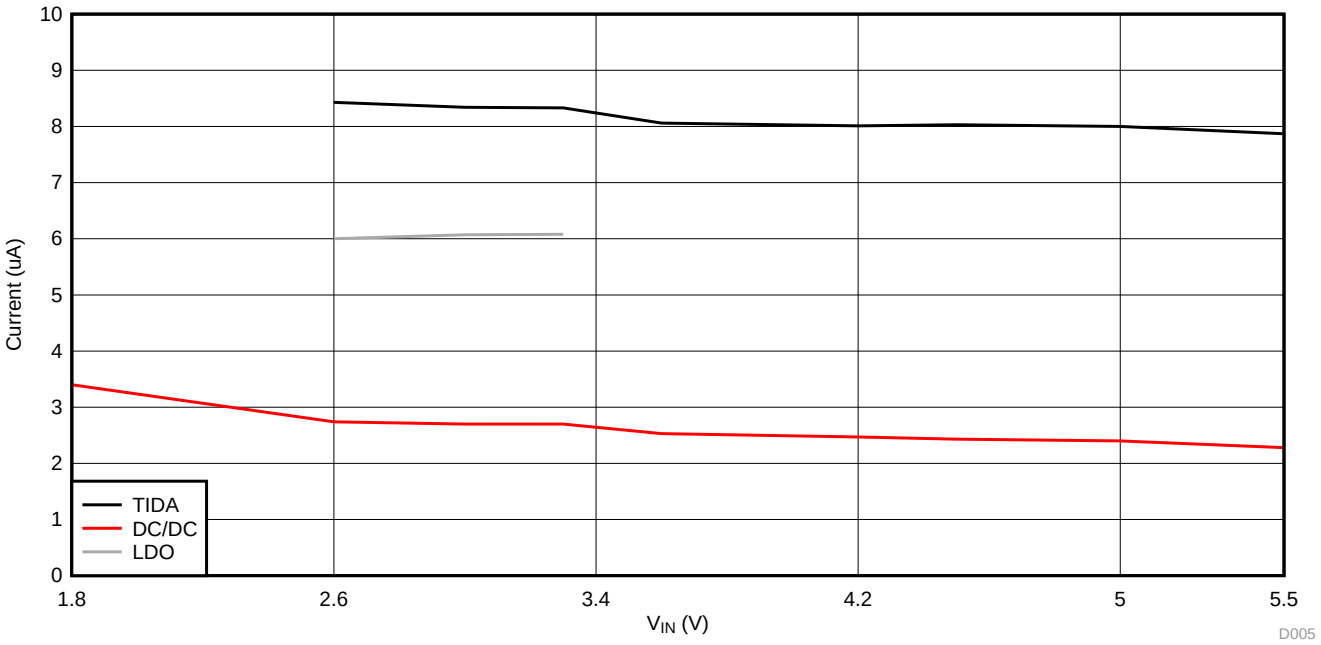


図 37. Switching Quiescent Current Comparison

3.2.2.4.3 Load Regulation

図 38 compares the load regulation of each design with a 3-V input voltage. The DC/DC has a higher output voltage at lower load currents, because the increased output voltage ripple averages up the DC output voltage.

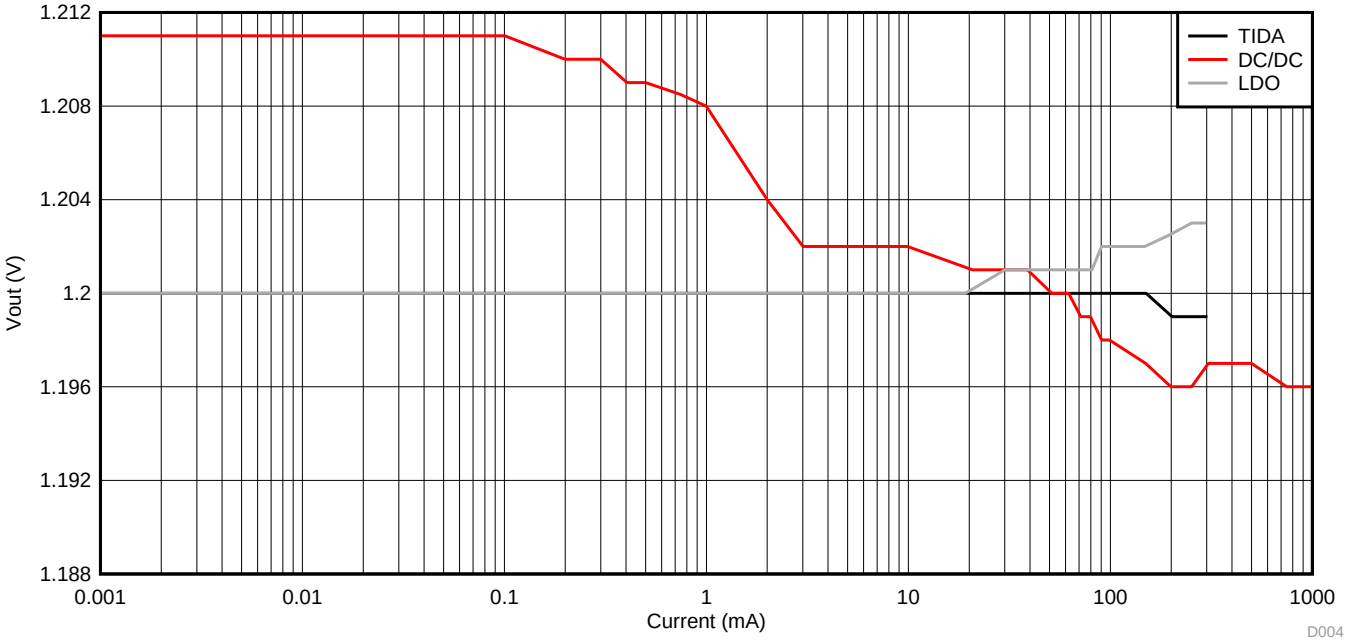


図 38. Load Regulation Comparison

3.2.2.4.4 Line Regulation

図 39 compares the line regulation of each design at both 100-µA and 300-mA load currents. The DC/DC has a higher output voltage at lower load currents, because the increased output voltage ripple averages up the DC output voltage.

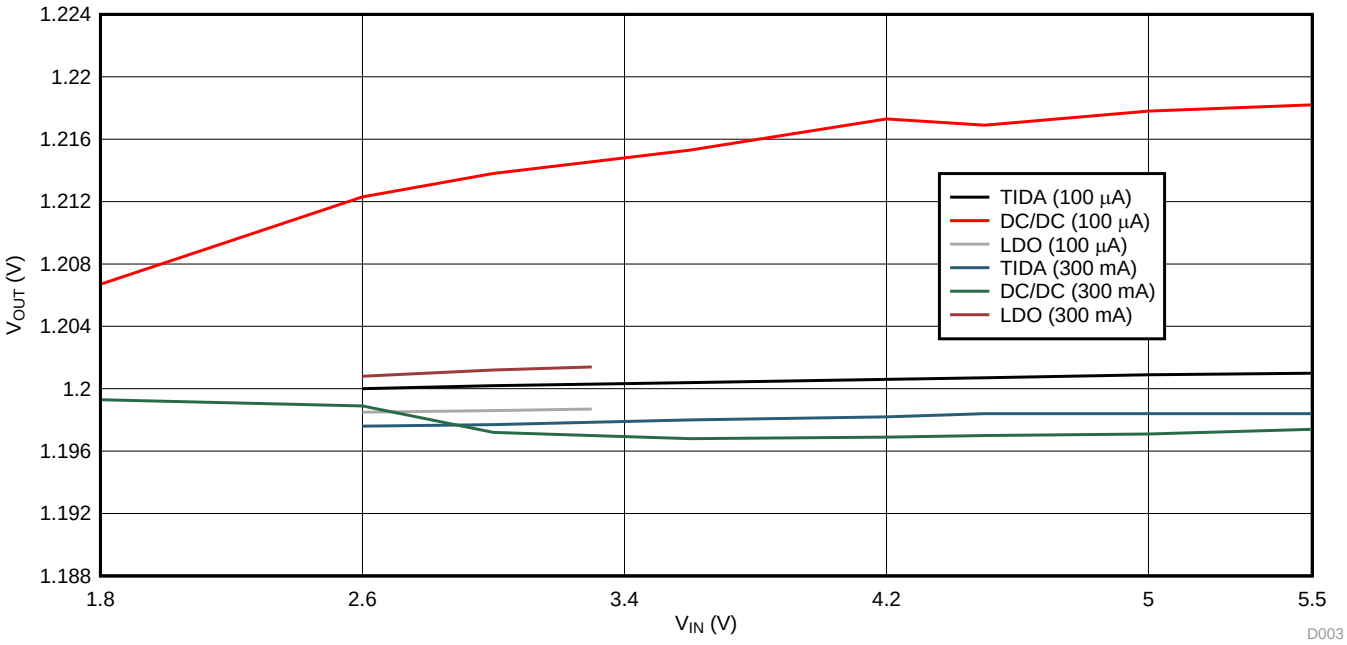


図 39. Line Regulation Comparison

3.2.2.4.5 Output Ripple

表 2 compares the output ripple of the TIDA-01566 to the TPS62801 DC/DC converter and the TPS7A10 LDO at different load currents, with a 3-V input voltage. The output voltage ripple waveforms are shown in the preceding sections.

表 2. Output Ripple Comparison

	1 mA	100 mA	300 mA
TIDA-01566	< 1 mV	< 1 mV	< 1 mV
TPS62801	25 mV	10 mV	3 mV
TPS7A10	< 1 mV	< 1 mV	< 1 mV

3.2.2.4.6 Noise Density

図 40 compares the noise density of each design with a 10 mA load. The LDO reduces the noise of the DC/DC by its PSRR.

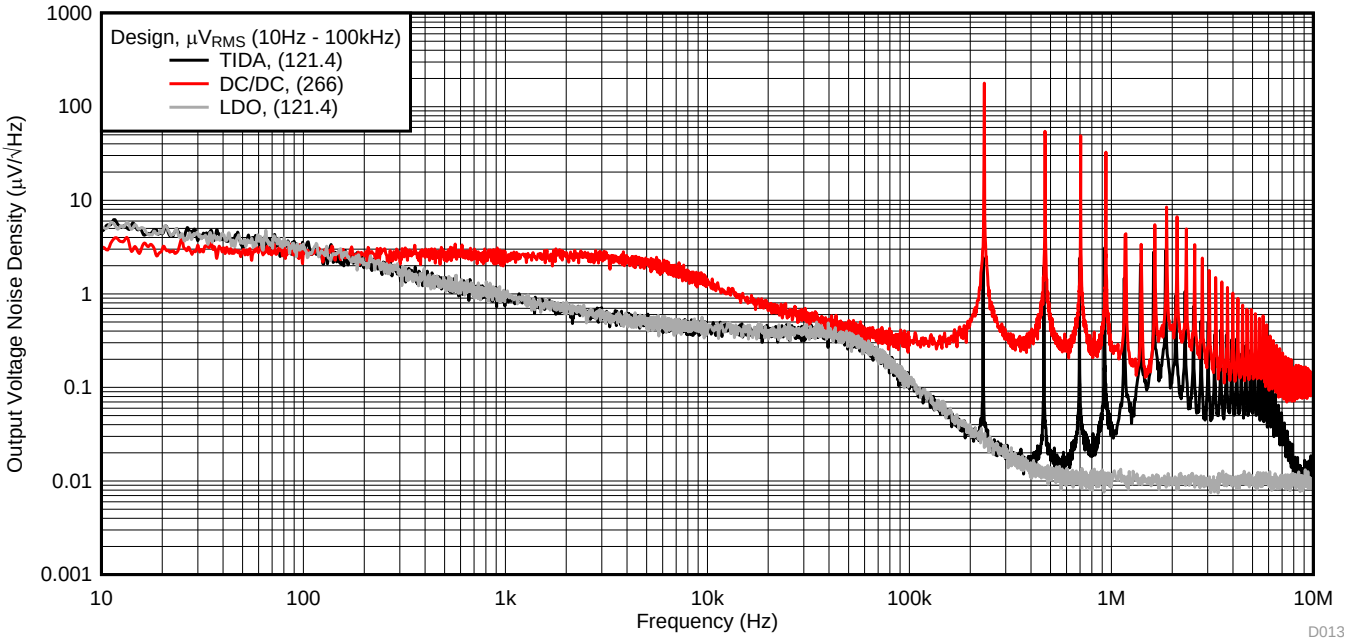


図 40. Noise Density Comparison (V_{in} = 3 V, Load = 10 mA)

3.2.2.4.7 Spurious Noise

図 41, 図 42, and 図 43 show the spurious noise of each design at 10 mA, 100 mA, and 300 mA, respectively. The LDO reduces the noise of the DC/DC by its PSRR.

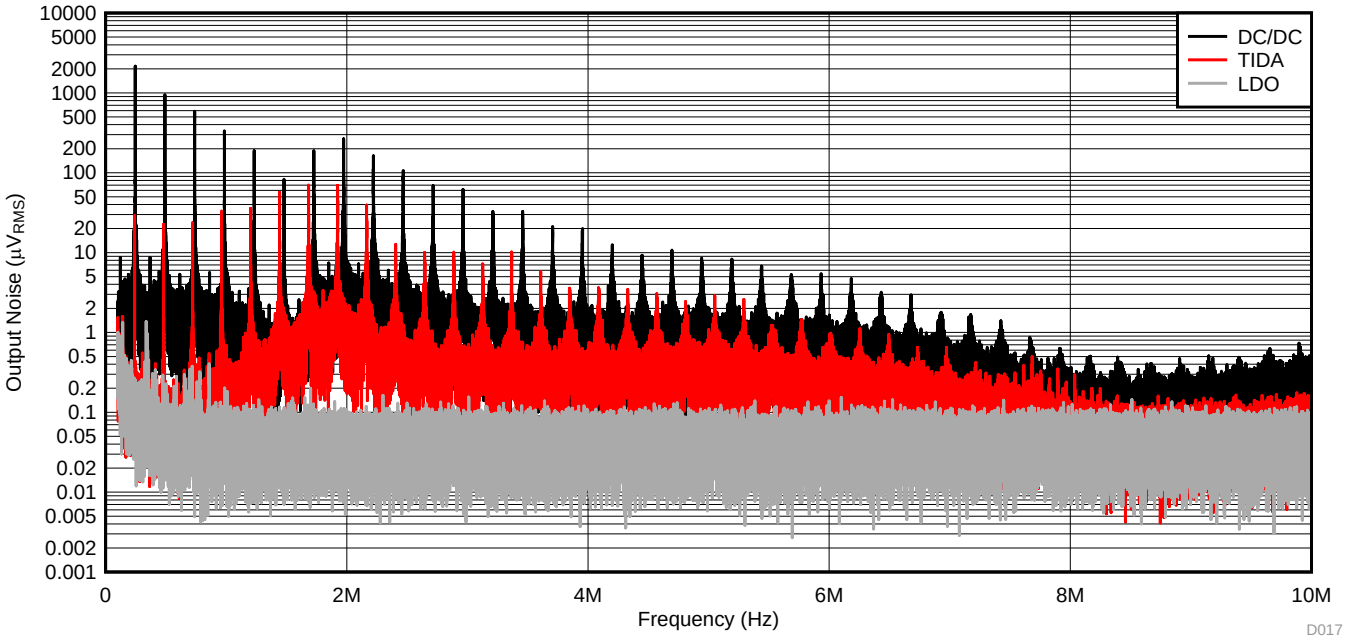


図 41. Spurious Noise Comparison (V_{in} = 3 V, Load = 10 mA)

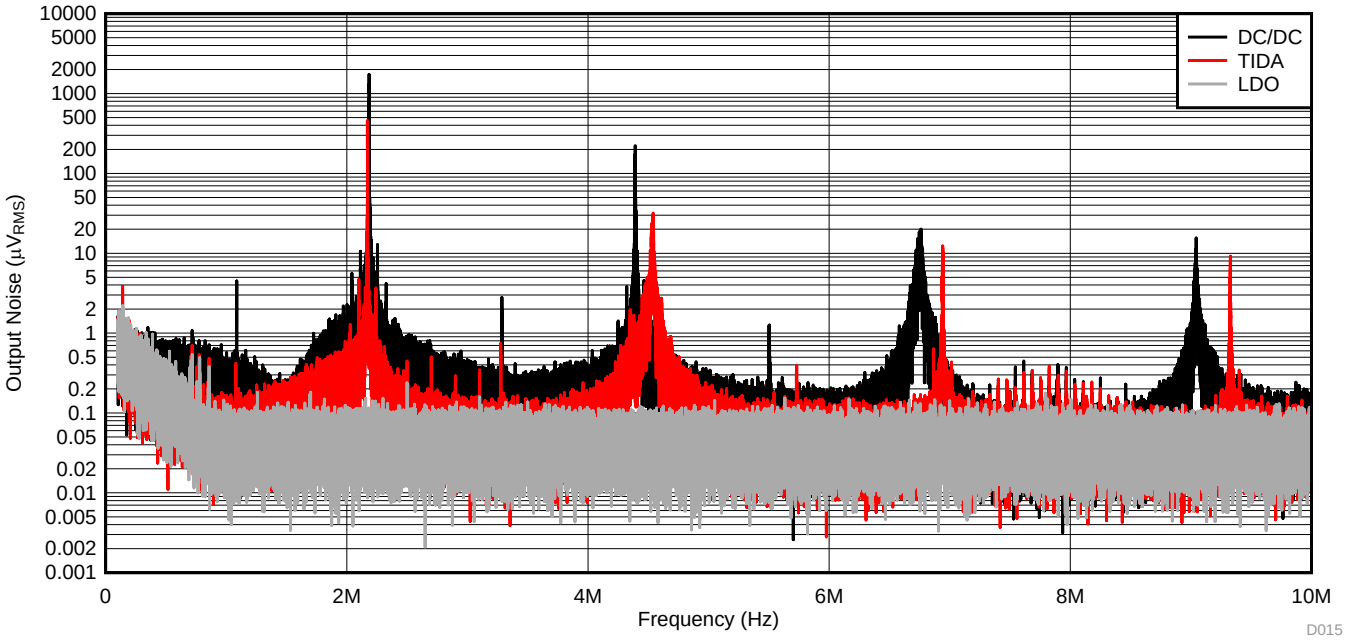


図 42. Spurious Noise Comparison (V_{in} = 3 V, Load = 100 mA)

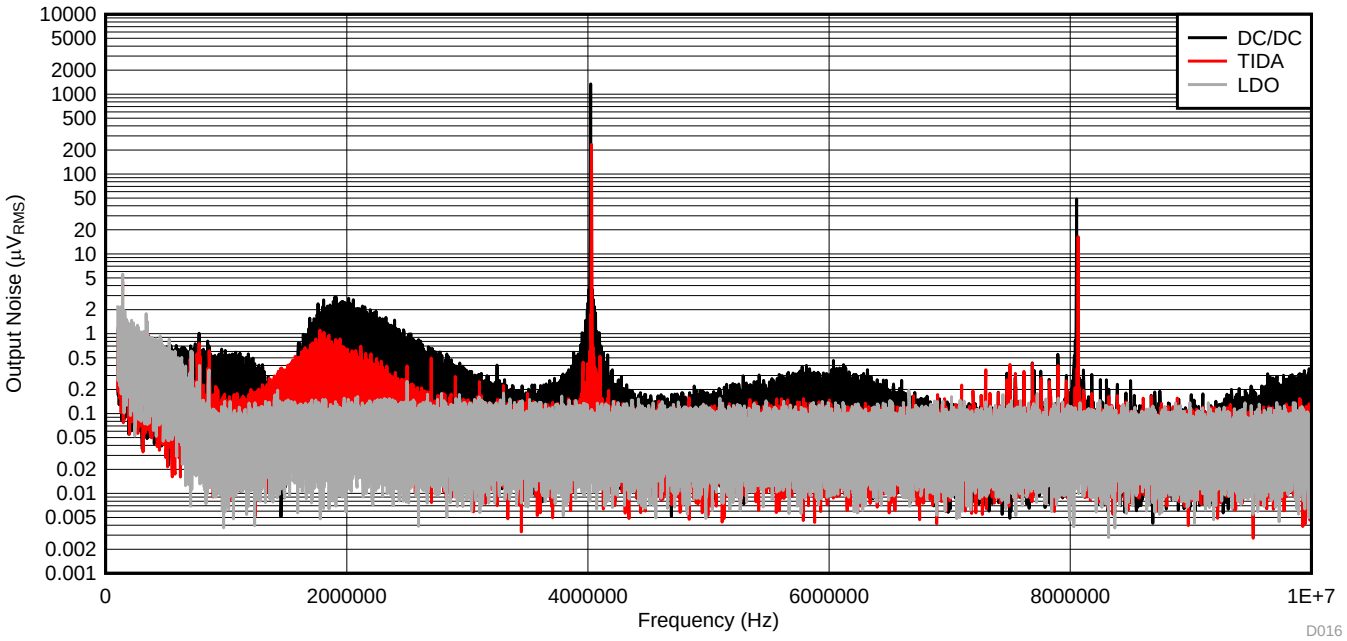


図 43. Spurious Noise Comparison (V_{in} = 3 V, Load = 300 mA)

3.2.2.4.8 Transient Response

表 3 compares the transient response of the TIDA-01566 to the TPS62801 DC/DC converter and the TPS7A10 LDO, with a 3-V input voltage and 1-µsec rise and fall times. Transient response does not change significantly with changes in input voltage.

表 3. Transient response Comparison

	Transient Response: 10-µA to 50-mA Step		Transient Response: 1-mA to 200-mA Step	
	Rising Load	Falling Load	Rising Load	Falling Load
TIDA-01566	81 mV	31 mV	91 mV	61 mV
TPS62801	76 mV	23 mV	65 mV	21 mV
TPS7A10	84 mV	28 mV	94 mV	52 mV

3.2.2.4.9 Thermal Performance

表 4 compares the thermal performance of the TIDA-01566 to the TPS62801 DC/DC converter and the TPS7A10 LDO. Each design is run with a 3-V input and 300-mA load current for 20 minutes.

表 4. Thermal Performance Comparison

	Temperature (°C)
TIDA-01566	33.8
TPS62801	30.5
TPS7A10	66.6

3.2.2.4.10 Solution Size

The solution sizes for the TIDA-01566, TPS62801 DC/DC converter, and the TPS7A10 LDO are shown in the list below. These solution sizes include the passive components required for each circuit. The TPS7A10 shares two capacitors that are included in the TPS62801's solution size and not included in the TPS7A10's solution size. These two capacitors are shaded by both red and blue in 図 44. The resistor used to set the TPS62801's output voltage is shaded in a hatched red color, because it is not required for certain TPS6280x device versions which support the desired output voltage without this resistor at the VSEL/MODE pin. 図 44 shows a picture of the physical circuit with measurements.

- TIDA-01566: 8.5 mm²
- TPS62801: 5.5 mm²
- TPS7A10: 3 mm²

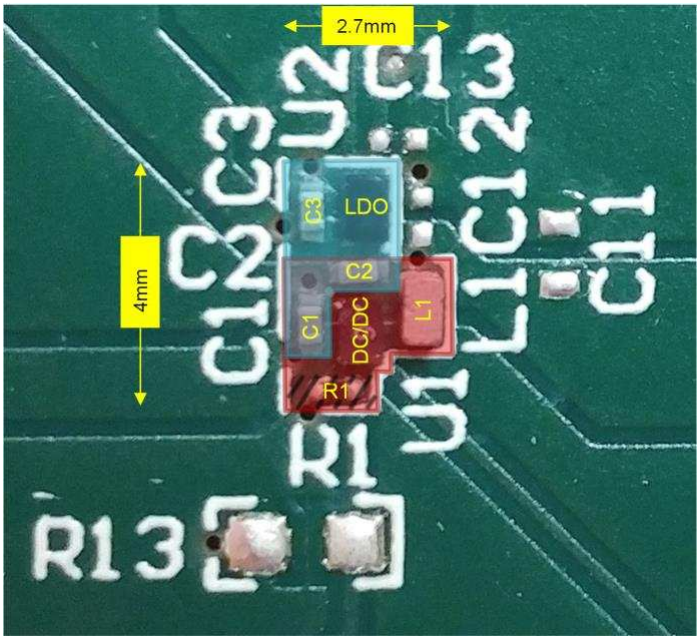


図 44. TIDA-01566 Solution Size

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01566.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01566.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01566.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01566.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01566.

5 Related Documentation

1. Texas Instruments, *TPS6280x 1.8-V to 5.5-V, 1-A, 2.3-μA I_Q Step Down Converter in a 6-Pin, 0.35-mm Pitch WCSP Package Data Sheet*
2. Texas Instruments, *TPS7A10 300-mA, Low-VIN, Low-VOUT, Ultra-Low-Dropout Regulator Data Sheet*
3. Texas Instruments, *TPS7A05 1-μA I_Q, 200-mA, Ultralow I_Q LDO in a 1-mm × 1-mm Package Data Sheet*
4. Texas Instruments, *Accurately measuring efficiency of ultralow-I_Q devices Technical Brief*
5. Texas Instruments, *Performing Accurate PFM Mode Efficiency Measurements Application Report*

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