参考資料

TI Designs: TIDA-060014
PLC用の96チャネル、双方向デジタル入力モジュールのリファレンス・デザイン

概要

このリファレンス・デザインは、絶縁デジタル入力レシーバのISO1212デバイスを使用して、96の絶縁デジタル入力チャネルをコンパクトに実装します。このデザインはISO1212デバイスの電流制限機能を示すもので、このデバイスは従来のオプトカプラ・ソリューションよりも熱特性が優れています。このデザインでは、より小型で、基板の発熱が低い(50℃未満)、複数のチャネルを持つデジタル入力ボードを作成できます。MUXおよびデコーダとISO1212デバイスにより、マイクロコントローラのピン数を96から8に減らしています。このデザインは、チャネルごとに100kHzの入力信号(200kbit)でテスト済みです。このデザインの入力電力は7.3W未満で、熱放散が抑えられます。すべての信号はIEC61000-4に従い、ESD、EFT、およびサージ・イベントに耐えられるよう設計されています。

リソース

TIDA-060014	デザイン・フォルダ
ISO1212	プロダクト・フォルダ
CD74HC4067	プロダクト・フォルダ
CD74HC238	プロダクト・フォルダ

TI E2E™ Community

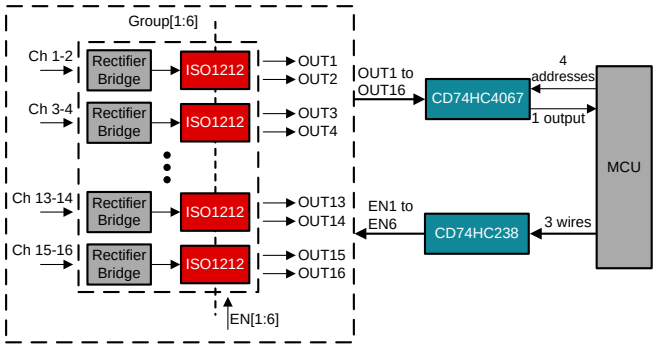
E2E™エキスパートに質問

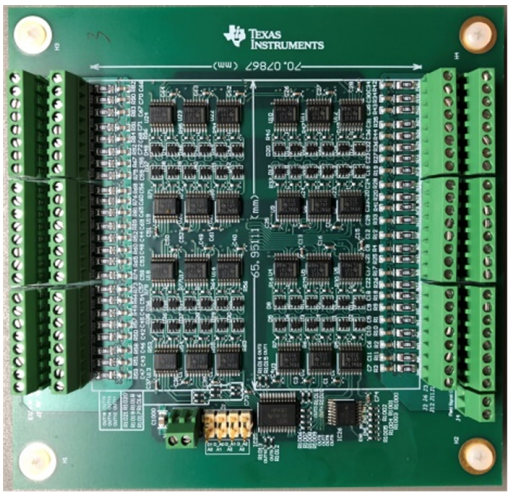
特長

- 96チャネルの双方向デジタル入力モジュール
- 電圧入力: 24VDC範囲、チャネルごとに3.1mAに制限
- 小型で温度上昇の低い設計(96チャネルすべてがオンの状態で、1時間後に50℃未満)
- 小さな基板サイズ、中核基板サイズは65×70mm^2
- シリアル出力オプション
- 0.5kVサージ(IEC61000-4-5、42Ω)でテスト済み、拡張により1kVにスケーリング可能
- LaunchPad™開発キット用のヘッダーにより迅速かつ簡単に評価可能

アプリケーション

- プログラム可能なロジック・コントローラおよびデジタル入力モジュール
- 分散制御システム
- コンピュータ数値制御
- 鉄道信号データ・ロガー





1 System Description

This reference design is a compact implementation of 96 isolated bidirectional digital input channels using TI's ISO1212 device. The ISO1212 device is a dual-channel isolated 24-V digital-input receiver for a digital input (DI) module with programmable logic controller (PLC) . The ISO1212 device has an accurate current limit to enable a more compact and high-density DI board design.

The 96 channels are divided into 6 groups of 16 channels. Each channel has 8 dual-channel ISO1212 devices. A MUX and decoder are used to read the output states of the 96 channels. The MUX and decoder with the output-enable function of the ISO1212 device decrease the number of pins of the microcontroller 96 to 8. The serials outputs of the MUX can be read out using any I/O pin on the microcontroller. A TI LaunchPad™ development kit detects the state of each channel and supplies power to the system.

The design was tested by using 100-kHz input signals (200-kbit) per channel. However, the ISO121x devices support data rates of up to 4 Mbps and can be used in a faster signal system. The design uses less than 7.3 W of input power which results in less heat dissipation. Each channel was designed to withstand surge (IEC 61000-4-5), ESD (IEC 61000-4-2) and EFT (IEC 61000-4-4) test. An RC low-pass filter was used for the surge test.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Number of channels	96 in groups of 16	—
High level threshold voltage (V_{IH})	15.34 V	2.3.1
Low level threshold voltage (V_{IL})	14.39 V	2.3.1
$I_{(IN+SENSEx)}$, typical sum of current drawn from the IN and SENSE pins	3.1 mA/per channel	2.3.1
Power consumption	7.3 W for 96 channels, 24-V V_{IN}	3.2.2.2
Thermal dissipation	40°C maximum after 1 hour of continuous operation, 24-V V_{IN}, 25°C ambient temperature	3.2.2.2
Total time to read output states	125.2 µs, reading 96 channels one time	3.2.2.4

2 System Overview

2.1 Block Diagram

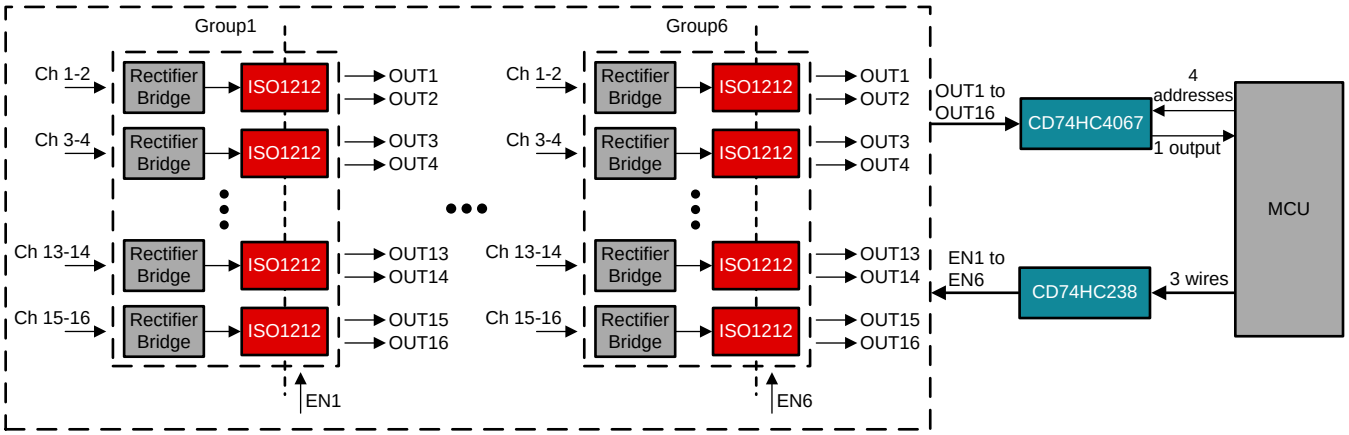


図 1. TIDA-060014 Block Diagram

2.2 Highlighted Products

2.2.1 ISO1212

The ISO1211 and ISO1212 devices are isolated 24-V to 60-V digital input receivers, compliant to IEC61131-2 Type 1, 2, and 3 characteristics, suitable for programmable logic controllers (PLCs) and motor control digital input modules. Unlike traditional optocoupler solutions with discrete, imprecise current limiting circuitry, the ISO121x devices provide a simple, low-power solution with an accurate current limit to enable the design of compact and high density I/O modules. These devices do not require field-side power supply and are configurable as sourcing or sinking inputs. The ISO121x devices operate over the supply range of 2.25 V to 5.5 V, supporting 2.5-V, 3.3-V, and 5-V controllers. A ±60-V input tolerance with reverse polarity protection helps ensure the input pins are protected in case of faults with negligible reverse current. These devices support up to 4-Mbps data rates passing a minimum pulse width of 150 ns for high-speed operation. The ISO1211 device is ideal for designs that require channel-to-channel isolation and the ISO1212 device is ideal for multi-channel space-constrained designs. 図 2 shows the conceptual block diagram of an ISO121x device.

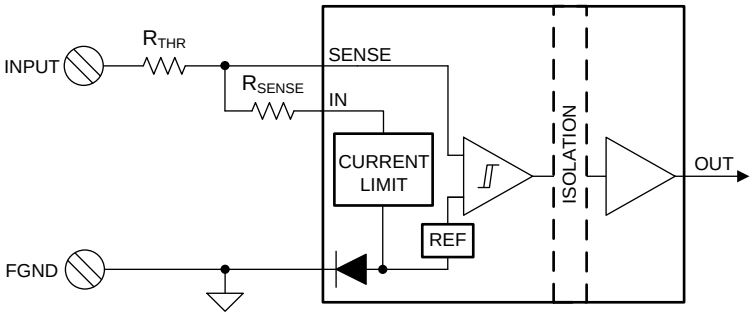


図 2. ISO1212 Functional Block Diagram

2.2.2 CD74HC238

The CD74HC238 device is a high-speed silicon-gate CMOS decoder. The device can be used in memory address decoding or data-routing applications. The device has low-power consumption that is usually associated with CMOS circuitry but has speeds comparable to low-power Schottky TTL logic. The device has three inputs for binary select (A0, A1, and A2). If the device is enabled, these inputs set the outputs to high that are usually low. 図 3 shows the functional block diagram of the CD74HC238 device.

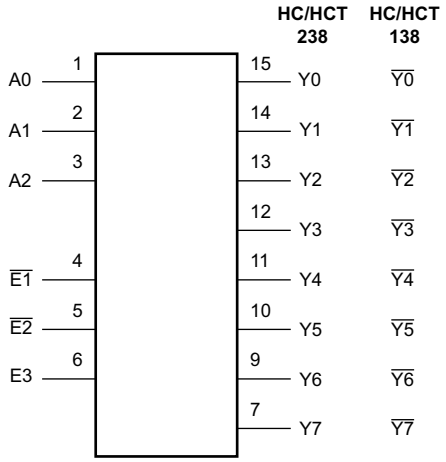


図 3. CD74HC238 Functional Block Diagram

2.2.3 CD74HC4067

The CD74HC4067 device is digitally controlled analog switches that utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits. They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low on resistance and low off leakages. In addition, these devices have an enable control which when high will disable all switches to their off state. 図 4 shows the conceptual block diagram of CD74HC4067 device.

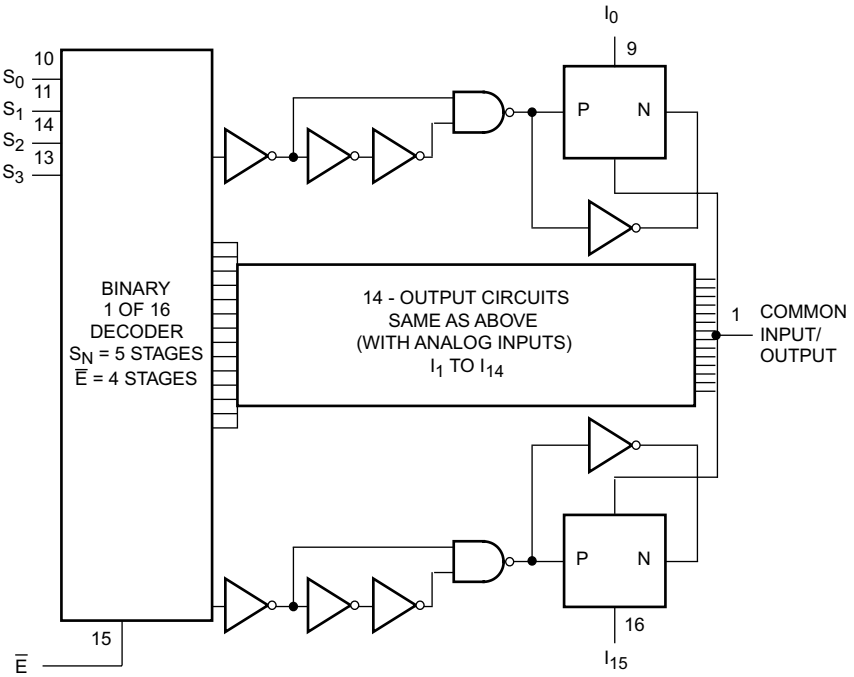


図 4. CD74HC4067 Functional Block Diagram

2.3 System Design Theory

2.3.1 Digital Input Stage

The 96 bidirectional inputs go into 48 ISO1212 devices. 図 5 shows the input stages of one ISO1212 device with two input signals.

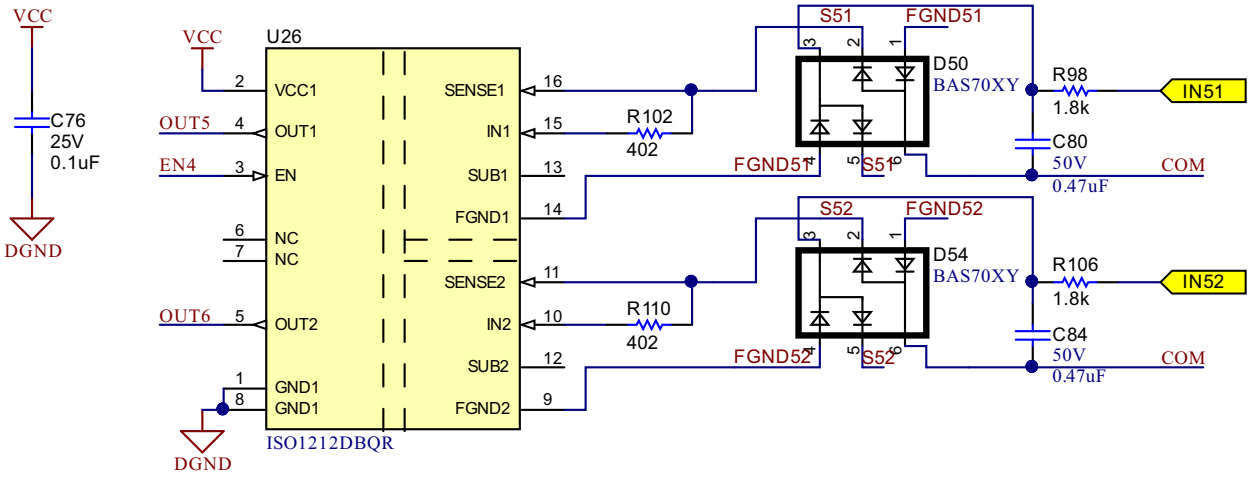


図 5. ISO1212 Input Stage Schematic

The input stage uses the rectifier and then the ISO1212 device. Each device can detect two bidirectional signals. The diodes of the rectifier must meet these specifications to rectify the bidirectional signal:

- $V_R > V_{LINE(max)}$

  where:

  - V_R is the reverse voltage.
  - $V_{LINE(max)}$ is the line voltage.
- $I_F > I_{(IN+SENSE)}$

  where:
  - I_F is the forward current.
  - $I_{(IN+SENSE)}$ is the typical sum of current drwan from the IN and SENSE pins.

This design is for the PLC DI board, BAS70XY with an I_F current of 200 mA and V_R voltage of 70 V. The BAS70XY board was selected because of the maximum line voltage and current limit. The COM pin in 図 5 is the common field ground for all digital inputs.

The ISO1212 device is a fully-integrated, isolated digital-input receiver with IEC 61131-2 Type 1, Type 2, and Type 3 characteristics. The R_{SENSE} resistor on the input signal path precisely sets the limit for the current drawn from the field input to be set for Type 1, Type 2, or Type 3 operation. The R_{THR} resistor sets the voltage thresholds and limits limit the surge current. An input capacitor, C_{IN}, is connected between the R_{THR} resistor and COM pin. The RTHR resistor to COM pin creates an RC filter for additional protection from ESD, EFT, and surge events. 表 2 shows the configurations for Type 1 and Type 3 digital inputs. 表 2 also shows the voltage rating results for the specific values of R_{THR}, R_{SENSE}, and C_{IN} according to IEC 61002-4-2, IEC 61002-4-4, and IEC 61002-4-5, respectively.

表 2. Surge, ESD, and EFT

IEC 61131-2 TYPE	R_{SENSE}	R_{THR}	C_{IN}	SURGE			ESD	IEC EFT
				LINE-TO-PE	LINE-TO-LINE	LINE-TO-FGND		
Type 1	562 Ω	3 kΩ	10 nF	±1 kV	±1 kV	±1 kV	±6 kV	±4 kV
Type 3	562 Ω	1 kΩ	10 nF	±1 kV	±1 kV	±500 V	±6 kV	±4 kV
			330 nF	±1 kV	±1 kV	±1 kV	±6 kV	±4 kV

All channels in this design are configured for Type 1 inputs. The R_{SENSE} resistor has a value of 280 Ω. The R_{THR} resistor has a value of 1.8 kΩ. The C_{IN} capacitor has a value of 470 pF to filter the input surge pulse further. Use Equation 1 to calculate the typical current limit (I_L). Use Equation 2 to calculate the typical high-level threshold ($V_{IH(typ)}$), Use Equation 2 to calculate the minimum low-level threshold ($V_{IL(typ)}$). Equation 1, Equation 2, and Equation 2 calculate the values at the ISO1212 input (including R_{THR}) for the high-level output high and low-level output.

$$I_L = (2.25\ mA \times 562\ \Omega) / R_{SENSE} = 3.1\ mA \quad (1)$$

$$V_{IH(typ)} = 8.25\ V + R_{THR} \times (2.25\ mA \times 562\ \Omega) / R_{SENSE} + 2 \times V_D = 15.34\ V \quad (2)$$

$$V_{IL(typ)} = 7.1\ V + R_{THR} \times (2.25\ mA \times 562\ \Omega) / R_{SENSE} + 2 \times V_D = 14.19\ V \quad (3)$$

2.3.2 Readout of Digital Outputs

表 3 shows the correspondence between the input signal and output signal for a specific group.

表 3. Correspondence Table Between Input and Output

Input Signal	Output Signal	Input Signal	Output Signal	Input Signal	Output Signal
Group 1 (EN1)		**Group 2 (EN2)**		**Group 3 (EN3)**	
IN1	OUT7	IN17	OUT9	IN33	OUT9
IN2	OUT8	IN18	OUT10	IN34	OUT10
IN3	OUT5	IN19	OUT4	IN35	OUT2
IN4	OUT6	IN20	OUT3	IN36	OUT1
IN5	OUT3	IN21	OUT6	IN37	OUT16
IN6	OUT4	IN22	OUT5	IN38	OUT15
IN7	OUT15	IN23	OUT8	IN39	OUT14
IN8	OUT16	IN24	OUT7	IN40	OUT13
IN9	OUT13	IN25	OUT16	IN41	OUT12
IN10	OUT14	IN26	OUT15	IN42	OUT11
IN11	OUT11	IN27	OUT14	IN43	OUT3
IN12	OUT12	IN28	OUT13	IN44	OUT4
IN13	OUT10	IN29	OUT12	IN45	OUT5
IN14	OUT9	IN30	OUT11	IN46	OUT6
IN15	OUT1	IN31	OUT1	IN47	OUT7
IN16	OUT2	IN32	OUT2	IN48	OUT8
Group 4 (EN4)		**Group 5 (EN5)**		**Group 6 (EN6)**	
IN49	OUT3	IN65	OUT10	IN81	OUT10
IN50	OUT4	IN66	OUT9	IN82	OUT9
IN51	OUT5	IN67	OUT8	IN83	OUT1
IN52	OUT6	IN68	OUT7	IN84	OUT2
IN53	OUT7	IN69	OUT6	IN85	OUT15
IN54	OUT8	IN70	OUT5	IN86	OUT16
IN55	OUT9	IN71	OUT4	IN87	OUT13
IN56	OUT10	IN72	OUT3	IN88	OUT14
IN57	OUT12	IN73	OUT15	IN89	OUT11
IN58	OUT11	IN74	OUT16	IN90	OUT12
IN59	OUT1	IN75	OUT13	IN91	OUT4
IN60	OUT2	IN76	OUT14	IN92	OUT3
IN61	OUT16	IN77	OUT11	IN93	OUT6
IN62	OUT15	IN78	OUT12	IN94	OUT5
IN63	OUT14	IN79	OUT2	IN95	OUT8
IN64	OUT13	IN80	OUT1	IN96	OUT7

表 4 shows the function table of the CD74HC238 device.

表 4. Function Table of CD74HC238

INPUT			OUTPUT							
D_A2 (C)	D_A1 (B)	D_A0 (A)	EN1 (Y0)	EN2 (Y1)	EN3 (Y2)	EN4 (Y3)	EN5 (Y4)	EN6 (Y5)	ENx (Y6)	ENx (Y7)
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

表 5 shows the function table of the CD74HC4067 device.

表 5. Function Table of CD74HC4067

A3	A2	A1	A0	SELECTED CHANNEL
0	0	0	0	I0 (OUT8)
0	0	0	1	I1 (OUT7)
0	0	1	0	I2 (OUT6)
0	0	1	1	I3 (OUT5)
0	1	0	0	I4 (OUT4)
0	1	0	1	I5 (OUT3)
0	1	1	0	I6 (OUT9)
0	1	1	1	I7 (OUT10)
1	0	0	0	I8 (OUT2)
1	0	0	1	I9 (OUT1)
1	0	1	0	I10 (OUT11)
1	0	1	1	I11 (OUT12)
1	1	0	0	I12 (OUT13)
1	1	0	1	I13 (OUT14)
1	1	1	0	I14 (OUT15)
1	1	1	1	I15 (OUT16)

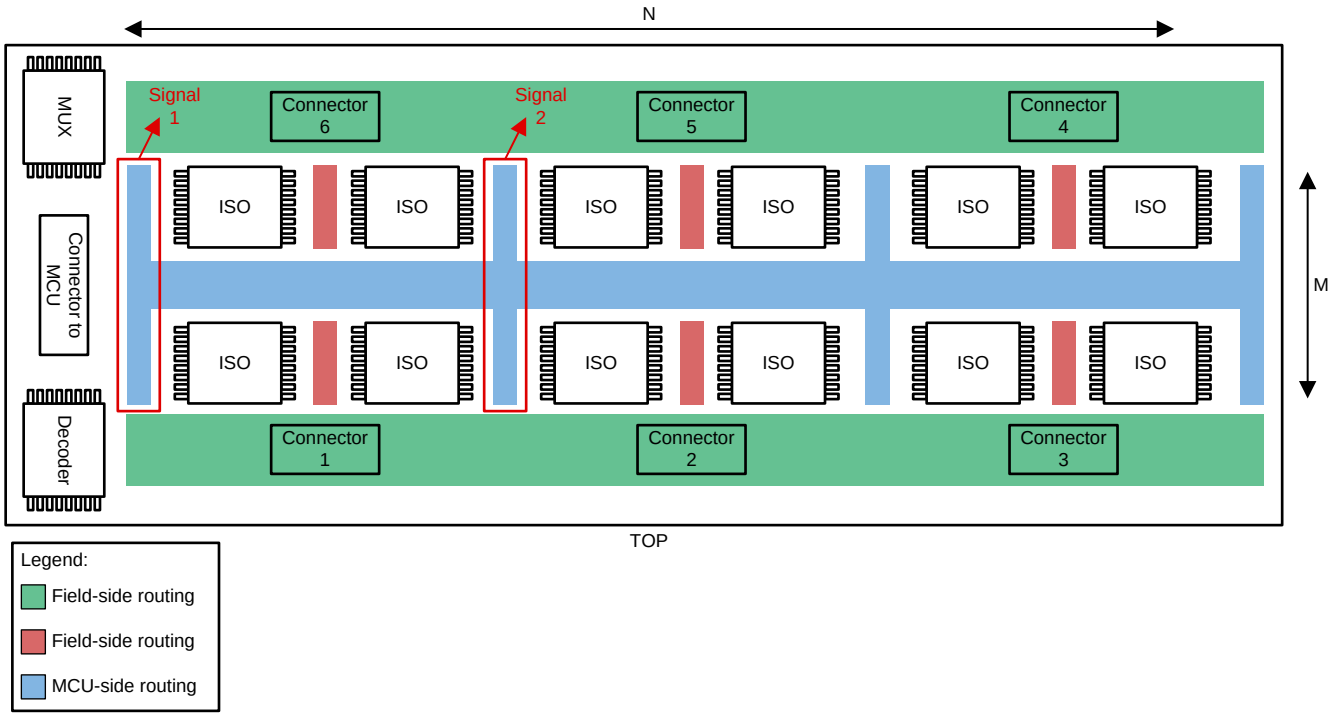
The ISO1212 device has an output-enable pin (EN) on the controller side. If the EN pin is set to 0, the output buffer is in the high-impedance state. This feature can multiplex the ISO1212 device on the controller side with an external multiplexer and decoder. The 96 digital input channels are divided into 6 groups in this design. Each group of channels has the same outputs from OUT1 to OUT16. A logical control signal must be applied to multiplexer and decoder to readout the 96 digital output signals. Readout of the data follows these steps:

Step 1. Select the group(x) from 表 4.
Step 2. Read the states of OUT1 to OUT16 from 表 5.
Step 3. Find the corresponding input channel in 表 3.
Step 4. Repeat Step 1, Step 2, and Step 3.

Only 6 outputs of the CD74HC238 device are used to control the 48 ISO1212 devices in this design. This design can be extended to detect 128 bidirectional digital signals. The other two CD74HC238 outputs can also control the additional 16 ISO1212 devices.

2.3.3 Floor Plan Diagram

Put the ISO1212 device on the bottom and top layer for a more compact design. Measure external spacing in clearance to pass safety standards. The shortest terminal-to-terminal distance through air of the ISO1212 device is 3.7 mm. 図 6 shows the design solution.



(1) M = 4 units, N = 6 units

図 6. Floor Plan Design of Multichannel DI Board

The design has a symmetrical layout and the shape of this design more square than is shown. The layout of the design has two basic advantages. The first advantage is that this design is more common in most applications. The second advantage is that this design decreases the clearance between the field side signal and MCU side signal. Signal 1 in 図 6 must be the MCU side signal to decrease the clearance. Use these methods to make this board more compact:

- Decrease the decoupling capacitance on the V_{CC1} side (signal 2 in 図 6). Only 4 decoupling capacitors are needed for the 8 ISO1212 device in this zone.
- Use more internal layers when routing the signal.
- Use symmetrical layout when routing the signal. If the output signals are multiplexed, give the outputs of the ISO1212 device on the bottom and top layers the same nets. Use vias to connect these nets to decrease the board size more.

3 Hardware, Software, Testing Requirements and Test Results

3.1 Required Hardware and Software

The J5 and J1 connectors power the board and let the user interface with the board. All field-side signals connect to the board through the J2 to J15 connectors. Use a LaunchPad development kit such as MSP-EXP430F5529LP to power and control the decoder and multiplexer to read the states of the input signals. Use the steps in 2.3.2 to read the signals.

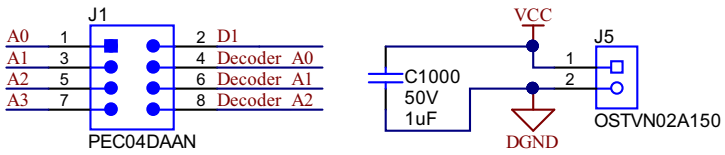


図 7. Interface of the Micro-controller

3.1.1 Hardware

The design must have this hardware:

- Laptop
- MSP430F5529 USB LaunchPad development kit: MSP-EXP430F5529LP
- Signal generator and scope: HEWLETT PACKARD 8114A
- System DC power supply: Agilent 6614C

3.1.2 Software

This design needs a microcontroller to serial readout the states of the 96 channels. Follow the steps in 2.3.2 to write the program code.

3.2 Testing and Results

3.2.1 Test Setup

The state of the 96 input signals can be read by any type of MCU. The MSP430F5529 LaunchPad development kit is used in this design to control the multiplexer and decoder and to read the states of each channel. The LaunchPad development kit connects through a USB to a laptop. The Agilent 6614C generates the digital input signal and gets the voltage thresholds. A current meter measures the total current consumption of the design. 図 8 shows the connection of the test setup.

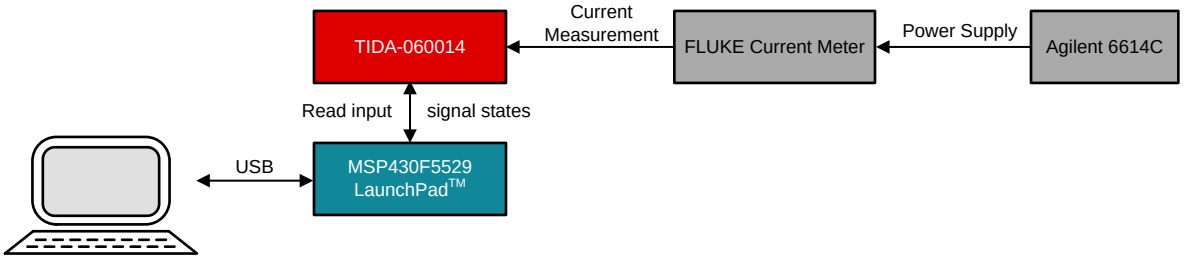


図 8. Test Setup of TIDA-060014

Follow these steps to do a functional test:

Step 1. Connect the field-side ground to J4 COM.

Step 2. Connect all field signals to J2, J3, J6, J7, J8, J9, J10, J11, J12, J13, J14, and J15.
Step 3. Connect a 5-V or 3.3-V supply from the MSP430F5529 LaunchPad development kit to J5.
Step 4. Apply voltage to each digital input field with the external power supply.
Step 5. Adjust the DC level to find the V_{IL} and V_{IH} hysteresis of the field inputs.
Step 6. Program the MSP430F5529 LaunchPad development kit.
Step 7. Apply the control signal to J1.
Step 8. Apply the group control signal to DecoderA0 through DecoderA3 to select the group number.
Step 9. Apply the control signal to the channels to select the channel number and store the value according to 表 3 to 表 5.

3.2.2 Test Results

3.2.2.1 Functional Test

The test results show that the performance of the digital input module is as expected. This section gives the test results to reference for this design.

3.2.2.1.1 Voltage Thresholds

The $V_{IH(typ)}$ voltage is 15.34 V and the $V_{IL(typ)}$ voltage is 14.19 V as calculated in 2.3.1. 図 9 shows the high-level threshold voltage of the TIDA-060014 design which is 15.47 V. 図 10 shows the low-level threshold voltage of the TIDA-060014 design which is 14.17 V. The voltage threshold results are in the normal range for a typical value.

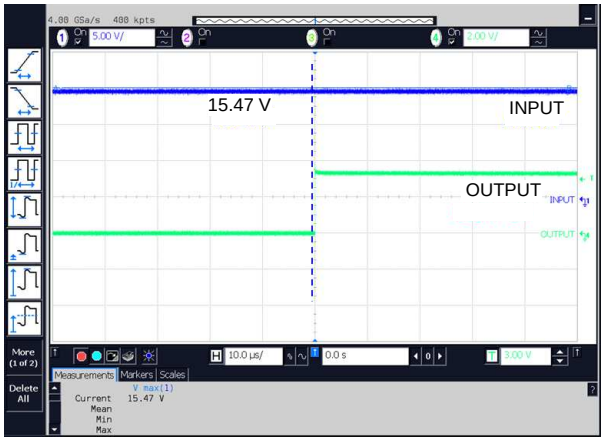


図 9. High-Level Threshold Voltage of TIDA-060014

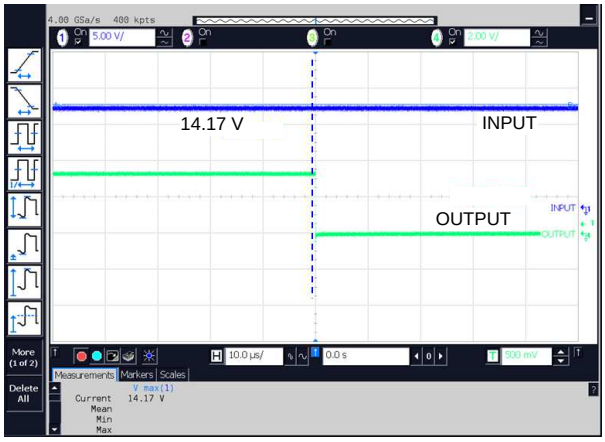


図 10. Low-Level Threshold Voltage of TIDA-060014

3.2.2.1.2 Propagation Delay Time

Only one channel can be selected to measure the propagation delay of ISO1212 device. A 24-V square waveform with a frequency of 500 kHz (data rate of 1 Mbps) was applied to the field signal connector. 図 11 shows the propagation delay time as approximately 230 ns. This propagation delay time is a little greater than the value specified in the ISO1212 data sheet.

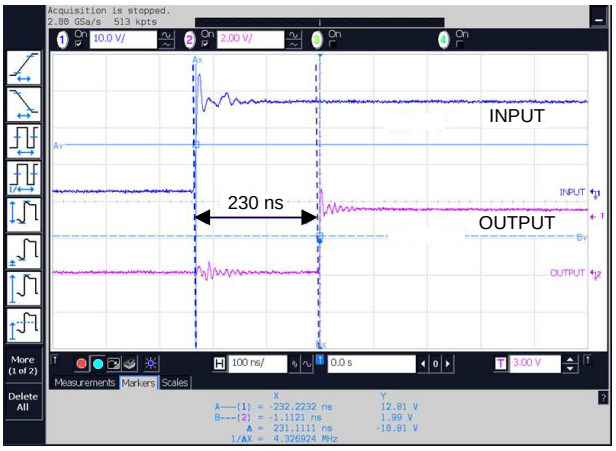


図 11. Propagation Delay Time of TIDA-060014

3.2.2.2 Power Dissipation and Temperature Rise

All inputs are connected together and 24 V of power is connected from the power supply to test the power dissipation of the 96 channels. The current value is measured by the current meter. If the current value shown on the power supply interface is used, it cannot express the accurate total current value. The setup was operated for 1 hour. The total current was measured and a thermal image was taken after 1 hour.

All 96 channels draw a current of approximately 301 mA. The power consumption of all 96 channels together is 7224 mW as shown in Equation 4.

$$24\ V \times 301\ mA = 7224\ mW \quad (4)$$

If the total power consumption is 7224 mW, each channel draws an average of 3.14 mA which is approximately the same value specified in 2.3.1.

The thermal images show that the temperature of this board quickly increases to a maximum of 59.7℃ when all inputs are connected to 24 V. The ambient temperature is approximately 23℃ which is a difference of 36.3℃. The temperature of the board increases to a maximum of 73.5℃ after power is supplied for 1 hour. The board stays stable in this temperature. The difference in temperature shows that the devices dissipate the primary quantity of energy. The total power consumption can bespreadout and this board can be used in applications with high ambient temperature.

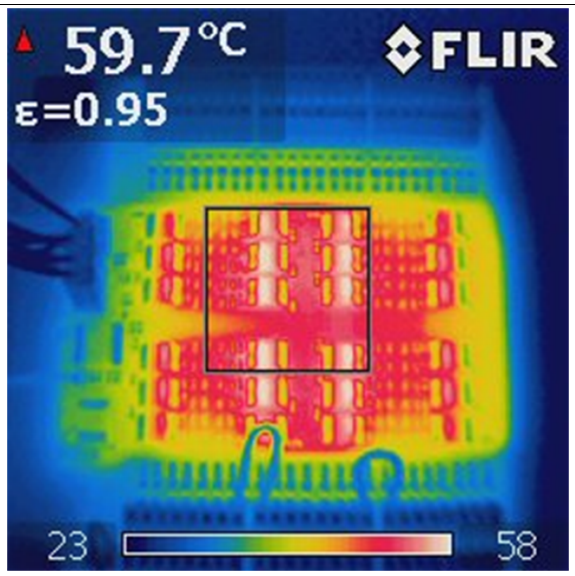


図 12. Thermal Image of TIDA-060014 With 24-V Input Connected to Each Channel

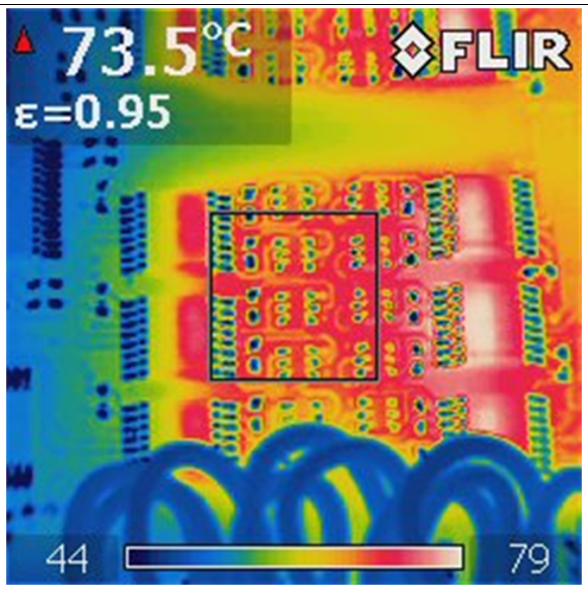


図 13. Thermal Image of TIDA-060014 After 1 Hour With 24-V Input Connected to Each Channel

3.2.2.3 R_{IO} Test

A high resistance meter, 6517A, is used to measure the insulation resistance of TIDA-060014. A 500-V DC voltage was applied to field-side ground and microcontroller-side ground with a resistance greater than 6.48 TΩ. The measured insulation resistance (R_{IO}) is within the range specified in the ISO1212 data sheet. This result shows that the TIDA-060014 design has good insulation between side 1 and side 2 and that it can withstand high isolation voltages similarly to the ISO1212 device.

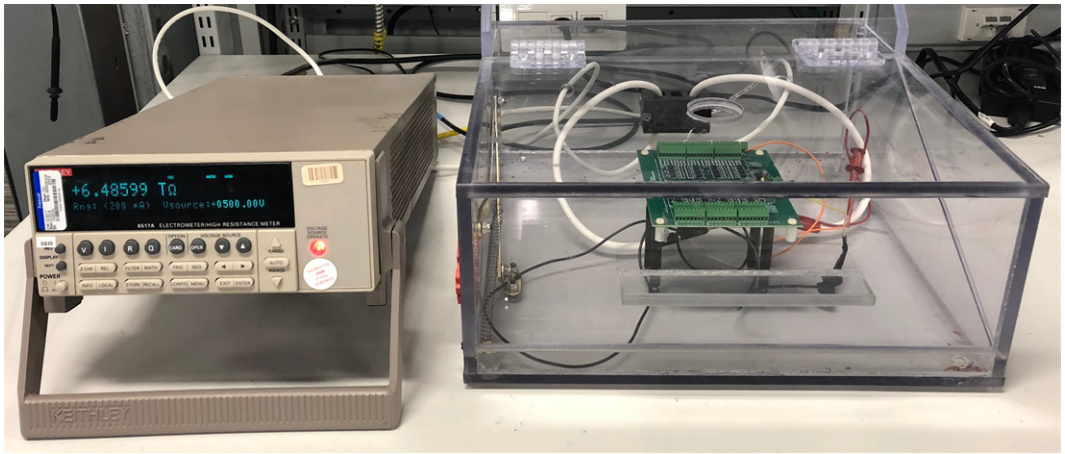


図 14. R_{IO} Test Platform of TIDA-060014

3.2.2.4 MCU Total Time to Read the 96 Channels State

Some applications need a fast response to external variation. The time to read the IO states is a key specification to give quick feedback. The system clock frequency of the microcontroller, connection type (parallel or serial), and program efficiency select the total time to read the states of the signals of the 96 channels. If more pins are used to read the states of each channel, the time to read all channels is shorter but less pins can be used to measure other signals. A lesser quantity of pins to measure other signals gives designers the option to select a lower cost MCU and decrease total system cost. Designers must select the total time to read all channels and pin count before an appropriate MCU is selected because of the tradeoff between pin count and time.

3.2.2.4.1 Use MSP430F5529 LaunchPad™ Development Kit to Read States of 96 Channels

This design uses the multiplexer and decoder to decease the total number of pins connected to the microcontroller. The MSP430F5529 LaunchPad development kit powers the TIDA-060014 and reads the states of the input signals of the 96 channels. 表 6 shows the pin configuration and primary code to read the state of each channel signal.

表 6. Pin Configuration of MSP430F5529

Board Label Signal	MSP430F5529 Pin	Function
D1	P2.0	Read state
D_A0	P3.0	Group number selection
D_A1	P3.1	
D_A2	P3.2	
A0	P6.0	Channel number selection
A1	P6.1	
A2	P6.2	
A3	P6.3	

```
*******************************************************************************
for(i=0;i<6;i++)
{
 P3OUT=i;
 for(j=0;j<16;j++)
 {
  P6OUT=j;
  channel_state[k]=P2IN&BIT0;
  k++;
 }
 Switch_input_state();
}
*******************************************************************************
```

The term *P3* in this code is used to select the group number. The term *P6* in this code is used to select the channel number. Use the Switch_input_state() function to map the states of the read states and input signal states.

3.2.2.4.2 Use MSP430F5529 Timer A to Calculate the Total Time

This code shows how to use Timer A to calculate the total time to read the states of all channels. Timer A is used to count the total time. The method to calculate the time is to enable timer A before the code reads the IO states and to disable the timer after the readout is complete. A breakpoint can be used to read the timer count number. The total time for a 25-MHz system clock frequency of the MSP430F5529 is 125.2 µs as shown in Equation 5.

3130 / 25 µs = 125.2 µs (5)

```
*******************************************************************************
Begin counting;
 for(i=0;i<6;i++)
{
 P3OUT=i;
 for(j=0;j<16;j++)
 {
  P6OUT=j;
  channel_state[k]=P2IN&BIT0;
  k++;
 }
}
*******************************************************************************
```

Expression	Type	Value
(x)= value	unsigned int	3130

```
Name : value
    Default:3130
    Hex:0x0C3A
    Decimal:3130
    Octal:06072
    Binary:0000110000111010b
```

図 15. Count Number of TA0R

3.2.2.5 Surge Test

The digital input module must pass tests for surge (caused by lightning strikes), ESD (component contact with human operators), and EFT (cables near high-voltage and high-frequency signal). The surge waveform impulse condition for the highest energy and widest pulse width is the hardest condition to pass and is therefore most important test to pass.

3.2.2.5.1 Test Set Up

The module needs these surge level 1 tests (500 V, 42 Ω) at the I/O connectors: line-to-PE (earth), line-to-line (differential-mode), and line-to-FGND (common-mode). All input channels must be exposed to a 500-V surge and 1-kV surge out of a 42-Ω generator impedance in accordance with the IEC 61000-4-5 standard. 図 16 shows a wiring diagram example of surge test.

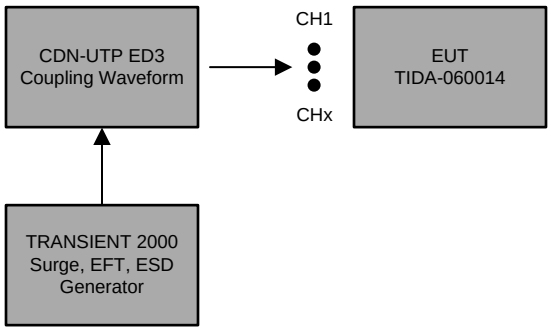


図 16. Surge Test Platform Wiring Diagram

The primary surge test steps are:

Step 1. Connect the element under test (EUT) as shown in 図 16.
Step 2. Connect the pulse output pin of UTP ED3 to TIDA-060014.
Step 3. Wait for five 25-A current peak pulses to be applied in the positive direction.
Step 4. Wait for five 25-A current peak pulses to be applied in the negative direction. The time between two pulses is 10 s. All test channels receive 0.5-kV and 1-kV DM and CM pulses in this test.
Step 5. Wait for characterization of the board after it is exposed to the surge events. This characterization focuses primarily on the current limit and functional level test.

The surge test is done with the board powered and unpowered.

3.2.2.5.2 Test Results

The surge test was done at a facility of the CSA Group. The equipment (generator, voltage levels, pulse shapes, and generator source impedances) and methods were in accordance with IEC 61131-2 and IEC 61000-4-5.

表 7 shows that the current limit is stable throughout the surge test when the board is unpowered. The current limit before and after the surge test is almost the same. This similarity shows that the filtering circuit has a good performance in this design. Use TVS diodes or varistors to meet EMC requirements for surge tests that need a higher voltage level or faster systems.

表 7. Board Unpowered Surge Test Results

Test Item	Test Level	Current Limit Before Surge Test, Each Channel	Current Limit After Surge Test, Each Channel	Test Result
Common mode (line to FGND)	0.5 kV	3.14 mA	3.14 mA	Pass
	1 kV	3.14 mA	3.14 mA	Pass
Differential mode (line to line)	0.5 kV	3.14 mA	3.14 mA	Pass
	1 kV	3.14 mA	3.14 mA	Pass

表 8 shows the voltage level of each channel to pass the surge test when the board is powered. This circuit can pass a surge voltage that is less than 800 V in the CM surge test. If the surge voltage is greater than 800 V, the current limit is greater than 3.1 mA. The circuit broke under these conditions in this test. This circuit can pass a surge voltage that is less than 900 V in the DM surge test.

表 8. Board Powered Surge Test Results (C_{IN} = 0.47 µF)

Channel Tested	±0.5 kV	±0.6 kV	±0.7 kV	±0.8 kV	±0.9 kV
IN72	Pass	Pass	Pass	Pass	Pass
IN71	—	—	—	Pass	Pass
IN66	—	—	—	Pass	Fail
IN65	—	—	—	Pass	Fail
IN61	Pass	Pass	Pass	Pass	Fail
IN54	—	—	Pass	Pass	Pass
IN70 to IN69	Pass	Pass	Pass	Pass	Pass
IN68 to IN67	—	—	Pass	Pass	Pass

表 9 shows that a greater value for C_{IN} increases the RC time constant and results in a higher voltage level of surge performance. A 1.1-µF capacitor was used in the ISO1212 input stage circuit. The LINE to FGND passes the 1.1-kV surge test. Use TVS diodes or varistors to meet EMC requirements for surge tests that need a higher voltage level or faster systems.

表 9. Board Powered Surge Test Results (C_{IN} = 1.1 µF)

Channel Tested	±0.5 kV	±0.6 kV	±0.7 kV	±0.8 kV	±0.9 kV	±1 kV	±1.1 kV
IN72 to FGND	Pass	Pass	Pass	Pass	Pass	Pass	Pass
IN71 to FGND	—	—	—	Pass	Pass	Pass	Pass
IN70 to IN69	Pass	Pass	Pass	Pass	Pass	Pass	Pass
IN68 to IN67	—	—	Pass	Pass	Pass	Pass	Pass
IN91 to PE	—	—	Pass	Pass	Pass	Pass	Pass
IN92 to PE	—	—	Pass	Pass	Pass	Pass	Pass

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060014.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060014.

4.3 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060014.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-060014.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060014.

5 Software Files

To download the software files, see the design files at TIDA-060014.

6 Related Documentation

For related documentation, see:

1. Texas Instruments, *ISO121x Isolated 24-V to 60-V Digital Input Receivers for Digital Input Modules*
2. Texas Instruments, CD74HC238*High-Speed CMOS Logic 3- to 8-Line Decoder/Demultiplexer Inverting and Noninverting*
3. Texas Instruments, CD74HC4067 *High-Speed CMOS Logic 16-Channel Analog Multiplexer/Demultiplexer*

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7 About the Author

Charles Lin is a field application engineer for the East China team at Texas Instruments. In this role, he supports industrial customers, writes application notes, and develops reference designs. Charles received his master's degree in electric engineering in 2017 at Xiamen University in China.

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