参考資料

TI Designs: TIDA-010000
380～480VACモータ・ドライブ用の50W、光レギュレーションのマルチ出力フライバック・コンバータのリファレンス・デザイン

概要

このリファレンス・デザインでは、UCC28740フライバック・コントローラを使用して、モータ・ドライブ用のDCMフライバック・トポロジによる堅牢、小型、高効率の電源を紹介します。このデザインは、290～1000VDCの広い入力電圧範囲で動作し、最大50Wの電力を連続的に供給できます。24V (1.25A)、15V (0.67A)、5V (2A)、3.3V (0.1A)の複数の出力レールを持ち、制御、ゲート・ドライブ、センサ、I/O、その他のアプリケーションに使用できます。また絶縁通信電力用に、絶縁された5V (0.1A)出力が用意されています。光レギュレーションされた帰還の使用により、全動作範囲にわたって負荷およびライン・レギュレーションは0.5%未満です。UCC28740デバイスの主要な利点として、バレー・スイッチングにより高い効率が得られること(550VDC、50Wで85%超)、内部HV FETにより外付け回路なしでセルフスタートが可能なこと、周波数ディザリングによりEMIを低減できることが挙げられます。

リソース

TIDA-010000	デザイン・フォルダ
UCC28740	プロダクト・フォルダ
TL431B	プロダクト・フォルダ
TLV1117	プロダクト・フォルダ

TI E2E™ Community

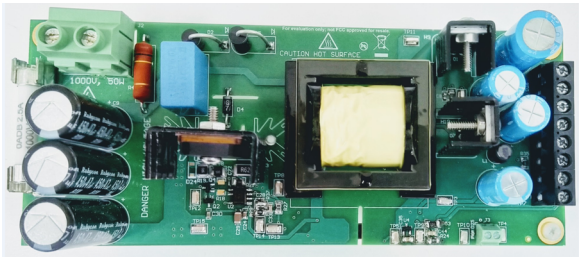
E2E™ エキスパートに質問

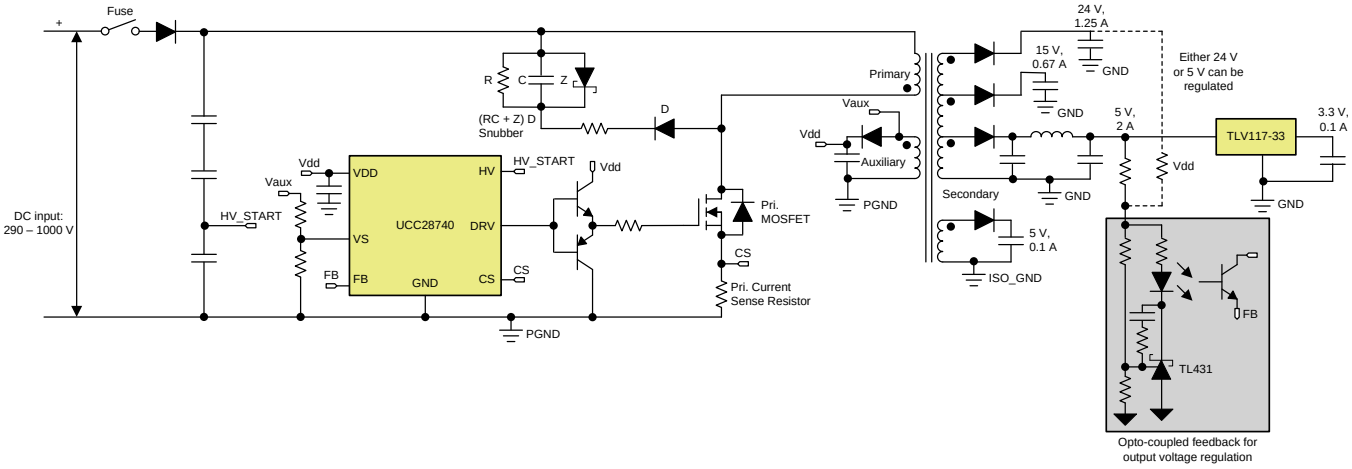
特長

- 290～1000VDCの広い入力電圧範囲
- 内蔵の700V HV FETにより、外付け回路なしでセルフスタート
- 複数の出力レール(24V (1.25A)、15V (0.67A)、5V (2A)、3.3V (0.1A))、および絶縁5V (0.1A)により、最高70℃までの周囲温度で50Wの出力電力を供給。最大85℃の周囲温度でのディレーティング動作
- 0.5%未満の負荷およびライン・レギュレーション
- 出力過電圧、入力低電圧、出力過電流からの保護
- 周波数ディザリングによりEMIを低減

アプリケーション

- ACインバータおよびVFドライブ
- サーボCNCおよびロボティクス
- 太陽光インバータ
- UPSシステム





1 System Description

図 1 shows a typical block diagram of a Variable Frequency Drive (VFD). As the block diagram shows, the input power is provided by a three phase voltage source. The three-phase AC power is rectified by a diode rectifier or an active front end rectifier to generate the DC link. The DC link is connected to the inverter stage that varies the magnitude and frequency of the motor input voltage to produce the desired torque-speed characteristics from the motor.

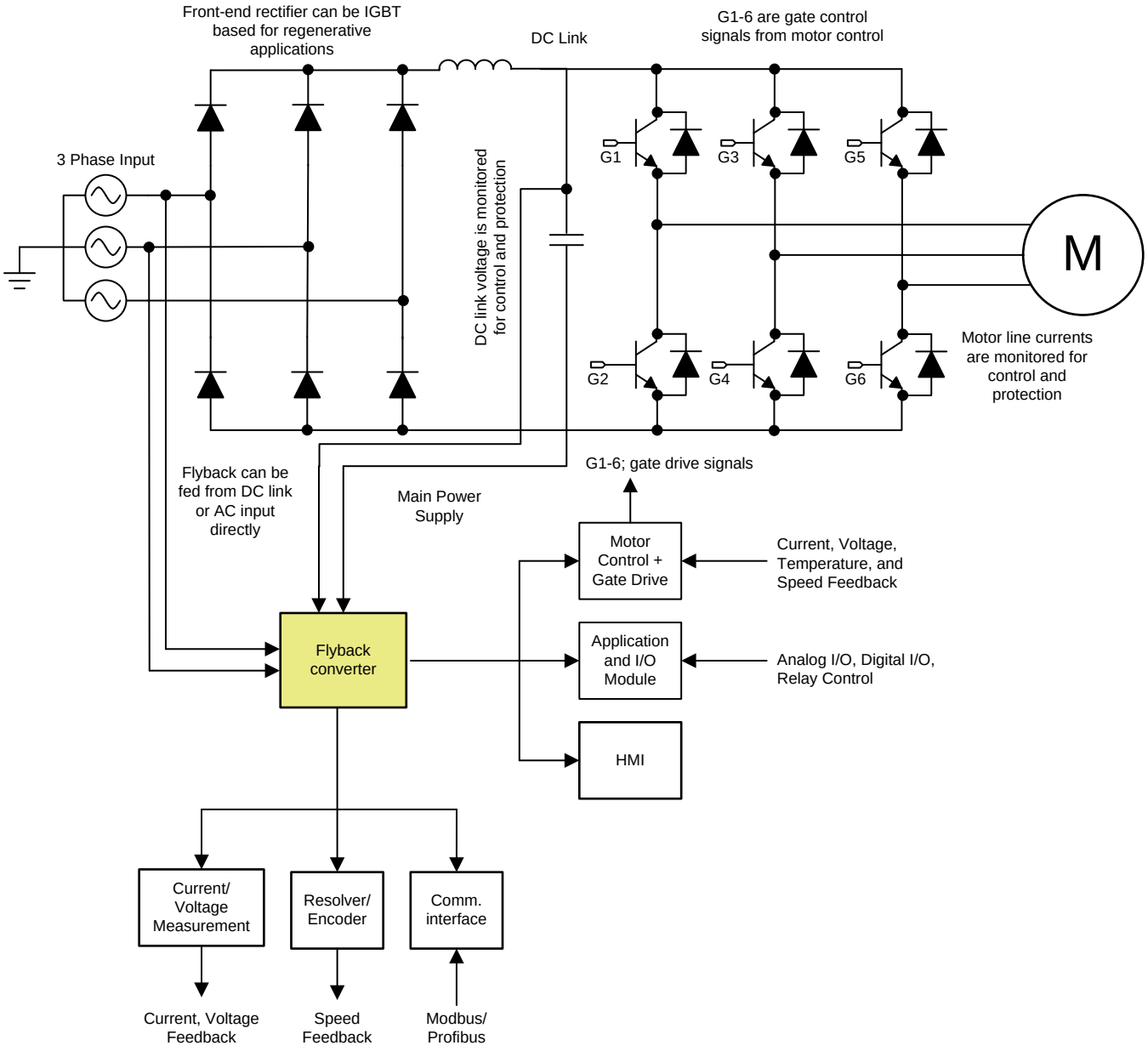


図 1. Variable Frequency Drive Block Diagram

図 1 shows that multiple low-voltage sub-systems in a VFD (like motor control, gate drive, current and voltage sensing, encoder, communication, I/O module, HMI, and so forth) require DC power at different voltage levels including 24 V, 15 V, 5 V, 3.3 V. In typical VFD applications, the only input power source to the VFD is the three-phase power and hence the low-voltage DC power needed by different sub-systems has to be derived from the DC link. For the reasons of cost, VFDs generally use one main power supply that feeds off the DC link and produces multiple output voltage rails that can be used to power the sub-systems directly or post downstream power processing. Thus, the main power supply in a VFD is a very critical sub-system and a potential single point of failure for the entire VFD unit. Hence, a robust main power supply that can operate reliably under harsh environments is imperative. Given the isolation and multiple output requirement, flyback is the topology of choice for the main power supply in VFDs.

Traditionally, main power supplies using flyback topology have been implemented using the UCx84x family of PWM controllers. These constant-frequency controllers need an external startup circuit adding to BOM cost and reducing reliability. The power dissipation in startup resistors reduces the efficiency. These controllers also face challenges in limiting short-circuit power dissipation across a wide input voltage range. Constant frequency operation creates EMI that must be suppressed with external EMI filters adding to cost and size. Fixed frequency operation can result in sub-optimal turn-off voltages leading to increased losses in the primary FET and hence, reduced lifetime.

This TI design implements a robust solution for the main power supply by using the UCC28740 flyback controller providing the following advantages over the UCx84x-based designs:

- Increased reliability
  - Elimination of external startup circuit
  - Integrated output OV and OC protection contribute to increased reliability
- Valley switching reduces losses in the primary FET thereby increasing the service life of the FET along with improving efficiency.
- Frequency dithering enables reduced EMI and hence a smaller EMI filter – therefore, a compact design.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	290–1000 VDC	
Output voltage	24 V (1.25 A), 15 V (0.67 A), 5 V (2 A), 3.3 V (0.1 A), Iso. 5 V (0.1 A)	
Output power	50 W	Inclusive of all output rails
Efficiency	> 85% at 50 W, 550 VDC	550 V is nominal DC link value for 380 VAC RMS
Regulation	Opto-regulated	Option to regulate 24 V or 5 V
Load regulation	< 1%	At regulated rail
Line regulation	< 1%	All rails at rated full-load
Output voltage ripple	< 2%	All rails
Ambient temperature	–25°C to 70°C	Derated operation up to 85°C
Clearance, creepage	As per IEC61800-5-2 for continuous operation at 1000-VDC input	
Protection	Output OV, OC limit, input UV	
PCB size, layer	156 mm × 65 mm, 2 layer, 1.6 mm, FR4	

2 System Overview

2.1 Block Diagram

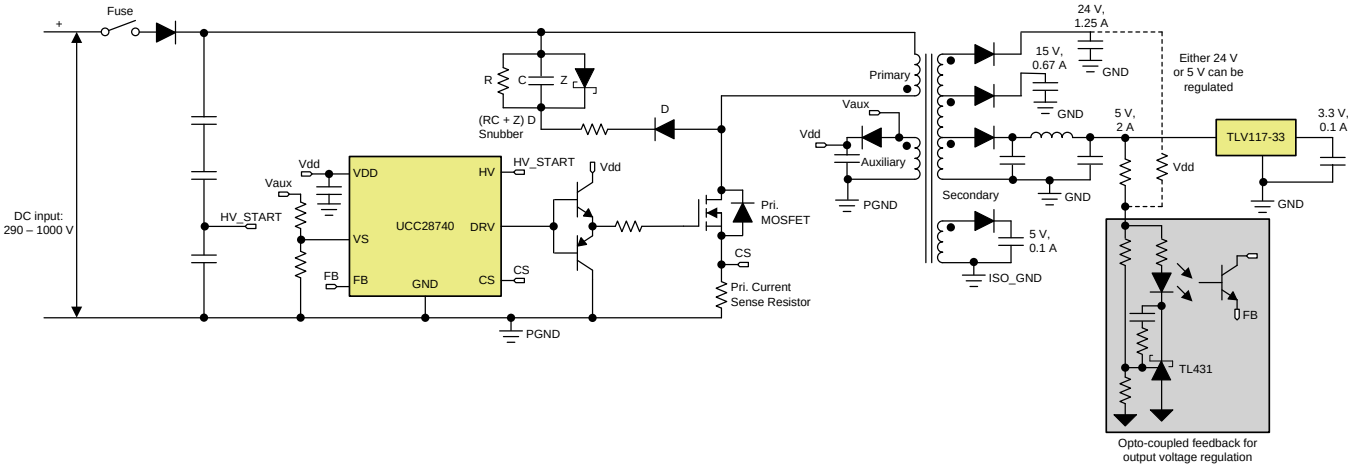


図 2. TIDA-010000 Block Diagram

This reference design is a robust, compact, wide-input flyback converter using the UCC28740 device. The UCC28740 device is a constant current, constant voltage flyback controller with opto-regulation. Therefore, the UCC28740 is an ideal fit for main power supply for VFDs. 図 2 shows that the reference design takes in an input voltage in the range of 290–1000 VDC via a fuse and diode. A fuse protects against overcurrent and a diode protects against the reversal of input voltage polarity. Three aluminum electrolytic capacitors, connected in series, are used as a bulk DC link to reduce input current ripple. The primary winding terminals of the flyback transformer are connected to the positive terminal of the DC link and the drain of the primary MOSFET, respectively. The auxiliary winding of the flyback transformer serves two key purposes – one, to provide an equivalent signal of the output voltage for output OV fault detection, valley switching, output current regulation during CC mode and two, to provide (rectified) power to the VDD pin of UCC28740. The secondary side of the flyback transformer has 2 windings (1) one winding provides 24 V (1.25 A), 15 V (0.67 A), 5 V (2 A) referenced to the same potential, and (2) the other winding provides 5 V (0.1 A) referenced to a different potential. 3.3 V is generated off the 5-V rail using an LDO TLV1117-33 device, and can provide up to 100 mA at 85°C.

The key part in the reference design is the flyback controller, the UCC28740 device. The self-start feature is implemented via the HV pin which is directly connected to one-third of the DC link voltage and enables self- start through a current source generated by the internal HV FET. The primary-side current sense resistor is connected between the source of the primary MOSFET and PGND (–ve of DC link) and feeds into the CS pin – this enables input peak current control. The primary MOSFET is driven by pulses from the DRV pin through a push-pull configuration to enable higher gate current (limited by gate resistors) operation. The output voltage is sensed via the resistor divider connected across the auxiliary winding and fed into the VS pin for output OV fault detection. Opto-regulated feedback is fed into the FB pin for accurate output voltage regulation.

The VDD voltage begins to raise when power is applied to the input DC link - the fixed current source inside the UCC28740 device via the internal HV FET starts charging the VDD rail. When VDD reaches 21 V, the DRV pulses start (and HV FET turns off until UVLO reset) and the UCC28740 device begins to regulate the output voltage and deliver the required power.

> **注:** The reference design delivers continuous output power only when the input DC voltage exceeds 200 V – below this level, the VDD will be in continuous reset mode and the converter will not deliver continuous power.

Continuous operation is possible from a minimum input voltage of 290 V only due to thermal limitations, even though the design begins to operate above 200 V. During continuous operation, the output voltage is regulated by the TL431 device and the opto-regulator based current feedback circuit – any variation in the regulated rail voltage due to load or input voltage change, results in a change in the LED current which is reflected as a change in the photo-transistor current and subsequently as a change in the FB pin current thereby enabling regulation. Also, during continuous operation, auxiliary winding provides power to the VDD rail. To protect the primary MOSFET from overvoltage spikes during turn-off, a (RC+Z)D based snubber circuit is used. This circuit ensures reliable operation of the flyback converter with minimal losses.

2.2 Highlighted Products

2.2.1 UCC28740

The UCC28740 isolated flyback power-supply controller provides Constant-Voltage (CV) using an optical coupler to improve transient response to large-load steps. Constant-Current (CC) regulation is accomplished through Primary-Side Regulation (PSR) techniques. This device processes information from opto-coupled feedback and an auxiliary flyback winding for precise high-performance control of output voltage and current.

An internal 700-V startup switch, dynamically controlled operating states, and a tailored modulation profile support ultra-low standby power without sacrificing startup time or output transient response.

Control algorithms in the UCC28740 allow operating efficiencies to meet or exceed applicable standards. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulation of switching frequency and primary current-peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

The controller has a maximum switching frequency of 100 kHz and always maintains control of the peak primary current in the transformer. Protection features keep primary and secondary component stresses in check. A minimum switching frequency of 170 Hz facilitates the achievement of less than 10-mW no-load power.

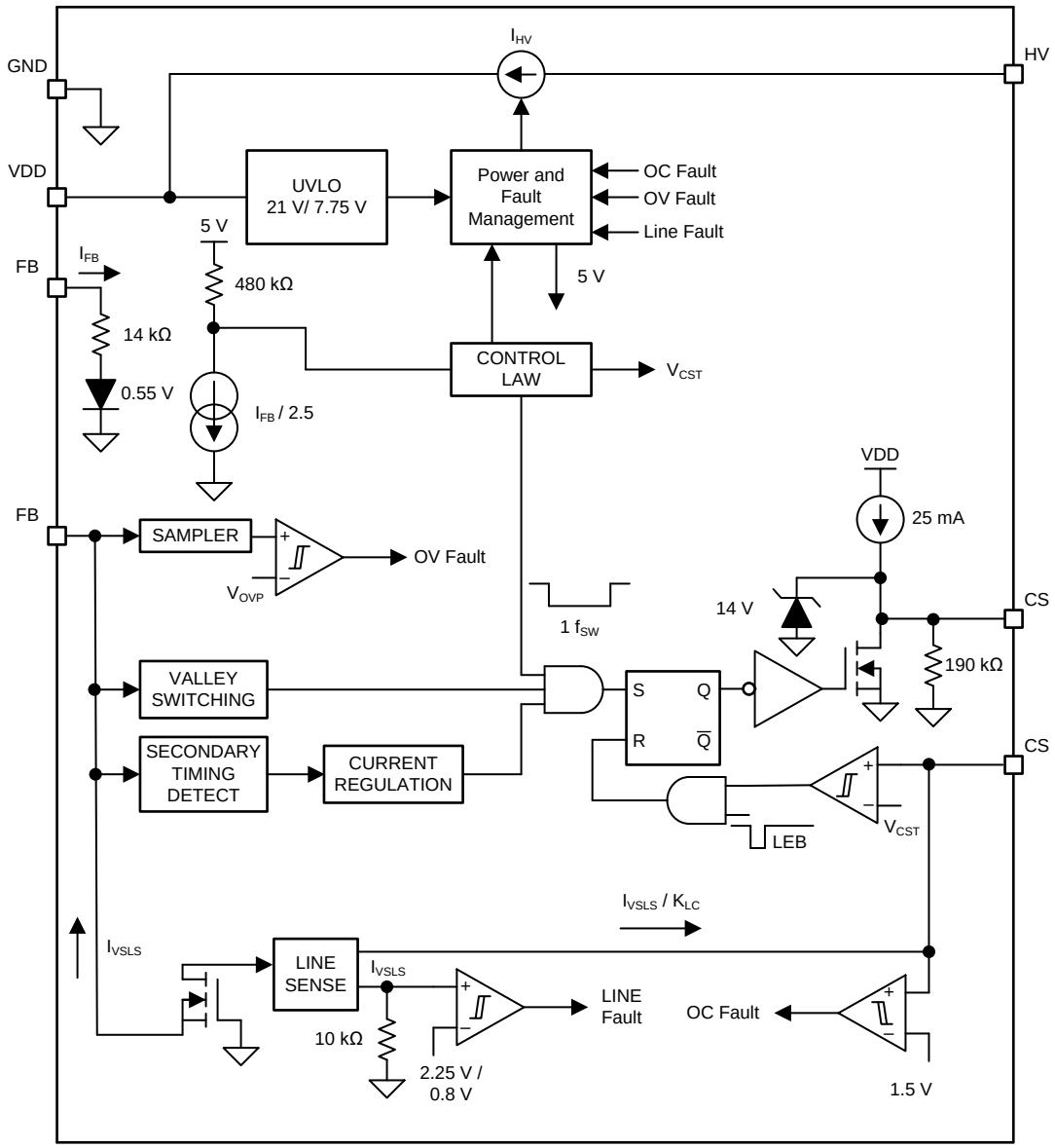


図 3. UCC28740 Functional Block Diagram

2.2.2 TL431B

The TL431B device consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin (negative input terminal of op amp in 図 4). The sink current is produced by the internal Darlington pair, shown in 図 5. A Darlington pair is used for this device to be able to sink a maximum current of 100 mA. When operated with enough voltage headroom (≥ 2.5 V), and cathode current, the TL431B device forces the reference pin to 2.5 V.

When feedback is applied from the cathode and reference pins, the TL431B device behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations for it to be in the proper linear region giving the TL431B device enough gain. Unlike many linear regulators, the TL431B device is internally compensated to be stable without an output capacitor between the cathode and anode.

When the cathode/output voltage or current of the TL431B device is being fed back to the reference or input pin in any form, this device is operating in closed loop. The majority of applications involving the TL431B device use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

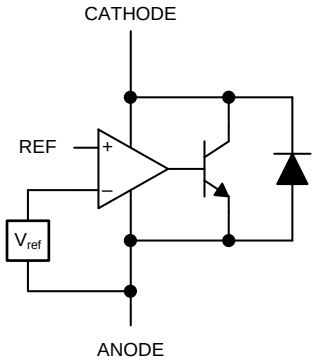


図 4. TL431 Functional Block Diagram

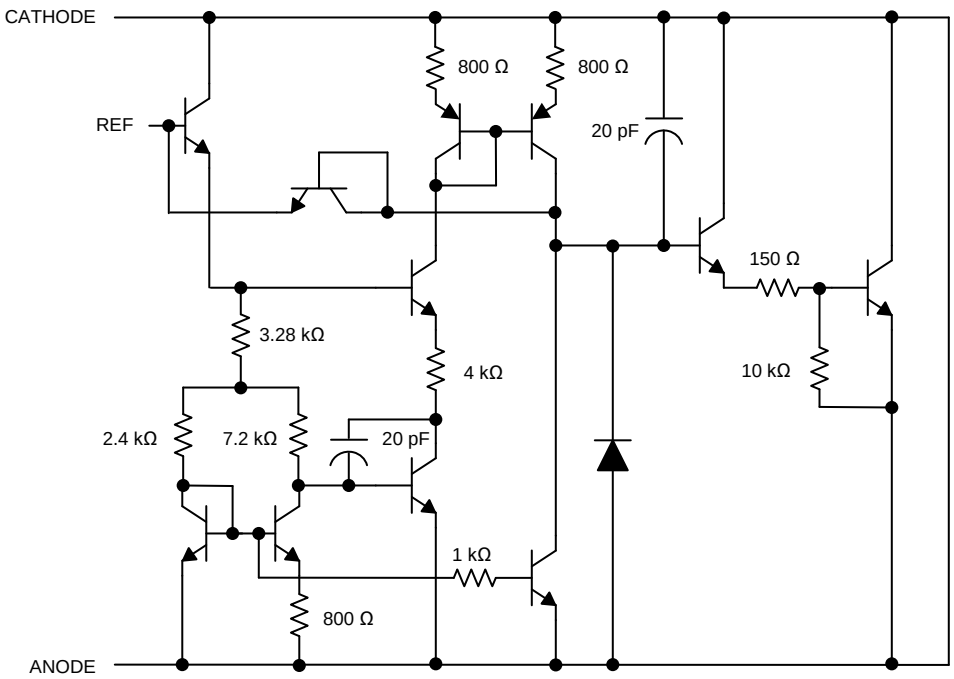


図 5. TL431 Detailed Schematic

2.2.3 TLV1117

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. device

The device is available in 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA decreasing at lower load currents.

In this reference design, fixed 3.3-V output part (TLV1117-33IDCYR) in SOT-223(4) package is used. Hence, the maximum current that can be delivered by the LDO at 85°C is 100 mA due to thermal limitations. For a higher current output from 3.3-V rail, LDO should be operated at a lower maximum ambient temperature than 85°C or a higher thermal capacity package should be used.

For more information on each of these devices, see the respective product folders at www.TI.com or click on the links for the product folders on the first page of this reference design.

2.3 System Design Theory

2.3.1 System Parameter Specifications and Definitions

表 2. System Parameters

VARIABLE	DEFINITION	VALUE
V_{input_max}	Maximum input voltage allowable for continuous operation	1000 V
V_{input_min}	Minimum input voltage allowable for continuous operation	290 V
V_{bulk_valley}	Minimum input voltage for converter to start-up and regulate output voltage	200 V
V_{out_cv}	Regulated output voltage in constant voltage mode	24 V
V_{out_cc}	Target minimum output voltage in constant current mode	20 V (design parameter)
V_{dd_nom}	Nominal value of VDD rail	12 V (design parameter)
V_{ovp_cv}	Output overvoltage limit	30 V (design parameter)
I_{out}	Full-load equivalent output current	2.1 A (50 W, 24 V)
I_{occ}	Target output current during constant current mode	2.3 A (110% of Iout)
η_{conv}	Target converter efficiency	85% (estimate)
η_{xfmr}	Target transformer efficiency	90% (estimate)
D_{demag_cc}	Demagnetizing duty cycle	0.425 (device parameter)
f_{max}	Maximum switching frequency	40 kHz (design parameter)
f_{res}	Resonant frequency during DCM dead time	500 kHz (estimate)
t_{res}	Time to first resonant valley	1 µs (from f_{res})
V_{ccr_nom}	Constant current regulation factor, nominal	330 mV (device parameter)
t_{csleb}	Leading edge blanking time, maximum	280 ns (device parameter)
K_{am}	Amplitude modulation control ratio	4 (device parameter)
V_{cst_nom}	Maximum current sense threshold voltage, nominal	773 mV (device parameter)
V_{ovp_nom}	Nominal overvoltage threshold at the VS pin	4.6 V (device parameter)
I_{run}	Current drawn from VDD by the UCC28740 device in run state	2 mA (device parameter)
K_{lc}	Line-current compensation ratio	25 A/A (device parameter)
I_{vslrun_max}	VS line sense run current, maximum	275 µA (device parameter)
I_{fbmax}	Current into FB pin, maximum	30 µA (device parameter)
V_{fbmax}	Voltage at FB pin, maximum	1 V (device parameter)
V_{vddon}	VDD level at which the UCC28740 device is out of UVLO reset and starts operating	21 V (device parameter)

表 2. System Parameters (continued)

VARIABLE	DEFINITION	VALUE
V_{vddoff}	VDD level at which the UCC28740 device enters UVLO reset and stops operating	7.75 V (device parameter)

See *UCC28740 Constant-Voltage Constant-Current Flyback Controller Using Optocoupled Feedback* for more information on variables marked as device parameters.

注: The V_{out_cv} value used in the design is 24 V (except wherever explicitly mentioned as 5 V). Regulation of 24 V or 5 V is achieved by changing three resistors as explained in 2.3.7 and does not affect any other design element like flyback transformer, MOSFETs, diodes, and so forth.

2.3.2 Flyback Transformer

The flyback transformer plays a critical role in deciding the voltage stresses on the semiconductor devices and the efficiency of the converter. Key design parameters of a flyback transformer are turns ratio, magnetizing inductance, and voltage and current ratings of the windings.

Primary-to-secondary turns ratio

The maximum duty cycle (D_{max_target}) at which the converter can operate is given by 式 1,

$$D_{max\_target} = (1 - (t_{res} \times f_{max}) - D_{demag\_cc}) = 1 - ((1 \times 10^{-6}) \times 40000) - 0.425 = 0.535 \quad (1)$$

式 2 determines the primary to secondary (24 V) turns ratio (N_{ps}):

$$N_{ps} = \frac{(D_{max\_target} \times V_{bulk\_valley})}{D_{demag\_cc} \times (V_{out\_cv} + V_f)} = \frac{0.535 \times 200}{0.425 \times (24 + 0.7)} = 10.19 \quad (2)$$

where

- V_f - Forward drop of 24-V secondary diode at full load = 0.7 V (estimate)

The N_{ps} design value is chosen as 9 instead of 10 to reduce the reflected flyback voltage and subsequently the peak V_{ds} stress experienced by the primary MOSFET. Lower reflected flyback voltage also reduces the snubber losses for the same V_{ds} clamp level; this helps offset the increase in losses due to higher primary peak current operation at lower N_{ps} for a given power output.

Primary-to-secondary (15 V) turns ratio, N_{ps1} and primary-to-secondary (5 V) turns ratio, N_{ps2} are derived from the selected N_{ps} value and ratio of each rail to 24 V. So $N_{ps1} = N_{ps} \times (24 / 15) = 14.4$ and $N_{ps2} = N_{ps} \times (24 / 5) = 43.2$. 表 3 shows that actual turns ratio values differ slightly from design values due to constraints like the integer turns ratio.

Current sense resistor

式 3 gives the value of the current sense resistor (R_{cs}):

$$R_{cs} = \frac{(V_{ccr\_nom} \times N_{ps} \times \sqrt{\eta_{xfmr}})}{(2 \times I_{occ})} = \frac{0.33 \times 9 \times \sqrt{0.9}}{2 \times 2.3} = 0.61\Omega \quad (3)$$

The R_{cs} design value is chosen to be **0.62 Ω, 1 W, 1%** – the closest available standard resistor value. See 式 13 for the power rating calculation. The nominal primary peak current (I_{pp_nom}) is given by 式 4:

$$I_{pp\_nom} = \frac{V_{cst\_nom}}{R_{cs}} = \frac{0.773}{0.62} = 1.247A \quad (4)$$

Actual output current during constant current mode (I_{occ_actual}) is given by 式 5:

$$I_{occ\_actual} = I_{pp\_nom} \times N_{ps} \times D_{demag\_cc} \times 0.5 = 1.247 \times 9 \times 0.425 \times 0.5 = 2.384 \text{ A} \quad (5)$$

Magnetizing inductance

式 6 estimates the magnetizing inductance (L_p) to meet the f_{max} target with the chosen R_{cs}:

$$L_p = \frac{2 \times (V_{out\_cv} + V_f) \times I_{occ\_actual}}{\eta_{xfmr} \times (I_{pp\_nom})^2 \times f_{max}} = \frac{2 \times (24 + 0.7) \times 2.384}{0.9 \times 1.247^2 \times 40000} = 2103.76 \ \mu H \quad (6)$$

To improve efficiency, the L_p value is chosen to be 2350 µH – this reduces the operating frequency at full-load to approximately 32 kHz. It is also critical to ensure that the L_p value chosen for the system is such that the minimum on-time (t_{on_min}) is greater than t_{csleb}. The minimum on-time for the given L_p is estimated using 式 7:

$$t_{on\_min} = \frac{L_p \times I_{pp\_nom}}{V_{input\_max} \times K_{am}} = \frac{2350 \times 10^{-6} \times 1.247}{1000 \times 4} = 732.61 \text{ ns} \quad (7)$$

Conversely, for a t_{csleb} of 280 ns, it is possible to calculate the minimum value of magnetizing inductance so as to ensure the on-time is never lower than the current sense leading edge blanking time, t_{csleb}. This minimum magnetizing inductance value (L_{p_min}) is given by 式 8,

$$L_{p\_min} = \frac{t_{csleb} \times V_{input\_max} \times K_{am}}{I_{pp\_nom}} = \frac{280 \times 10^{-9} \times 1000 \times 4}{1.247} = 898.16 \ \mu H \quad (8)$$

As the magnetizing inductance reduces, the operating frequency at full-load increases (magnetizing inductance of 2104 µH results in full-load operation at 40 kHz for the chosen R_{cs}). For L_p = 898.16 µH, as given by 式 8, f_{max} increases to 93.69 kHz instead of the targeted 40 kHz – in 式 6, substitute L_p as 898.16 µH and solve for f_{max}, keeping other variables unchanged. Since the flyback converter is a high-voltage, low-current (peak turn-off current is always I_{pp_nom} when the operating frequency is above 32 kHz) switching losses are significant compared to conduction losses; hence, reducing switching frequency as much as possible improves efficiency.

However, features like frequency dithering are activated only when the switching frequency is higher than 32 kHz. Therefore, the L_p value is chosen as 2350 µH to enable such features while keeping switching losses low. Choose an L_p value between 2104 µH and 2350 µH (for chosen R_{cs}) to operate within 32–40 kHz at full-load – this improves efficiency while also providing the full range of features including frequency dithering.

Primary-to-auxiliary turns ratio

Auxiliary winding is used for output OV detection, provide power to VDD, and regulate the output current during CC mode, amongst other functions. 式 9 provides the auxiliary-to-secondary turns ratio (N_{as}):

$$N_{as} = \frac{V_{dd\_nom} + V_{fa}}{V_{out\_cv} + V_f} = \frac{12 + 0.4}{24 + 0.7} = 0.502$$

where

- V_{fa} - Forward drop of auxiliary diode at full-load = 0.4 V (estimate) (9)

The primary-to-auxiliary turns ratio (N_{pa}) is given by 式 10:

$$N_{pa} = \frac{N_{ps}}{N_{as}} = \frac{9}{0.502} = 17.93 \quad (10)$$

Winding RMS currents

For the chosen design value of L_p = 2350 µH, f_{max} is calculated as 32 kHz from 式 6. The switching period (t_{sw}) = (1 / f_{max}) = 31.01 µs. The maximum on-time (t_{on_max}) is given by 式 11:

$$t_{on\_max} = \frac{I_{pp\_nom} \times L_p}{V_{input\_min}} = \frac{1.247 \times 2350 \times 10^{-6}}{290} = 10.11 \ \mu s \quad (11)$$

The primary peak current (I_{pk_pri}) is I_{pp_nom} = 1.247 A, the primary RMS current (I_{pri_rms}) is given by 式 12:

$$I_{pri\_rms} = \frac{I_{pp\_nom} \times \sqrt{\frac{t_{on\_max}}{t_{sw}}}}{\sqrt{3}} = \frac{1.247 \times \sqrt{\frac{10.11 \times 10^{-6}}{31.01 \times 10^{-6}}}}{\sqrt{3}} = 0.41 \ A \quad (12)$$

The power dissipation in the current sense resistor (P_{cs}) is given by 式 13:

$$P_{cs} = I_{pri\_rms}^2 \times R_{cs} = 0.41^2 \times 0.62 = 0.104 \ W \quad (13)$$

式 14 and 式 15 provide the peak and RMS current in the secondary and auxiliary windings:

$$I_{pk} = \frac{P_{out} \times 2}{V_{out} \times D_{demag\_cc}} \quad (14)$$

$$I_{rms} = I_{pk} \times \sqrt{\frac{D_{demag\_cc}}{3}} \quad (15)$$

- 24-V secondary winding peak and RMS currents are 5.88 A and 2.21 A, respectively.
- 15-V secondary winding peak and RMS currents are 3.14 A and 1.18 A, respectively.
- 5-V secondary winding peak and RMS currents are 9.41 A and 3.54 A, respectively.
- Isolated 5-V secondary winding peak and RMS currents are 0.47 A and 0.18 A, respectively.
- Auxiliary winding peak and RMS currents are 0.47 A and 0.18 A, respectively.

Transformer Design Summary

Based on design values previously listed, Wurth Electronik constructed a custom flyback transformer. The turns ratio of 15 V, 5-V windings is calculated based on N_{ps} and the ratio of each rail voltage to 24 V. Due to practical constraints like integer number of turns, parameters like N_{pa} have changed marginally from the calculated or design values; parameters and actual values are listed in 表 3. Triple insulated wires are used for the secondary side windings to provide the required isolation from HV input windings.

表 3. Transformer Parameters

PARAMETER	VALUE	COMMENTS
N_{ps}	9	Turns ratio for primary to 24-V secondary
N_{ps1}	14.63	Turns ratio for primary to 15-V secondary
N_{ps2}	39	Turns ratio for primary to 5-V secondary
N_{ps_iso}	39	Turns ratio for primary to 5-V isolated secondary
N_{as}	16.71	Integer turns reduced N_{as} from 17.93 to 16.71
L_p	2350 µH	Operating frequency at full-load = 32 kHz

2.3.3 Primary MOSFET

Two critical parameters for choosing a MOSFET are drain-to-source voltage (V_{ds}), and continuous RMS current (I_{rms}) ratings. MOSFET RMS current in this design will be 0.41 A (see 式 12).

式 16 gives the peak drain-to-source voltage to be blocked by MOSFET during turn-off:

$$V_{ds} = V_{input\_max} + N_{ps} \times (V_{out\_cv} + V_f) \times 2 = 1000 + 9 \times (24 + 0.7) \times 2 = 1444 \ V \quad (16)$$

Twice the reflected flyback voltage (N_{ps} × (V_{out_cv} +V_f)) is a reasonable estimation for the V_{ds} rating of the MOSFET – snubber overvoltage is assumed to be equal to the reflected flyback voltage providing a good balance between efficiency, snubber size, and MOSFET V_{ds} stress.

式 16 shows that a 1500-V MOSFET is required to handle the V_{ds} stress in this design. Based on V_{ds} and I_{rms} ratings, a **1500-V, 4-A MOSFET** is chosen (**2SK1835-E**) with the following characteristics:

- Maximum drain-to-source static resistance, R_{dson_max} = 7 Ω
- Output capacitance, C_{oss} = 230 pF (at V_{ds_test} = 10 V)
  - At V_{input_min}:

$$C_{oss\_290} = 2 \times C_{oss} \times \sqrt{\frac{V_{ds\_test}}{V_{input\_min}}} = 2 \times 230 \times 10^{-12} \times \sqrt{\frac{10}{290}} = 85.42 \text{ pF}$$

  - At V_{input_max}:

$$C_{oss\_1000} = 2 \times C_{oss} \times \sqrt{\frac{V_{ds\_test}}{V_{input\_max}}} = 2 \times 230 \times 10^{-12} \times \sqrt{\frac{10}{1000}} = 46 \text{ pF}$$

- Gate charge, Q_g = 60 nC (just above the Miller plateau at V_{ds} = 600 V)
- Fall-time, t_f = 80 ns

MOSFET Conduction Loss

式 17 gives the MOSFET conduction loss (P_c) at V_{input_min} (290 V):

$$P_c = I_{pri\_rms}^2 \times R_{dson\_max} = 0.41^2 \times 7 = 1.17 \text{ W} \quad (17)$$

At V_{input_max}, P_c reduces by the inverse ratio of input voltages (due to the decrease in I_{pri_rms} at higher input line voltages), that is, P_c at V_{input_max} (1000 V) is (290 / 1000) × 1.17 = 0.34 W.

MOSFET Gate Charge Loss

式 18 estimates the gate charge loss in the MOSFET (P_g),

$$P_g = V_g \times Q_g \times f_{max} = 12 \times 60 \times 10^{-9} \times 32000 = 0.023 \text{ W} \quad (18)$$

where

- V_g is the gate voltage – 12 V in this design

MOSFET Switching Loss

The switching loss is composed of 2 parts – turn-off loss (P_{to}) and turn-on (C_{oss}) loss (P_{coss}) . 式 19 provides the turn-off loss and 式 20 provides the C_{oss} loss:

$$P_{to} = 0.5 \text{ x } (V_{input\_max} + (V_{out\_cv} + V_f) \times N_{ps}) \text{ x } I_{pp\_nom} \text{ x } t_f \text{ x } f_{max} \quad (19)$$

$$P_{coss} = 0.5 \times C_{oss} \times (V_{input\_max} - (V_{out\_cv} + V_f) \times N_{ps})^2 \times f_{max} \quad (20)$$

At $V_{input} = V_{input\_min} = 290$ V:

$$P_{to} = 0.5 \times (290 + (24 + 0.7) \times 9) \times 1.247 \times 80 \times 10^{-9} \times 32000 = 0.82 \text{ W}$$

$$P_{coss} = 0.5 \times 85.42 \times 10^{-12} \times (290 - (24 + 0.7) \times 9)^2 \times 32000 = 0.006 \text{ W}$$

At $V_{input} = V_{input\_max} = 1000$ V:

$$P_{to} = 0.5 \times (1000 + (24 + 0.7) \times 9) \times 1.247 \times 80 \times 10^{-9} \times 32000 = 1.95 \text{ W}$$

$$P_{coss} = 0.5 \times 46 \times 10^{-12} \times (1000 - (24 + 0.7) \times 9)^2 \times 32000 = 0.45 \text{ W}$$

Therefore, the total MOSFET loss at 290 V is:

$$1.17 \text{ W (conduction loss)} + 0.023 \text{ W (gate charge)} + (0.82 \text{ W} + 0.006 \text{ W}) \text{ (switching loss)} = 2.02 \text{ W}$$

Therefore, the total MOSFET loss at 1000 V is:

$$0.34 \text{ W (conduction loss)} + 0.023 \text{ W (gate charge)} + (1.95 \text{ W} + 0.45 \text{ W}) \text{ (switching loss)} = 2.76 \text{ W}$$

Heat Sink Selection

The maximum operating junction temperature for MOSFET is 150°C. Select a heatsink to restrict the maximum device temperature within 125°C (margin of 25°C) at an ambient temperature of 70°C – so the allowable temperature rise is 125°C – 70°C = 55°C while dissipating 2.76 W. Hence, thermal resistance of heat sink should be (55°C / 2.76 W) = 19.92°C/W. Therefore, a screw-mounted heat sink (**V2109B**) with a thermal resistance of 20°C/W during natural convection is selected.

2.3.4 Output and Auxiliary Diodes

式 21 gives the reverse blocking voltage required of each diode (V_r):

$$V_r = V_{out} + \frac{V_{input\_max}}{\text{Turns ratio}} \quad (21)$$

where

- V_{out} is the voltage level of rail supplied by the diode
- Turns ratio is the ratio of primary-to-secondary / auxiliary turns for that specific rail

For example, for the 15-V rail, V_{out} will be 15 V and the turns ratio will be $N_{ps1} = 14.63$. 式 22 determines the peak current in each diode (I_{pk_d}):

$$I_{pk\_d} = \frac{P_{out} \text{ x } 2}{V_{out} \text{ x } D_{demag\_cc}}$$

where

- P_{out} is power output from specific rail
- V_{out} is the voltage level of the specific rail supplied by the diode (22)

式 23 shows the RMS current in each diode (I_{rms_d}):

$$I_{rms\_d} = I_{pk\_d} \times \sqrt{\frac{D_{demag\_cc}}{3}} \quad (23)$$

式 24 shows the average (rectified) current in each diode (I_{avg_d}):

$$I_{avg\_d} = \frac{P_{out}}{V_{out}} \quad (24)$$

Diode for 24-V rail

$V_r = 24 + 1000 / 9 = 135.11$ V

$I_{pk\_d} = (30 \times 2) / (24 \times 0.425) = 5.88$ A

$I_{rms\_d} = 5.88 \times \sqrt{0.425 / 3} = 2.21$ A

$I_{avg\_d} = (30 / 24) = 1.25$ A

Based on the required current and voltage ratings, a **200-V, 20-A Schottky diode (MBR20200CTTU)** with a forward drop (V_d) of 0.9 V (at 25°C) at 10 A is chosen for 24-V output rail.

Power loss, $P_d = V_d \times I_{avg\_d} = 0.9 \times 1.25 = 1.13$ W

A screw-mounted heat sink **(577202B00000G)** is selected for heat dissipation.

Diode for 15-V rail

Based on 式 21 through 式 24, the following values are calculated; assuming at full-load (10 W), demagnetization duty-cycle is D_{demag_cc}:

$V_r = 15 + (1000 / 14.63) = 83.35$ V

$I_{pk\_d} = (10 \times 2) / (15 \times 0.425) = 3.14$ A

$I_{rms\_d} = 3.14 \times \sqrt{0.425 / 3} = 1.18$ A

$I_{avg\_d} = (10 / 15) = 0.67$ A

Based on the required current and voltage ratings, a **200-V, 3-A Schottky diode (MURS320-E3/57T)** with a forward drop (V_d) of 0.875 V (at 25°C) at 3 A is chosen for the 15-V output rail.

Power loss, $P_d = V_d \times I_{avg\_d} = 0.875 \times 0.67 = 0.59$ W

Diode for 5-V rail

Based on 式 21 through 式 24, the following values are calculated; assuming at full-load (10 W), demagnetization duty-cycle is D_{demag_cc}:

$V_r = 5 + (1000 / 39) = 30.64$ V

$I_{pk\_d} = (10 \times 2) / (5 \times 0.425) = 9.41$ A

$I_{rms\_d} = 9.41 \times \sqrt{0.425 / 3} = 3.45$ A

$I_{avg\_d} = (10 / 5) = 2$ A

Based on the required current and voltage ratings, a **200-V, 20-A Schottky diode (MBR20200CTTU)** with a forward drop (V_d) of 0.9 V (at 25°C) at 10 A is chosen for 5-V output rail.

Power loss, $P_d = V_d \times I_{avg\_d} = 0.9 \times 2 = 1.8$ W

A screw-mounted heat sink **(577202B00000G)** is selected for heat dissipation.

Diode for Isolated 5-V rail

Based on 式 21 through 式 24, the following values are calculated; assuming at full-load (0.5 W), demagnetization duty-cycle is D_{demag_cc}:

$$V_r = 5 + (1000 / 39) = 30.64 \quad V$$

$$I_{pk\_d} = (0.5 \times 2) / (5 \times 0.425) = 0.47 \quad A$$

$$I_{rms\_d} = 0.47 \times \sqrt{0.425 \ / \ 3} = 0.18 \quad A$$

$$I_{avg\_d} = (0.5 \ / \ 5) = 0.1 \quad A$$

Based on the required current and voltage ratings, **a 200-V, 3-A Schottky diode (MURS320-E3/57T)** with a forward drop (V_d) of 0.875 V (at 25°C) at 3 A is chosen for the isolated 5-V output rail.

$$\text{Power loss,} \quad P_d = V_d \times I_{avg\_d} = 0.875 \times 0.1 = 0.088 \quad W$$

Auxiliary Diode for VDD

Based on 式 21 through 式 24, the following values are calculated; assuming at full-load (1.2 W), demagnetization duty-cycle is D_{demag_cc}:

$$V_r = 12 + (1000 / 16.71) = 71.84 \quad V$$

$$I_{pk\_d} = (1.2 \times 2) / (12 \times 0.425) = 0.47 \quad A$$

$$I_{rms\_d} = 0.47 \times \sqrt{0.425 \ / \ 3} = 0.18 \quad A$$

$$I_{avg\_d} = (1.2 / 12) = 0.1 \quad A$$

Based on the required current and voltage ratings, a **200-V, 3-A Schottky diode (MURS320-E3/57T)** with a forward drop of 0.875 V (at 25°C) at 3 A is chosen for the VDD rail.

$$\text{Power loss,} \quad P_d = V_d \times I_{avg\_d} = 0.875 \times 0.1 = 0.088 \quad W$$

2.3.5 VS Feedback

Auxiliary winding voltage is fed back as an input to UCC28740 at VS pin through a voltage divider comprising of R_{vs1} and R_{vs2} (R_{vs1} is R29 and R_{vs2} is R37 in 図 7) – this feedback is used for output OV protection, input line sensing, valley switching and for regulating output current in CC mode.

$$R_{vs1} = \frac{V_{bulk\_valley}}{N_{pa} \times I_{vslrun\_max}} = \frac{200}{16.71 \times 275 \times 10^{-6}} = 43.52 \ k\Omega \tag{25}$$

R_{vs1} is chosen as **44.2 kΩ, 0.125 W, 1%**

$$R_{vs2} = \frac{R_{vs1} \times V_{ovp\_nom}}{(N_{as} \times (V_{ovp\_cv} - V_f)) - V_{ovp\_nom}} = \frac{44.2 \times 10^3 \times 4.6}{(0.539 \times (30 - 0.7)) - 4.6} = 18.17 \ k\Omega$$

where

- N_{as} is actual auxiliary-to-secondary turns ratio from 表 3 (26)

R_{vs2} is chosen as **17.8 kΩ, 0.125 W, 1%**.

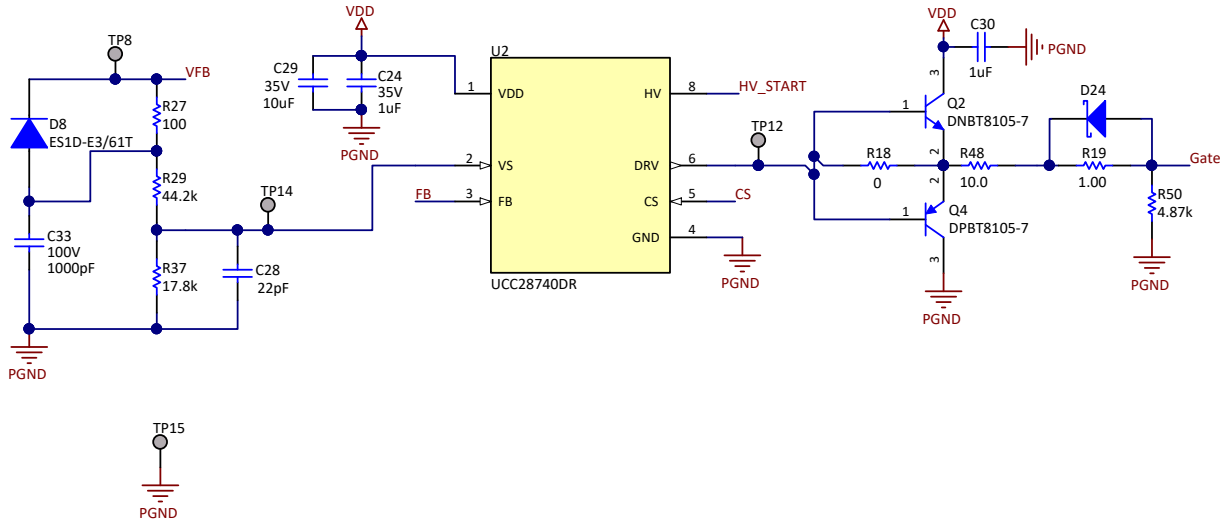


図 6. VS Pin Feedback

2.3.6 Line Sense Current Compensation

式 27 provides the value of current sense line compensation resistor (R_{lc}), R21 in 図 7.

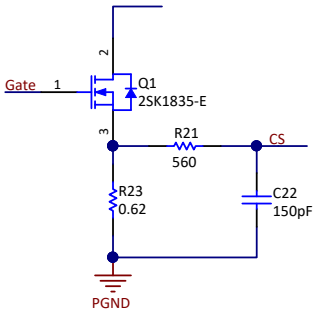


図 7. Current Sense Circuit

$$R_{lc} = \frac{K_{lc} \times R_{vs1} \times R_c \times t_{csleb} \times N_{pa}}{L_p} = \frac{25 \times 44.2 \times 10^3 \times 0.62 \times 280 \times 10^{-9} \times 16.71}{2350 \times 10^{-6}} = 1.36 \ \text{k}\Omega \quad (27)$$

The value determined in 式 27 may require adjustments based on the noise and ringing on the current sense which is dependent on routing of the signals. **562 Ω, 0.125 W, 1%** is used in the design. C22 (≤ 150 pF) is used for filtering noise on current measurement

2.3.7 Output Voltage Feedback

図 8 shows the feedback circuit used for output voltage regulation. Output voltage is fed into the reference pin of TL431 through a voltage divider formed by R_{fb1} and R_{fb2}. In 図 8, R_{fb1} and R_{fb2} are R31 and R24, respectively.

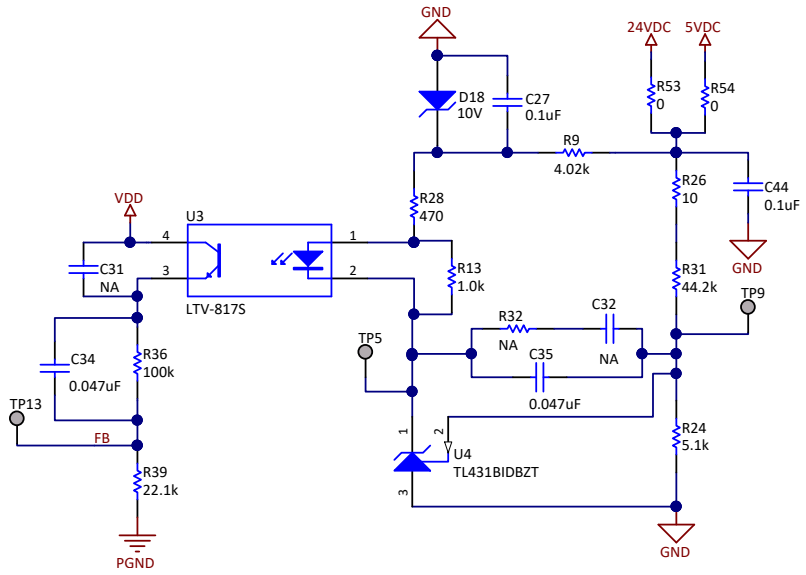


図 8. Opto-Regulated Feedback Circuit

Voltage Divider

式 28 determines the maximum value of R_{fb2} to enable proper operation of TL431.

$$R_{fb2} \leq \frac{V_{ref}}{(I_{ref} \times 15) - I_{ref}} \leq \frac{2.495}{\left(4 \times 10^{-6} \times 15\right) - 4 \times 10^{-6}} \leq 44.55\ k\Omega$$

where

- V_{ref} is nominal internal reference voltage of TL431 = 2.495 V
- I_{ref} is reference input current needed for proper operation of TL431 = 4 µA(maximum value) (28)

See *TL43xx Precision Programmable Reference*, for more information.

R_{fb2} is chosen as **44.2 kΩ, 0.125 W, 0.1%**.

R_{fb1} (R31) is given by 式 29,

$$R_{fb1} = \frac{V_{out\_cv} - V_{ref}}{\left(\frac{V_{ref}}{R_{fb2}}\right)} \quad (29)$$

To regulate the 5-V output rail, V_{out_cv} is 5 V and from 式 29, R_{fb1} = 44.38 kΩ (See 式 30). R_{fb1} is chosen as **44.2 kΩ, 0.125 W, 0.1%**.

$$R_{fb1} = \frac{5 - 2.495}{\left(\frac{2.495}{44.2 \times 10^{3}}\right)} = 44.38\ k\Omega \quad (30)$$

For regulating 24-V output rail, V_{out_cv} is 24 V. However, instead of changing R_{fb1}, we changed R_{fb2} according to 式 31 (derived from 式 29). This is to have a lower (R_{fb1} + R_{fb2}) so as to have a higher current in the voltage divider.

$$R_{fb2} = \frac{R_{fb1} \times V_{ref}}{V_{out\_cv} - V_{ref}} = \frac{44.2 \times 10^{3} \times 2.495}{24 - 2.495} = 5.13\ k\Omega \quad (31)$$

R_{fb2} is chosen as **5.1 kΩ, 0.125 W, 0.1%**.

FB pin Current Biasing Resistors

R_{fb3} and R_{fb4} are used to limit the current drawn in to the FB pin to improve the dynamic performance of the feedback loop. In 図 8, R_{fb3} and R_{fb4} are R36 and R39 respectively. During no-load, opto-coupler output current, I_{cenl} is given by 式 32,

$$I_{cenl} = I_{fbmax} + \frac{V_{fbmax}}{R_{fb4}} \quad (32)$$

R_{fb4} is empirically chosen as **22.1 kΩ, 0.125 W, 1%** resulting in a I_{cenl} value of 75µA. Depending on dynamic performance during testing, R_{fb4} can be modified, if needed. For fast response, the opto-coupler output transistor is biased to minimize the variation of VCE (phototransistor C-E voltage) between full-load and no-load operation. Connecting the emitter directly to the FB input is possible; however, an unload-step response may unavoidably drive the opto-coupler into saturation which will overload the FB input with full VDD applied. A series-resistor R_{fb3} is necessary to limit the current into FB and to avoid excess draining of VDD capacitor during this type of transient situation. The value of R_{fb3} is chosen to limit the excess I_{fb} and R_{fb4} current to an acceptable level when the opto-coupler is saturated. Like R_{fb4}, the R_{fb3} value is also chosen empirically during prototype evaluation to optimize performance based on the conditions present during that situation. A starting value may be estimated using 式 33,

$$R_{fb3} = \frac{V_{dd\_nom} - 1}{I_{cenl}} = \frac{12 - 1}{75 \times 10^{-6}} = 146 \text{ k}\Omega \quad (33)$$

R_{fb4} is chosen as **100 kΩ, 0.125 W, 1%**. As with R_{fb4}, R_{fb3} can be modified during evaluation for better dynamic performance.

Capacitor C_{fb3} (C34 in 図 8) across R_{fb3} helps to improve the transient response during load change. The value of C_{fb3} is estimated initially by equating the R_{fb3} C_{fb3} time constant to 1 ms, and later is adjusted higher or lower for optimal performance during prototype evaluation. C_{fb3} is chosen as **0.047 µF, 50 V, X7R**.

Opto-LED and TL431 Biasing Resistor

The opto-coupler input current (I_{opt}) is sum of opto-coupler output current divided by current transfer ration (CTR) of opto-coupler and TL431 bias current needed, at near-zero opto-coupler current (during full-load), to keep TL431 in linear region. This is given by 式 34:

$$I_{opt} = \frac{I_{cenl}}{CTR} + I_{bias\_TL431} = \frac{75 \times 10^{-6}}{0.1} + 1 \times 10^{-3} = 1.75 \text{ mA} \quad (34)$$

where

- CTR is current transfer ratio - 10% is a good estimate at low currents of 75–100 µA
- I_{bias_TL431} is minimum cathode current in TL431 for linear operation. At full-load, opto-LED current is near zero and hence a bias current needs to be provided in a parallel path for TL431 to be biased in linear region. To ensure this condition, TL431 biasing resistor R_{opt} (R13 in 図 8) of 1 kΩ is connected in parallel across the LED of opto-coupler – this is based on the assumption that forward drop of LED is approximately 1 V at near-zero current and a 1 kΩ in parallel will draw 1 mA necessary for TL431 to be biased properly for good regulation under all operating conditions.

式 34 gives the minimum current in opto-coupler input for proper regulation. To draw I_{opt} of 1.75 mA, the series bias resistance in input of opto-coupler, R_{tl} is calculated by 式 35. In 図 8, (R9 + R28) is R_{tl}.

$$R_{tl} = \leq \frac{V_{out\_cv} - V_{k\_TL431} - V_{f\_led}}{I_{opt}}$$

where

- V_{k_TL431} is voltage at cathode of TL431 = 2.5 V (minimum)

- V_{f_led} is forward drop of LED in opto-coupler = 1 V
- I_{opt} is minimum opto-coupler input current = 0.75 mA (LED current) + 1 mA (TL431 bias current) = 1.75 mA
- V_{out_cv} is regulated output voltage, either 24 V or 5 V (35)

For 24-V regulation, using 式 35, $R_{tl} \leq 11.71$ kΩ (chosen value is **4.49 kΩ** with R9 as **4.02 kΩ, 0.25 W, 1%** and R28 as **470 Ω, 0.25 W, 1%**)

For 5-V regulation, using 式 35, $R_{tl} \leq 857$ Ω (chosen value is **470 Ω** with R9 as **0 Ω, 0.25 W, 1%** and R28 as **470 Ω, 0.25 W, 1%**)

Compensation Network

In this design, only a capacitor C_z (C35 in 図 8) is used in the compensation path. A series R-C (R32, C32 in 図 8) option is provided but not used. In case, the series R-C is used for compensation, D18 and C27 in 図 8 are needed for fast lane removal. Value of C_z is estimated for a phase margin of 75° from the closed loop response of the system and chosen as **0.047 µF, 25 V, C0G**.

For regulation of 24 V, in 図 8, remove R54, R31 = 44.2 kΩ, R24 = 5.1 kΩ, R9= 4.02 kΩ, R28 = 470 Ω, R39 = 100 kΩ, R39 = 22.1 kΩ, C345 = 0.047 µF, C35 = 0.047 µF

For regulation of 5 V, in 図 8, remove R53, R31 = 44.2 kΩ, R24 = 44.2 kΩ, R9= 0 Ω, R28 = 470 Ω, R39 = 100 kΩ, R39 = 22.1 kΩ, C345 = 0.047 µF, C35 = 0.047 µF

注: R26 is to inject small signals for testing the closed loop response and can either be a 0-Ω resistor or a small value resistor (< 100 Ω) required to fine-tune the regulated output voltage.

2.3.8 VDD Capacitor

The capacitance on VDD supplies operating current to the device until the output of the converter reaches the target minimum operating voltage in constant-current regulation (V_{out_cc}). Once V_{out_cc} is reached, the auxiliary winding can sustain the VDD rail. The total output current available to the load and to charge the output capacitors is the constant-current regulation which is equated to 2.3 A at 24 V. Since there are multiple windings, it is assumed that each output rail is charge by its respective full-load currents. 式 36 provides the minimum VDD capacitor needed to sustain the VDD above UVLO limit (8 V) during the startup and output voltage build-up sequence.

$$C_{VDD} = \frac{\left(I_{run} + Q_g \times f_{max}\right) \times \left(\frac{C_{out\_24} \times V_{out\_24}}{I_{o\_24}} + \frac{C_{out\_15} \times V_{out\_15}}{I_{o\_15}} + \frac{C_{out\_5} \times V_{out\_5}}{I_{o\_5}} + \frac{C_{out\_iso5} \times V_{out\_iso5}}{I_{o\_iso5}}\right)}{V_{vddon} - (V_{vddoff} + 1)}$$

$$= \frac{\left(2 \times 10^{-3} + 60 \times 10^{-9} \times 32000\right) \times \left(\frac{470 \times 10^{-6}}{1.25} \times 24 + \frac{330 \times 10^{-6}}{0.67} \times 15 + \frac{940 \times 10^{-6}}{2} \times 5 + \frac{10 \times 10^{-6}}{0.1} \times 5\right)}{21 - (7.75 + 1)} = 6.16\ \mu F$$

where

- $(Q_g \times f_{max})$ is the gate current supplied from the VDD rail
- C_{out_xx} is the output capacitor on specific output rail
- V_{o_xx} is the voltage level of specific output rail
- I_{o_xx} is the maximum load current of specific output rail
- 1 V is subtracted from V_{vddon} in the denominator to add a margin to the C_{VDD} estimation (36)

C_{VDD} chosen is 12 µF comprising of one **10 µF, 35 V, X7R** and two **1 µF, 35 V, X7R**.

2.3.9 HV Startup

The UCC28740 device has a self-start feature using an internal 700 HV FET that can be accessed through HV pin as 図 9 shows. The input DC voltage is supplied to three equal capacitors (47 µF, 450 V) in series and the voltage on lower most capacitor (equal to one-third the input voltage in steady state) is connected directly to HV pin. When input power is turned ON, the HV FET starts charging the VDD capacitor through a constant current source – the current source turns OFF, when VDD reaches 21 V (V_{vddon}) and restarts only when VDD drops to 7.75 V (V_{vddoff}) again.

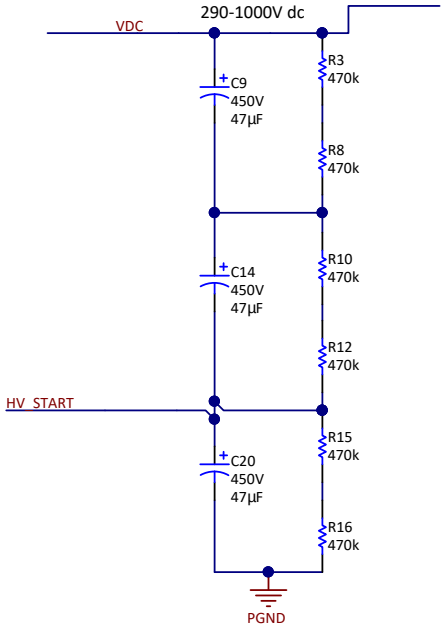


図 9. HV Start

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Input power(up to 1000 VDC) is provided to TIDA-010000 at two-pin connector, J2 in the top left corner of 図 10. A 1000-V, 2.5-A fuse protects against input overcurrent. Outputs are available on 2 connectors - J1 provides the 24-, 15-, 5-, and 3.3-V outputs (current ratings as in 図 10), all referenced to the same potential, while J3 provides the isolated 5-V output. Primary MOSFET with heatsink is in the left side , flyback transformer in the center and output diodes on the right side of 図 10 with a creepage of 8 mm between input and output for required isolation.

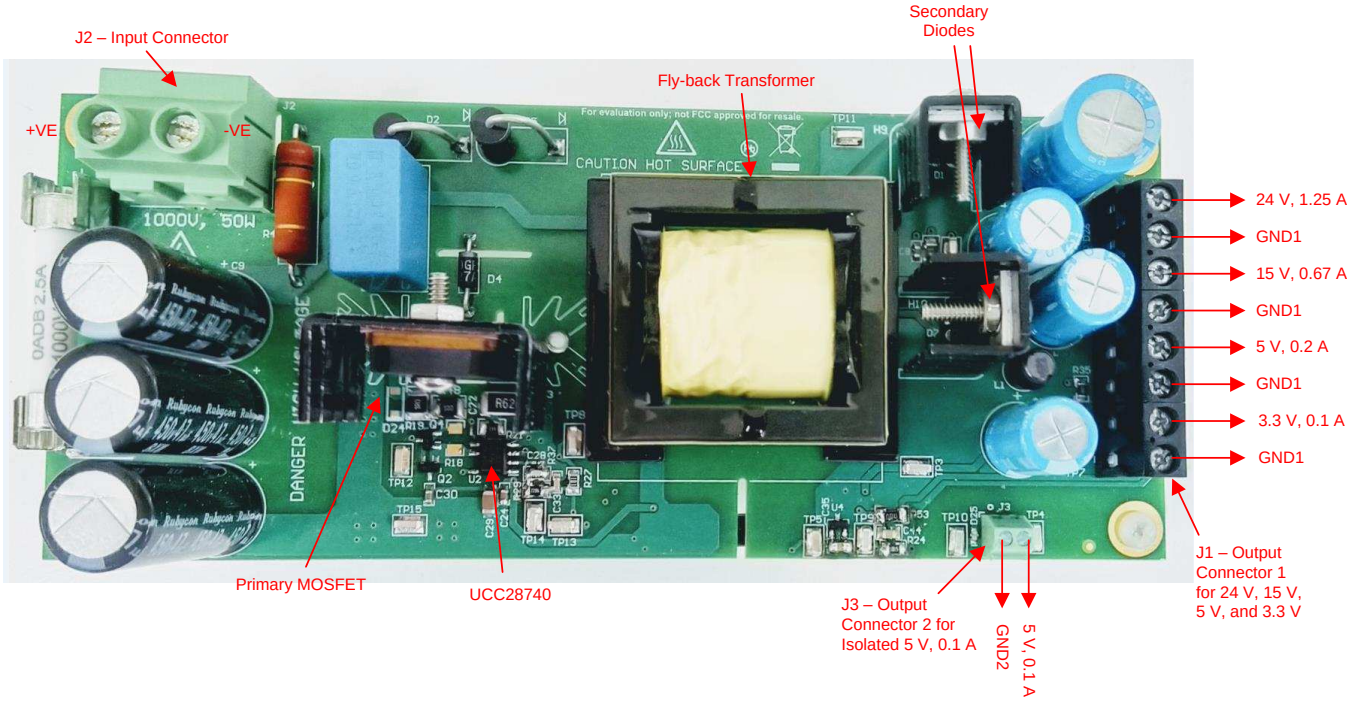


図 10. TIDA-010000 PCB Overview

3.2 Testing and Results

The TIDA-010000 is tested for various performance parameters including start-up, efficiency, line regulation, cross regulation, load regulation, step load response, temperature rise and so forth, The test setup used for the testing is broadly defined by 図 11.

3.2.1 Test Setup

As 図 11 shows, the input power to TIDA-010000 is provided by a 1000-V, 5-A controlled current DC power supply, Ametek SGI 1000/5. The input current is measured using the Tektronix PA4000 power analyzer. The output rails are loaded using decade resistor boxes. Output currents and voltages and input voltage are measured using digital multimeters. Thermal (IR) images are captured using Fluke Ti480 thermal imager. Waveforms are captured using Tektronix MSO2024B. All voltage measurements are taken at the input/ output terminals to ensure connecting cable resistances do not interfere with the results.

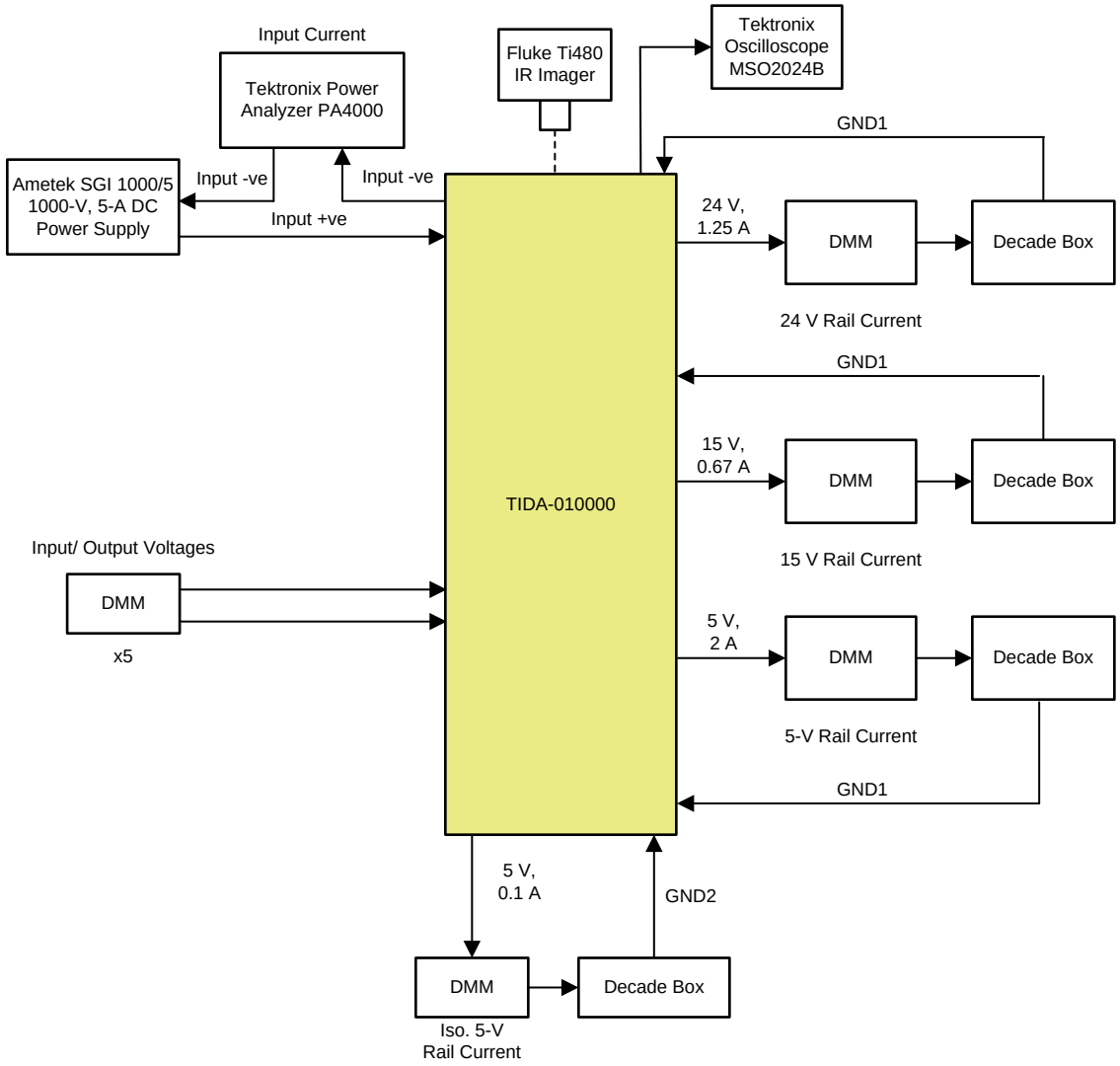


図 11. Test Setup

3.2.2 Test Results

3.2.2.1 UCC28740 Start-up Transitions

図 12 shows that when the input voltage is 180 V, VDD rail is in UVLO reset mode oscillating between 21 V and 7.75 V and the DRV pin is held low indicating UCC28740 is not in operation; at an input voltage of 220 V, VDD is at a constant 21 V and the DRV pin is switching indicating operation of UCC28740. This verifies the design input threshold voltage of 200 V.

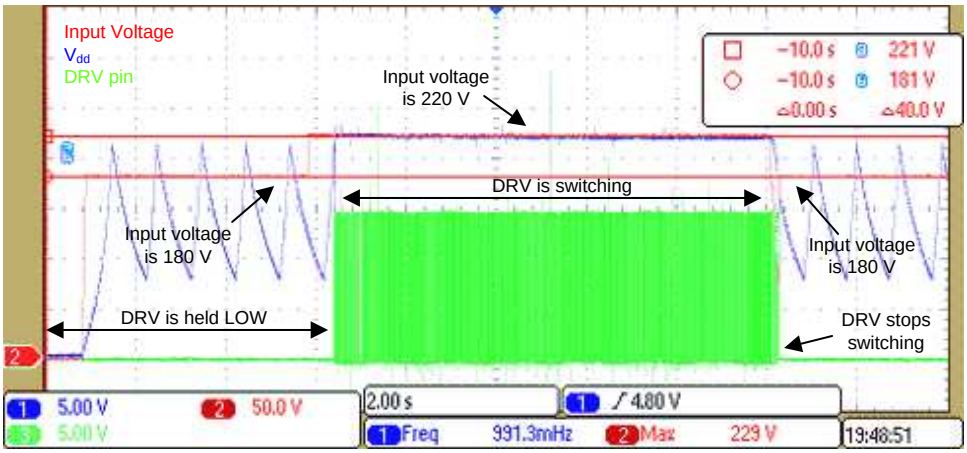


図 12. UCC28740 On-Off Threshold

Time taken by VDD rail to reach UVLO turn-on threshold (21 V) is largely dependent on C_{vdd}, see 図 13 and 図 14.

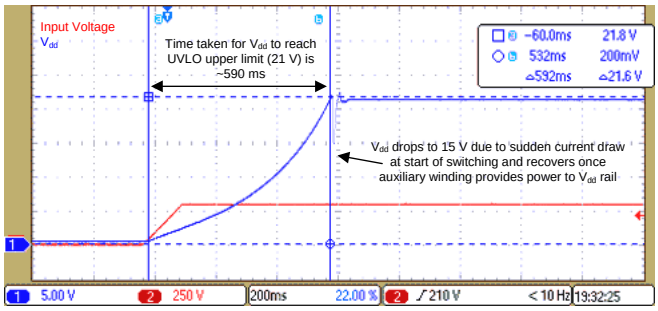


図 13. V_{DD} Build-Up at 290 V_{IN}

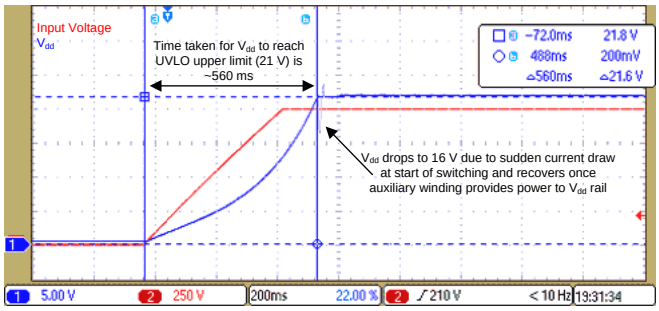


図 14. V_{DD} Build-Up at 990 V_{IN}

Output rails start ramping up after VDD reaches 21 V (UVLO turn-on threshold), see 図 15 and 図 16.

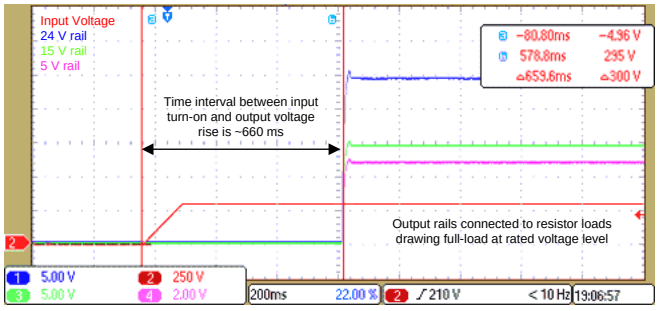


図 15. Startup at 290 V_{IN}

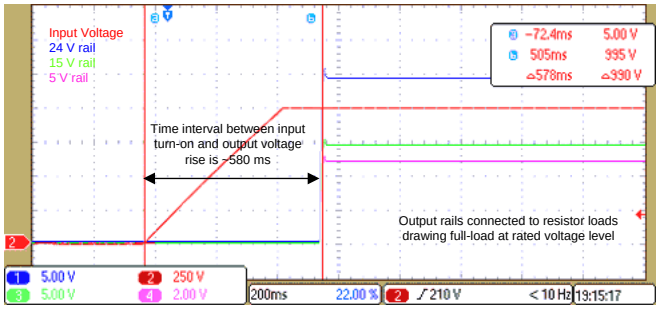


図 16. Startup at 990 V_{IN}

Time taken by output rails to reach steady state is largely dependent on the C_{out} and load, see 図 17 and 図 18

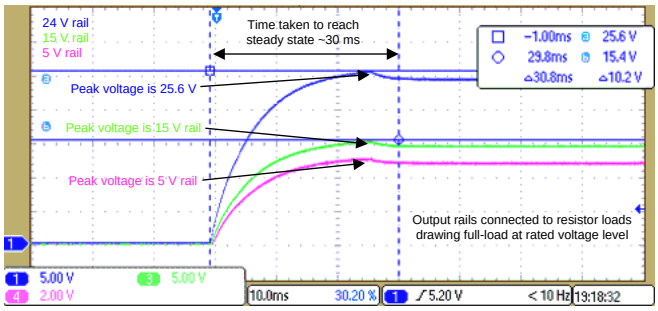


図 17. Output Voltage Ramp-Up at 290 V_{IN}

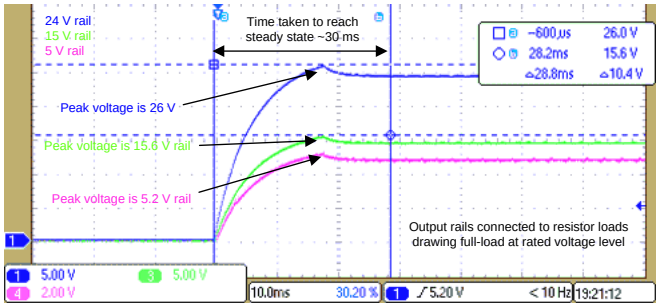


図 18. Output Voltage Ramp-Up at 990 V_{IN}

The regulated rail in 図 12 through 図 18 is 24 V.

3.2.2.2 Efficiency vs Output Power

図 19 shows efficiency vs output power curves at three input voltage levels while 24-V rail is regulated. 550 VDC is nominal DC link for 380 VAC RMS, 700 VDC is nominal DC link for 480 VAC RMS. 990 VDC is maximum permissible input. At a given measurement point, each of the 24 V, 15 V and 5-V rails are loaded at same percentage of rated power. For example if output power is 25 W (50% of rated), 24-V rail is delivering 15 W (50% of rated), 15 V is delivering 5 W (50% of rated) and 5 V is delivering 5 W (50% of rated). 図 20 shows similar efficiency vs output power curves while 5-V rail is regulated.

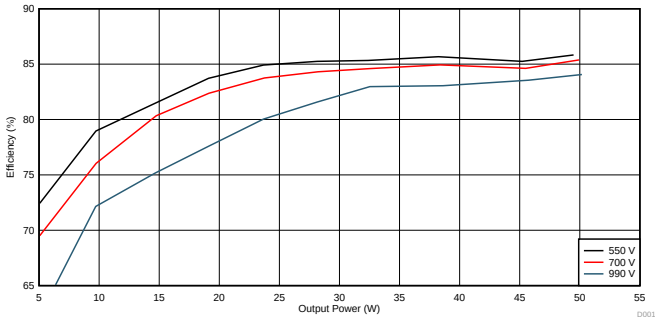


図 19. Efficiency vs Output Power: Regulated Rail 24 V

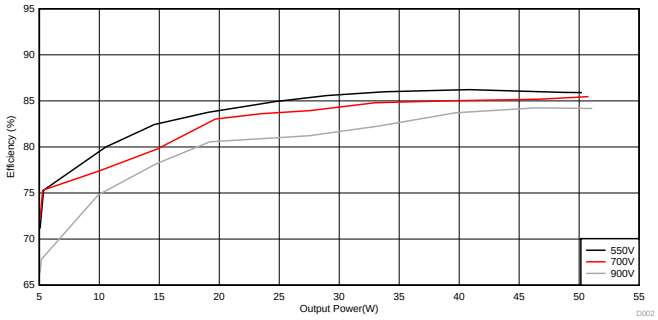


図 20. Efficiency vs Output Power: Regulated Rail 5 V

It is seen that the full-load efficiency at 550 VDC and 700 VDC is >85% . This meets the design target of 85% efficiency at full-load at nominal input voltage.

3.2.2.3 Efficiency vs Input Voltage

図 21 shows the efficiency vs input voltage at rated output power of 50 W while the 24-V rail is regulated. The efficiency at 990 V is 84.1%. 図 22 shows similar characteristics while 5-V rail is regulated.

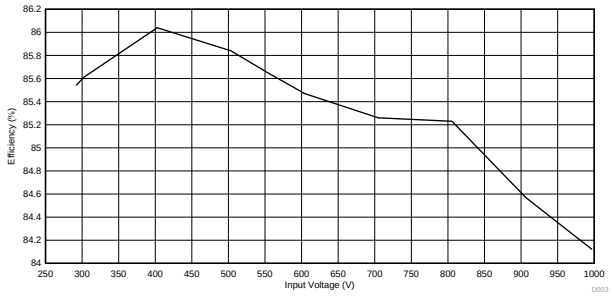


図 21. Efficiency vs Input Voltage: Regulated Rail 24 V

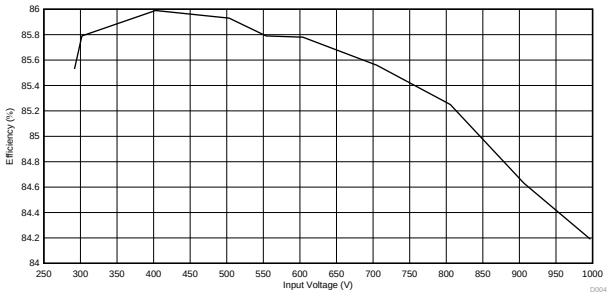


図 22. Efficiency vs Input Voltage: Regulated Rail 5 V

3.2.2.4 Line Regulation

図 23 through 図 25 show the output voltage vs input voltage curves while each output rail is delivering rated power and 24 V is the regulated rail.

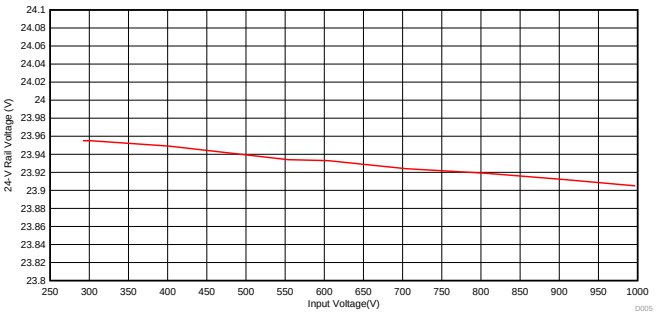


図 23. 24-V Line Regulation at 30-W Output Power: Regulated Rail 24-V

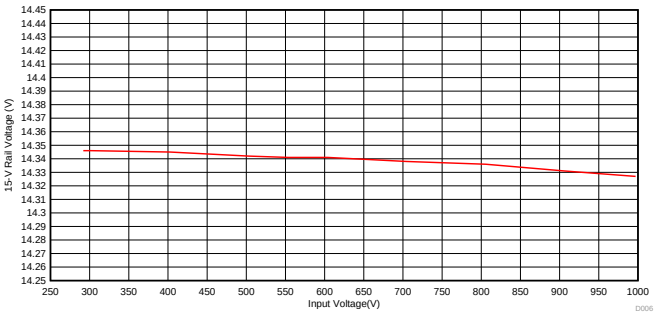


図 24. 15-V Line Regulation at 10-W Output Power: Regulated Rail 24-V

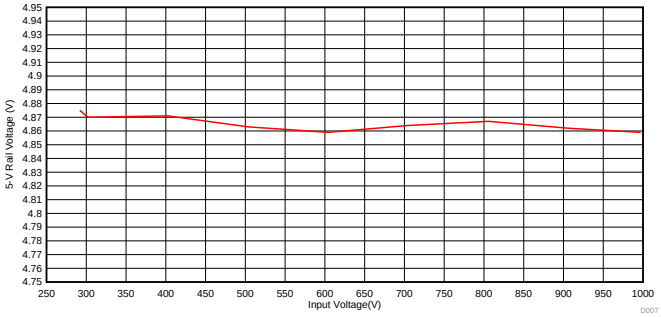


図 25. 5-V Line Regulation at 10-W Output Power: Regulated Rail 24-V

図 26 through 図 28 show the output voltage vs input voltage curves while each output rail is delivering rated power and 5 V is the regulated rail.

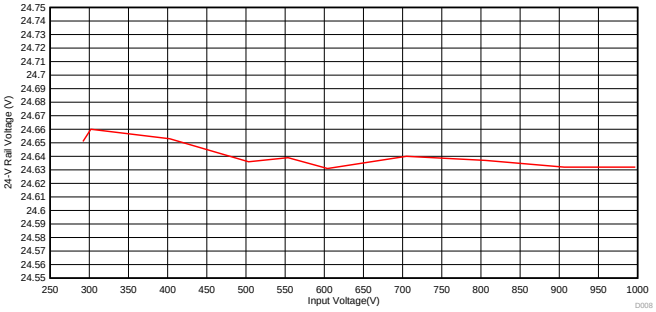


図 26. 24-V Line Regulation at 30-W Output Power: Regulated Rail 5-V

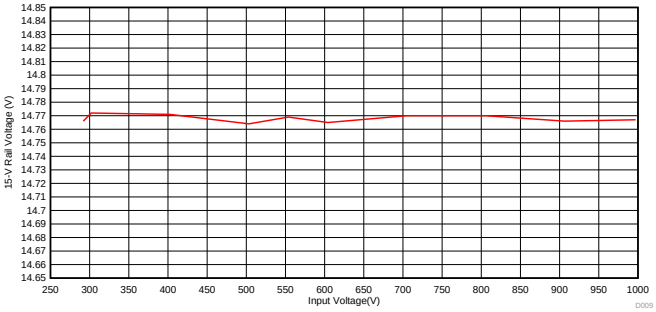


図 27. 15-V Line Regulation at 10-W Output Power: Regulated Rail 5-V

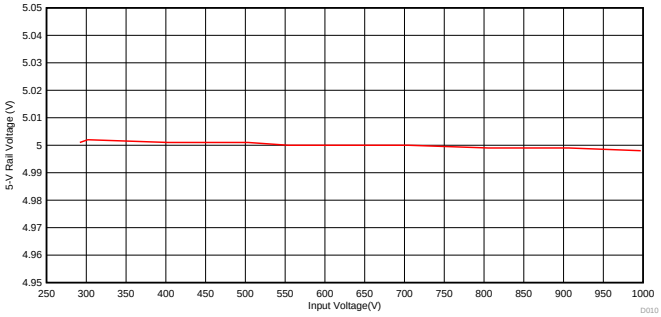


図 28. 5-V Line Regulation at 10-W Output Power: Regulated Rail 5-V

Thus, it is seen that the line regulation of all rails at respective rated loads is < 0.4% . This is well within the design target of 1%.

3.2.2.5 Cross Regulation

図 29 through 図 31 show the cross regulation performance while 24 V is the regulated rail. Each of the tested rails had less than 1% rated load while load on 24-V rail is varied from 0–30 W. The tests were performed at 550-V and 990-V input voltages.

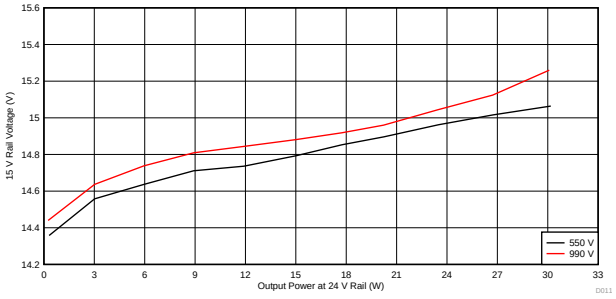


図 29. 15-V Cross Regulation: Regulated Rail 24-V

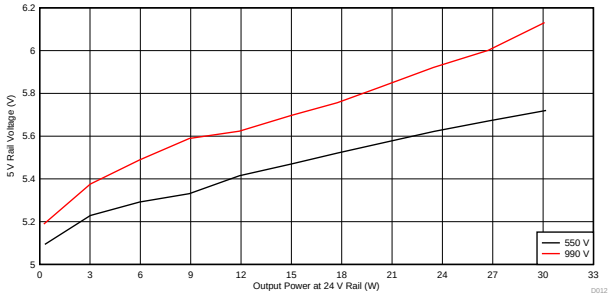


図 30. 5-V Cross Regulation: Regulated Rail 24-V

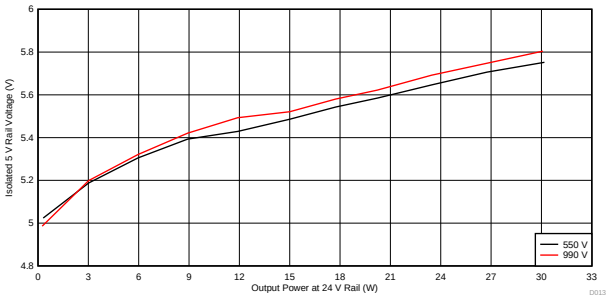


図 31. Isolated 5-V Rail Cross Regulation: Regulated Rail 24-V

図 32 through 図 34 show the cross regulation performance while 5 V is the regulated rail. 24 V and 15-V rails had 10% of rated load (3 W for 24-V rail and 1 W for 15-V rail) and isolated 5-V rail had less than 1% rated load while load on 5-V rail is varied from 0 W–10 W. The tests were performed at 550-V and 990-V input voltages. During 5-V regulation, a minimum of 10% load on 24 V (3 W) and 15 V (1 W) is simultaneously needed - else, 24-V rail exceeded 30 V and triggered output OV fault.

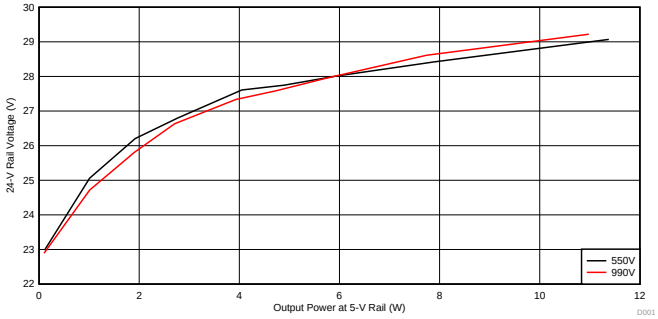


図 32. 24-V Cross Regulation: Regulated Rail 5 V

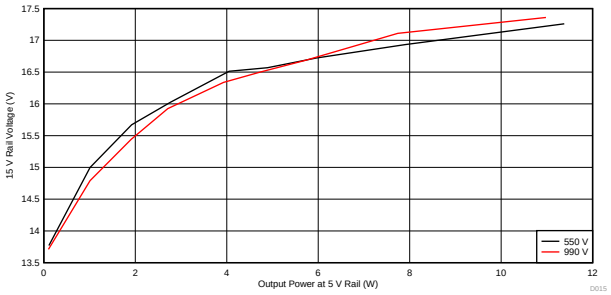


図 33. 15-V Cross Regulation: Regulated Rail 5 V

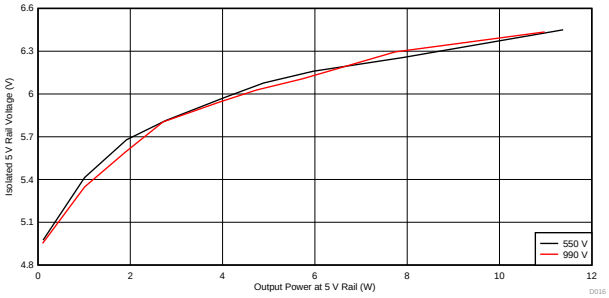


図 34. Isolated 5-V Rail Cross Regulation: Regulated Rail 5 V

3.2.2.6 Load Regulation

図 35 shows the load regulation of regulated 24-V rail at input voltages of 550 V and 990 V.

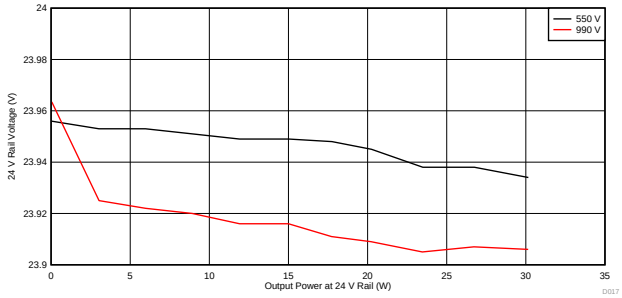


図 35. 24-V Load Regulation: Regulated Rail 24 V

図 36 through 図 37 show the load regulation of 15-V rail at input voltages of 550 V and 990 V. Load regulation of 15-V rail is performed under two cases- regulated 24-V rail at no-load and full-load respectively. 5-V rail is at no-load in all four cases.

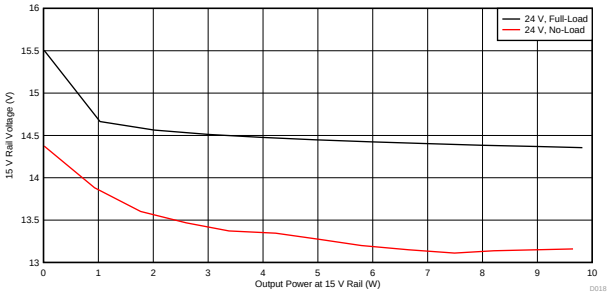


図 36. 15-V Rail Load Regulation, 550 V: Regulated Rail 24 V

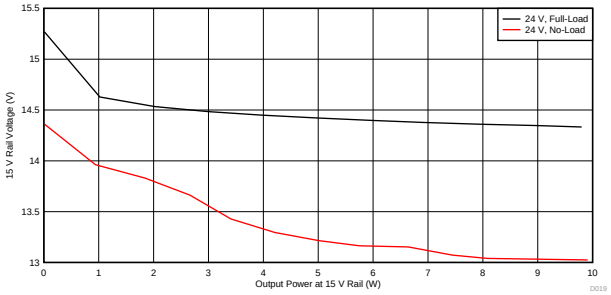


図 37. 15-V Rail Load Regulation, 990 V: Regulated Rail 24 V

図 38 through 図 39 show the load regulation of 5-V rail at input voltages of 550 V and 990 V. The load regulation of 5-V rail is performed under two cases- regulated 24-V rail at no-load and full-load respectively. 15-V rail is at no-load in all four cases. In 図 38 and 図 39, it is observed that 5-V rail is poorly regulated (and unable to deliver rated load of 10 W) when the regulated 24-V rail is at no-load.

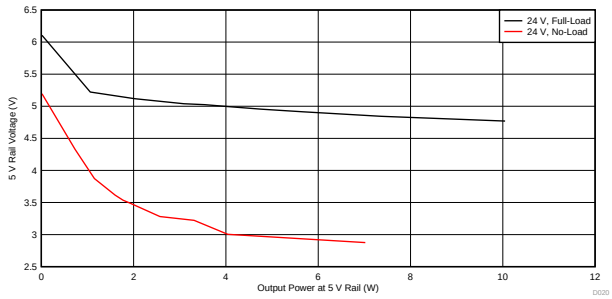


図 38. 5-V Rail Load Regulation, 550 V: Regulated Rail 24 V

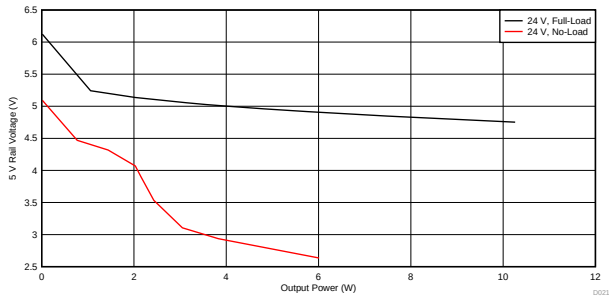


図 39. 5-V Rail Load Regulation, 990 V: Regulated Rail 24 V

図 40 shows the load regulation of regulated 5-V rail at input voltages of 550 V and 990 V.

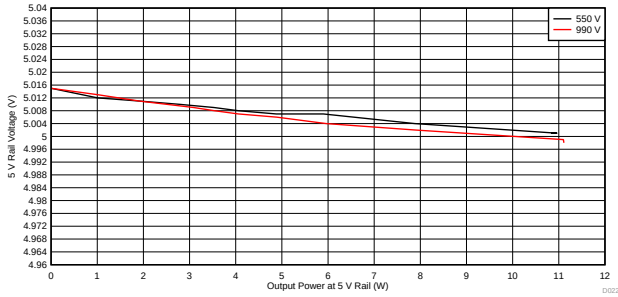


図 40. 5-V Rail Load Regulation: Regulated Rail 5 V

図 41 through 図 42 show the load regulation of 24-V rail at input voltages of 550 V and 990 V. Load regulation of 24-V rail is performed under two cases- regulated 5-V rail at no-load and full-load respectively. 15-V rail is at 10% load (1 W) in all four cases.

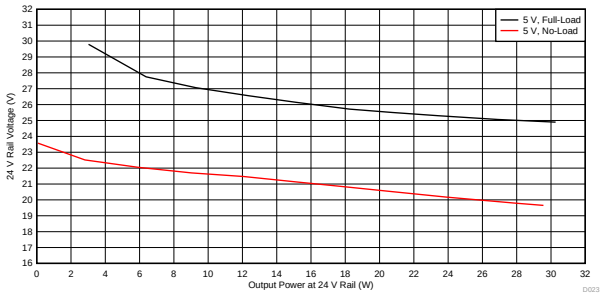


図 41. 24-V Rail Load Regulation, 550 V: Regulated Rail 5 V

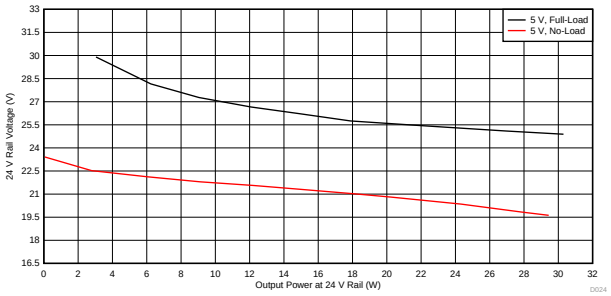


図 42. 24-V Rail Load Regulation, 990 V: Regulated Rail 5 V

図 43 through 図 44 show the load regulation of 15-V rail at input voltages of 550 V and 990 V. Load regulation of 15-V rail is performed under two cases- regulated 5-V rail at no-load and full-load respectively. 24-V rail is at 10% load (3 W) in all four cases.

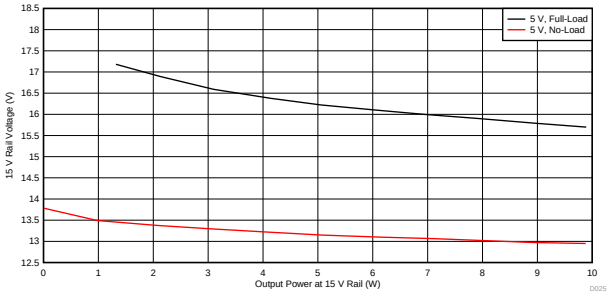


図 43. 15-V Rail Load Regulation, 550 V: Regulated Rail 5 V

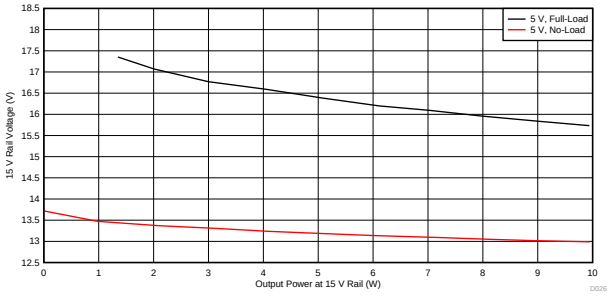


図 44. 15-V Rail Load Regulation, 990 V: Regulated Rail 5 V

Thus, it is seen that the regulated rail (be it 24 V or 5 V as the case maybe) has a load regulation of < 0.4%. This is well within the design target of 1%. It is also observed that the load regulation of unregulated rails is more impacted when regulated rail is at lighter loads.

3.2.2.7 Overload Limit

From 式 5, it is seen that the actual overcurrent limit (I_{occ_actual}) is 2.384 A. This is the equivalent current assuming all output power is delivered at 24 V. To verify this limit, 15 V and 5-V rails are connected to resistance values that draw rated load (10 W for each rail) at rated voltage. 24 V (regulated rail) load is increased till voltage regulation is lost and voltage rails start dropping.

図 45 shows the 24-V rail voltage vs 24-V rail equivalent current. Equivalent current is calculated as dividing total output power (sum of all rails' output power) by 24-V rail voltage. It is seen in 図 45 that UCC28740 regulates the 24-V rail voltage until the equivalent current (or power) reaches the design limit of 2.384 A (or 57.2 W). 図 46 shows the output power vs equivalent current at 24-V rail. This plot gives the maximum output power (58 W) that can be delivered by TIDA-010000 before regulation is lost.

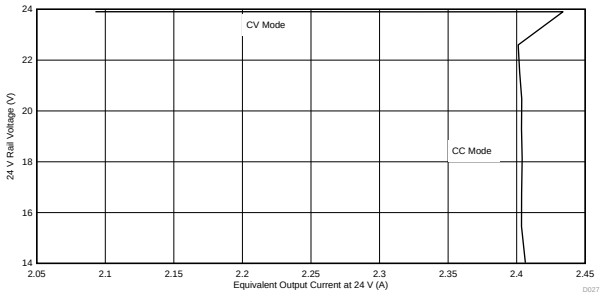


図 45. Current Limit: Regulated Rail 24 V

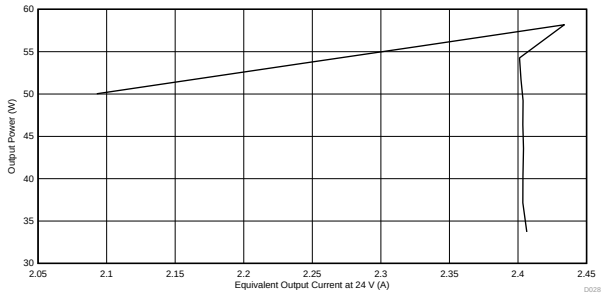


図 46. Output Power Limit: Regulated Rail 24 V

図 47 shows the output power vs 24-V rail voltage in CC mode. Once CC mode is entered (when output power reaches 58 W), voltage regulation is lost and any additional load causes a drop in output voltage and output power as seen in 図 47 from right to left. In the CC mode, equivalent output current is regulated at approximately 2.4 A and output voltage (and power) vary accordingly based on equivalent resistance at output.

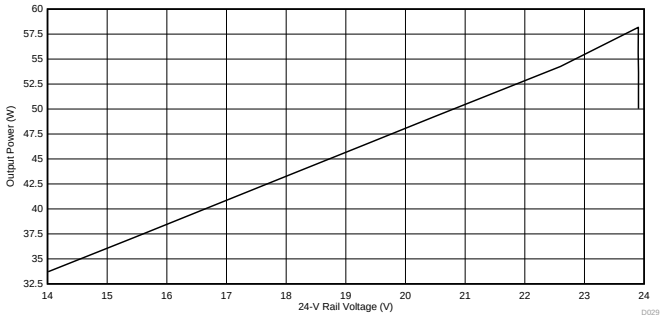


図 47. 24-V Rail Voltage in CC Mode: Regulated Rail 24 V

3.2.2.8 Waveforms

図 48 shows the V_{ds} and V_{gs} waveforms at 550-V input, no-load. 図 49 shows the V_{ds} and V_{gs} waveforms at 550-V input, full-load.

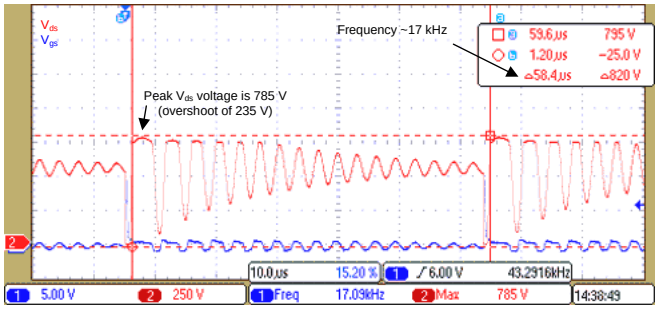


図 48. V_{DS}, V_{GS} at 550-V Input, No-Load

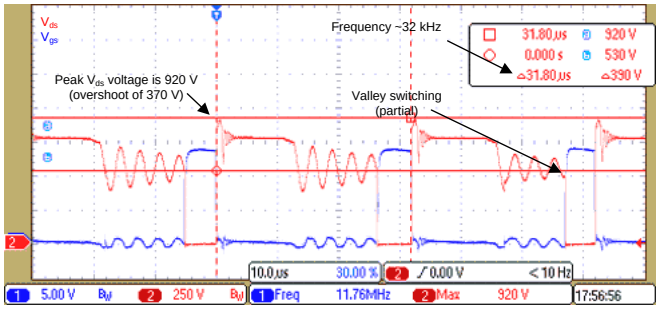


図 49. V_{DS}, V_{GS} at 550-V Input, Full Load

図 50 shows the V_{ds} and V_{gs} waveforms at 990-V input, no-load. 図 51 shows the V_{ds} and V_{gs} waveforms at 990-V input, full-load. It is seen from 図 51 that the maximum V_{ds} is 1340 V (margin of 160 V from rated 1500 V).

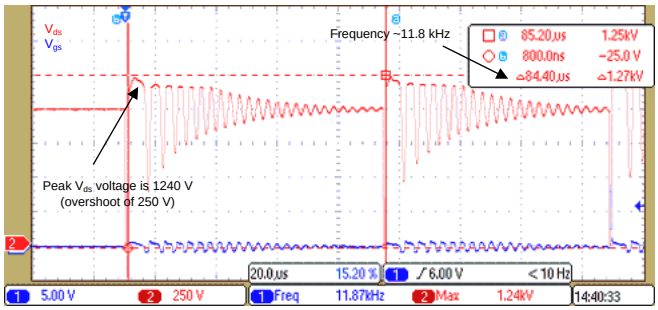


図 50. V_{DS}, V_{GS} at 990-V Input, No-Load

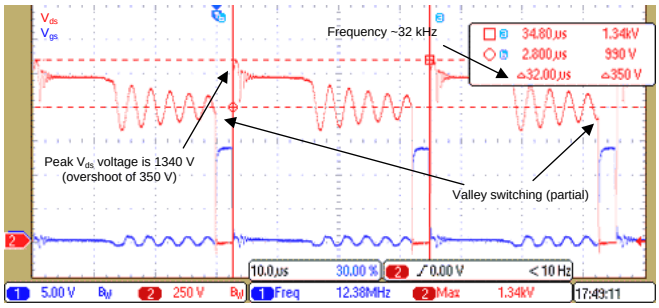


図 51. V_{DS}, V_{GS} at 990-V Input, Full Load

図 52 and 図 53 show the step-load response of the converter.

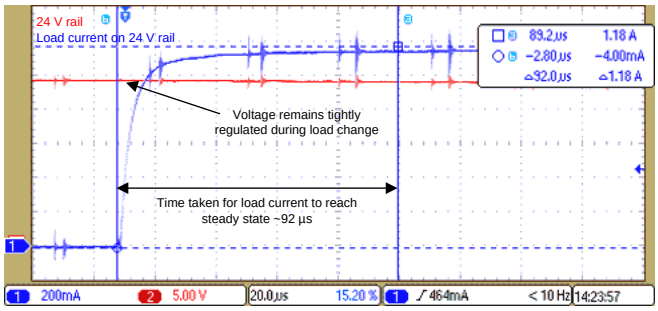


図 52. Step-Load Change 24 V, 0 to 100%

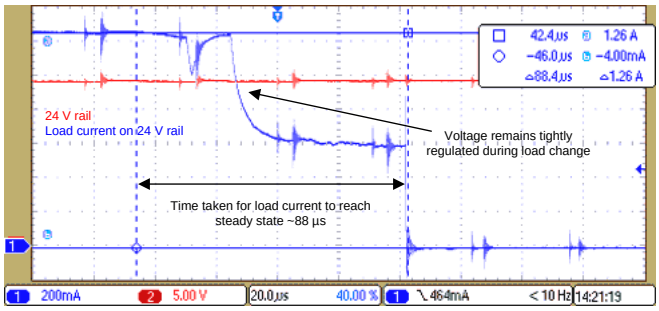


図 53. Step-Load Change 24 V, 100 to 0%

図 54 through 図 56 show the ripple on output voltage rail when each of the rail is delivering rated output power.

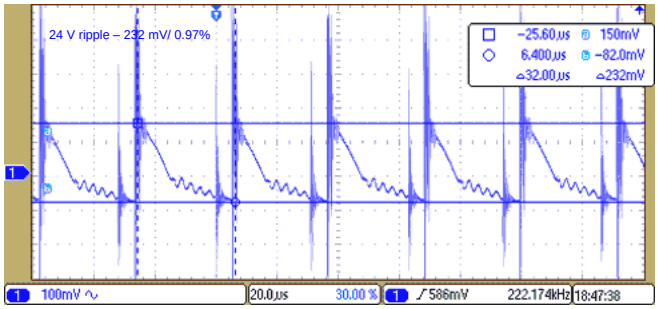


図 **54. Voltage Ripple on 24-V Rail (30 W)**

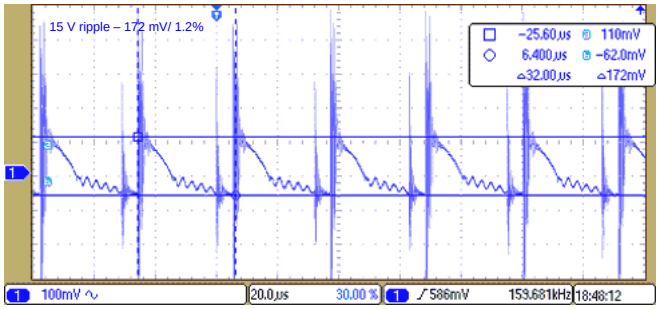


図 **55. Voltage Ripple on 15-V Rail (10 W)**

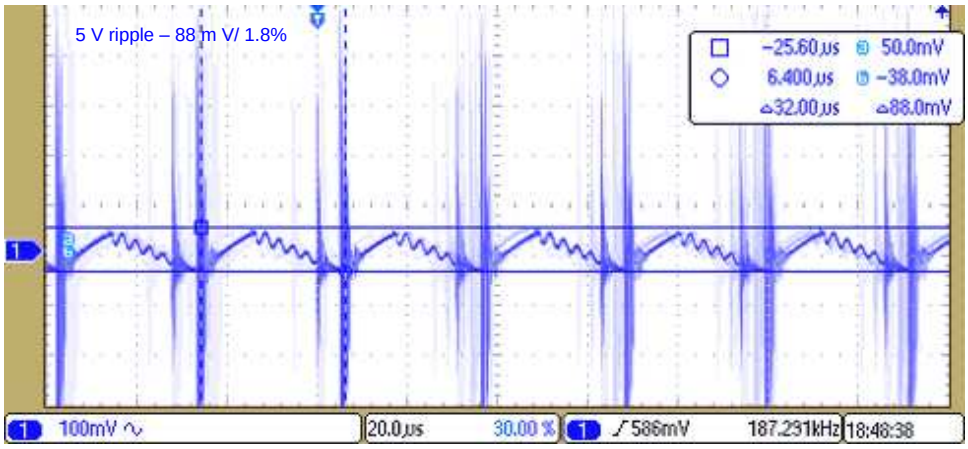


図 **56. Voltage Ripple on 5-V Rail (10 W)**

The regulated rail in 図 48 through 図 56 is 24 V.

3.2.2.9 Thermal Performance

The thermal images in 図 57 through 図 63 were captured on the TIDA-010000 after operating continuously for 30 minutes. The operating conditions include 990-V input, 50-W output power in an ambient temperature of 25°C.

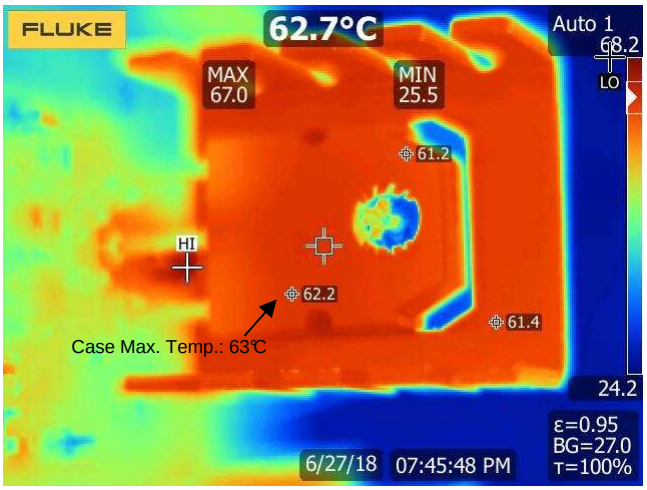


図 57. Primary MOSFET

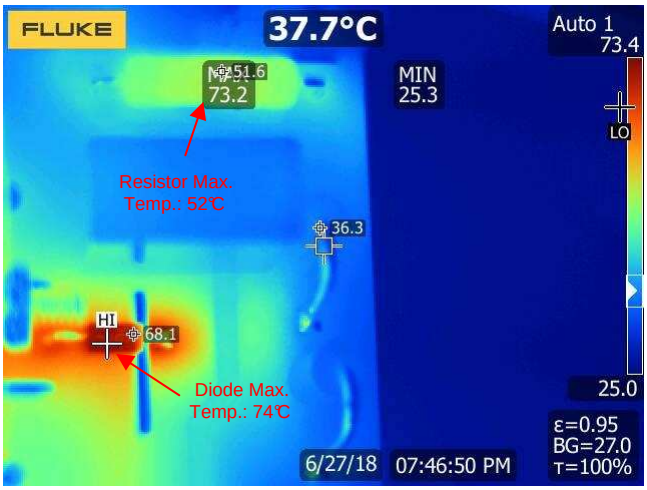


図 58. Snubber Circuit

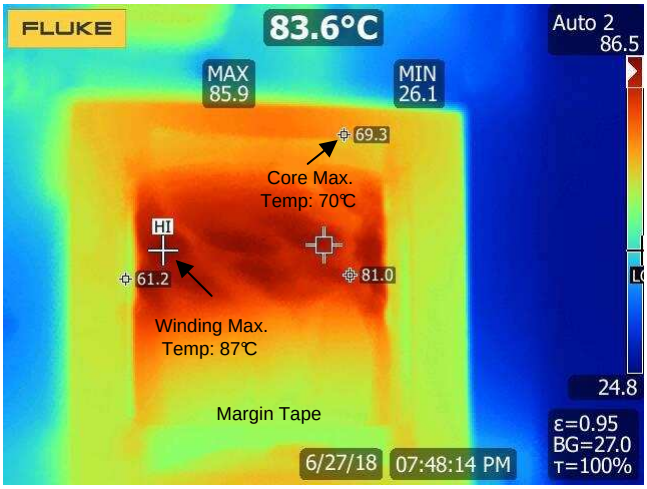


図 59. Flyback Transformer

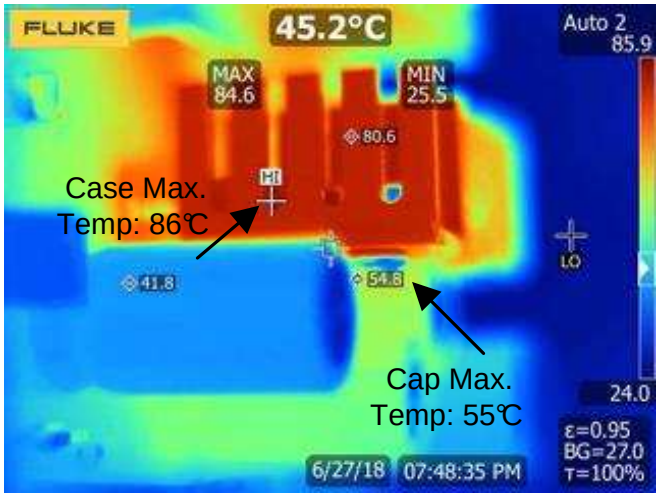


図 **60. 5-V Secondary Diode**

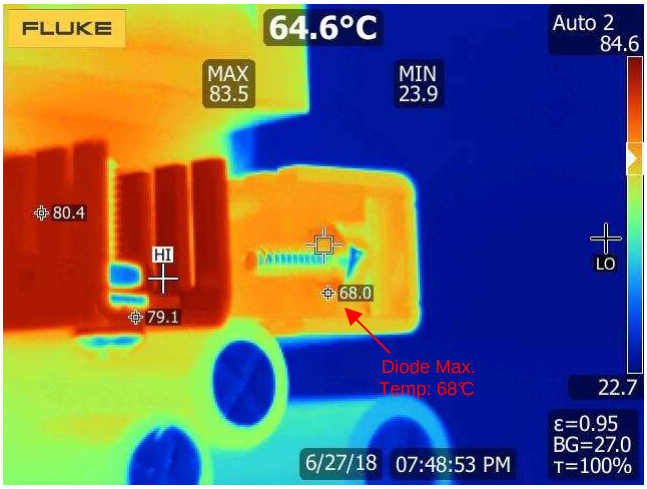


図 **61. 24-V Secondary Diode**

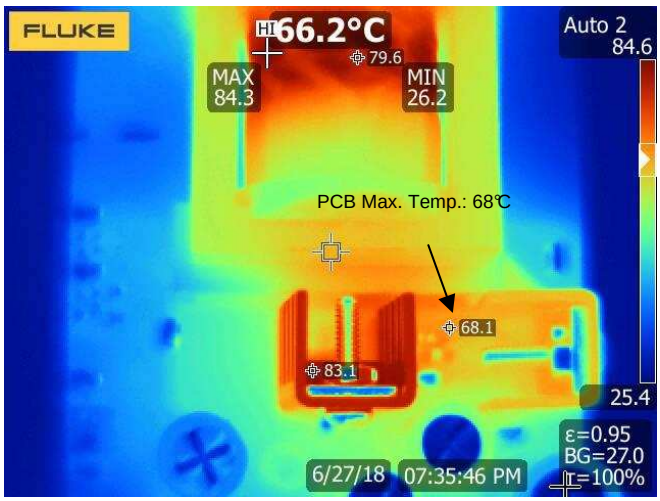


図 **62. Secondary Side**

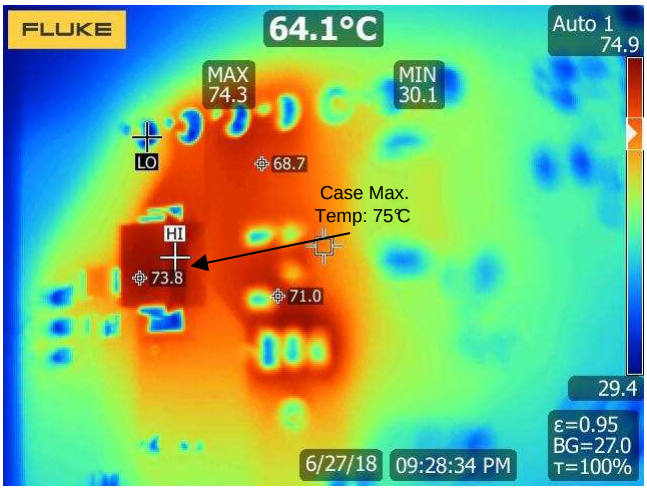


図 **63. 15-V Secondary Diode**

The thermal limits and margins of the key components are summarized in 表 4. From 表 4, it is clearly seen that operation at 85°C ambient is not advisable due to low temperature margin available for 5-V secondary diode, transformer winding insulation and PCB. Given the temperature rise at 25°C, it is seen that the safe maximum ambient temperature for full-load (50 W) operation is 70°C.

表 4. Thermal Analysis Summary

COMPONENT	MAXIMUM TEMPERATURE AT 25°C	MAXIMUM ALLOWABLE TEMPERATURE	MAXIMUM PROJECTED TEMPERATURE AT 85°C	MARGIN AT 85°C AMBIENT	MAXIMUM PROJECTED TEMPERATURE AT 70°C	MARGIN AT 70°C AMBIENT
Primary MOSFET	63	150	123	27	108	42
Snubber diode	74	175	134	41	119	56
Transformer winding	87	155 (Class F ins.)	147	8	132	23
Transformer core	70	150	130	20	115	35
5-V Sec. diode	86	150	146	4	131	19
24-V Sec. diode	68	150	128	22	113	37
15-V Sec. diode	75	175	135	40	120	55
PCB	68	130 (FR-4)	128	2	113	17

図 64 through 図 65 show the 5-V secondary diode, transformer winding insulation and PCB temperature when output power is 33 W at 25°C. It is seen that the temperature rise of 5-V secondary diode, transformer winding insulation and PCB are 40°C, 45°C, and 30°C respectively. The absolute temperatures of 5-V secondary diode, transformer winding insulation, and PCB projected in an ambient of 85°C are 125°C, 130°C, and 115°C, respectively - hence, the converter should be derated to 30 W at 85°C for safe operation.

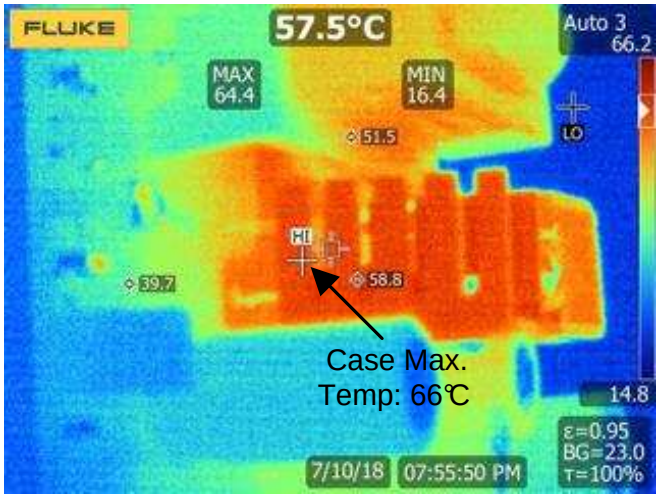


図 64. 5-V Secondary Diode

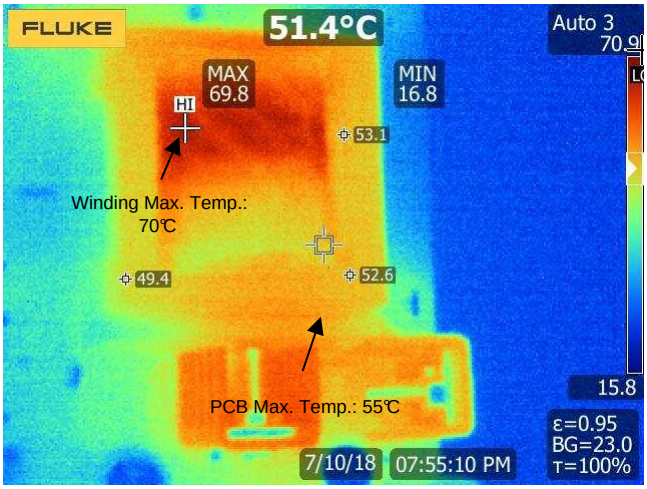


図 65. Secondary Side

3.2.3 Precautions During Testing

3.2.3.1 High Voltage (HV)

TIDA-010000 can work with a HV input of up to 1000 VDC. These HV sections are exposed to human contact and hence extreme care needs to be exercised while testing. The HV areas are marked in the PCB with the text "DANGER HIGH VOLTAGE" and following warning symbol (図 66) in yellow. The HV sections are also marked in 図 67 with a dotted red rectangle - users need to ensure proper HV safety precautions are observed before and while testing. All exposed terminals (high voltage or otherwise) should NOT be handled directly when power is turned on - all connections should be done only in powered down state.

図 66. High Voltage Warning

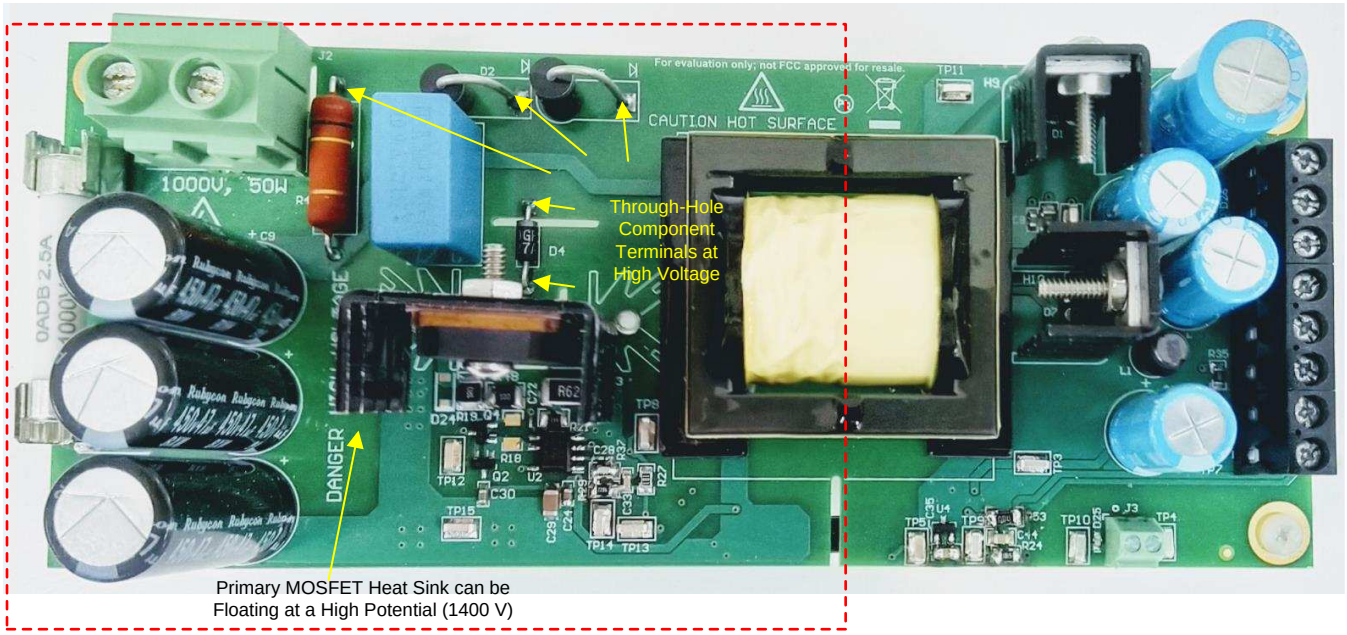


図 67. High Voltage Areas on TIDA-010000

3.2.3.2 High Temperature(HT)

During operation at room temperature (25°C), some components and parts of the PCB surface can reach high temperatures (up to 90°C). Some of these are marked in PCB with the text "CAUTION HOT SURFACE" and following warning symbol (図 68). The high temperature areas are also marked in 図 69 within the red dotted rectangle.

WARNING

Exercise adequate caution during and after testing to avoid burns and other risks linked to high temperature. Also, remember that the components and PCB surface can take a long time (approximately 30 minutes) to cool down to room temperature after shutting down power.

See 図 57 through 図 65 in 3.2.2.9 for detailed information on maximum temperature of critical components and PCB surface.

図 68. High Temperature Warning

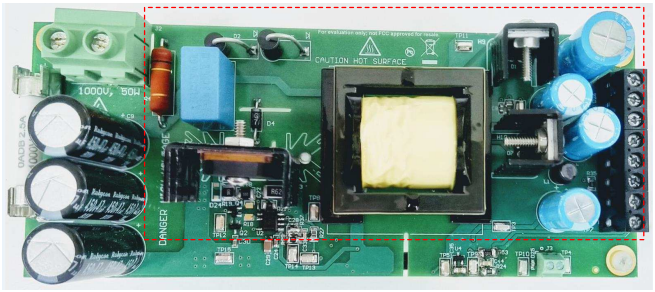


図 69. High Temperature Areas on TIDA-010000

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010000.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010000.

4.3 PCB Layout Recommendations

For PCB layout recommendations related to the UCC28740 device, see 図 70 and 図 71.

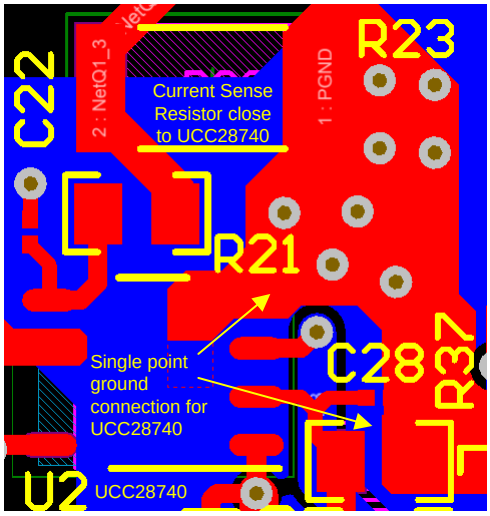


図 70. UCC28740 Current Sense and GND

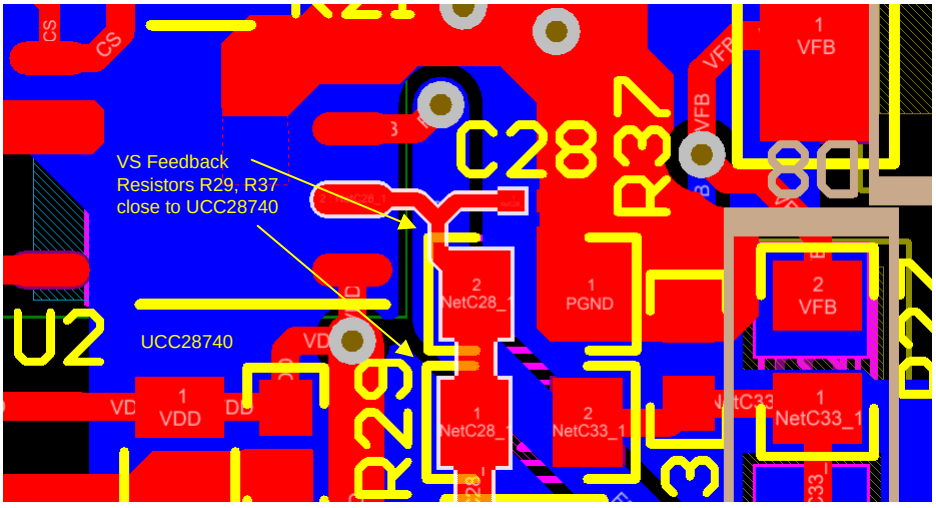


図 71. VS Feedback Resistors

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010000.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010000.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010000.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010000.

5 Related Documentation

1. Texas Instruments, *UCC28740 Constant-Voltage Constant-Current Flyback Controller Using Optocoupled Feedback Data Sheet*
2. Texas Instruments, *UCC28740 Design Calculator*

5.1 商標

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年9月発行のものから更新 **Page**

- ブロック図で、DC入力を「290～100V」から「290～1000V」に 変更 1
- DC input from '290 - 100 V' to '290 - 1000 V' in the block diagram. 変更 4

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