参考資料

TI Designs: TIDA-060002
大きな容量性負荷のアプリケーションのための100MHz、1A出力電流ドライバのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このTI Designは、THS3491高速高電圧電流帰還アンプを使用して、20V_{PP}で100MHzの大信号帯域幅を維持しながら、小さな抵抗性または大きな容量性負荷に1Aを超える出力電流を供給する駆動能力を紹介します。2つ以上のTHS3491アンプを負荷共有構成で使用することで、大きな出力電流駆動を達成し、大信号帯域幅と歪み性能を最適化します。

THS3491デバイスは、900MHzの帯域幅と、±420mAの線形出力電流駆動能力を持つため、大きな容量性負荷のアプリケーションを可能にします。このデザインでは、最良の大信号帯域幅、小さな歪み、最良の熱特性を得るため、VQFN-16 (RGT)パッケージを使用します。

リソース

TIDA-060002	デザイン・フォルダ
THS3491	プロダクト・フォルダ

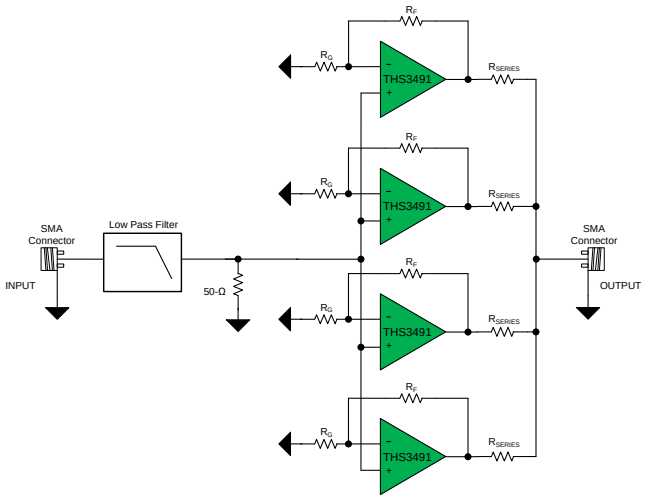
TI E2E™ Community　E2E™ エキスパートに質問

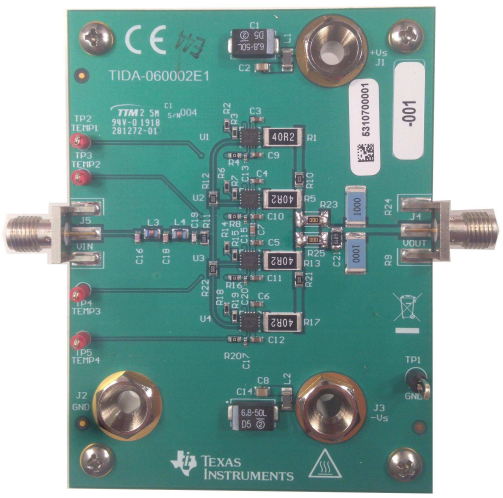
特長

- 出力電流駆動 ≥ 1A
- 大きな容量性負荷の駆動:100pF～1000pF
- 大信号帯域幅:> 100MHz
- 20V_{PP}の出力電圧スイング(100MHz、R_L = 20Ω時)
- 20V_{PP}の出力電圧スイング(30MHz、C_L = 1nF時)
- 出力電流駆動の柔軟性(2、3、4個の並列アンプ)
- 複数のサブシステムに対応するスケーラブルな小型フォーム・ファクタ

アプリケーション

- 任意波形の生成器
- 半導体試験用機器
- バッテリ・テスタ
- LCDおよびLEDテスタ
- LCRメータの電力出力ドライバ
- 大容量性負荷ピエゾ素子ドライバ
- パワーFETドライバ
- レーザー・ドライバ
- ラボ計測機器





1 System Description

This design guide describes a building block design involving the use of two to four THS3491 current-feedback amplifiers in a load-sharing configuration when driving a low-resistive or high-capacitive load (approximately 100 pF to 1000 pF) for a 1-A output current drive capability. 図 1 shows a sub-system where such a building block can be used to drive high input capacitance power field-effect transistors (FETs). High output current drive is important for applications such as power field-effect transistors (FETs), LCD and LED testers, or semiconductor test equipment where the capacitive load can range from 100 pF to 1000 pF (and sometimes even higher). For driving a 1000-pF capacitive load with 5-Ω series resistance isolation, the design delivers a 20-V_{PP} output voltage swing up to a 30-MHz signal frequency. (The signal frequency is limited by the bandwidth roll-off of the RC circuit.) In addition, a large-signal bandwidth of 100 MHz at 20 V_{PP} is achieved when driving a purely resistive load of 20 Ω.

High-frequency and large-signal applications typically require high slew rate amplifiers for minimal distortion of the high-frequency sinusoidal signal. Operating on a wide supply voltage range from ±7 V to ±15 V, the THS3491 can deliver a 20-V_{PP} output swing at 100 MHz (R_L = 100 Ω) resulting in an 8000-V/µs slew rate performance. In-addition, the ±420 mA of linear output current drive makes the THS3491 amplifier an ideal candidate for low-resistive or high-capacitive load applications.

In the design, each of the load-sharing THS3491 amplifiers are configured in a noninverting voltage gain (G) of 5 V/V with a feedback resistor value (R_F) of 576 Ω. The input is matched for a 50-Ω source impedance and includes a fifth-order Bessel topology passive low-pass filter with a –3-dB cutoff bandwidth of 150 MHz. Using a Bessel filter topology maintains the group delay of the adjacent frequencies, which is ideal for maintaining the pulse response shape in applications such as arbitrary waveform generators (AWGs) or high voltage clock drivers.

The design uses the VQFN-16 (RGT) package to attain the best large-signal bandwidth, distortion, and thermal performance possible. Operating supply voltage ranges from ±7 V to ±15 V depending upon the desired output voltage swing, and consumes a quiescent current of less than 70 mA when all four amplifiers are turned on.

1.1 Key System Specifications

表 1 lists key specifications for this design.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Supply voltage	±7 V to ±15 V	See the THS3491 data sheet
Output load type	1000-pF capacitive load	See 図 53
Target bandwidth (BW)	f = 100 MHz at 20 V_{PP}, minimum R_L = 20 Ω	See 図 29
	f = 30 MHz at 20 V_{PP}, R_S = 5 Ω, C_L = 1000 pF	See 図 53
HD2, HD3	< –30 dBc at 100 MHz for 20 V_{PP} and R_L = 20 Ω	See 図 26 and 図 27
Steady-state or quiescent current consumption	< 70 mA for four parallel amplifiers on a ±15-V supply	See the THS3491 data sheet
Maximum operating temperature	Maximum operating temperature dependent upon the internal device power dissipation to limit $T_{J(MAX)}$< 150°C	See 2.3.4
Form factor	85 mm × 48 mm	See fab drawings

2 System Overview

2.1 Block Diagram

図 1 shows the system-level block diagram of the TIDA-060002 that can be used with a digital-to-analog converter (DAC) interface at the input and drives high input capacitance power FETs at the output.

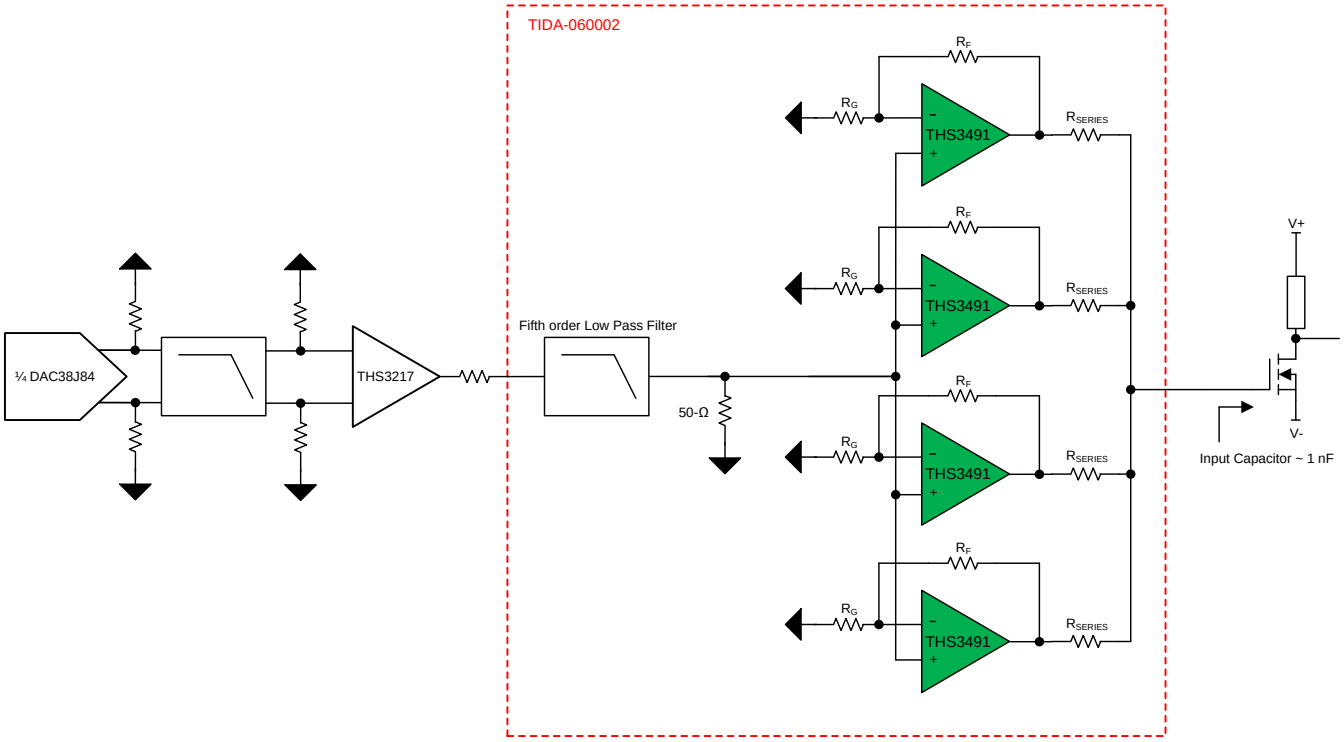


図 1. TIDA-060002 Block Diagram

2.2 Highlighted Products

2.2.1 THS3491 Current Feedback Amplifier Specifications

- Bandwidth:
  - 900 MHz (V_O = 2 V_{PP}, A_V = 5 V/V)
  - 320 MHz (V_O = 10 V_{PP}, A_V = 5 V/V)
- Slew Rate: 8000 V/µs (V_O = 20 V_{PP})
- Input Voltage Noise: 1.7 nV/√Hz
- Bipolar Supply Range: ±7 V to ±16 V
- Single Supply Range: 14 V to 32 V
- Output Swing: 28 V_{PP} (±16-V Supplies, 100-Ω Load)
- Linear Output Current: ±420 mA (Typical)
- 16.8-mA Trimmed Supply Current (Low Temperature Coefficient)
- HD2, HD3: Less than –75 dBc (50 MHz, V_O = 10 V_{PP}, 100-Ω Load)
- Rise and Fall Time: 1.3 ns (10-V Step)

- Overshoot: 1.5% (10-V Step, A_V = 5 V/V)
- Current Limit and Thermal Shutdown Protection
- Power-Down Feature

2.3 System Design Theory

2.3.1 Theory of Operation

This section discusses the various elements for operating this system design.

2.3.1.1 Concept of Load-Sharing Configuration

The design involves the use of two to four THS3491 current-feedback amplifiers in a load-sharing configuration, as shown in 図 2, when driving a low-resistive or high-capacitive load (approximately 100 pF to 1000 pF). The concept of load sharing involves multiple parallel amplifiers driving a shared output load, where each amplifier is driven by the same source. Driving a shared output load with multiple parallel amplifiers effectively reduces the output current requirement of each amplifier by 1 / N, where *N* is the number of parallel amplifiers.

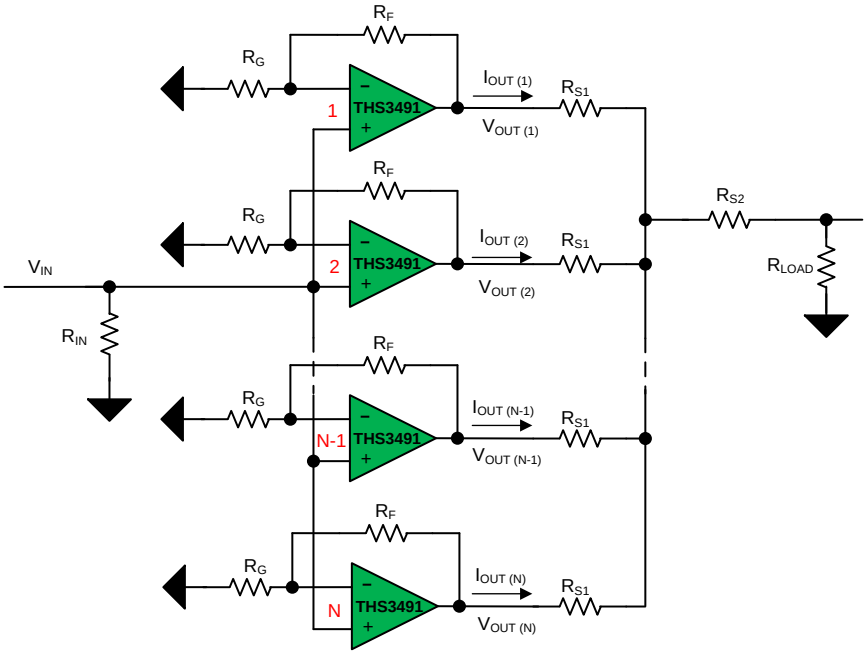


図 2. N THS3491 Amplifiers in a Load-Sharing Configuration

In a load-sharing configuration, each amplifier in parallel must be set to the same gain. This configuration results in the output of each parallel amplifier to be at the same voltage when driven from the same input source (V_{IN}) and avoids any push or pull output current among the amplifiers. The design is tested with each THS3491 amplifier in a noninverting voltage gain (G) of 5 V/V, with a feedback resistor (R_F) of 576 Ω. The current feedback architecture of the THS3491 allows it to be configured in different gains while simultaneously keeping the closed loop bandwidth constant. (see the *OA-13 Current Feedback Loop Gain Analysis and Performance Enhancement* application report for additional details).

2.3.1.2 Input and Output Interface

The design input includes a 5th-order Bessel topology passive low-pass filter with a 150-MHz cutoff frequency to filter out unwanted input signal harmonics, and is matched for a 50-Ω source impedance. Series isolation resistors (R_{SERIES}) help isolate the large capacitive load from the individual THS3491 amplifier outputs; see 図 1. These series isolation resistors help stabilize the amplifier outputs and prevent them from shorting to each other. The R_{SERIES} resistors can be split into R_{S1} and R_{S2}, as shown in 図 2, for better output matching and distortion performance at the cost of increased push or pull output current mismatch among the amplifiers.

2.3.1.3 Slew Rate and Maximum Output Current Calculation

The supply voltage range, output voltage swing, and output current drive capability of an amplifier are important device parameters to consider when driving low-resistive or high-capacitive loads. For the THS3491 with a class AB style output, there are two ways in which the device output signal shows increased distortion when achieving high voltage swing at high frequency. Increased distortion occurs when:

1. The amplifier output reaches the supply headroom for the maximum output swing while driving a lighter resistive load of greater than 200 Ω
2. The amplifier output reaches the maximum output current limit while driving a low resistive load of less than 50 Ω, or a capacitive load of greater than 100 pF

The primary focus of this design is to address the second scenario using the load-sharing concept.

For driving a low-resistive load at a high-voltage swing, an amplifier begins to show increased distortion because of slew-rate limitations where the amplifier is unable to source or sink the required output current at high frequencies. The slew rate limitation can be understood by slightly modifying the slew rate equation for large-signal bandwidth, as shown in 式 1, in terms of peak output current (I_P). To maintain constant slew rate with a decrease in R_L, the peak linear output current (I_P) must increase for a given peak output voltage (V_P). Depending upon the R_L, sometimes this linear output current requirement can be quite significant, which automatically places severe constraints on the output current drive capability of an amplifier and limits high-frequency operation.

$$\text{Slew Rate} = \sqrt{2}\pi f_{3dB} V_P = \sqrt{2}\pi f_{3dB} I_P R_L \quad (1)$$

where:

- f_{3dB} = –3-dB bandwidth of the amplifier for a given peak output voltage (V_P)
- I_P = Peak linear output current
- R_L = Total resistive load at the amplifier output

For capacitive loads, the effect of reduced linear output current is even more pronounced because of decreasing impedance with frequency increase. Driving a large-signal swing into a capacitive load requires fast charging and discharging of the capacitor, which again is tied to the slew rate of an amplifier for distortion performance. As a rule of thumb, the amplifier slew rate is recommended to be at least 5 to 10 times the slew rate requirement at the frequency of interest to achieve greater than –50-dBc distortion performance. At a minimum, the amplifier slew rate must meet the requirement shown in 式 2 for a capacitive load drive.

$$\text{Slew Rate} \left(\frac{dV_{OUT}}{dT} \right) \geq \frac{I_{OUT}}{C_{LOAD}} \quad (2)$$

where:

- I_{OUT} = Output current to generate the required output voltage
- C_{LOAD} = Capacitive load at the amplifier output

In both a low-resistive or high-capacitive load drive, the maximum output current drive of an amplifier is usually limited by the maximum current density in the output transistors in order to not exceed the maximum junction temperature or $T_{J(MAX)}$ of 150°C. In such situations, the output load-sharing concept becomes useful in boosting the total available output current and overcoming the current-drive limitation from a single amplifier.

For example, take a scenario of 20 V_{PP} or ±10-V output swing drive into a 1000-pF capacitive load with a 5-Ω series isolation resistance (R_{SERIES}). The –3-dB cutoff bandwidth of the RC circuit is approximately 30 MHz. 式 3 describes that the total impedance (or $|Z_L|$) detected by the amplifier output at 30 MHz is approximately 7.28-Ω. This calculation results in a ±1.372-A output current drive at a ±10-V output swing at the amplifier.

$$I_{OUT} = \frac{V_{OUT}}{|Z_L|}$$

$$\text{Where, } |Z_L| = \sqrt{|R_{SERIES}|^2 + |X_C|^2} \text{ and } X_C = -j\frac{1}{2\pi f C_L}$$

- I_{OUT} = Required linear output current
- V_{OUT} = Required output voltage
- $|Z_L|$ = Total output impedance

(3)

The minimum slew rate required in this case is 1372 V/µs from 式 2. The THS3491 amplifier slew rate is 8000 V/µs for a 20-V_{PP} output (derived from the large-signal BW), which is sufficient for driving the 1-nF capacitive load. However, the linear output current is limited to ±420 mA. The solution is by using four parallel THS3491 devices in a load-sharing configuration, which results in only ±343 mA from each amplifier for a total output current of ±1.372 A (see 図 53).

The concept of a load-sharing configuration using THS3491 amplifiers requires paying careful attention to stability and the possibility of increased output push or pull current mismatch. In addition, power dissipation and thermal performance are key factors to consider for the design. All these factors will eventually determine the maximum number of parallel amplifiers that can be added, and are discussed in detail further in this document.

2.3.2 Stability Considerations

2.3.2.1 Inclusion of Series Isolation Resistance (R_{SERIES})

For an amplifier directly driving a capacitive load, the amplifier is prone to oscillations as a result of the additional phase shift introduced in the loop-gain expression by the amplifier open-loop output impedance and the capacitive load. For a current-feedback amplifier such as the THS3491, the open-loop output impedance and the capacitive load introduce a pole in the open-loop transimpedance gain response. If the pole is at a frequency lower than the non-dominant pole of the amplifier, then the transimpedance loop-gain is reduced and the phase margin is reduced. To counteract the effect of this pole, a series isolation resistor (R_{SERIES}) is used between the device output and the capacitive load that introduces a zero in the response. TI recommends placing R_{SERIES} close to the device output to avoid the printed circuit board (PCB) trace parasitic affecting the frequency response of the amplifier.

Depending upon the capacitive load, and as shown in 図 3, R_{SERIES} must be adjusted for a flat frequency response. The R_{SERIES} values in 図 3 are applicable for a single THS3491 amplifier and can be extended to N parallel amplifiers in a load-sharing configuration by making the series isolation resistance equal to N × R_{SERIES}. The inclusion of R_{SERIES} can result in an increased voltage drop across the series resistor at higher output currents and limits the available output voltage swing at the capacitive load. However, when selecting the series isolation resistance, stability must be of greater concern than output voltage drop.

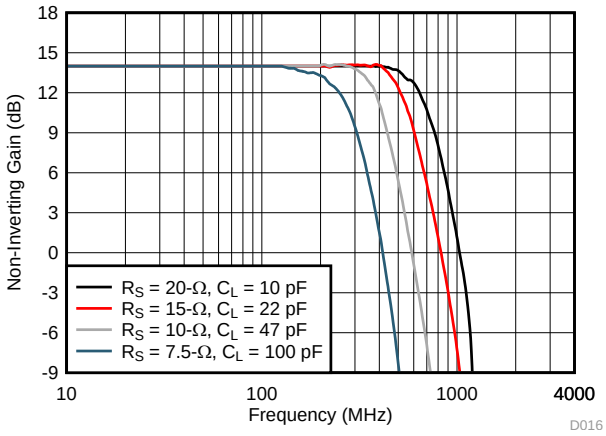


図 3. Flat Frequency Response Using Different R_S for a Given C_L (Single THS3491)

2.3.2.2 *Input Transmission Line Effects and Inclusion of De-Q Resistance (R_{DE_Q})*

In a load-sharing configuration for high-frequency amplifiers, a long transmission line can be developed when connecting multiple parallel device inputs. As shown in 図 4, a long transmission line can develop parasitic capacitance (C_{TX_LINE}) at the noninverting input of an amplifier. Additionally, not having a termination resistor to GND close to the device inputs results in the long transmission line behaving like a stub, which is very susceptible to high-frequency coupling. In an actual PCB layout, this stub on the noninverting input can be very close to the inverting input of the device, resulting in a parasitic coupling capacitor (C_{IN_PAR}).

For a high-frequency, current-feedback amplifier such as the THS3491, the output impedance of the internal unity-gain buffer at the inverting input becomes increasingly inductive at high frequency. When there are multiple parallel amplifiers with no shunt termination to GND (such as 50 Ω) close to the noninverting input, a parasitic LC oscillator circuit can develop because of the high-frequency inductance of the inverting input and the parasitic capacitance (C_{TX_LINE}) of the long transmission line at the noninverting input. Adding a small input series resistor (R_{DE_Q}) ranging from 30 Ω to 50 Ω helps eliminate this high-frequency oscillation caused by the parasitic coupling from the inverting to the noninverting device input.

The transmission line effect is usually not an issue for two parallel amplifiers where the connection distance between the two inputs is short. However, when there are more than two amplifiers in a load-sharing configuration, the length of the parallel input connection and the proximity of the input termination certainly play a role in the stability of the circuit for high-voltage, high-frequency operation.

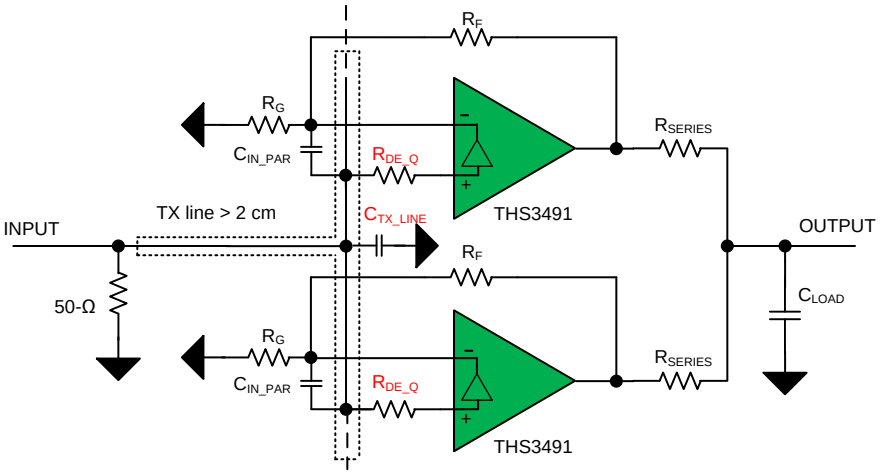


図 4. Input Series Resistor (R_{DE_Q}) for Eliminating High-Frequency Oscillation

2.3.3 Output DC Offset Voltage Induced Output Current Mismatch Considerations

The goal of the load-sharing concept is to reduce the current load of each amplifier by equally distributing the total current load among all amplifiers. No single amplifier can source or sink the majority of the load current. Without these two prerequisites, load sharing cannot occur. Although this concept reduces the output current requirement for a given amplifier, it is required for all amplifiers to output the same voltage swing.

In reality, mismatched output voltages can result in imbalanced load currents and one possible source of mismatch is output-referred offset voltage. 式 4 calculates the worst-case offset voltage.

$$\left|V_{OS\,RTO}\right| = \left|V_{OS\,RTI}\right| \times \left(1 + \frac{R_F}{R_G}\right) + \left|I_{B+}\right| \times \left(R_{IN} \| R_S\right) \times \left(1 + \frac{R_F}{R_G}\right) + \left|I_{B-}\right| \times R_F \quad (4)$$

where:

- V_{OS_RTO} = Output-referred offset voltage
- V_{OS_RTI} = Input-referred offset voltage
- I_{B+} = Noninverting input bias current
- I_{B-} = Inverting input bias current
- R_{IN} = Equivalent termination resistance at the noninverting input
- R_{SOURCE} = Source resistance

表 2 lists the maximum input-referred offset voltage (V_{OS_RTI}), maximum noninverting (I_{B+}), and inverting (I_{B-}) input bias currents from the THS3491 data sheet. Assuming the noise gain (or 1 + R_F / R_G) equals 5 V/V for R_F = 576 Ω and R_G = 144 Ω and assuming the equivalent series resistance of R_{IN} || R_S = 25 Ω, then 式 4 calculates the worst-case output offset voltage as ±22.5 mV.

表 2. THS3491 Device Parameters

PARAMETER		VALUE	UNIT
V_{OS_RTI}	Maximum input-referred offset voltage	±2	mV
I_{B+}	Maximum noninverting bias current	±7	µA
I_{B-}	Maximum inverting bias current	±20	µA

2.3.3.1 Output Mismatch Current Calculation for Two Load-Sharing Amplifiers

For calculating the output current mismatch, as shown in 図 5, first consider a case of two THS3491 amplifiers in a load-sharing configuration where the input is at 0 V. Resulting from the non-ideal input offset and bias currents of the amplifiers, the outputs of the amplifier are not centered at 0 V. In the worst-case situation, one amplifier output (say amplifier 1) can be at 22.5-mV offset voltage and the other (amplifier 2) at –22.5-mV offset voltage, respectively. Assuming perfectly matched series output resistors (R_{SERIES}) are used, the voltage at the capacitive load (V_{OUT}) is 0 V.

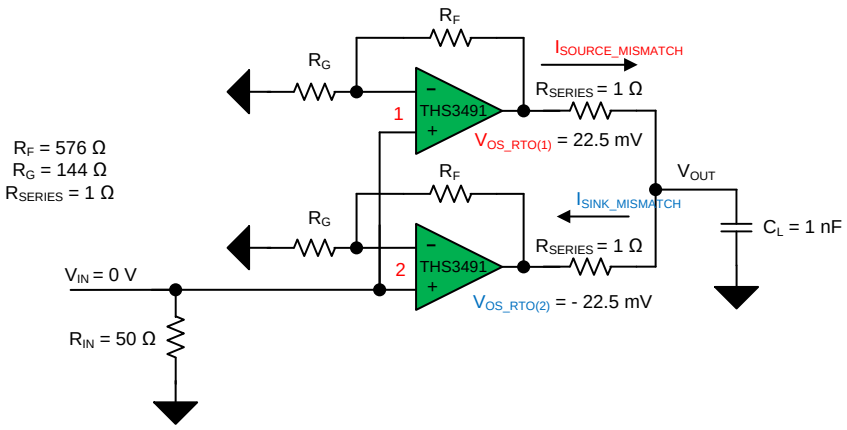


図 5. Output Current Mismatch for Two Load-Sharing Amplifiers

Solving by the Kirchoff's current law (KCL) equation, the resulting mismatch current of the positive output offset voltage from amplifier 1 is calculated as in 式 5, which is a source mismatch current ($I_{SOURCE\_MISMATCH}$) and equals 11.25 mA. The resulting mismatch current of the negative output offset voltage from amplifier 2 is essentially the negative of the source mismatch current as in 式 6, which is the sink mismatch current ($I_{SINK\_MISMATCH}$) and equals –11.25 mA.

$$I_{SOURCE\,MISMATCH\,(1)} = \frac{\left|V_{OS\,RTO\,(1)}\right| + \left|V_{OS\,RTO\,(2)}\right|}{2R_{SERIES}} \quad (5)$$

$$I_{SOURCE\,MISMATCH\,(2)} = -I_{SOURCE\,MISMATCH\,(1)} \quad (6)$$

Amplifier 1 with a positive output offset sources current into the output of amplifier 2, which has a negative output offset without generating any signal on the load. This behavior is not preferable. Such a situation dissipates unnecessary power, and can affect long-term reliability of the amplifiers.

In practice, avoiding offset voltage effects can be difficult, especially when the DC path is desired along with high-frequency performance. A simple solution, as indicated in 式 5, is to limit the output source or sink current mismatch by increasing the series resistor (R_{SERIES}).

2.3.3.2 Output Mismatch Current Calculation for N Load-Sharing Amplifiers

The source or sink mismatch current calculation for two parallel amplifiers can be extended to N parallel amplifiers, as shown in 図 6, in a load-sharing configuration. For N parallel amplifiers, the worst-case *source* output current mismatch occurs when only one amplifier has the maximum positive offset voltage and the remaining N-1 amplifiers have the maximum negative offset voltage. On the other hand, the worst-case *sink* output current mismatch occurs when only one amplifier has the maximum negative offset voltage and the remaining N-1 amplifiers have the maximum positive offset voltage.

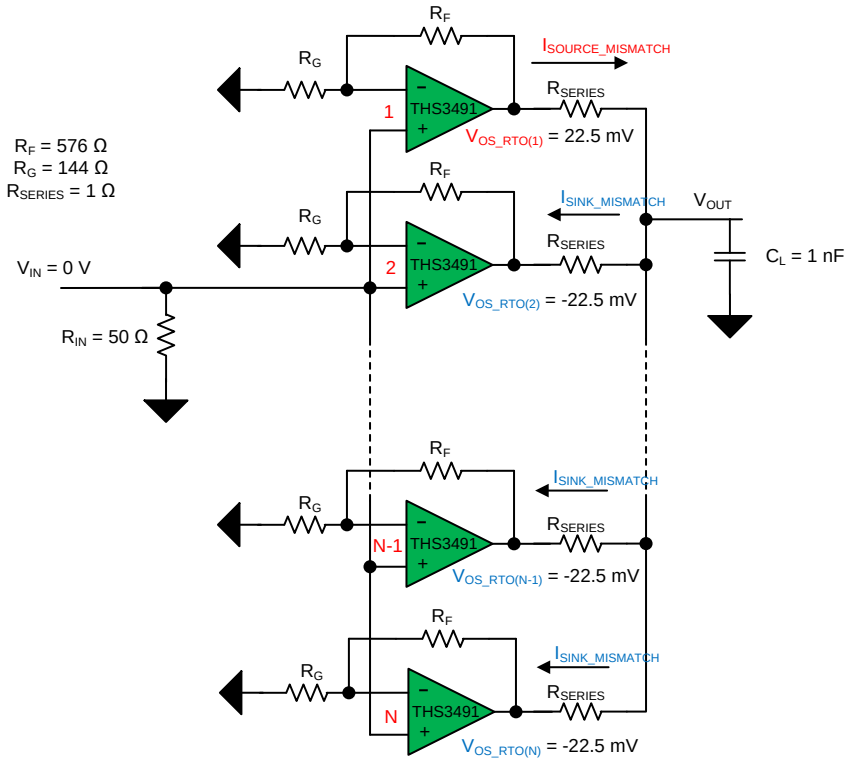


図 6. Output Current Mismatch for *N* Load-Sharing Amplifiers

The source and sink mismatch current for the N parallel amplifier scenario can be calculated as in 式 7 and 式 8, respectively. Similar to the two parallel amplifier scenario, the source mismatch current ($I_{SOURCE\_MISMATCH\ (1)}$) is the additional current that the positive offset amplifier (amplifier 1) must source to maintain the output voltage (V_{OUT}) at the load. On the other hand, the sink mismatch current ($I_{SINK\_MISMATCH\ (j)}$) is the additional current that each of the remaining (N-1) negative offset amplifiers must sink to maintain the output voltage (V_{OUT}) at the load.

式 7 and 式 8 are derived for worst-case source output current mismatch when only one amplifier has the maximum positive offset voltage and the remaining N-1 amplifiers have the maximum negative offset voltage. For calculating the worst-case sink output current mismatch for a single amplifier with maximum negative offset voltage, these equations can simply be swapped with respect to each other where the term source is replaced by sink.

$$I_{SOURCE\,MISMATCH\,(1)} = \frac{1}{R_{SERIES}} \times \left(\left| V_{OS\,RTO(1)} \right| + \frac{(N-2)}{N} \times \left| V_{OS\,RTO(j)} \right| \right) \quad (7)$$

where:

- $I_{SOURCE\_MISMATCH\ (1)}$ = The worst-case source mismatch current for amplifier 1
- $V_{OS\_RTO(1)}$ = The maximum positive offset voltage for amplifier 1
- $V_{OS\_RTO(j)} = -V_{OS\_RTO(1)}$ and is the maximum negative offset voltage for the rest of the (N-1) amplifiers, assuming they all generate the same offset voltage
- j = An integer from either 2 to N

$$I_{SOURCE\,MISMATCH\,(j)} = \frac{1}{(N-1)} \times I_{SOURCE\,MISMATCH\,(1)}$$

where:

- $I_{SINK\_MISMATCH\ (j)}$ = The worst-case sink mismatch current for each of the remaining (N-1) amplifiers (8)

To illustrate the output current mismatch problem in N parallel amplifiers, consider an example with four THS3491 amplifiers in a load-sharing configuration (as shown in 図 7) and assuming an R_{SERIES} of 2 Ω. Assuming that none of the amplifiers generate an output-referred offset voltage, let us consider the nominal output of each THS3491 amplifier is 5 V. In this scenario, the nominal output current of each THS3491 amplifier in a load-sharing configuration is 24.75 mA as 式 9 describes using the KCL equation.

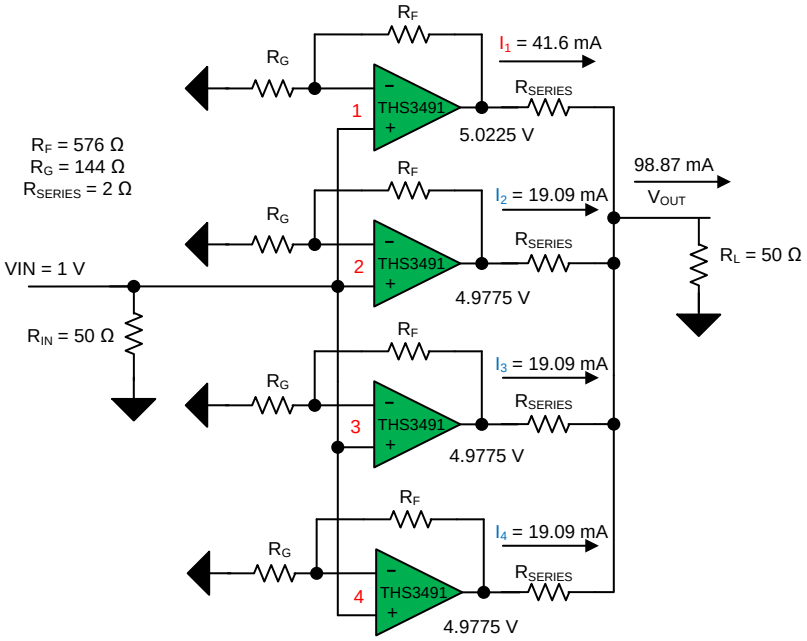


図 7. Example Output Current Mismatch Resulting From Output Offset Voltage

$$I_{OUT} = \frac{1}{(N \times R_L + R_{SERIES})} \times V_{OUT} = 24.75\ mA$$

where:

- I_{OUT} = Output current of each amplifier without accounting for any output-referred offset voltage (9)

Using the KCL equation for the circuit in 図 7 and taking offset voltage into consideration, the output current for the positive offset voltage amplifier of 5 V + 22.5 mV is calculated as 41.6 mA. The output current for the remaining three amplifiers with a worst-case negative offset voltage of 5 V – 22.5 mV is calculated as 19.09 mA. As expected, amplifier 1 with the positive offset voltage supplies 16.8 mA more output current than the nominal output current of 24.75 mA. The remaining three amplifiers sink an additional 5.61 mA output current each. Thus, amplifier 1 must dissipate more heat because of the additional current and is prone to long-term reliability issues. Also, because of the higher output current in amplifier 1, the harmonic distortion from amplifier 1 increases for a sinusoidal output signal.

Now, calculating for the worst-case output current mismatch using 式 7 and 式 8 for only THS3491 amplifier 1 at a 22.5-mV offset and the other three THS3491 amplifiers at a –22.5-mV offset results in the source and sink current mismatch to be at 16.84 mA and –5.61 mA, respectively. This calculation shows that 式 7 and 式 8 provide an easy way of calculating the same mismatch currents without having to delve into the cumbersome KCL equations.

The mismatch in amplifier currents can be plotted against the series resistor (R_{SERIES}). However, this document does not plot this graph because each application is specific and must be plotted individually.

2.3.4 Power Dissipation

The THS3491 is designed for high-speed, high output power applications that require paying special attention to the thermal considerations when designing the PCB. The amplifier includes automatic thermal shutdown protection circuitry that shuts down the device when the internal junction temperature (T_J) exceeds approximately 160°C, and turns on the device when the device cools down to approximately 145°C. When delivering high output power into capacitive loads, the internal junction temperature (T_J) can exceed the 160°C limit because of internal power dissipation, resulting in thermal shutdown of the device. The occasional $T_{J(MAX)}$ operation of 160°C is allowed. However, for long-term reliability of the device, TI recommends keeping the maximum internal device junction temperature (T_J) below 150°C. Any increase in the device junction temperature is the result of an increased internal power dissipation for a given ambient temperature (T_A). As a result, the internal power dissipation must be limited to prevent the amplifier from continuously running into thermal shutdown.

The following subsections discuss internal amplifier power dissipation (both DC and AC) for a purely resistive output load, as well as the average power dissipation for a simple RC output load.

2.3.4.1 Internal Amplifier Power Dissipation for a Purely Resistive Output Load: DC Power Dissipation

For symmetrical supplies where $V_{S+} = -V_{S-} = V_S$ and the load referenced to midsupply, 式 10 shows the internal power dissipation at DC ($P_{AMP(DC)}$) for a single amplifier.

$$P_{AMP(DC)}(W) = P_Q + P_{OUT(DC)}$$

where:

- P_Q(W) = Quiescent (no load) power dissipation
- $P_{OUT(DC)}$(W) = DC power dissipated in the output transistors (10)

The quiescent power dissipation (P_Q) shown in 式 11 is the internal amplifier power dissipation when the amplifier output is open or when there is no output current drive out of the amplifier.

$$P_Q(W) = (V_{S+} - V_{S-}) \times I_Q = 2V_S I_Q$$

where:

- $2\,V_S = (V_{S+}) - (V_{S-})$ = Total supply across the device
- I_Q = Total quiescent current drawn from the devices (11)

The THS3491 has a class AB output stage as shown in 図 8, where only one of the output transistors is turned on for high or low output voltage depending upon the source or sink current. 式 12 shows the DC power dissipated in the output transistors ($P_{OUT(DC)}$), which is essentially the voltage developed across the output transistor ($V_S - V_{OUT}$) multiplied by the output current drive (I_{OUT}).

$$P_{OUT(DC)}(W) = (V_S - V_{OUT}) \times I_{OUT} = \frac{1}{R_L}(V_S - V_{OUT}) \times V_{OUT}$$

where:

- V_{OUT} = Output voltage of the amplifier
- I_{OUT} = Output current drive of the amplifier

(12)

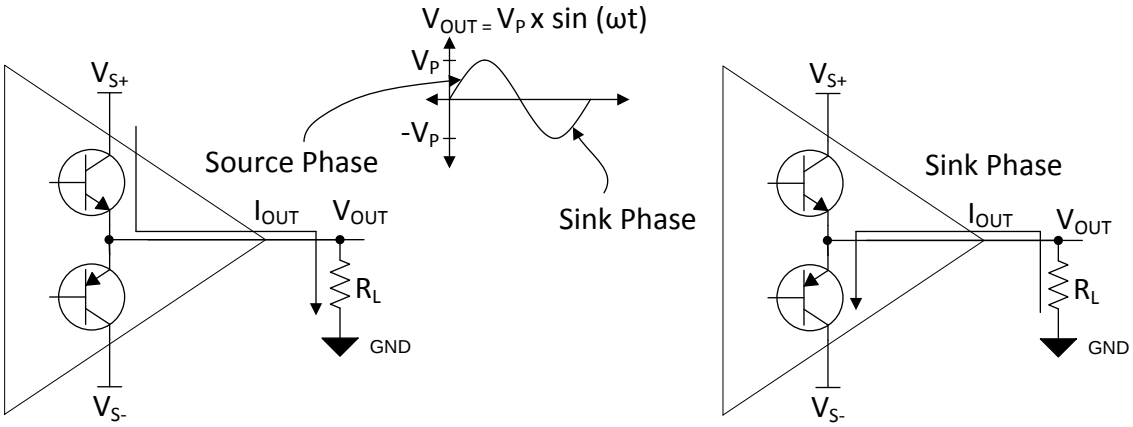


図 8. THS3491 Class AB Output Structure

Substituting 式 11 and 式 12 into 式 10 results in 式 13, which gives the total internal power dissipation at DC for a single amplifier.

$$P_{AMP(DC)}(W) = 2V_S I_Q + \frac{1}{R_L}(V_S - V_{OUT}) \times V_{OUT}$$

(13)

For N amplifiers in a load-sharing configuration driving a shared load (R_L), the output current (I_{OUT}) drive is shared between the amplifiers (or is divided by N) for the same output voltage (V_{OUT}). As a result, the power dissipation in output transistors (or $P_{OUT(DC)}$) is divided by N. 式 14 calculates the total internal power dissipation at DC for each of the N amplifiers in a load-sharing configuration. The quiescent power dissipation (or P_Q) stays the same because all amplifiers conduct the same quiescent current drawn from the shared power-supply voltage.

$$P_{AMP(DC)(j)}(W) = 2V_S I_Q + \frac{1}{N \times R_L}(V_S - V_{OUT}) \times V_{OUT}$$

where:

- j = Integer for either 1 to N parallel amplifiers in a load-sharing configuration

(14)

Using 式 14, the internal power dissipation can be plotted as illustrated in 図 9 across output voltage for each of the single to four parallel amplifiers. As you can see, the maximum internal power dissipation at DC occurs when $V_{OUT} = V_S / 2$. Substituting for $V_{OUT} = V_S / 2$ in 式 14 results in 式 15, which gives the maximum internal power dissipation at DC for each of the N parallel amplifiers.

$$P_{AMP(DC)(j)}(W)(max) = 2V_S I_Q + \frac{1}{4N \times R_L} V_S^2$$

(15)

For a single THS3491 amplifier on a symmetric dual supply of ±15 V and driving an R_L = 20 Ω, the maximum internal DC power dissipation is 3.33 W at V_{OUT} = 7.5 V. For two THS3491 amplifiers in a load-sharing configuration under similar conditions, the maximum internal DC power dissipation for each of the amplifier is 1.93 W at V_{OUT} = 7.5 V. As 図 9 shows, using N parallel amplifiers in a load-sharing configuration helps reduce the internal power dissipation (or $P_{OUT(DC)}$) burned in the output transistors because the output current is shared across all the amplifiers. However, the quiescent power dissipation (or P_Q) for each of the N parallel amplifiers stays the same at approximately 0.5 W.

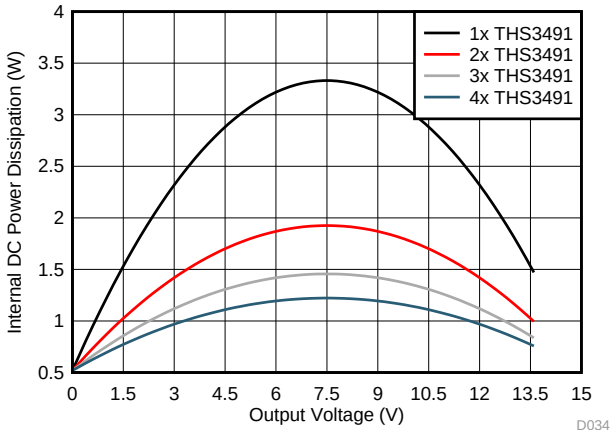


図 9. DC Power Dissipation per Amplifier vs Output Voltage

2.3.4.2 AC or Average Power Dissipation for a Sinusoidal Signal

For a continuous sinusoidal output signal driving a purely resistive load and referenced to midsupply, the internal average power dissipated ($P_{OUT(AVG)}$) in the output transistors is calculated as shown in 式 16 by integrating the sinusoid for half a cycle and taking an average. As illustrated in 図 8, only one of the output transistors is turned on for the high or low phase of the sinusoidal output voltage depending upon the source or sink phase.

$$P_{OUT(AVG)}(W) = \frac{1}{\pi R_L}\int_0^{\pi}(V_S - V_{OUT}) \times V_{OUT}\,d\omega t \tag{16}$$

式 17 is the result of solving the integral for half a cycle (0 to π) by substituting $V_{OUT} = V_P \times \sin(\omega t)$ for a sinusoidal output signal and dividing by π.

$$P_{OUT(AVG)}(W) = \frac{2}{\pi R_L}V_S V_P - \frac{1}{2R_L}V_P^2 \tag{17}$$

Thus, 式 18 calculates the total average (or AC) power dissipation for a single amplifier driving a sinusoid into a purely resistive load. The quiescent power dissipation (P_Q) in this scenario is still given by 式 11.

$$P_{AMP(AVG)}(W) = 2V_S I_Q + \frac{2}{\pi R_L}V_S V_P - \frac{1}{2R_L}V_P^2 \tag{18}$$

式 18 can be expanded to accommodate N parallel amplifiers in a load-sharing configuration driving a shared load (R_L). 式 19 calculates the resulting internal power dissipation for each of the N parallel amplifiers.

$$P_{AMP(AVG)(j)}(W) = 2V_S I_Q + \frac{1}{N} \times \left(\frac{2}{\pi R_L}V_S V_P - \frac{1}{2R_L}V_P^2\right) \tag{19}$$

図 10 shows a curve where the internal average power dissipation is plotted with respect to individual amplifiers from single to four amplifiers in a load-sharing configuration. The maximum internal average power dissipation occurs when $V_P = 2\ V_S / \pi$ by substituting for V_P in 式 19, with 式 20 being the result.

$$P_{AMP(AVG)(j)}(W)(max) = 2V_S I_Q + \frac{1}{N} \times \left(\frac{2}{\pi^2 R_L} \times V_S^2 \right) \quad (20)$$

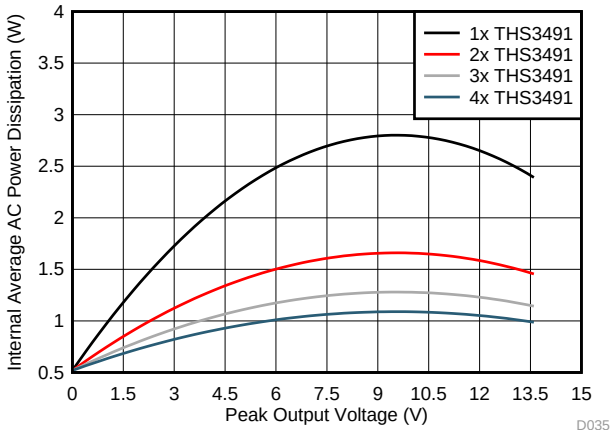


図 10. Average AC Power Dissipation per Amplifier vs Output Peak Voltage

For a single THS3491 amplifier on a symmetric dual supply of ±15 V and driving a continuous sinusoidal wave into an R_L = 20 Ω, the maximum internal average power dissipation is 2.8 W at V_P = 9.54 V. On the other hand, for two THS3491 amplifiers in a load-sharing configuration under similar conditions, the maximum internal average power dissipation for each amplifier is reduced to 1.66 W at V_P = 9.54 V, which improves thermal performance significantly. The quiescent power dissipation (or P_Q) for each of the N parallel amplifiers still stays the same at approximately 0.5 W.

2.3.4.3 Internal Average Power Dissipation for an RC Output Load

For a continuous sinusoidal wave driving an RC output load, the internal average power dissipation ($P_{OUT(AVG)}$) in the output transistors can be calculated as 式 21 shows by subtracting the average power delivered to the load from the average power provided by the supply. Again, the quiescent power dissipation (P_Q) in this scenario is still given by 式 11.

$$P_{OUT(AVG)}(W) = P_{SUPPLY(AC)} - P_{LOAD(AC)}$$

where:

- $P_{SUPPLY(AVG)}$ = Average input power from the supply while driving the RC load
- $P_{LOAD(AVG)}$ = Average output power delivered to the RC load (21)

図 11 shows the output structure for an RC load, and 式 22 gives the total reactive load (Z_L).

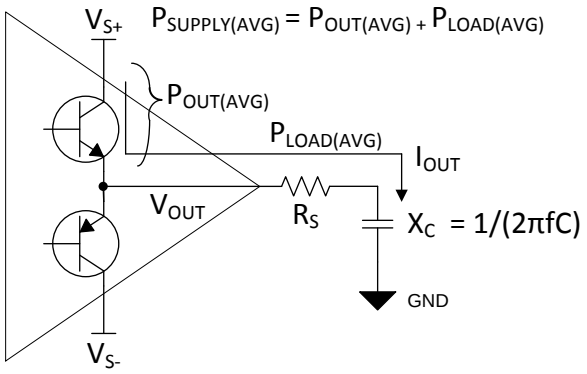


図 11. Output Structure for an RC Load (Source Phase)

$$Z_L = R_S + jX_C$$

$$\text{Where, } X_C = -j\frac{1}{2\pi f C_L}$$

- and R_S = Series isolation resistor (or interchangeably R_{SERIES}) (22)

式 23 shows the average input power provided by the supply while driving an RC load, when alternating current is drawn from the supply in both halves of the sinusoidal output cycle.

$$P_{SUPPLY(AC)}(W) = \frac{2}{\pi|Z_L|}V_S V_P$$

$$\text{Where, } |Z_L| = \sqrt{|R_S|^2 + |X_C|^2} \quad (23)$$

式 24 shows the average output power delivered to the RC load. The cos(φ) is the power factor and gives the phase difference between the output voltage and output load current. The power factor corrects for the phase relationship between the voltage and current for the average output power calculation in an RC load. For a purely resistive load, the power factor equals 1 indicating no phase difference between the voltage and currents.

$$P_{LOAD(AC)}(W) = \frac{1}{2|Z_L|}V_P^2\cos(\phi) = \frac{R_S}{2|Z_L|^2}V_P^2$$

$$\text{Where, } \cos(\phi) = \frac{R_S}{|Z_L|} = \text{power factor of the circuit} \quad (24)$$

As a result, 式 25 shows the internal average power dissipation in the output transistors for a single amplifier driving an RC load with a sinusoidal output.

$$P_{OUT(AVG)}(W) = \frac{2}{\pi|Z_L|}V_S V_P - \frac{R_S}{2|Z_L|^2}V_P^2 \quad (25)$$

By accounting for the quiescent power dissipation, 式 26 shows the total internal average power dissipation for a single amplifier driving an RC load.

$$P_{AMP(AVG)}(W) = 2V_S I_Q + \frac{2}{\pi|Z_L|}V_S V_P - \frac{R_S}{2|Z_L|^2}V_P^2 \quad (26)$$

For N parallel amplifiers in a load-sharing configuration, 式 27 shows the individual amplifier average power dissipation.

$$P_{AMP(AVG)(j)}(W) = 2V_S I_Q + \frac{1}{N} \times \left(\frac{2}{\pi |Z_L|} V_S V_P - \frac{R_S}{2|Z_L|^2} V_P^2 \right) \quad (27)$$

Graphs similar to 図 9 and 図 10 can be generated that show the internal power dissipation versus peak voltage for a shared RC load at a particular frequency. This graph however is not generated in this document and is left to the reader as an exercise.

2.3.5 Thermal Performance

The device package and the PCB material are responsible for thermal performance and conduction of heat out of the device die. The internal power dissipation of the device increases the internal die junction temperature, and the topic is extensively discussed in 2.3.4. When there is no heat sink on the bottom of the PCB and the free-air operating ambient temperature (T_A) is known, use 式 28 to calculate the maximum power dissipation permitted for a particular package. For the THS3491RGT package with a maximum T_J value of 150°C and θ_{JA} of 49.6°C/W, the maximum internal power dissipation is 2.52 W at a free-air operating ambient temperature (T_A) of 25°C.

$$P_{AMP}(W)(max) = \frac{\left(T_{J(max)} - T_A\right)}{\theta_{JA}} \quad (28)$$

where:

- $P_{D(MAX)}$ (W) = Maximum internal power dissipation of the amplifier
- $T_{J(MAX)}$ (°C) = Absolute maximum junction temperature
- T_A (°C) = Free-air operating ambient temperature
- θ_{JA} (°C/W) = Junction-to-ambient thermal resistance of the device package from the data sheet

For an RGT package with an exposed thermal pad, the heat sink at the PCB bottom plane allows the least resistive path for heat transfer compared with only the exposed pad soldered to the PCB and no heat sink attached. As a result, θ_{JA} or the junction-to-ambient thermal resistance reduces with heat sink. Because of the higher thermal handling capability, the inclusion of a heat sink at the bottom of the device allows for higher internal device power dissipation and subsequently allows for driving higher output current from the device.

For a heat sink design, 図 12 shows the various sources of thermal resistances. Because power dissipation causes a rise in junction temperature that is similar to the voltage drop across a resistor resulting from current flow, a simplified thermal model (see 図 13) can be developed that is analogous to an electrical circuit. The temperature, power dissipation, and thermal resistance are represented as voltage, current, and resistors, respectively. These parameters, as described in 式 29, allow the maximum internal power dissipation to be solved for by using a simple KCL equation.

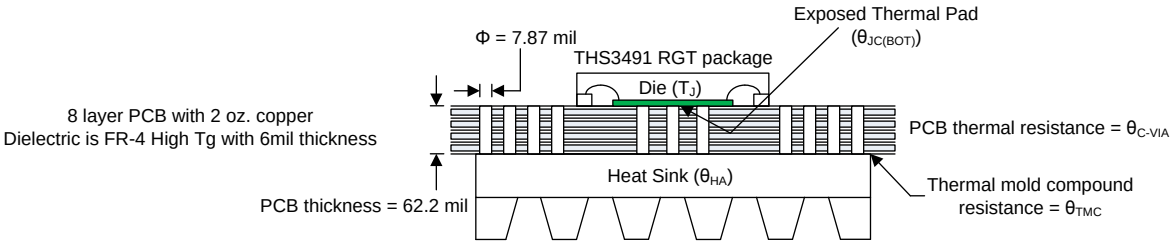


図 12. TIDA-060002 PCB Cross Section of Different Thermal Resistances

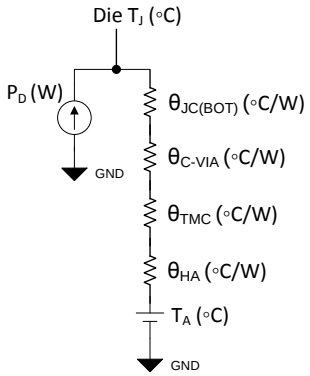


図 13. Simplified Thermal Model for Heat Sink Design

$$P_{AMP}(W)(max) = \frac{\left(T_{J(max)} - T_A\right)}{\left(\theta_{JC(BOT)} + \theta_{C-VIA} + \theta_{TMC} + \theta_{HA}\right)}$$

where:

- $P_{D(MAX)}$ (W) = Maximum internal power dissipation of the amplifier
- $T_{J(MAX)}$ (°C) = Absolute maximum junction temperature
- T_A (°C) = Free-air operating ambient temperature
- $\theta_{JC(BOT)}$ (°C/W) = Bottom junction-to-case thermal resistance of the device package from the data sheet
- θ_{C-VIA} (°C/W) = Case to via thermal resistance
- θ_{TMC} (°C/W) = Thermal mold compound resistance between the PCB and heat sink
- θ_{HA} (°C/W) = Heat sink to ambient thermal resistance (29)

To calculate the maximum power dissipation allowed for a heat sink design, each of the individual thermal resistance parameters in 式 29 must be known. For the TIDA-060002 EVM, a ball-park estimation can be made of the thermal resistances that should hold true for most practical applications:

1. The bottom junction-to-case thermal resistance ($\theta_{JC(BOT)}$) is usually provided in the device data sheet. For the THS3491RGT package, this value is 7.8°C/W.
2. The PCB thermal resistance is the thermal resistance of the flooded vias (θ_{C-VIA}), and is estimated from the via pad diameter, the via height, and PCB material of the via. The EVM has two ounces of copper on each layer with a via diameter of 7.87 mil and a PCB thickness of 62.2 mil that results in a single via thermal resistance of 180°C/W. This thermal resistance estimation is based on the Saturn PCB toolkit for an FR-4 dielectric. The PCB is flooded with 80 vias in and around the bottom of the device, which results in an effective θ_{C-VIA} of approximately 3°C/W to 3.5°C/W. For a more accurate PCB thermal resistance estimation, finite element software tools can be used from vendors such as ANSYS or Keysight for thermal modeling of the PCB.
3. The thermal resistance of the heat sink adhesive or the thermal mold compound (θ_{TMC}) is approximately 0.3°C/W to 0.5°C/W for a maximum heat transfer from the PCB to the heat sink.
4. BDN18-6CB/A01 is the heat sink selected for this design. The BDN18-6CB/A01 has a natural convection free-air standing thermal resistance of θ_{HA} at approximately 8.1°C/W.

Plugging in these individual estimated thermal resistances into 式 29 results in a combined thermal resistance of 19.4°C/W. For a maximum T_J of 150°C and a free-air operating ambient temperature (T_A) of 25°C, the resulting maximum internal power dissipation allowed is 2.52 W without a heat sink, as compared to 6.44 W with a heat sink (almost 2.5 times higher).

2.3.5.1 Linear Safe Operating Area (SOA)

To be within a linear safe operating area, an amplifier is required to either limit the maximum linear output current drive or the maximum internal power dissipation ($P_{D(MAX)}$) to prevent the device from exceeding the maximum junction temperature ($T_{J(MAX)}$) of 150°C. This limit is usually represented by a linear safe operating area (SOA) graph that defines the operational boundary by plotting the linear output current drive (I_{OUT}) on the y-axis and the voltage developed across the output transistor ($V_S – V_{OUT}$) on the x-axis.

As 図 14 to 図 16 show, the upper bound of the safe operating area is defined by the maximum linear output current drive of the amplifier starting from the left of the x-axis. When the voltage developed across the output transistor ($V_S – V_{OUT}$) increases towards the right of the x-axis, the linear output current reduces to maintain a fixed internal power dissipation across the output transistors. The fixed internal power dissipation is given by 式 28 to keep the $T_{J(MAX)}$ below 150°C for a given ambient temperature (T_A). Also, the linear output current is derived from 式 30 by sweeping ($V_S – V_{OUT}$) from right to left on the x-axis until the I_{OUT} equals the maximum linear output current drive. The ($V_S – V_{OUT}$) on the x-axis must be equally applicable for either ($V_{S+} – V_{OUT}$) or ($V_{OUT} – V_{S–}$) depending upon the output source or sink current cycle for a sinusoidal signal (see 図 8).

$$I_{OUT} = \frac{P_{D(MAX)} - 2V_S I_Q}{(V_S - V_{OUT})} \tag{30}$$

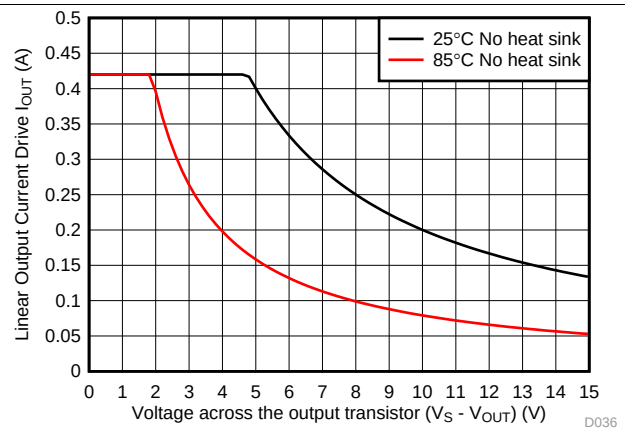


図 14. Linear SOA for a Single THS3491 Amplifier (Without Heat Sink)

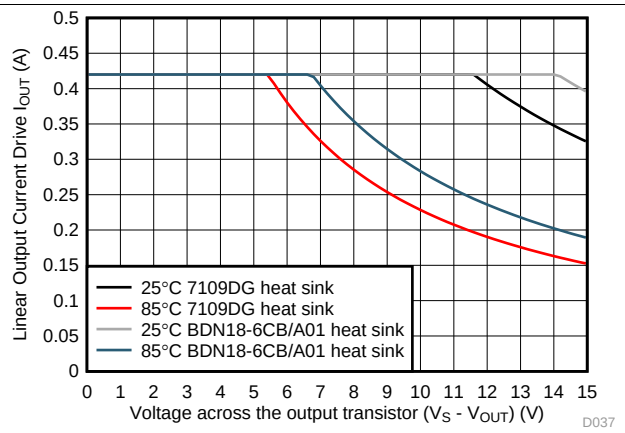
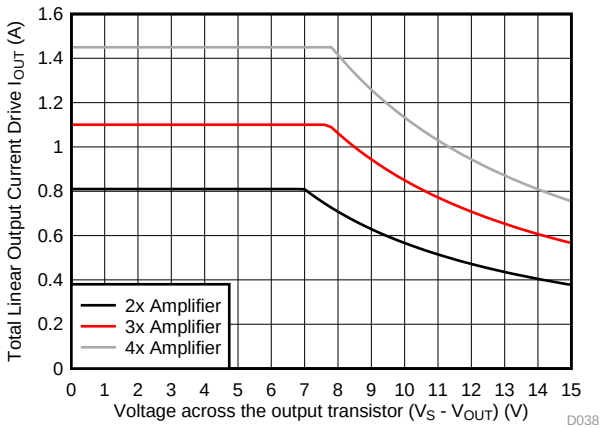


図 15. Linear SOA for a Single THS3491 Amplifier (With Heat Sink)



T_A = 85°C

図 16. Linear SOA for Multiple THS3491 Amplifiers in Parallel (With Heat Sink)

For an SOA graph of a single THS3491 amplifier with no heat sink (see 図 14), the 420 mA of maximum linear output current drive determines the upper limit. The upper limit is considered as the maximum linear output current of ±420 mA instead of the maximum peak output current of ±500 mA to define the *linear* operating boundary for the THS3491. As 図 14 illustrates, the safe operating area for a free-air operating ambient temperature (T_A) of 25°C is shifted to the upper right compared to the 85°C, indicating higher output current drive capability at 25°C.

Comparing 図 14 with 図 15, the linear output current limit shifts even further to the upper right for a single THS3491 amplifier with a heat sink, which indicates even better thermal handling capability for a fixed internal power dissipation across the output. The curves in 図 15 are generated for the 7109DG and BDN18-6CB/A01 heat sinks that have an estimated θ_{JA} of 24.3°C/W and 19.4°C/W, respectively, for a similar PCB construction as illustrated in 図 12.

In a similar fashion, the safe operating area was developed for the TIDA-060002 EVM (see 図 16) using the BDN18-6CB/A01 heat sink on the bottom that gives a θ_{JA} value of 19.4°C/W. As 図 16 illustrates, the total linear output current limit on the upper left increased because of using multiple THS3491 amplifiers in a load-sharing configuration. However, the linear output current increase is not directly proportional to the number of amplifiers added because of the push or pull mismatch currents associated with paralleling multiple load-sharing amplifiers.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This reference design uses the TIDA-060002 EVM as described on the front page of the document for the measurements in 3.2.2. 図 17, 図 18, and 図 19 to describe the required hardware set up for the frequency response, harmonic distortion, and pulse response measurements, respectively.

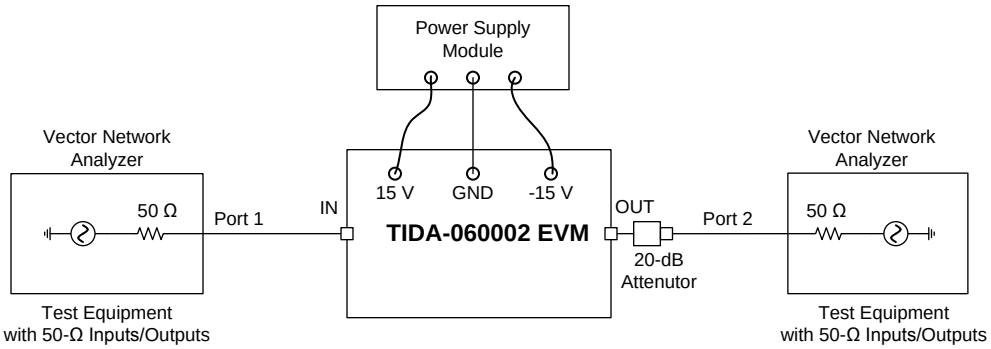


図 17. Frequency Response Setup

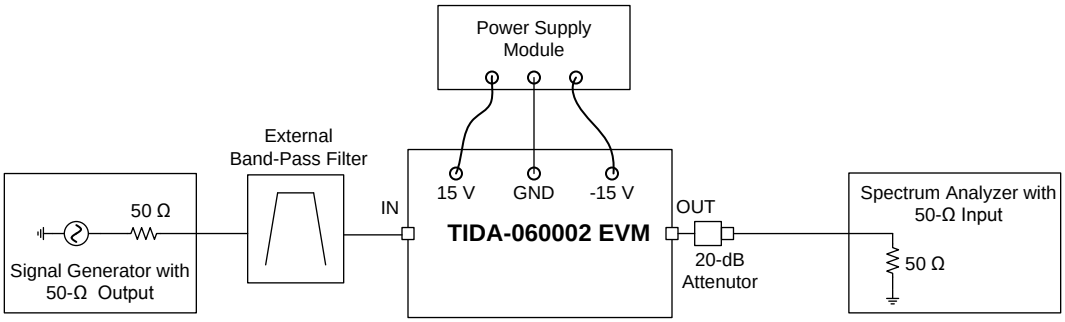


図 18. Harmonic Distortion Setup

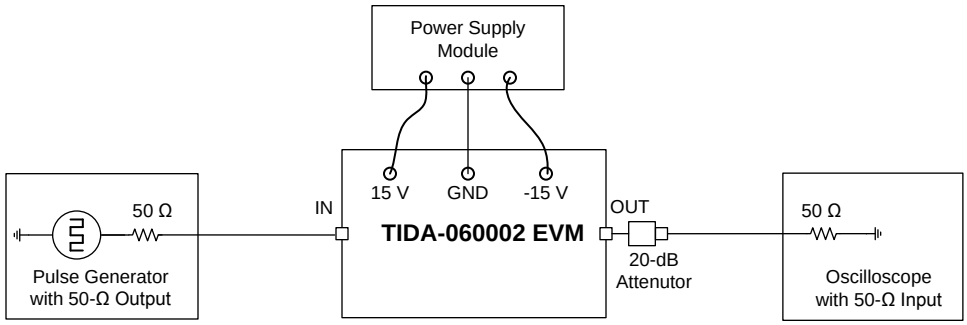


図 19. Pulse Response Setup

3.1.2 Software

There is no required software for design testing.

3.2 Testing and Results

3.2.1 Test Setup

図 20 through 図 25 illustrate the test setup for two, three, and four THS3491 amplifiers in a load-sharing configuration driving resistive or capacitive loads. Each of the individual amplifiers are configured for a voltage gain of 5 V/V with a feedback resistor (R_F) value of 576 Ω and a gain resistor (R_G) value of 143 Ω. The amplifiers are powered with a dual power supply of ±15 V and the results are taken with a 20-V_{PP} output swing referred to the amplifier output, unless otherwise noted. The test results are taken at a free-air operating ambient temperature value (T_A) of 25°C with no forced air regulating temperature of the EVM, unless otherwise noted in the results.

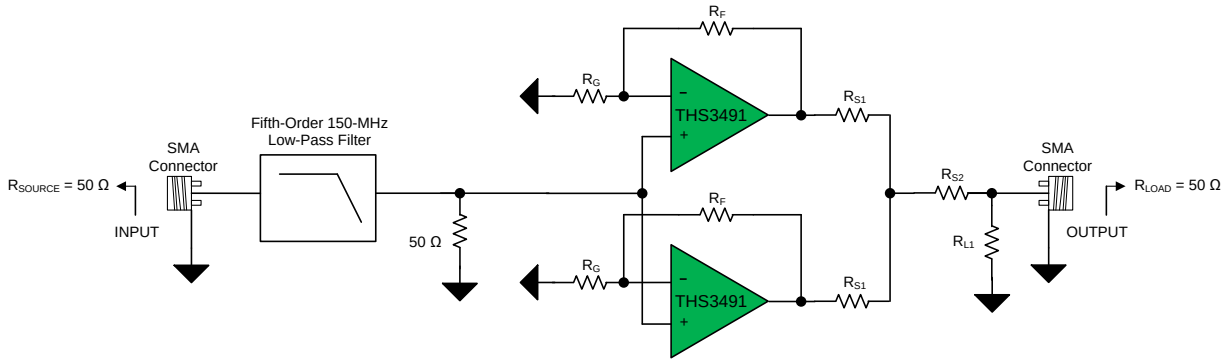


図 20. Two THS3491 Parallel Amplifiers Driving a Resistive Load (R_{LOAD})

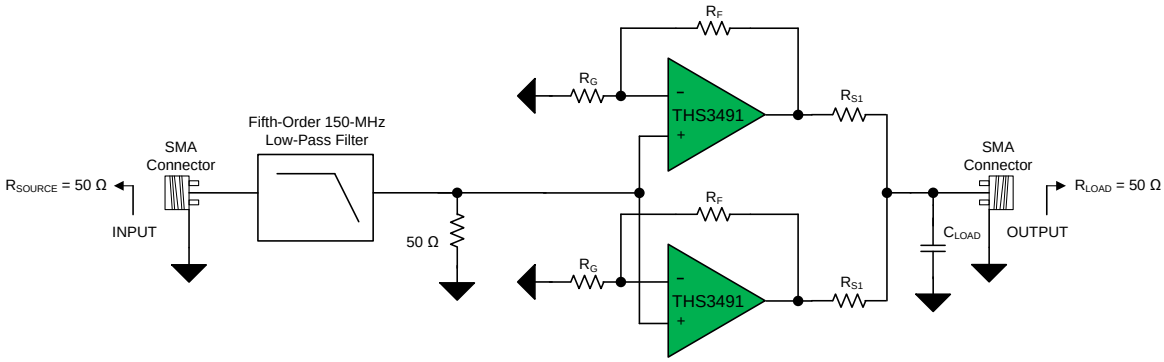


図 21. Two THS3491 Parallel Amplifiers Driving a Capacitive Load (C_{LOAD})

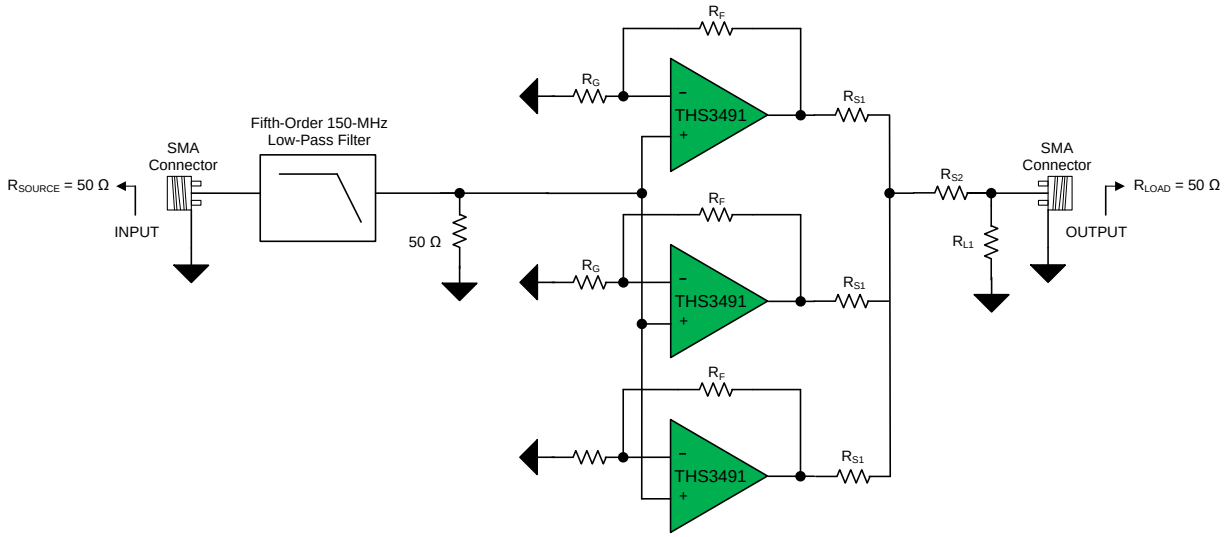


図 22. Three THS3491 Parallel Amplifiers Driving a Resistive Load (R_{LOAD})

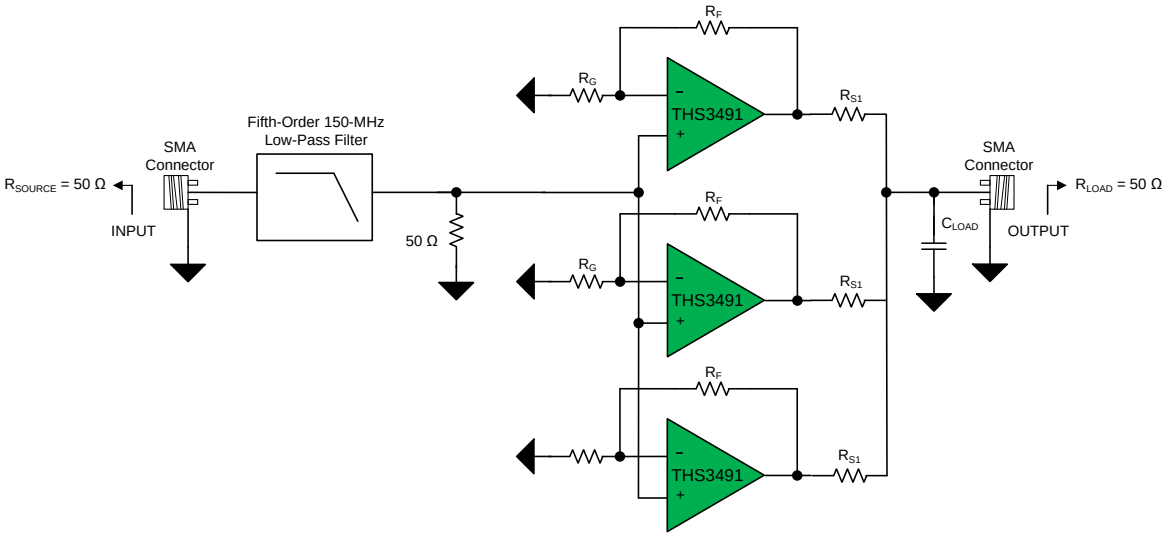


図 23. Three THS3491 Parallel Amplifiers Driving a Capacitive Load (C_{LOAD})

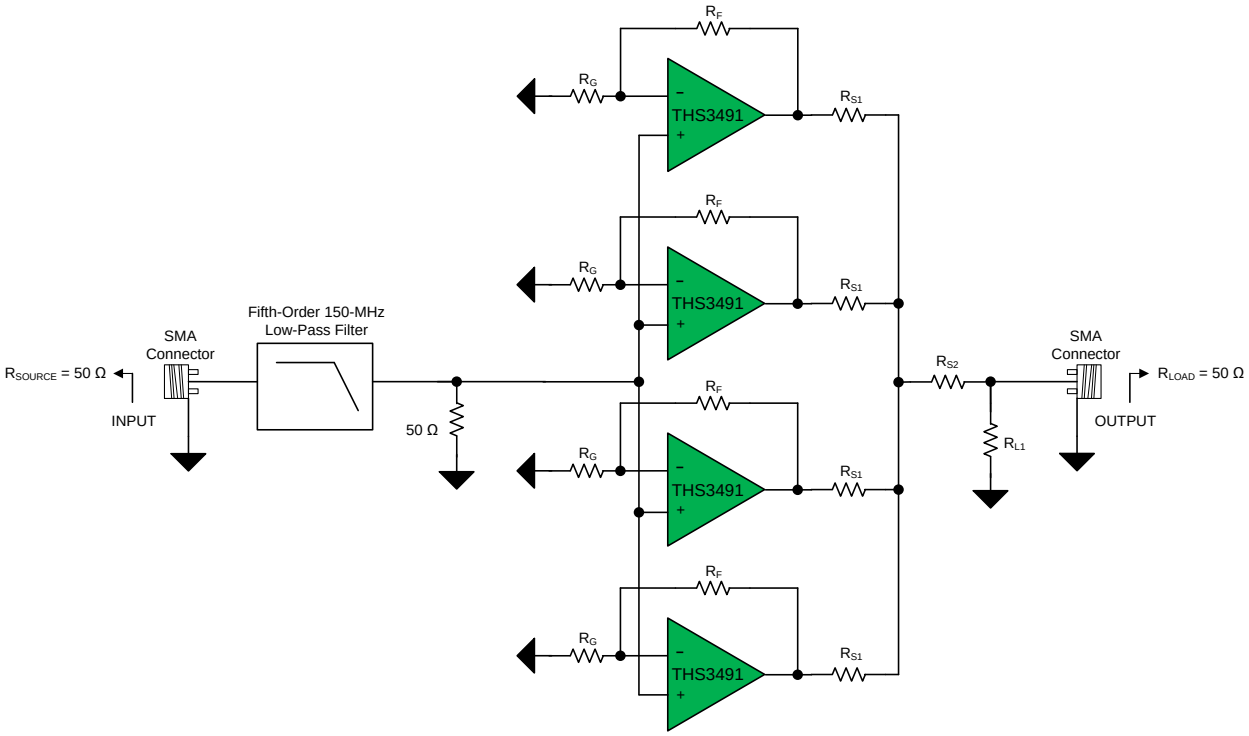


図 24. Four THS3491 Parallel Amplifiers Driving a Resistive Load (R_{LOAD})

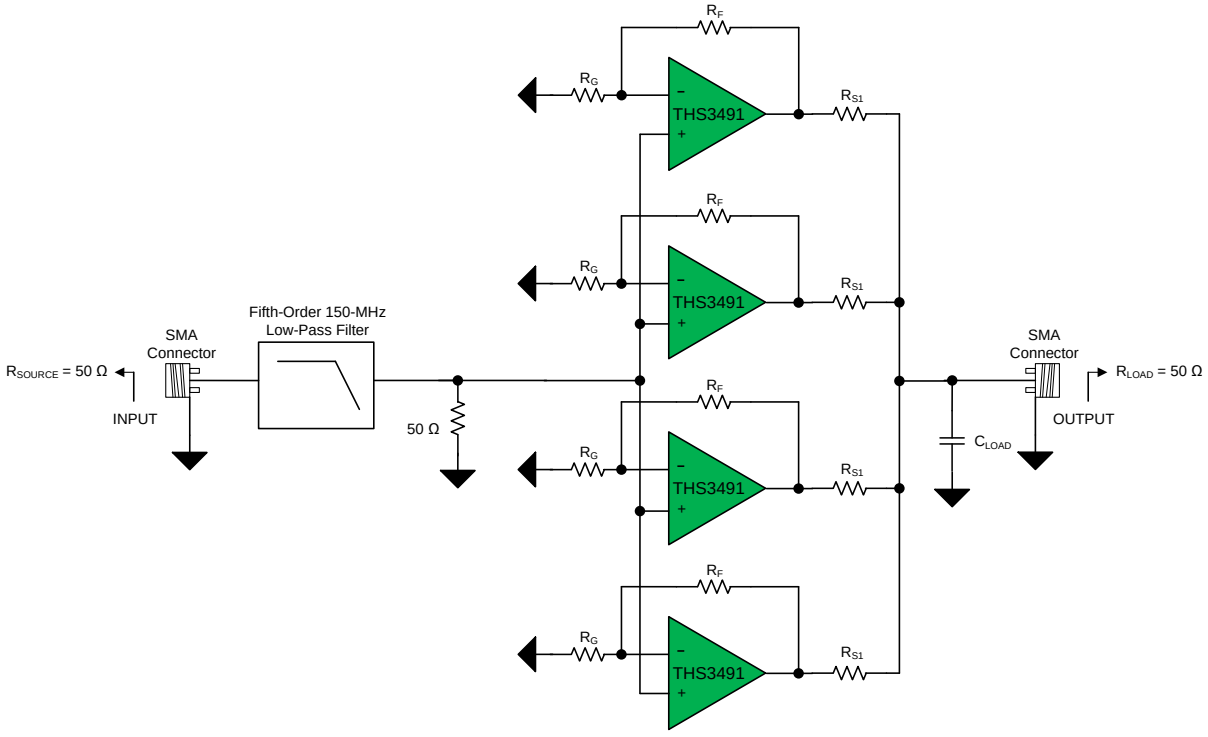


図 25. Four THS3491 Parallel Amplifiers Driving a Capacitive Load (C_{LOAD})

表 3 and 表 4 list the output resistor values used for the test results when driving a resistive or capacitive load, respectively. All test setups are configured for simple interfaces with a 50-Ω test equipment at the input and output.

表 3. Output Resistor Values for a Given Resistive Load (R_{LOAD})

NUMBER OF AMPLIFIERS IN PARALLEL	TOTAL R_{LOAD} (Ω)	R_{S1} (Ω)	R_{S2} (Ω)	R_{L1} (Ω)
Two THS3491s (see 図 20)	10	10	0	6.04
	20	12	4	12.5
	50	40	5	50
	100	40	30	Open
Three THS3491s (see 図 22)	10	12	0	6.8
	20	12	0	22
	50	30	15	50
	100	60	30	Open
Four THS3491s (see 図 24)	10	12	0	7.5
	20	12	0	27
	50	40	15	50
	100	80	30	Open

表 4. Output Resistor Values for a Given Capacitive Load (C_{LOAD})

NUMBER OF AMPLIFIERS IN PARALLEL	TOTAL C_{LOAD} (pF)	R_{S1} (Ω)
Two THS3491s (see 図 21)	100	10
	270	10
	390	10
	1000	10
Three THS3491s (see 図 23)	270	12
	560	12
Four THS3491s (see 図 23)	560	20
	1000	20

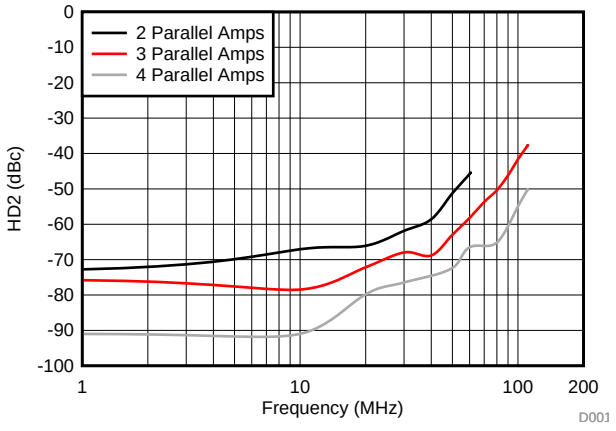
3.2.2 Test Results

The test results are divided into three subcategories: two, three, and four parallel amplifiers in a load-sharing configuration showing data on the frequency response, harmonic distortion, and pulse response for the respective test conditions.

図 26 and 図 27 show second harmonic (HD2) and third harmonic (HD3) distortion measurements, respectively, comparing the two, three, and four THS3491 parallel amplifiers when driving 20 V_{PP} with an R_L of 20 Ω. As described by the distortion plots of 図 26 and 図 27, there is clearly an advantage of improved distortion performance in the load-sharing configuration. The harmonic distortion improves for each amplifier that is added to the load-sharing configuration because each individual amplifier outputs less current for the same output voltage swing. The third harmonic distortion (HD3) degrades beyond –30 dBc beyond 60 MHz with two parallel amplifiers. On the other hand with three or four parallel amplifiers that extend the output drive strength, the HD2 and HD3 are below –30 dBc and are well beyond the 100 MHz required for the same 20-V_{PP} output swing.

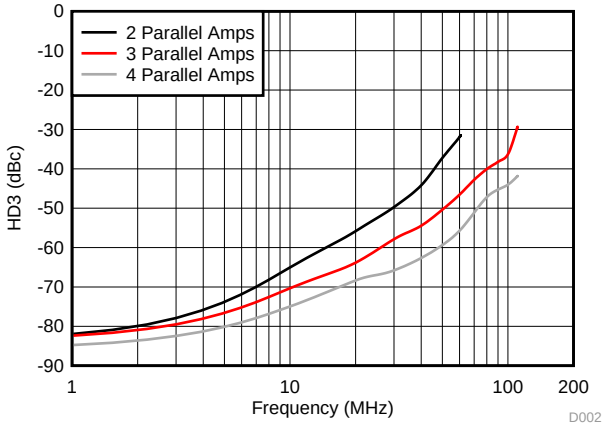
Two things can be deduced from the output load-sharing configuration:

1. Each additional amplifier now outputs less current for the same output voltage swing while keeping the same output load, thus extending the frequency of operation within the f_{3dB} point.
2. An increase in the number of parallel amplifiers allows the circuit to drive an even heavier output load for the same output swing and operating frequency. This ability is because of the increased output current boost offered by the parallel amplifiers.



V_O = 20 V_{PP}, R_L = 20 Ω

図 26. HD2 vs Frequency

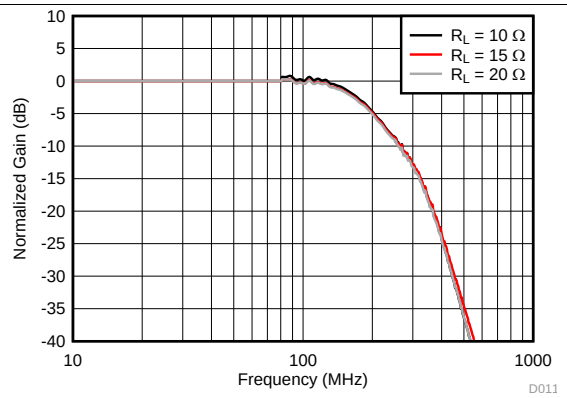


V_O = 20 V_{PP}, R_L = 20 Ω

図 27. HD3 vs Frequency

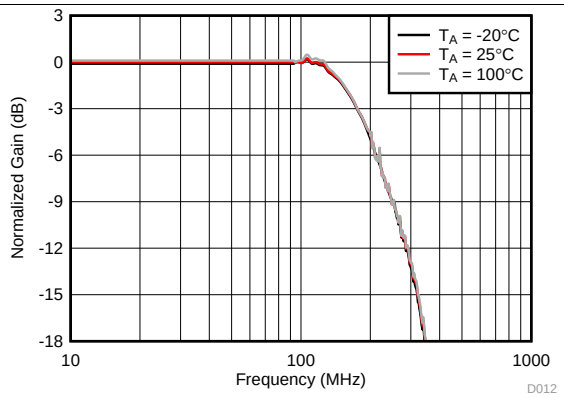
3.2.2.1 Two Parallel Amplifiers in a Load-Sharing Configuration

Test Conditions: two THS3491 op amps in parallel (see 図 20 and 図 21), (VS+) – (VS–) = 30 V, gain (G) = 5 V/V, R_F = 576 Ω, R_L = 20 Ω, V_O = 20 V_{PP}, and T_A = 25°C (unless otherwise noted)



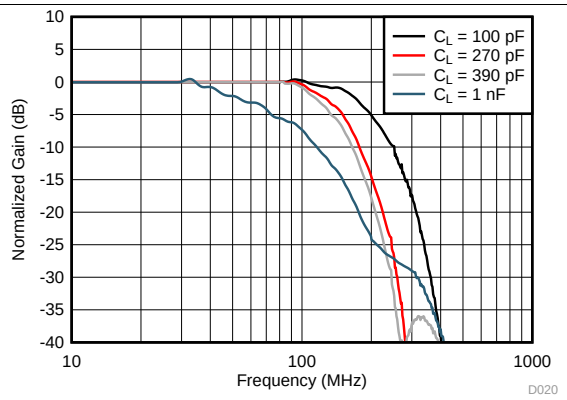
V_O = 15 V_{PP}

図 28. Frequency Response vs R_{LOAD}



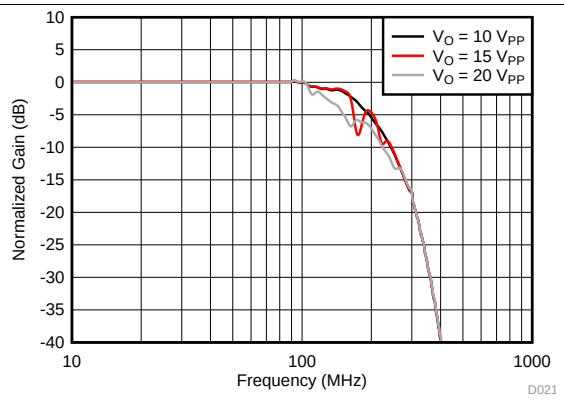
V_O = 20 V_{PP}, R_L = 20 Ω

図 29. Frequency Response vs Temperature (T_A)



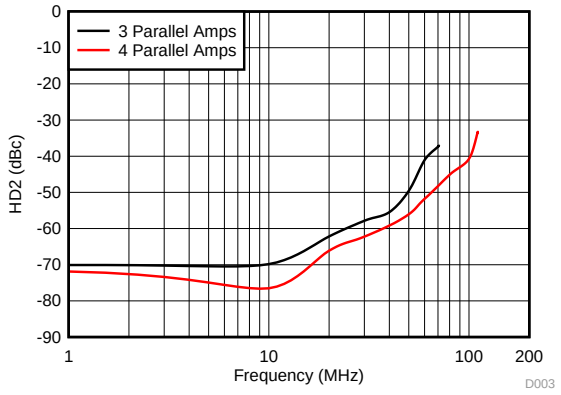
V_O = 10 V_{PP} (see 表 4)

図 30. Frequency Response vs C_{LOAD}



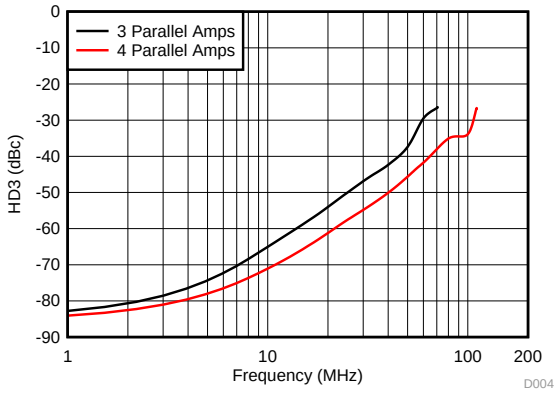
R_S = 5 Ω, C_L = 100 pF (see 表 4)

図 31. Frequency Response vs Output Swing



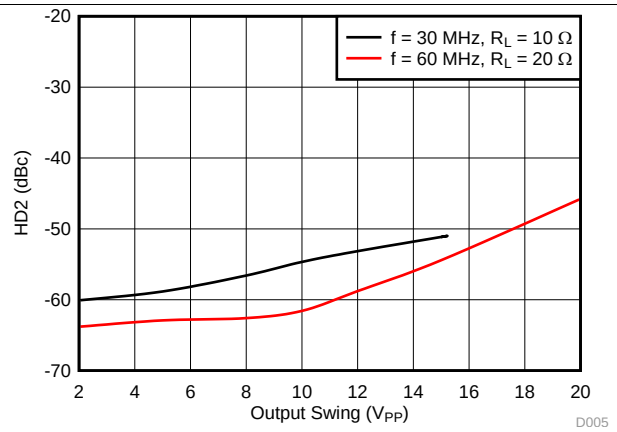
V_O = 20 V_{PP}, R_L = 10 Ω

図 32. HD2 vs Frequency



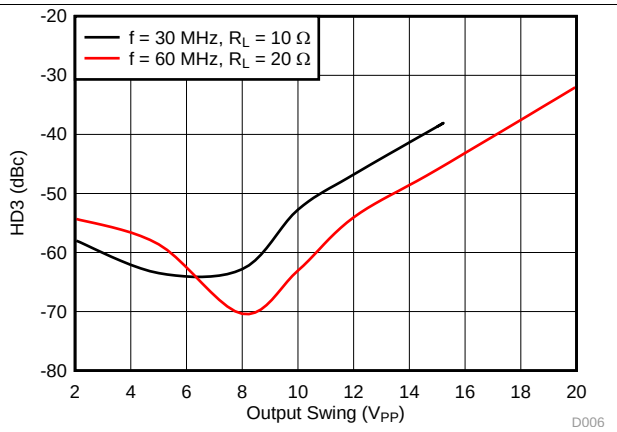
V_O = 20 V_{PP}, R_L = 10 Ω

図 33. HD3 vs Frequency



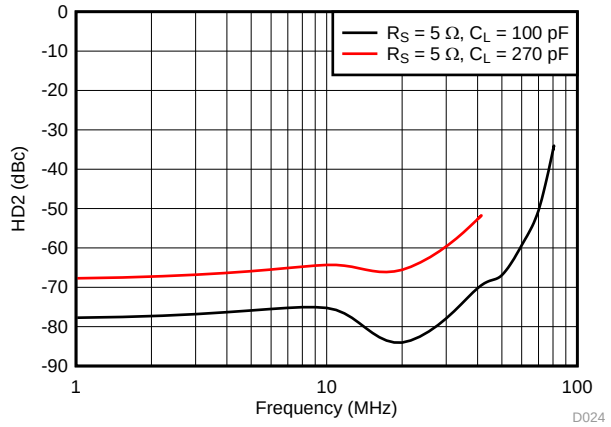
See 図 20

図 34. HD2 vs Frequency



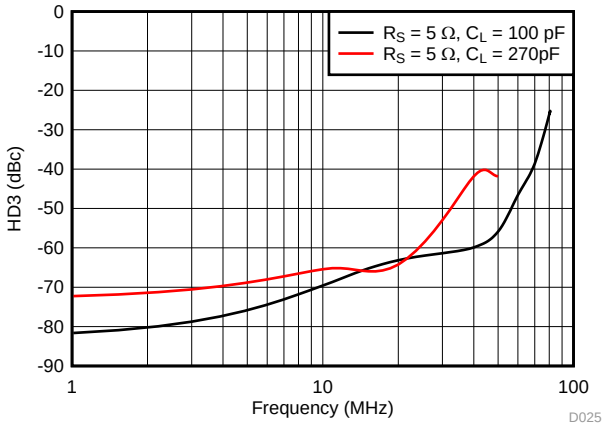
See 図 20

図 35. HD3 vs Frequency



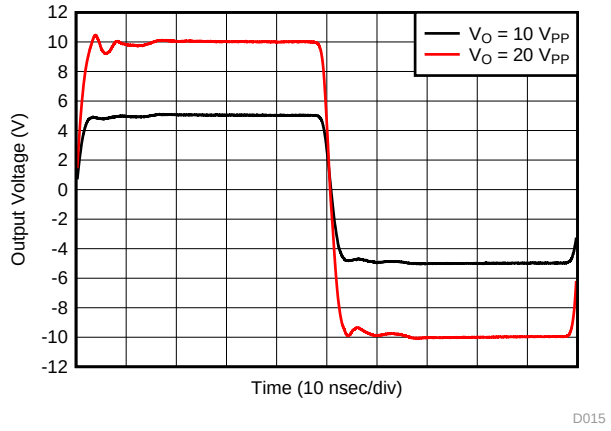
V_O = 20 V_{PP}

図 36. HD2 vs Frequency and C_{LOAD}



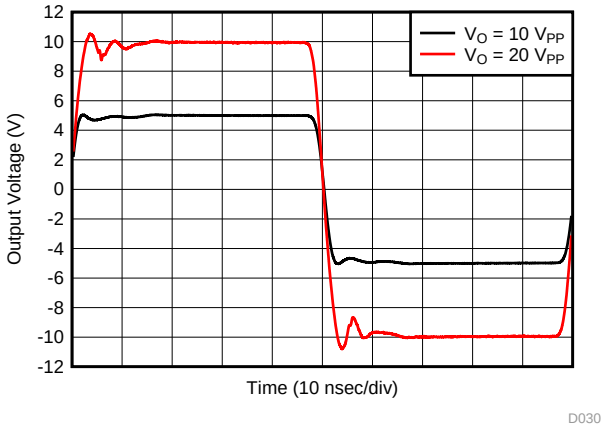
V_O = 20 V_{PP}

図 37. HD3 vs Frequency and C_{LOAD}



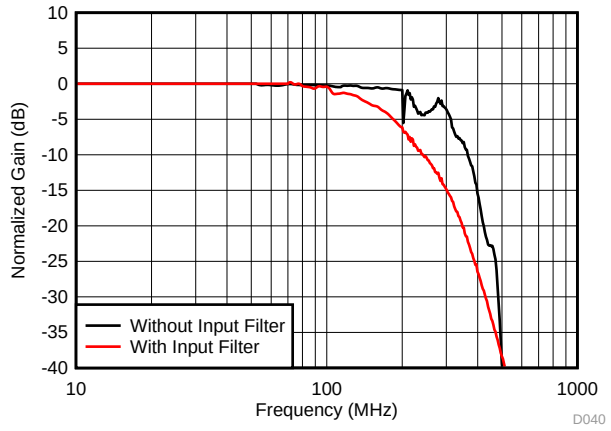
Average $T_{RISE/FALL}$ = 3.1 nsec
R_L = 20 Ω

図 38. Pulse Response



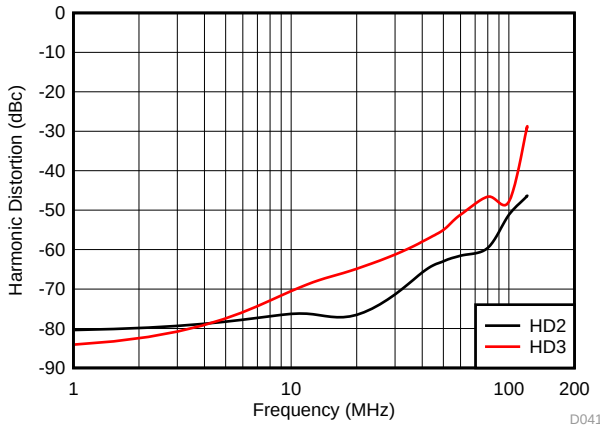
Average $T_{RISE/FALL}$ = 3.8 nsec
R_S = 5 Ω, C_L = 100 pF

図 39. Pulse Response



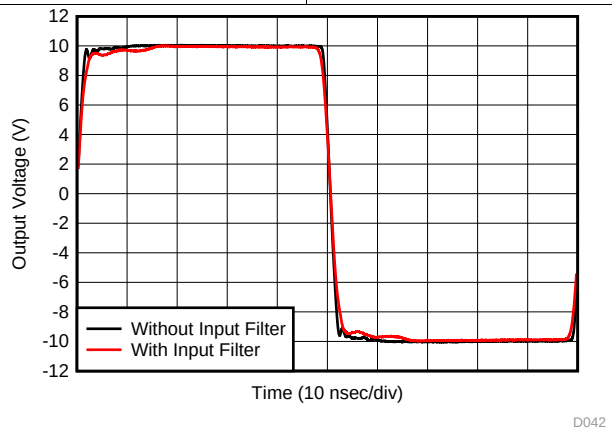
R_L = 50 Ω

図 40. Frequency Response With and Without an Input Filter



R_L = 50 Ω

図 41. Harmonic Distortion Without an Input Filter

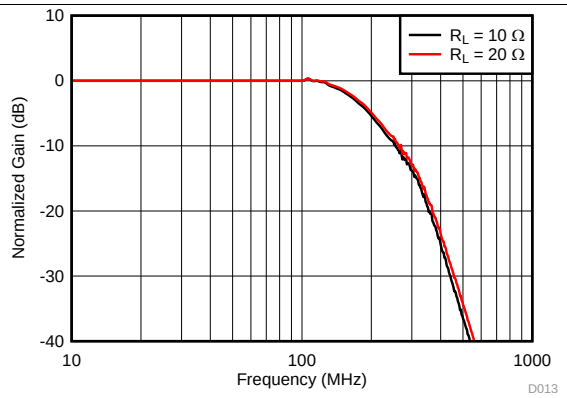


Average $T_{RISE/FALL}$ = 2.4 nsec (Without Input Filter)
Average $T_{RISE/FALL}$ = 3.1 nsec (With Input Filter)
R_L = 50 Ω

図 42. Pulse Response With and Without an Input Filter

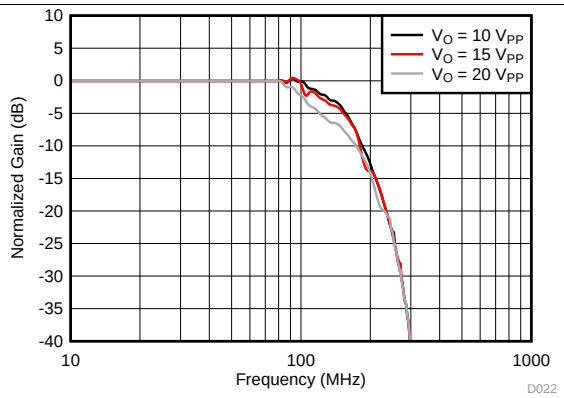
3.2.2.2 Three Parallel Amplifiers in a Load-Sharing Configuration

Test Conditions: three THS3491 op amps in parallel (see 図 22 and 図 23), (VS+) – (VS–) = 30 V, gain (G) = 5 V/V, R_F = 576 Ω, R_L = 20 Ω, V_O = 20 V_{PP}, and T_A = 25°C (unless otherwise noted)



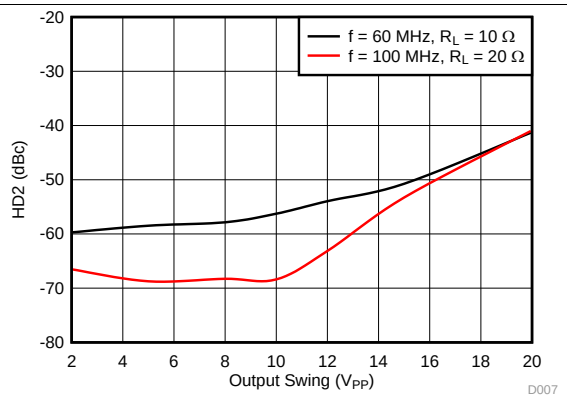
V_O = 20 V_{PP}

図 43. Frequency Response vs R_{LOAD}



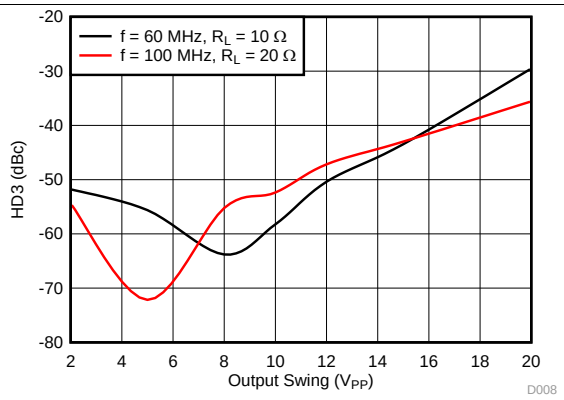
R_S = 5 Ω, C_L = 270 pF (see 表 4)

図 44. Frequency Response vs Output Swing



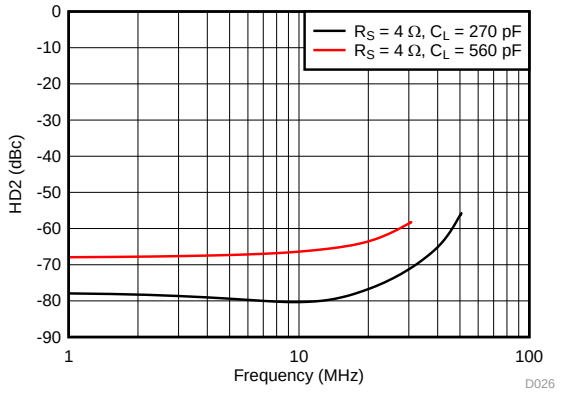
See 図 22

図 45. HD2 vs Output Swing and Frequency



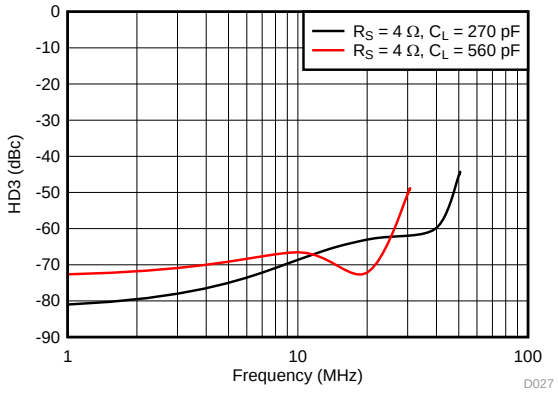
See 図 22

図 46. HD3 vs Output Swing and Frequency



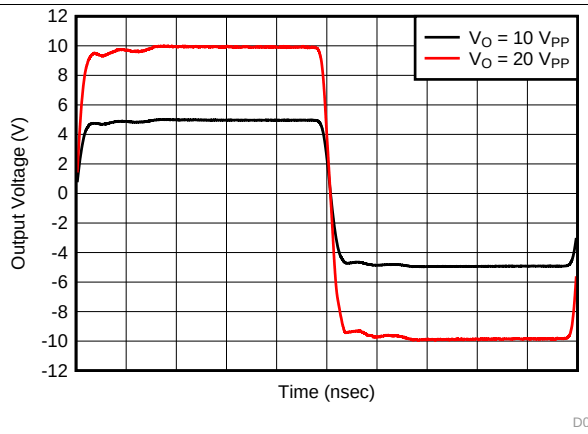
V_O = 20 V_{PP}

図 47. HD2 vs Frequency and C_{LOAD}



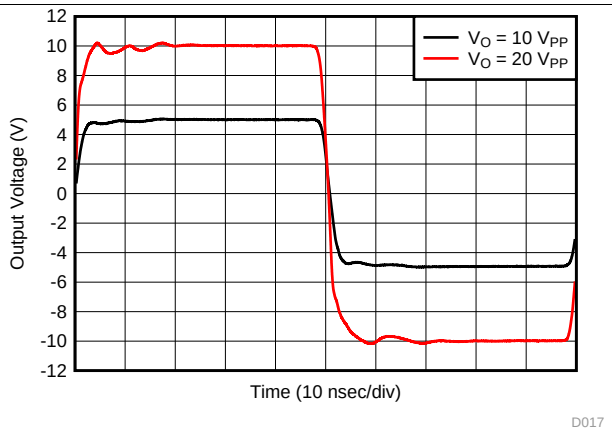
V_O = 20 V_{PP}

図 48. HD3 vs Frequency and C_{LOAD}



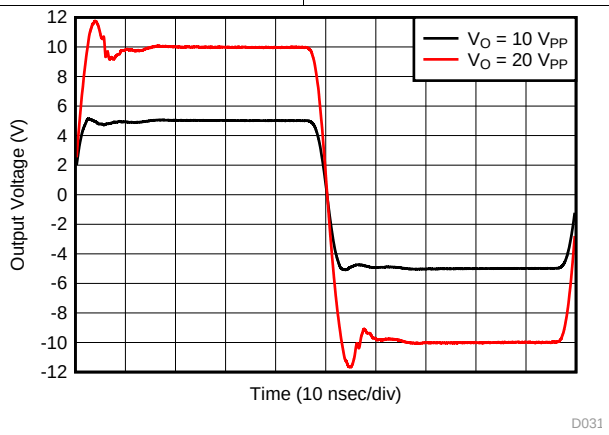
Average $T_{RISE/FALL}$ = 3.6 nsec
R_L = 20 Ω

図 49. Pulse Response



Average $T_{RISE/FALL}$ = 3.6 nsec
R_L = 10 Ω

図 50. Pulse Response

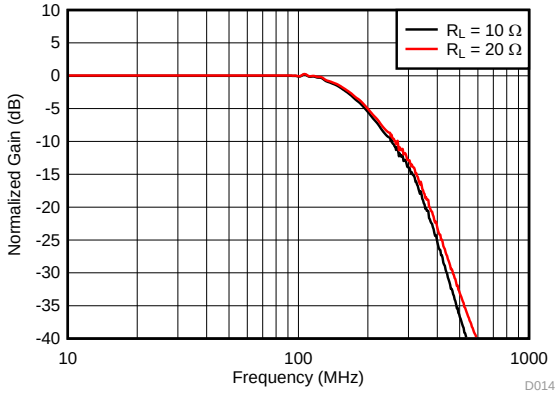


Average $T_{RISE/FALL}$ = 4.2 nsec
R_S = 4 Ω, C_L = 270 pF

図 51. Pulse Response

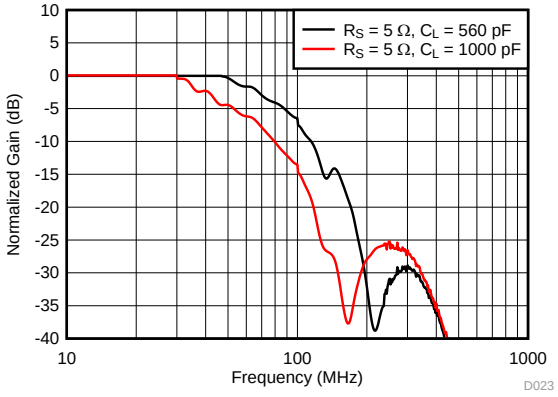
3.2.2.3 Four Parallel Amplifiers in a Load-Sharing Configuration

Test Conditions: four THS3491 op-amps in parallel (see 図 24 and 図 25), (VS+) – (VS–) = 30 V, gain (G) = 5 V/V, R_F = 576 Ω, R_L = 20 Ω, V_O = 20 V_{PP}, and T_A = 25°C (unless otherwise noted)



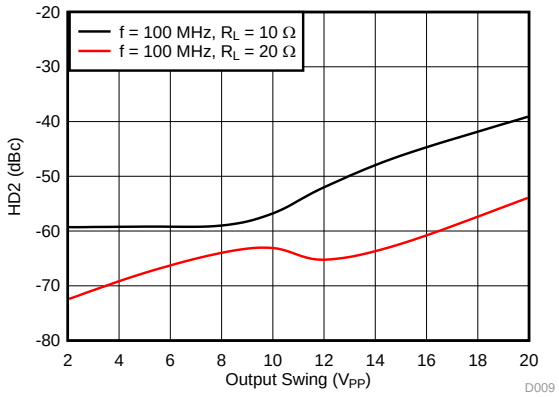
V_O = 20 V_{PP}

図 52. Frequency Response vs R_{LOAD}



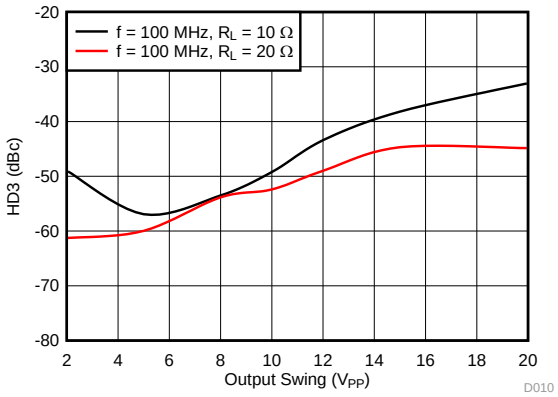
V_O = 20 V_{PP} (see 表 4)

図 53. Frequency Response vs C_{LOAD}



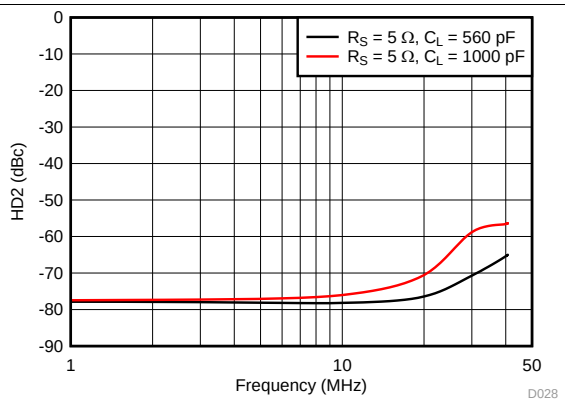
See 図 24

図 54. HD2 vs Output Swing and Frequency



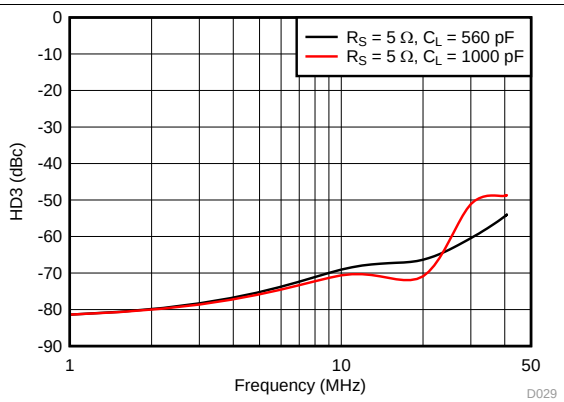
See 図 24

図 55. HD3 vs Output Swing and Frequency



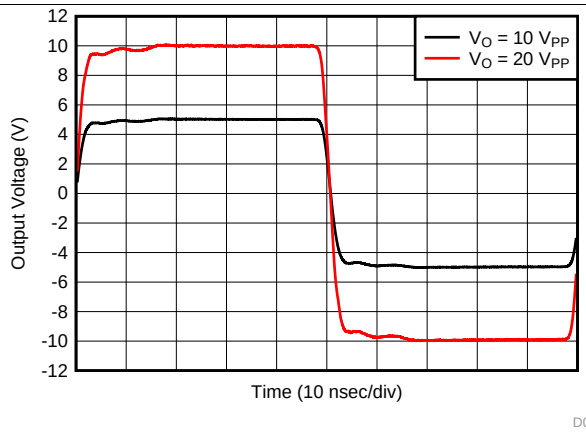
V_O = 20 V_{PP}

図 56. HD2 vs Frequency and C_{LOAD}



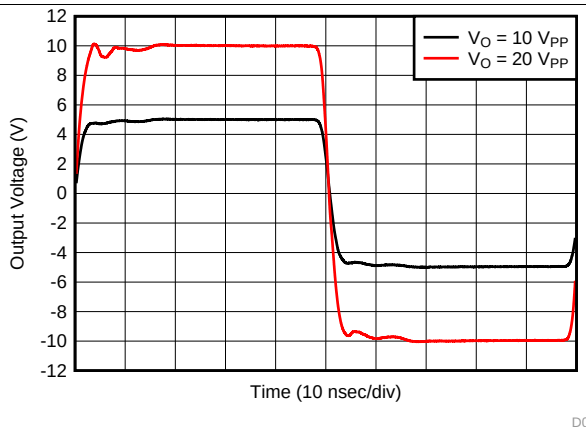
V_O = 20 V_{PP}

図 57. HD3 vs Frequency and C_{LOAD}



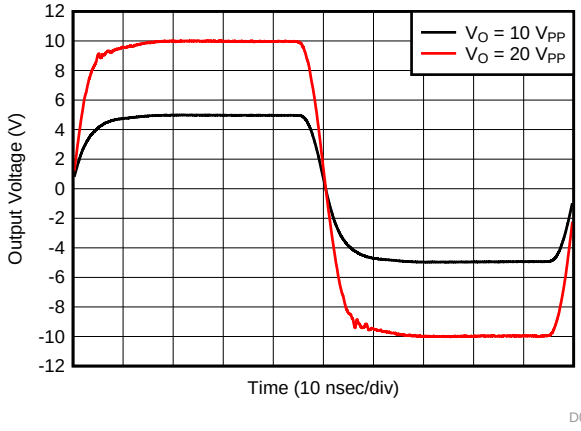
Average $T_{RISE/FALL}$ = 3.3 nsec
R_L = 20 Ω

図 58. Pulse Response



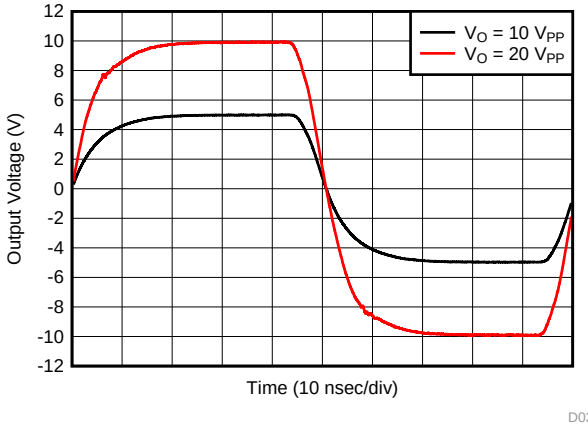
Average $T_{RISE/FALL}$ = 3.3 nsec
R_L = 10 Ω

図 59. Pulse Response



Average $T_{RISE/FALL}$ = 7 nsec
R_S = 5 Ω, C_L = 560 pF

図 60. Pulse Response



Average $T_{RISE/FALL}$ = 12 nsec
R_S = 5 Ω, C_L = 1000 pF

図 61. Pulse Response

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060002.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060002.

4.3 PCB Layout Recommendations

The PCB layout recommendations are similar to the layout guidelines provided in the THS3491 datasheet. The thermal performance for the design is provided in 2.3.5.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060002.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060002.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060002.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060002.

5 Related Documentation

1. Texas Instruments, *THS3491 900-MHz, 500-mA High-Power Output Current Feedback Amplifier* data sheet
2. Texas Instruments, *OA-13 Current Feedback Loop Gain Analysis and Performance Enhancement* application report
3. Texas Instruments, *Reference Design for Implementation of the Load Sharing Concept for Large-Signal Applications*
4. Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report

5.1 商標

6 About the Author

ROHIT BHAT has been an applications engineer with Texas Instruments since 2012. Rohit has been supporting TI's high-speed amplifiers in applications requiring high-speed analog signal processing which includes, but is not limited to, video, test and measurement, and communications.

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