参考資料

TI Designs: TIDA-01525
8チャネル、16ビット、200mA電流出力、デジタル/アナログ・コンバータのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

多くのシステム、たとえば光学レーザー駆動アプリケーションなどでは、チャネル数が多く、柔軟で、高精度の電流源が必要です。さらに業界は、必要なチャネル数の増大と同時に、より小型のソリューションへと向かっています。このリファレンス・デザインは、DAC80508 8チャネル、16ビットDACの小さなサイズと高性能を、高精度オペアンプと組み合わせることで、高密度かつ高精度の電流ソース・ソリューションを実現します。このリファレンス・デザインは最大200mAの電流を出力でき、最低限のPVDD電源電圧で動作するため、消費電力の低減と高効率を実現できます。また、DAC80508の基準電圧ノイズが小さく、OPA2376の電圧および電流ノイズが小さいため、このリファレンス・デザインは電流出力のノイズが小さいことも特長です。

リソース

TIDA-01525	デザイン・フォルダ
DAC80508	プロダクト・フォルダ
OPA2376	プロダクト・フォルダ
CSD13381F4	プロダクト・フォルダ
CSD23285F5	プロダクト・フォルダ

TI E2E™ Community

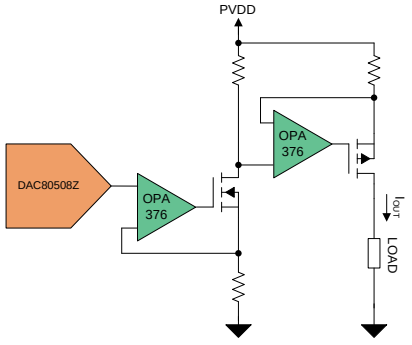
E2Eエキスパートに質問

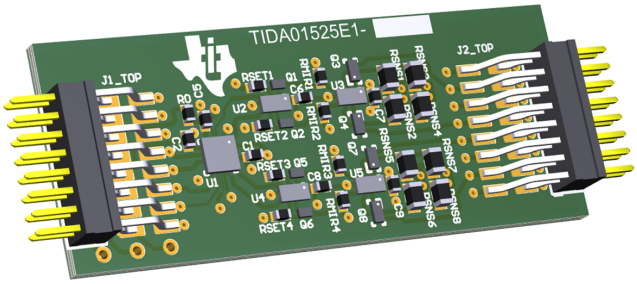
特長

- 8チャネルのプログラム可能な電流（200mAレンジ）
- 16ビット分解能
- 高いチャネル密度
- 120µA未満のオフセット誤差
- 1.5%未満の合計未調整誤差
- 最小1.75VのPVDD電源
- 帯域幅が制限された3.4μA_{RMS}の電流ノイズ
- 10kHzで10nA/$\sqrt{Hz}$の電流ノイズ

アプリケーション

- 光学モジュールのレーザー駆動
- 調節可能なレーザー光学モジュール





1 System Description

The objective of this reference design is to demonstrate a compact high-side current-source design that can be implemented with a multichannel DAC, op amps, and discrete components. This design uses components that offer a high level of flexibility, and can be used in many different environments. The key component of the design is the DAC80508 device. The device features eight DAC channels at 16-bit resolution that can be set to either a 1.25-V, 2.5-V, or 5-V range while using the internal reference. This DAC is a voltage-output device, so an external voltage-to-current (V/I) stage is added to the design. To implement the V/I stage, create an accurate reference current that is amplified using a current mirror.

Laser-diode applications generally require a precisely controlled current to regulate the output power. An adjustable current is advantageous because the laser output-power can shift over temperature. For this reason, a DAC can be used to dynamically update the forward current. In addition, use a low-noise source to reduce the intensity noise (instability in the output power) of a laser output. The DAC 16-bit resolution allows the power to be fine-tuned, but the same design could be used with the 14-bit DAC70508 and 12-bit DAC60508 devices, which are pin-for-pin compatible with the DAC80508.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Current-source supply voltage	2 V, nominal	2.2.3
DAC80508 and OPA2376 supply voltage	5 V	2.2.1
DAC resolution and performance	16-bit, ±1 LSB INL/DNL	2.3.1
Current-source full-scale output current	200 mA	2.2.3
Total unadjusted error	< 1.5% FSR at 25°C	3.2.2.1
Current-noise density	10 nA/$\sqrt{\text{Hz}}$ at 10 kHz and full-scale output	3.2.2.2
Bandwidth limited RMS current noise	3.4 μA_{RMS} at midscale output	3.2.2.3
Zero-scale error	< 120 µA	3.2.2.4
Minimum PVDD supply voltage	1.75 V at full-scale output	3.2.2.5

2 System Overview

2.1 Block Diagram

図 1 shows a block diagram of the system.

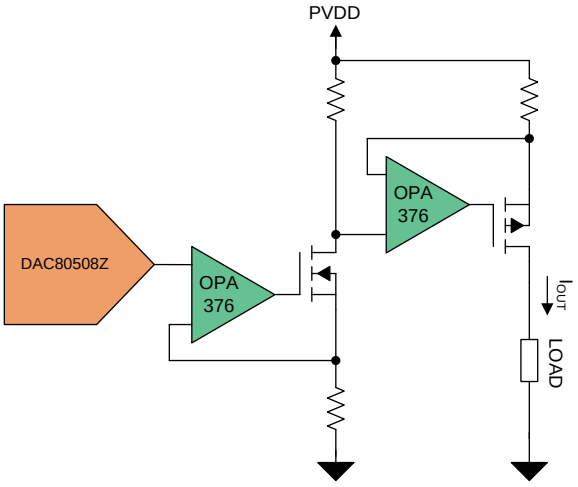


図 1. TIDA-01525 Block Diagram

2.2 Design Considerations

This section describes the system, and the major subcircuits in the design. The system design can be considered to be made up of three main sections: the DAC stage, the V/I converter first stage, and the V/I converter second stage, as shown in 図 2.

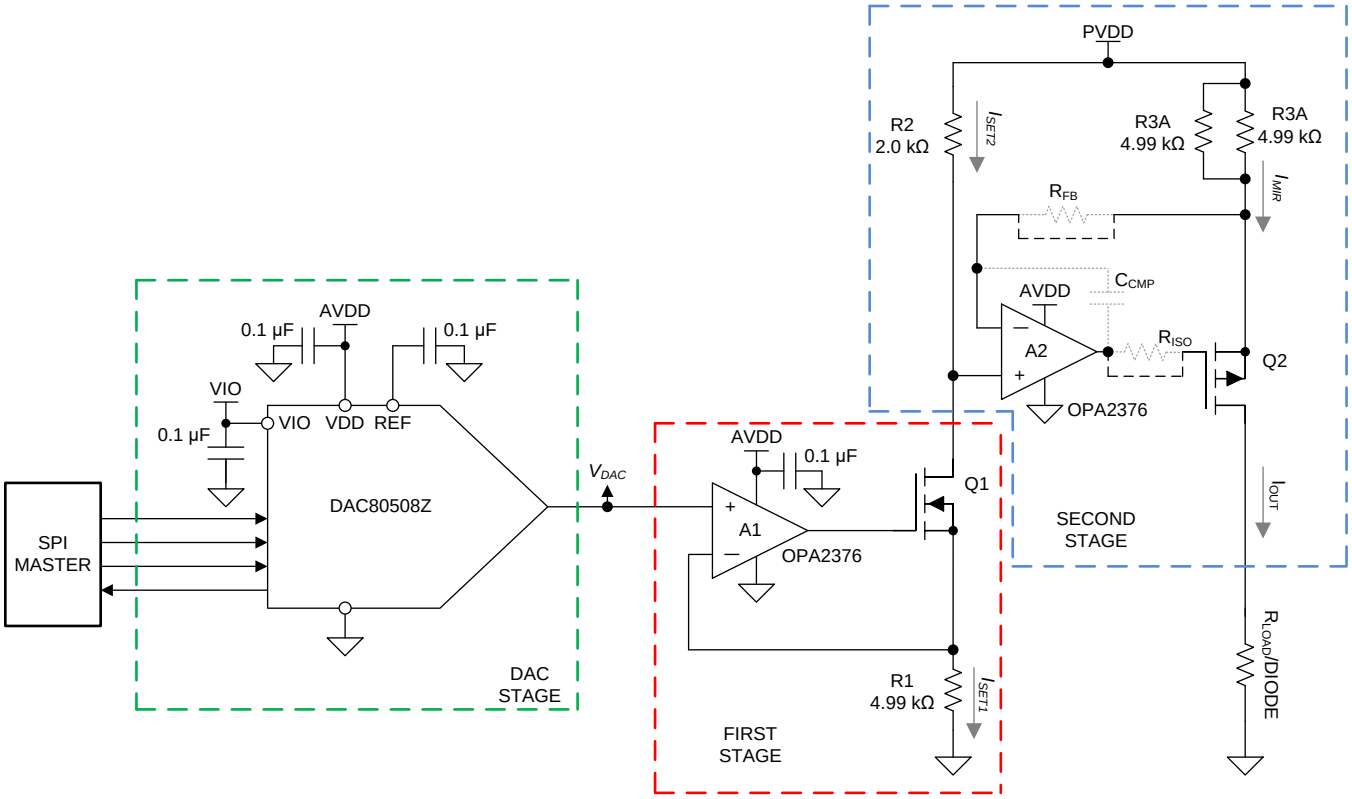


図 2. TIDA-01525 Theory of Operation

2.2.1 DAC Output Stage

For this design, the DAC is configured externally with an SPI master. The voltage level of the communication is determined by VIO, which is supplied externally at 3.3 V. The analog portion of the DAC is powered with AVDD, which is also shared with the op amps. For the purpose of the device testing, 5 V is used for AVDD. The DAC80508 allows for 2.7 V minimum, whereas the OPA2376 can operate as low as 2.2 V. Therefore, power consumption of AVDD can be reduced by operating at 2.7 V.

The DAC80508 is configured to use the internal reference, which has an external 0.1-µF capacitor that helps filter noise generated by the reference. The internal reference is the primary source of noise in the system, so an external, low-noise reference provides superior noise performance. However, an external low-noise reference adds additional cost and board space to the system, so the external reference was not featured in this design.

The DAC80508 features a reference attenuator that divides the reference by two. This setting is used by the system to allow the maximum output range of the DAC to be 1.25 V. This lower voltage allows the PVDD supply to be minimized, and reduces the power dissipated by the output MOSFET, Q2.

2.2.2 First Op Amp Stage

The first stage of the V/I circuit creates a reference current across sense resistor R1 in series with n-channel MOSFET Q1. By applying the DAC voltage output, V_{DAC}, to the noninverting node of op amp A1. The device uses negative feedback to force the same voltage to the high-side of R1. The reference current, I_{SET1}, can be calculated with 式 1.

$$I_{SET1} = V_{DAC} \div R1 \quad (1)$$

注: The absolute value of the R1 influences the final output gain of the circuit, and any difference between the real and ideal value appears as a gain error on the final output current. For this reason, make sure to select a precise resistor.

The current generated by this stage does not contribute to the final output current; therefore, minimizing this current is critical for optimizing the efficiency of the system. Power dissipated in the R1 can be calculated using 式 2

$$P_{R1} = V_{DAC}^2 / R1 \quad (2)$$

For this design, R1 is set to be 4.99 kΩ. When the DAC is at full-scale output voltage, I_{SET1} is calculated to be approximately 250 µA, as shown in 式 3:

$$I_{SET1\ FULL\text{-}SCALE} = 1.25\ V \div 4.99\ k\Omega = 250.5\ \mu A \quad (3)$$

2.2.3 Second Op Amp Stage

The second stage of the system is a precision current-mirror with a gain set by R2 and R3. The voltage across resistor R2 is determined by the reference current created by the first stage. Current I_{SET2} is ideally the same as I_{SET1}, and creates a voltage drop across R2. The voltage across R2 is the same voltage across R3 because amplifier A2 uses p-channel MOSFET Q2 to draw the current from PVDD to make sure that the input nodes are the same potential. This relationship is shown in 式 4:

$$I_{SET1} \times R2 = I_{MIR} \times R3 \quad (4)$$

The current gain of this system is then expressed by 式 5:

$$\text{Current Gain} = I_{MIR} \div I_{SET1} = R2 \div R3 \quad (5)$$

In this system, R2 is selected to be 2 kΩ and R3 is selected to be 2.495 Ω. This value is created in the application by using two resistors in parallel, which allows smaller resistors with lower power ratings to be used. 式 6 shows the current gain given these resistor values.

$$\text{Current Gain} = 2\ \text{k}\Omega \div 2.495\ \Omega = 801.6\ \text{A/A} \quad (6)$$

The gain of the system can now be express using 式 7:

$$I_{OUT} = (V_{DAC} \times R2) / (R1 \times R3) \quad (7)$$

Using the values selected for the system, the full-scale output current can be calculated as shown in 式 8:

$R1 = 4.99\ k\Omega,\ R2 = 2\ k\Omega,\ R3 = 2.495\ \Omega$ (8)

$I_{OUT\text{-}MAX} = (1.25\ V \times 2\ k\Omega) / (4.99\ k\Omega \times 2.495\ \Omega)$ (9)

$I_{OUT\text{-}MAX} = 200.801\ mA$ (10)

There are a few sources of error in this stage. Firstly, the gain error of the stage is determined by how well resistors R2 and R3 are proportionally matched; for this reason, use precision resistors. Secondly, amplifier A2 contributes to error with the voltage offset of the inputs. The offset results in a voltage across R2 that is not the same as the voltage across R3. This offset ultimately looks like an offset error on the output, and necessitates the selection of an amplifier that has low offset voltage. Finally, the bias current of the amplifier causes the current flowing through R2, I_{SET2}, to not exactly match the reference current, I_{SET1}. This mismatch also results in an offset error on the output. Selecting an amplifier with a a bias current that is much lower than the reference current minimizes this error. The bias current also impacts the I_{MIR} current, but as that current is already very large, the impact is only a small offset error.

For the reasons discussed, the OPA2376 is selected because this device has low bias current and offset, while still being a small package and capable of rail-to-rail operation.

2.2.4 PCB Design

図 3 shows the printed circuit board (PCB) layout of the TIDA-01525 design top and bottom layer. This board has two internal layers: a ground layer and supply layer for PVDD. A majority of the PCB is dedicated to input and output headers that are necessary to improve the usability of the design during testing. The denoted box on the figure show the approximate area that was used on the top and bottom layer to implement all eight channels of the design. The selection of small components and compact layout result in a high-density design.

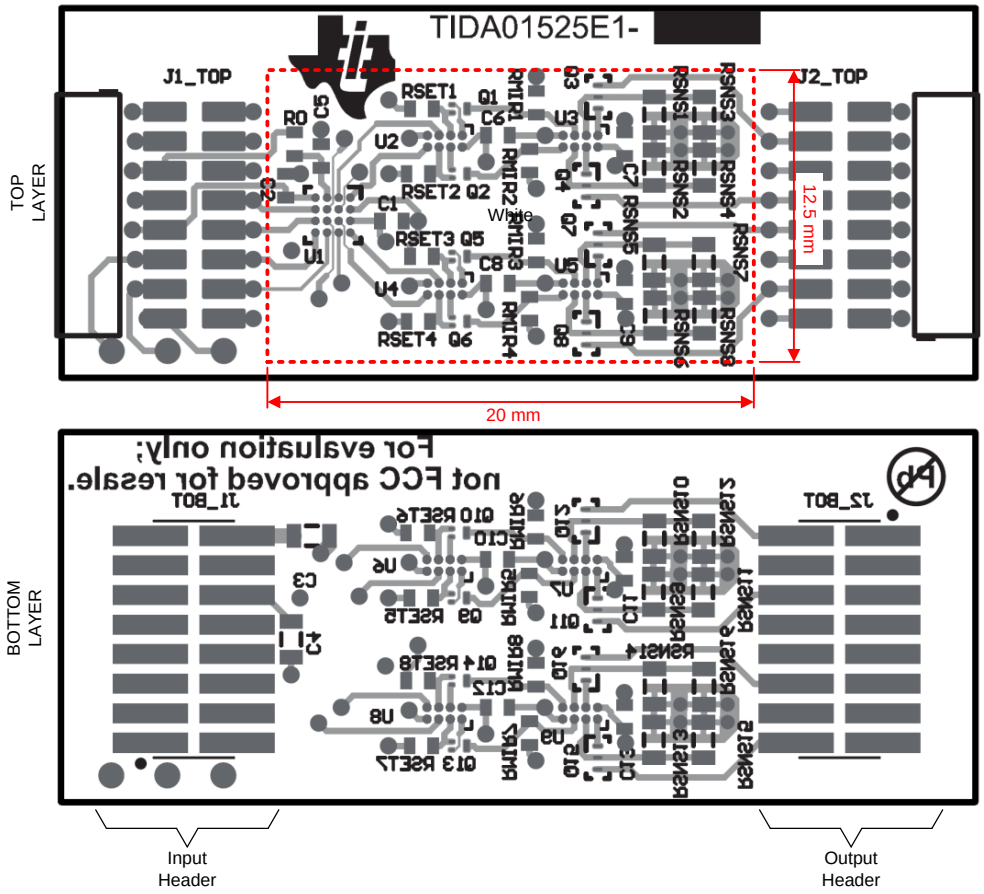


図 3. TIDA-01525 PCB Design

2.2.5 TINA-TI™ Simulation Software

The output transfer function can be verified using the TINA-TI™ simulation software. 図 4 shows the simulation. The DAC80508 is simulated with an ideal voltage source for this experiment. Accurate models for the OPA2376 and both MOSFETs are available at the product pages for those devices. 図 5 shows the simulated results, and verifies that the transfer function result is the expected full-scale output current.

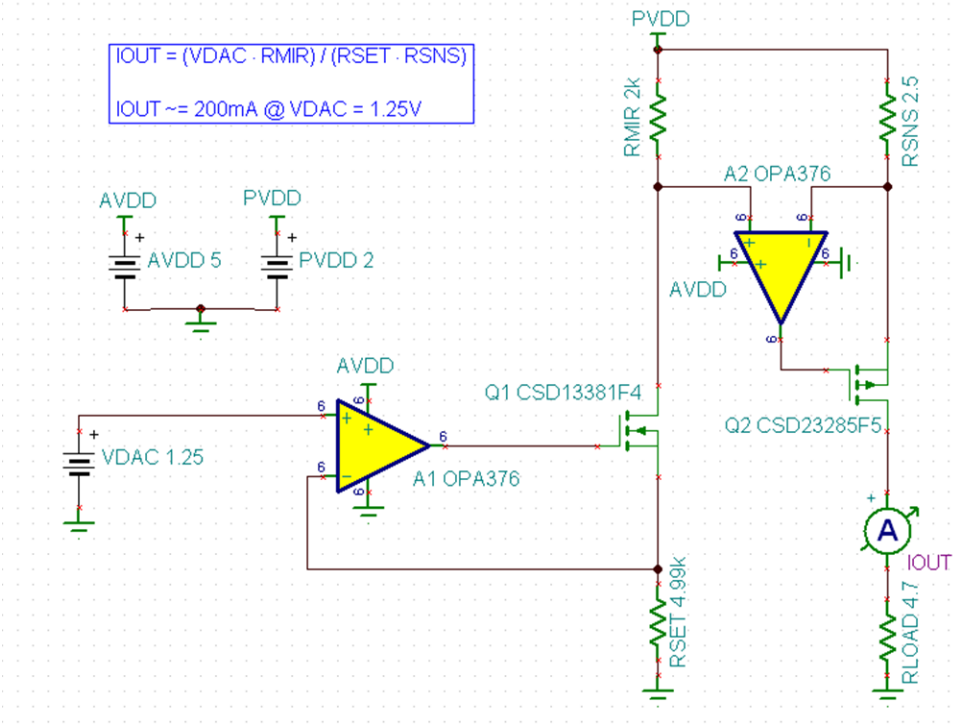


図 4. Simulation Using TINA-TI™ Software

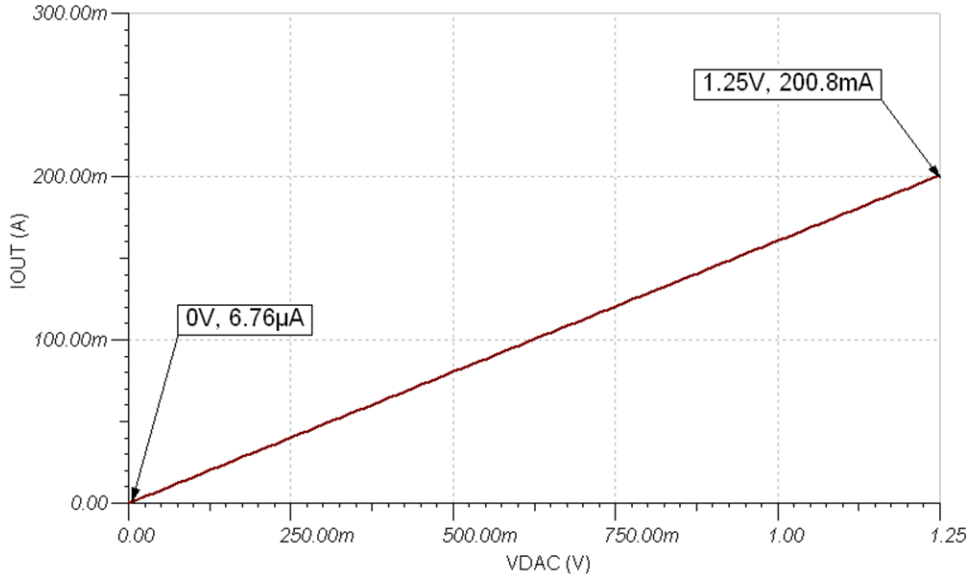


図 5. I_{OUT} Transfer Function TINA-TI™ Simulation Software Results

2.3 Highlighted Products

The following highlighted products are used in this reference design. The key features for selecting the devices for this reference design are outlined in the following subsections. For the complete details of the highlighted devices, refer to the respective product data sheets. As many laser drive applications require a high channel density, a major factor in the component selection for this reference design is a small package size. 図 6 shows a relative comparison of the size of the major components of the system.

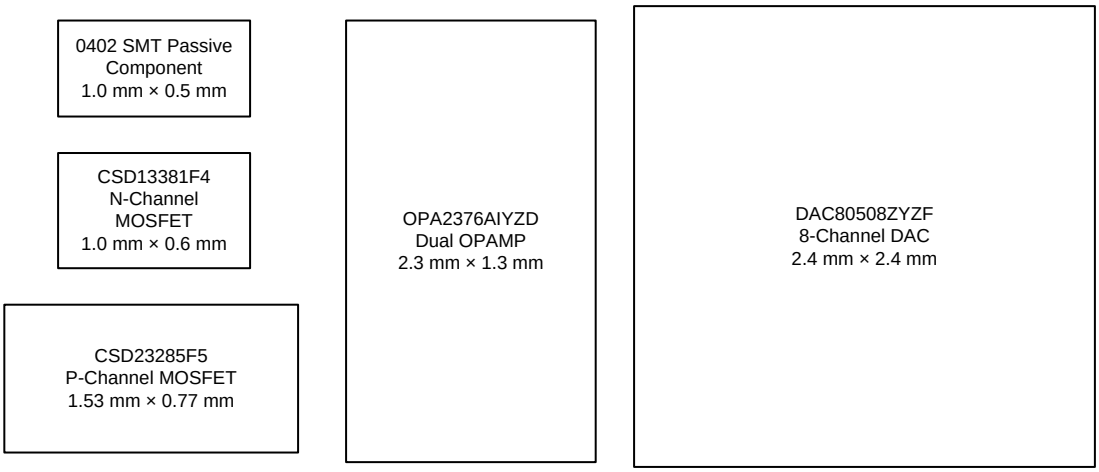


図 6. Package Size Comparison

2.3.1 DAC80508

The DAC80508 is a pin-compatible family of low-power, eight-channel, buffered voltage-output, digital-to-analog converters (DACs) with 16-bit resolution. The DAC80508 includes a 2.5-V, 5-ppm/°C internal reference that eliminates the need for an external precision reference in most applications. A user-selectable gain configuration provides full-scale output voltages of 1.25 V (gain = ½), 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7-V to 5.5-V supply, is specified monotonic, and provides high linearity of ±1 LSB INL.

Communication to the DAC80508 is performed through a serial interface that operates at clock rates of up to 50 MHz. The VIO pin enables serial interface operation from 1.7 V to 5.5 V. The flexible interface of the DAC80508 enables operation with a wide range of industry-standard microprocessors and microcontrollers.

The DAC80508 incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device. The device consumes low current of 0.6 mA/channel at 5.5 V, making the device suitable for battery-operated equipment. A per-channel power-down feature reduces the device current consumption to 15 µA.

The DAC80508 is characterized for operation over the temperature range of –40°C to +125°C, and is available in a 2.4-mm × 2.4-mm WCSP package. This small package size makes this device an excellent choice for high-density applications.

2.3.2 OPA2376

The OPA2376 is a dual, low-noise, e-trim™ operational amplifier that offers outstanding dc precision and dc performance. Rail-to-rail input and output, low offset (25 µV, maximum), low noise (7.5 nV/√Hz), quiescent current of 950 µA (maximum), and a 5.5-MHz bandwidth make this device very attractive for a variety of precision and portable applications. The PVDD supply used for the laser is often minimized to reduce power consumption of the MOSFET and resistor on the output stage of the design. Therefore, the rail-to-rail output feature of the device makes it an excellent choice for the high-side current source for laser-drive applications. This dual op amp is offered in a small, 2.3-mm × 1.3-mm DSBGA package.

2.3.3 CSD13381F4 and CSD23285F5

The FemtoFET™ MOSFETs in this design are selected because of their very small package size. The CSD13381F4 is a 140-mΩ, 12-V N-channel MOSFET designed and optimized to minimize the footprint in many handheld and mobile applications. The N-channel MOSFET is offered in a 1.0-mm × 0.6-mm package. The CSD23285F5 is a 29-mΩ, –12-V, P-Channel MOSFET that features a 1.53-mm × 0.77-mm package.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Hardware

図 7 shows that the design hardware consists of the TIDA-01525 reference design PCB and a custom test bench PCB. The test bench allows for easier access to the supplies and current output connections. The test bench also enables the design PCB to remain very dense while still having the convenience of connectors for common lab equipment.

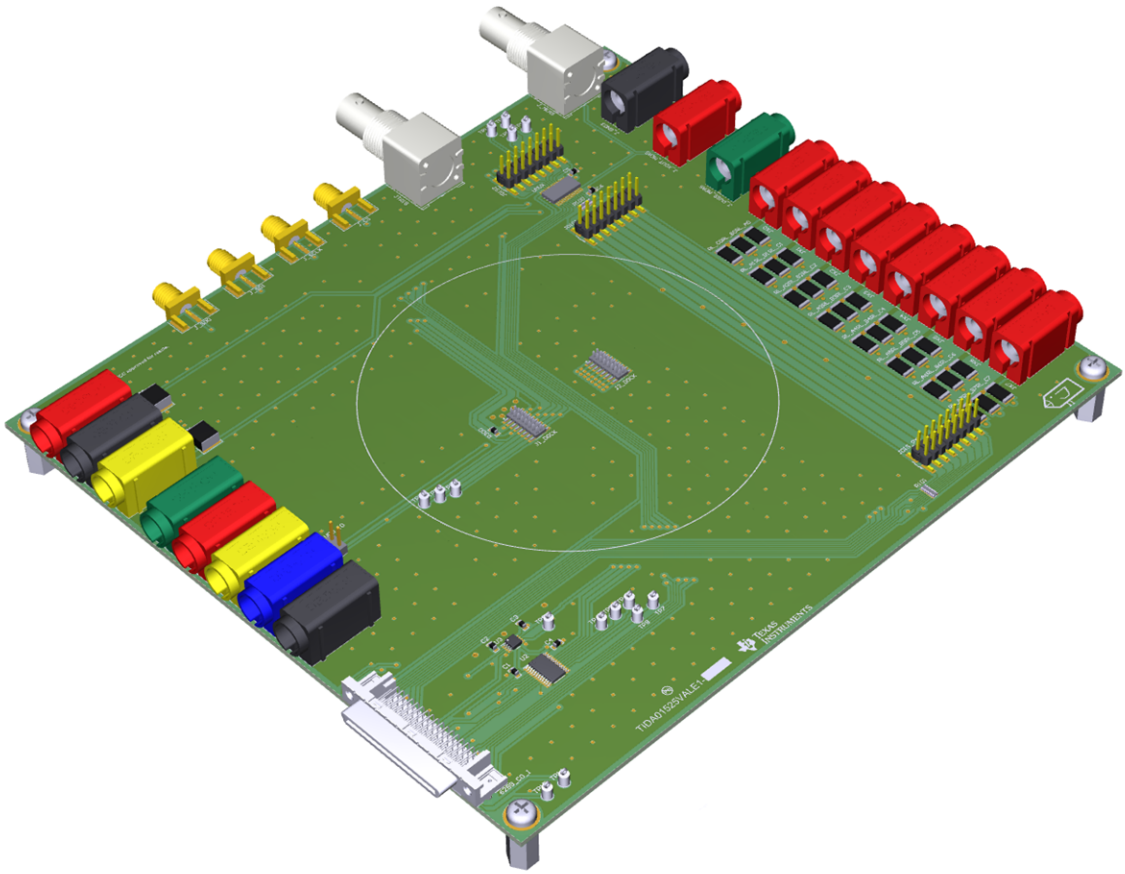


図 7. Test Board

3.2 Testing and Results

3.2.1 Test Setup

The test setup for this design features four pieces of external equipment.

The National Instrument PXI-6289 features digital I/O used to generate the SPI data that control the DAC80508 device on the TIDA-01525 board. In addition, the digital I/O is used to control the MUX featured on the test board that connects the IOUT signals to external meters. Although not shown in 図 8, the PXI-6289 18-bit ADC analog inputs are also connected to the IOUT signals. This connection allows for fast parallel measurement of the IOUT signals, although higher levels of averaging must be implemented to achieve very accurate measurements.

The meter in this system is the Agilent 3458B, an 8.5-digit, digital multimeter (DMM). For the majority of the tests, the 3458B is configured to operate in a 1-V range, with two power-line cycles per acquisition. For some of the test, the DMM was removed from the system and replaced with an oscilloscope or spectrum analyzer.

The system is powered by two supplies. The first supply, an Agilent E3631A triple-rail supply, is used to power the onboard MUX. To provide accurate measurements of the IOUT pins, the MUX needs additional negative headroom, so the negative supply input of the MUX is connected to a –5-V potential. The other supply is a Keysight N6702A modular power supply mainframe. This supply sources the nominal +5-V input for the DAC80508 and OPA2376s featured in the design. The high-current PVDD supply was also sourced from the N6702A. Take care to select a supply that can source the maximum expected current of 1.6 A (8 channels × 200 mA).

図 8 shows that 4.7-Ω load resistors are used on the IOUT signals to convert the current output to a voltage for easy measurement with the 3458B. Given that our expected maximum current is approximately 200 mA, a load of 4.7 Ω has a maximum voltage differential of 940 mV. This output range is optimized for the DMM high-precision 1-V range.

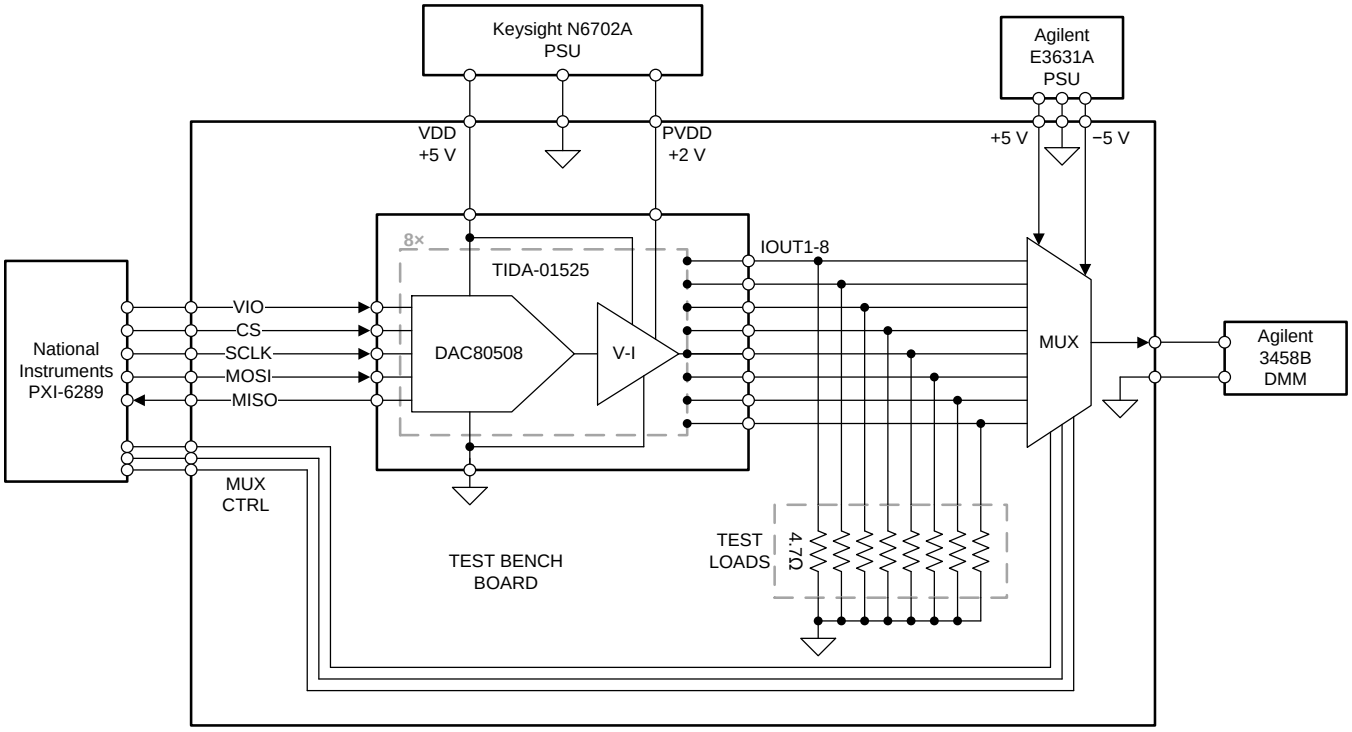


図 8. Test Setup Block Diagram

3.2.2 Test Results

This section describes the test measurements accomplished on the system, and describes the setup and configuration used to realize them.

3.2.2.1 Total Unadjusted Error

3.2.2.1.1 Total Unadjusted Error Test Configuration

Total unadjusted error is measured on the system using the configuration shown in 図 9. Total unadjusted error, or TUE, is the difference between the actual measured transfer function of the system and the ideal transfer function as calculated. This error is unadjusted; therefore, error from sources like resistor mismatch, reference inaccuracy, and DAC nonlinearity are not removed from the calculation.

The resistive values of the test loads must be accurately known, so that any error in those resistors is not represented in the measurement. To validate this condition, the individual resistance values were directly measured on the board and logged. The resistors must be directly measured so that the ON resistance of the MUX is not added to the resistor values. In addition, care must be taken to insulate these resistors from temperature change during the test.

The data for the measurement is collected by using the PXI-6289 to sweep the DAC80508 input code for all channels. After each code is sent to the DAC, the PXI-6289 sets the MUX to each channel, and the 3458A measures the value. This value is then divided by the known resistor value of the test loads, and the calculated current value is then logged. Make sure to allow a short time delay after changing the MUX input to allow the output to settle.

3.2.2.1.2 Total Unadjusted Error Measurement Results

図 9 shows the total unadjusted error for three systems, all channels. There are two main components to the error, offset error and gain error. The offset error is mostly the result of the DAC itself, with some additional offset contributed by the V_{OS} of the two amplifiers. The gain error can be attributed to the errors in the resistor values, with the DAC reference also contributing a small portion. An external reference for the DAC improves the accuracy, but at the expense of board space and additional cost.

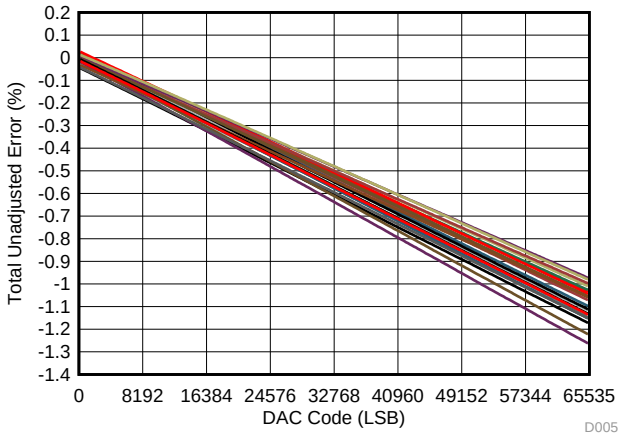


図 9. Total Unadjusted Error

3.2.2.2 Current Noise Density

3.2.2.2.1 Current Noise Density Measurement Setup

The current noise density is measured with the National Instruments PXI-5922, a high-precision oscilloscope. For this test configuration, the DAC80508 is programmed by the PXI-6289 to the full-scale output current, 200 mA. The test board is configured to connect a channel through the MUX to the PXI-5922, taking the place of the 3458B DMM. The PXI-5922 is then used to capture many thousands of samples for a few seconds, which are then processed by a program to generate a FFT of the data. This result was also scaled back to a current value and converted to the power domain.

3.2.2.2.2 Current Noise Density Results

The current noise density is measured from 10 Hz to 100 kHz. The noise in the system is dominated by the DAC80508 internal voltage reference. Using the internal reference results in the system being less complex, and allows for cost savings; however, noise can be improved by using an external reference.

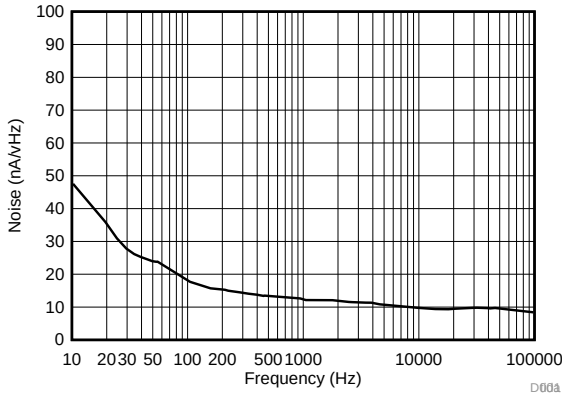


図 10. Current Noise Density

3.2.2.3 Bandwidth-Limited RMS Current Noise

3.2.2.3.1 Bandwidth-Limited RMS Current Noise Setup

The bandwidth-limited RMS noise is measured in the same fashion as 図 10, with additional measurements at one-quarter scale and half scale. The RMS noise value is calculated from the noise spectral density. This calculation is achieved by integrating the square of the current noise spectral density over the bandwidth of interest to calculate noise power. The RMS noise current is the square-root of the noise power, which is the integral of the square of the noise density, as shown in 式 11. In this case, the bandwidth of the measurement is limited from 10 Hz to 100 kHz.

$$\text{Noise Current} = \sqrt{\text{Noise Power}} = \sqrt{\int_{f_1}^{f_2} i_n^2 \, df} \tag{11}$$

3.2.2.3.2 Bandwidth-Limited RMS Current Noise Measurement

表 2 shows the calculated current noise based from the noise spectrum measurements at the different DAC output values.

表 2. Bandwidth-Limited RMS Current Noise

DAC Output Code (LSB)	Approximate Current Output (mA)	Current Noise (μA_{RMS})
0x4000	50	3.1
0x8000	100	3.4
0xFFFF	200	4.3

3.2.2.4 Zero-Scale Error

Zero-scale error (ZSE) is the output current when the DAC is outputting the lowest possible value. The DAC80508 features a unipolar supply input, meaning that the device does not have a negative supply. As a result, the output at code zero is not 0 V, but rather the closest voltage the output buffer can supply with respect to ground. ZSE can be critical in current-source applications, specifically laser-drive, because the zero-scale current can be considered wasted energy or even enable some low-power output state to occur.

3.2.2.4.1 Zero-Scale Error Setup

The zero-scale error is measured by using the PXI-6289 to configure the DAC80508 device to the 1.25-V output range and configure the DAC values to code zero. The DMM is then used to measure the current on the output of each channel. The ZSE is calculated as the difference between the real output current and the ideal output current. The ZSE is easy to calculate because the ideal current at code zero is 0 A, so any current measured is entirely error.

3.2.2.4.2 Zero-Scale Error Measurement

The output behavior of the system is seen in 図 11. As discussed previously, the DAC cannot output 0 V, and requires a minimum headroom for the output buffer to accurately drive the output voltage. 図 11 shows that the system requires approximately 64 LSB before the DAC can operate in the linear region. 図 12 shows the distribution of the zero-scale error for all eight channels of three systems. The maximum voltage measured is below 120 µA of error.

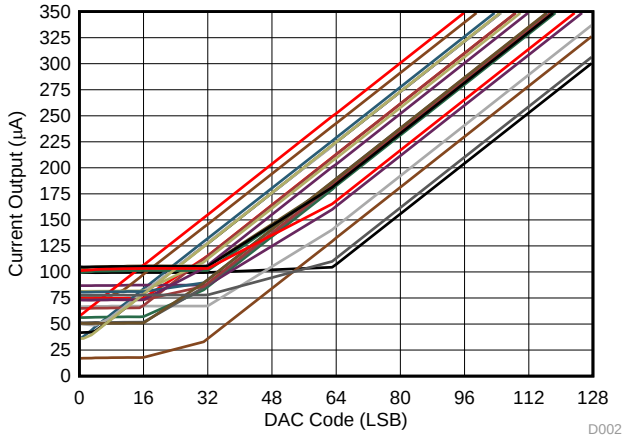


図 11. I_{OUT} Near Zero-Scale

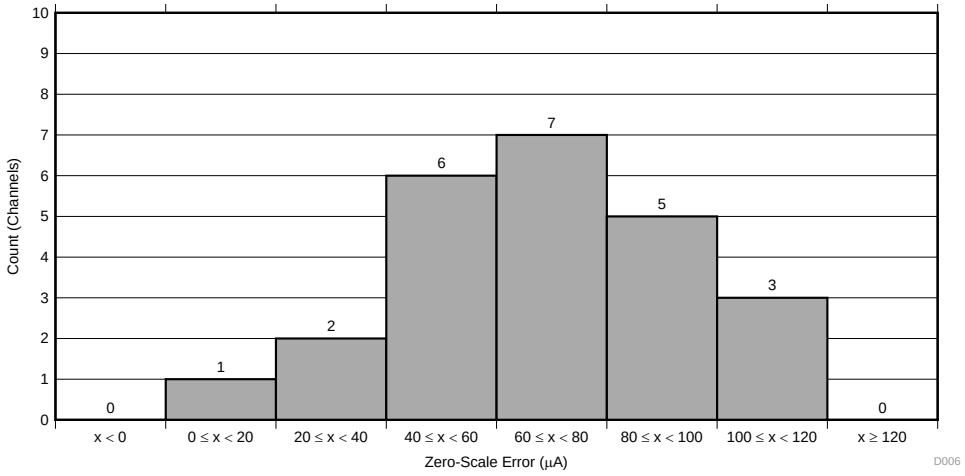


図 12. Zero-Scale Error Measurement

3.2.2.5 Minimum PVDD Supply Voltage

Any voltage headroom that is not necessary for the voltage drop across the load or diode and the voltage across R3 results in extra power dissipation across the P-channel MOSFET. Therefore, a key design goal for high-side current-sources in laser drive applications is to minimize the PVDD supply. However, minimizing PVDD can result in extra heat generation and general inefficiency. The minimum supply voltage is the lowest PVDD voltage the system can use while still being able to source the desired full-scale current.

3.2.2.5.1 Minimum PVDD Supply Voltage Setup

The minimum supply voltage was measured by using the PXI-6289 to set the DAC output to the full-scale value, 0xFFFF, or approximately 200 mA on the current output. While in this state, the DMM is used to measure the current output, while the N6702A is used to incrementally lower the PVDD supply. The full-scale current error is calculated at each point. At some point, the system cannot source the correct current and the FSE rapidly changes.

3.2.2.5.2 Minimum PVDD Supply Voltage Measurement

図 13 shows the FSE as the PVDD is varied from 1.5 V to 4 V. 図 13 shows that the FSE is relatively constant until the PVDD supply becomes less than 1.75 V. This This supply voltage is the minimum required headroom voltage for the system. The voltage across R1 will be 1.25 V unless the DAC range is modified, and the reference current created induces a voltage of approximately 500 mV across R2. These two voltages make the required 1.75 V, as shown in 図 13. If lower voltage (and power dissipation) is desired, scale back the resistor values of R2 and R3 to a lower value, while still maintaining the same ratio.

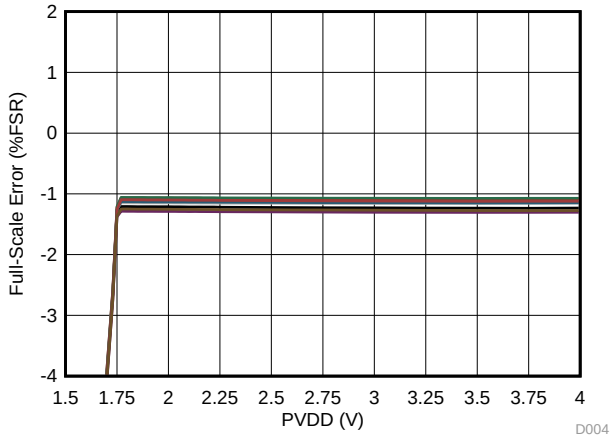


図 13. Minimum PVDD Voltage

4 Design Files

4.1 Altium Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-01525.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01525.

4.1.3 PCB Layout Recommendations

When designing the PCB for the reference circuit, consider the following layout recommendations:

- Place the capacitor for the DAC80508 reference output close to the pin in order to minimize external noise from being coupled into the reference voltage.
- Bypass all power supply pins to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1-µF to 0.22-µF ceramic with a X7R or NP0 dielectric.
- Use wider trace widths for the current output path that can accommodate the full-scale current.
- Connect R3 to a large copper area to assist in heat dissipation.

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01525.

4.2 Gerber Files

To download the Gerber files, see the design files at TIDA-01525.

4.3 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01525.

5 Related Documentation

1. *High-Side Voltage-to-Current (V-I) Converter Design Guide*
2. *High-Density DACs Offer Superior Noise And Accuracy Performance in Laser-Drive Applications Application Brief*

5.1 商標

6 About the Author

Paul Frost is an Applications Engineer with the Digital to Analog Converters team supporting catalog, industrial, and audio DACs. He earned his BSCE from University of Arizona.

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。