参考資料

TI Designs: TIDA-050023
Type 3 IEEE802.3bt対応のフライバック・コンバータPoE受電デバイスのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このTIリファレンス・デザインでは、PoE受電デバイス(PD)用のType-3、Class 6、51Wのフライバック・コンバータを紹介します。TPS2373-3 PDコントローラは検出と分類を行うと同時に、高度なセットアップ機能によりLM5155-Q1 PWMコントローラを起動します。このデザインは42V～57VのPoE入力および出力と、IPネットワーク・カメラやワイヤレス・アクセス・ポイント用の12Vレールを持ちます。

リソース

TIDA-050023	デザイン・フォルダ
TPS2373	プロダクト・フォルダ
LM5155-Q1	プロダクト・フォルダ
TL431LI	プロダクト・フォルダ

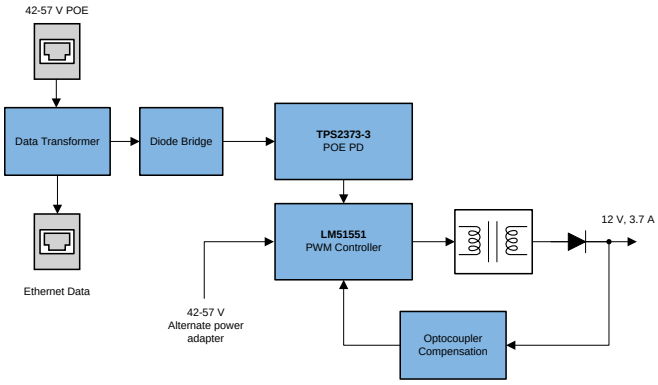
TI E2E™ Community　E2E™エキスパートに質問

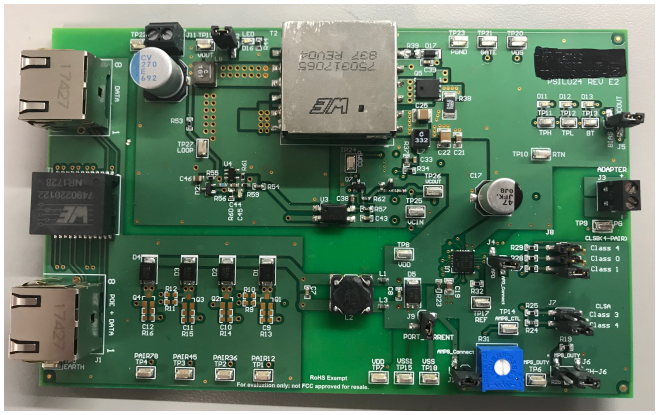
特長

- IEEE802.3bt Type 3の電力レベルをサポート
- 絶縁ダイオード整流のフライバック・デザイン
- ヒカップ・モード保護を内蔵
- 過電流フォルト時の優れた熱特性
- PMWコントローラ用のPD Advancedスタートアップ
- 論理和回路によるAC/DC経由の補助電力
- 自動電源シグネチャ保持(MPS)
- 内蔵の低い0.3Ω電源スイッチにより60WのPSE電力をサポート

アプリケーション

- IPネットワーク・カメラ
- ワイヤレス・アクセス・ポイント
- 25Wを超えるPoE PDデザイン





1 System Description

The IEEE802.3bt standard allows the implementation of >25-W PoE designs on a compliant, uniform standard over all four data pairs of the ethernet connector. This Type-3, 50-W PoE flyback converter design is intended for users to develop such end products for various cost sensitive communication and industrial applications that require over 25 W of power on a 12-V rail. This reference design provides a complete guide for the hardware design of a diode rectified flyback converter. The design files include Schematics, Bill of Materials (BOMs), Atlium files, Gerber Files and Fabrication Files.

This isolated flyback design has an input voltage range of 42 V - 57 V for PoE and an optional auxiliary 42-V to 57-V power supply path which will be prioritized if enabled. The output of this design is 12-V at 3.7-A (44.4 W) which provides higher power than the previous sub-25-W IEEE802.3at standard allowed. As mentioned earlier, this design was optimized for low cost applications so a diode rectified implementation was selected along with a low cost, lower voltage PWM controller: LM5155-Q1.

To allow for the use of a lower voltage PWM controller on a high voltage 42-V to 57-V input rail, the advanced startup feature of the IEEE802.3bt compliant TPS2373-3 was enabled to provide a startup mechanism for the LM5155-Q1. This design also has hiccup mode protection enabled which provide excellent thermal protection during faults.

1.1 Key System Specifications

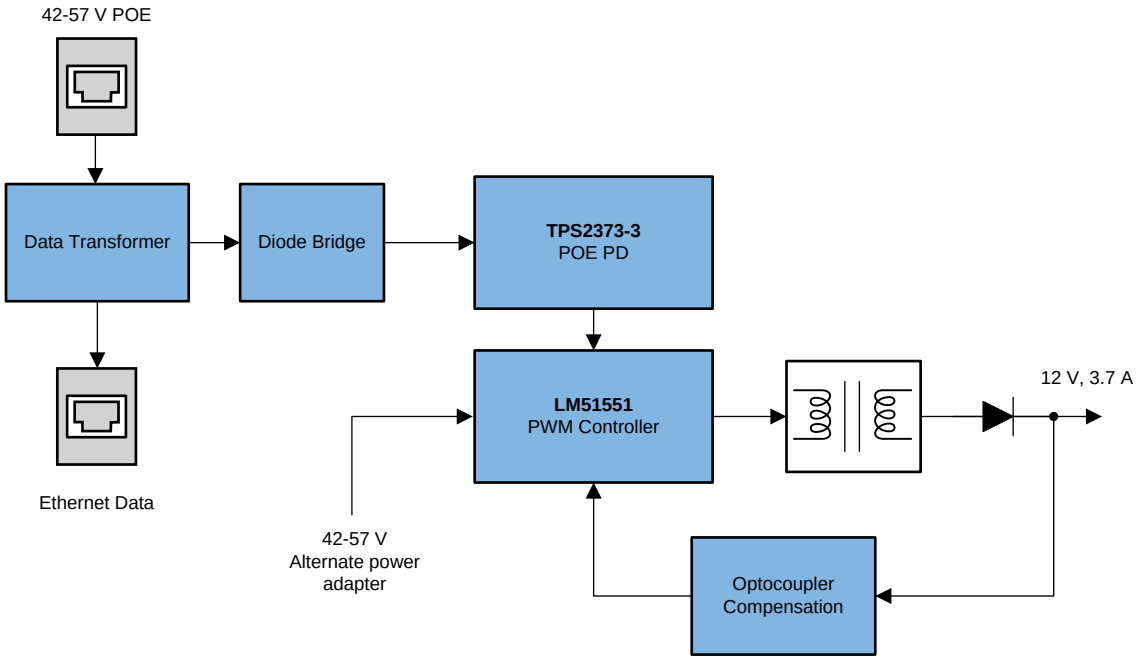
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
PoE Input voltage range	42 V - 57 V
Adaptor input voltage range	42 V - 57 V
Output voltage	12 V
Output current (PoE input)	3.7 A
Output current (adapter input)	4.25 A
PoE PD Classification	Class 6
PoE Efficiency	88%
Converter Efficiency	91%

2 System Overview

2.1 Block Diagram

図 1. TIDA-050023 Block Diagram



2.2 Highlighted Products

2.2.1 TPS2373-3

The TPS2373-3 is a IEEE802.3bt compliant powered device (PD) interface that supports Type-3 PoE. All basic functionality such as detection, classification, inrush current limit (200 mA) and automoatic maintain power signature (MPS) are integrated into a small form factor. A 0.3-Ω internal switch supports Type-3 up to 60 W of continuous power from the PSE which allows beyond 1.2 A through the PD during normal operation.

A critical TPS2373-3 feature to the design of this application is the advanced startup function. After proper detection, classification and inrush management, the TPS2373-3 will power up the downstream PWM controller through an internal regulator (V_{COUT}). Once the downstream DC-DC converter has ramped up its output voltage on the bias winding of the power transformer (V_{CIN}), the TPS2373-3 will internally connect the bias winding to V_{COUT} and complete startup. This feature allows a lower voltage and lower cost PWM controller to be used in a higher power design.

The TPS2373-3 also features an auxiliary power detect (APD) input that allows an auxiliary supply to power the load. In scenarios where both PoE and the auxiliary supply are present, the TPS2373-3 allows the auxiliary supply to take priority over PoE.

The TPS2373-3 also contains several protection features such as thermal shutdown, current limit foldback and a robust 100-V internal switch.

2.2.2 LM5155-Q1

The LM5155-Q1 is a wide input range, non-synchronous controller that can be used in boost, SEPIC and flyback topologies. Its input voltage range of 3.5 V to 45 V is lower than PoE voltage (57 V) but can be used in PoE applications because of the advanced startup feature of the TPS2373-3. This device also has a configurable switching frequency from 100 kHz to 2.2 MHz with a 1.5-A standard MOSFET driver and a low 100-mV current limit threshold. In addition, low operating current and pulse skipping operation improves efficiency at light load.

The LM5155-Q1 also has built in protection features such as cycle-by-cycle current limit, overvoltage protection, undervoltage lockout (UVLO), thermal shutdown and hiccup mode protectionwhich improves thermal performance during faults. Additional features include low shutdown I_Q , programmable soft start, programable slope compensation, precision reference, power good indicator and external clock synchronization.

2.2.3 TL431LI

The TL431LI is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

2.3 System Design Theory

2.3.1 IEEE802.3bt Introduction

PoE hardware classification allows the Power Sourcing Equipment (PSE) to determine the power requirements of a Powered Device (PD) before supplying power. This classification processes assists with power budgeting and efficiency. Prior to the IEEE802.3bt standard, the IEEE802.3at standard allowed up to 30 W of power sourced at the PSE and 25.5 W of power at the PD for Class 4 across two pairs of the ethernet cable.

表 2. IEEE802.3at Power Types and Classes

Class	Type	Number of Pairs	Power Sourced at PSE	Minimum Power at PD
0	1	2	15.4 W	13.0 W
1	1	2	4 W	3.84 W
2	1	2	7 W	6.49 W
3	1	2	15.4 W	13.0 W
4	2	2	30 W	25.5 W

The IEEE802.3bt standard utilizes all four pairs of the ethernet connector and increases the maximum power the load can consume as well as the power the PSE can supply. Two new types are established under the IEEE802.3.bt standard: Type 3 (60-W PSE) and Type 4 (90-W PSE). With this increased power rating, various end equipments such as surveillance cameras and access points can incoporate more features such as analytics, rotation and heaters. 表 3 highlights the IEEE802.3bt types and classes.

表 3. IEEE802.3bt Power Types and Classes

Class	Type	Number of Pairs	Power Sourced at PSE	Minimum Power at PD
0	1 or 3	2	15.4 W	13.0 W
1	1 or 3	2 or 4	4 W	3.84 W
2	1 or 3	2 or 4	7 W	6.49 W
3	1 or 3	2 or 4	15.4 W	13.0 W
4	2 or 3	2 or 4	30 W	25.5 W
5	3	4	45 W	40.0 W
6	3	4	60 W	51.0 W
7	4	4	75 W	62.0 W
8	4	4	90 W	71.3 W

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This Type-3, Class 6 PoE reference design can be configured in multiple modes of operation. This section will cover the setup required to evaluate this design.

3.1.1 Hardware

図 2. TIDA-050023 Reference Board (Top)

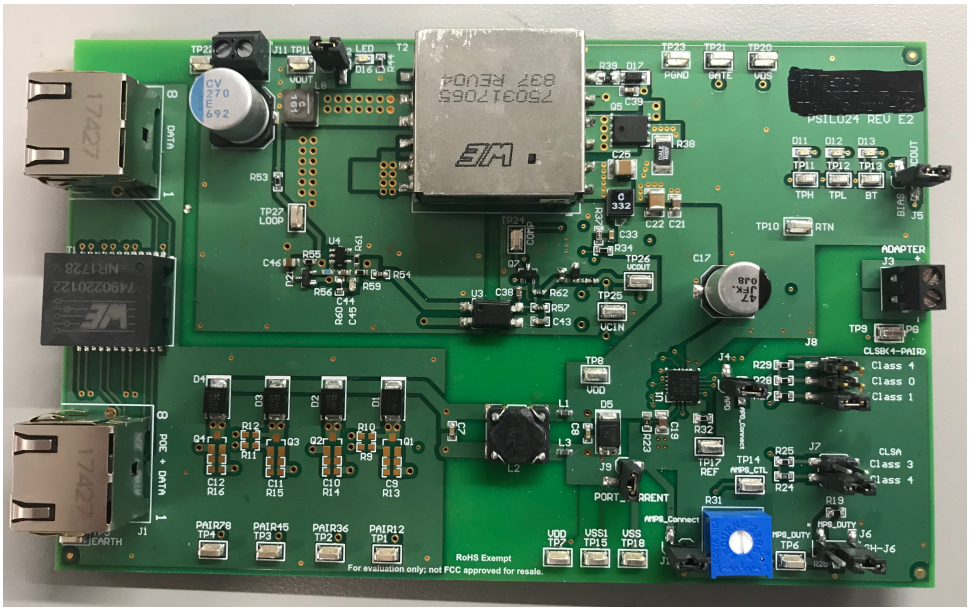


図 3. TIDA-050023 Reference Board (Bottom)

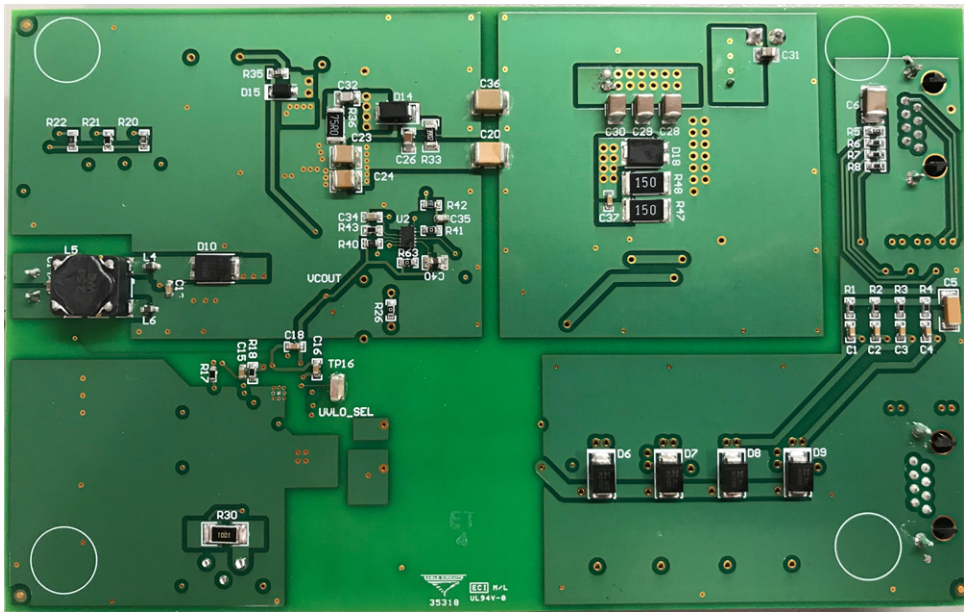


表 4. Table of Jumpers and Connectors

Type	Label	Connector /Jumper	Description
Input	Ethernet Power	J1	Input connector for PoE
	Ethernet Data	J2	Data ouput after data transformer
	Adaptor Input	J3	42-V to 57-V adaptor input. J4 jumper must be connected to enable adaptor power delivery

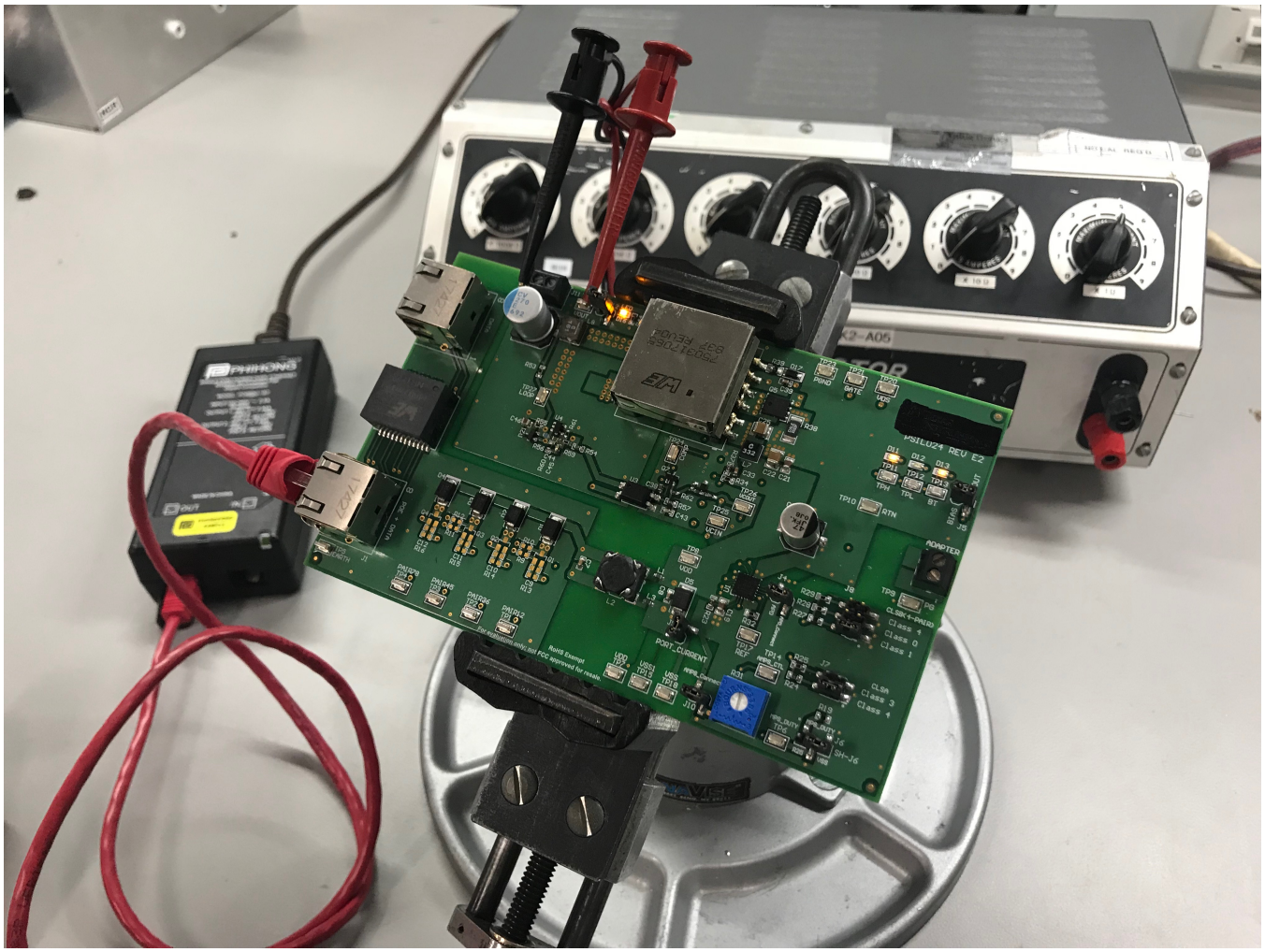
表 4. Table of Jumpers and Connectors (continued)

Type	Label	Connector /Jumper	Description
PD Configuration	APD_Connect	J4	Enable to allow adaptor power delivery
	BIAS	J5	Enable to provide pull up voltage for open drain, active low classification outputs.
	MPS_DUTY	J6	Configurable duty cycles for MPS pulse: 8.1% (60.4 kΩ), 12.5% (short), 5.4% (open).
	Classification Resistors	J7	1st PD Class Resistor Setting
		J8	2nd PD Class Resistor Setting
	Port Current	J9	Enable for PoE port current
	AMPS_CTL	J10	Automatic MPS control. Enable to allow adjustable resistor to program MPS current amplitude.
Output	V_{OUT}	J11	12-V output of design
	Output LED	J12	Enable to provide LED output during 12-V regulation.

3.2 Testing and Results

This section describes the test setup and test results for the TIDA-050023 board.

図 4. TIDA-050023 Setup with Power Supply and Load



3.2.1 Test Setup

The jumpers and connectors configurations is shown in 表 5:

表 5. TIDA Jumper and Connector Configuration

Type	Label	Jumper/Connector	Value
Input	Ethernet Power	J1	Power supply with voltage from 42 V to 57 V.
	Ethernet Data	J2	Open
	Adaptor Input	J3	Open for PoE tests. Connected to 42-V to 57-V power supply for adaptor tests
PD Configuration	APD_Connect	J4	Connected
	Bias	J5	Connected
	MPS_Duty	J6	12.5% (1-3)
	Classification Resistors	J7	1-2 (Class 4)
		J8	1-2 (Class 1)
	Port Current	J9	Connected
	AMPS_CTL	J10	Connected
Output	V_{OUT}	J11	Connected to electronic load. At full load, resistor load is 3 Ω.
	Output LED	J12	Connected

3.2.2 Test Results

The following section provides the performance and test results of this design.

3.2.2.1 Efficiency

図 5 shows the efficiency performance of the design across the entire operating voltage range and load current. 図 6 shows the efficiency performance at 48 V for PoE, Adatpor input and DC/DC only.

図 5. 42-V to 57-V PoE Efficiency

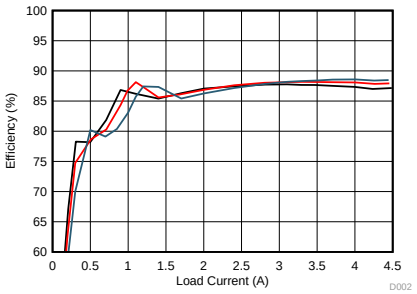
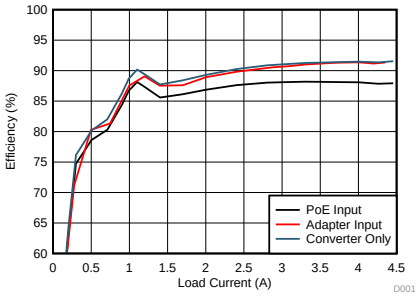


図 6. 48-V Efficiency for PoE, Adapter and DC/DC Converter



3.2.2.2 Control Loop Gain/Stability

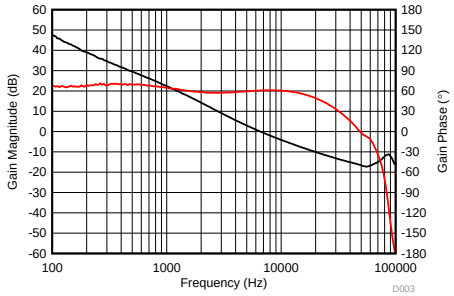
The loop gain margin, phase margin and crossover frequency are listed below along with the Bode plot 48 V at full load.

Gain Margin: –16 dB

Phase Margin: 60.8°

Crossover Frequency: 6.6 kHz

図 7. Loop Gain and Phase Margin at 48 V



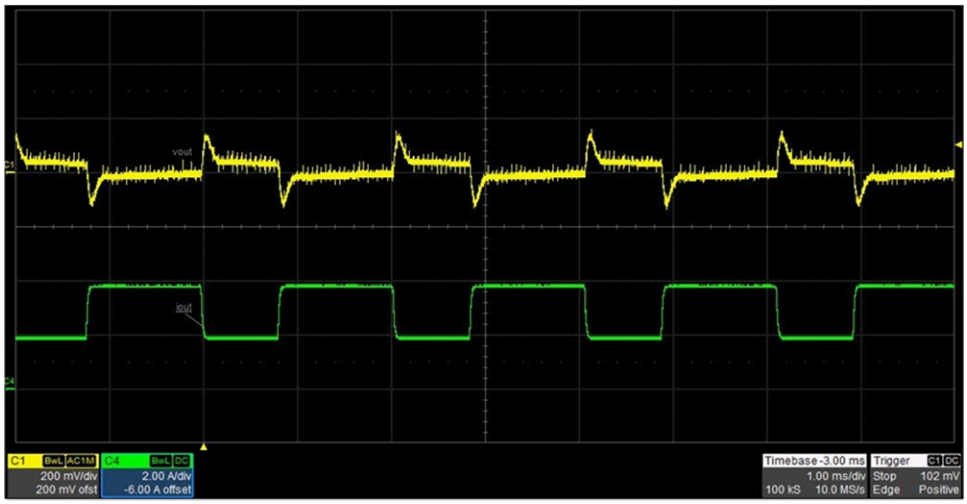
3.2.2.3 Load Transient

図 8 shows the 12-V output voltage (at J11) when the load current pulses between 0.37 A and 3.7 A. The input voltage is 48 V at J1.

図 8. 0.37-A to 3.7-A Load Step, 48 V_{IN}, 200 mV/div, 1 ms/div

図 9 shows the 12-V output voltage (at J11) when the load current pulses between 1.85 A and 3.7 A. The input voltage is 48 V at J1.

図 9. 0.37-A to 3.7-A Load Step, 48 V_{IN}, 200 mV/div, 1 ms/div



3.2.2.4 Input and Ouput Ripple

The input ripple shown in 図 10 and output ripple shown in 図 11 were measured with an input voltage of 48 V (at J1), an output load of 3.7 A (at J11) and 20-MHz BWL.

図 10. Input Ripple, 20 mV/div, 1 µs/div

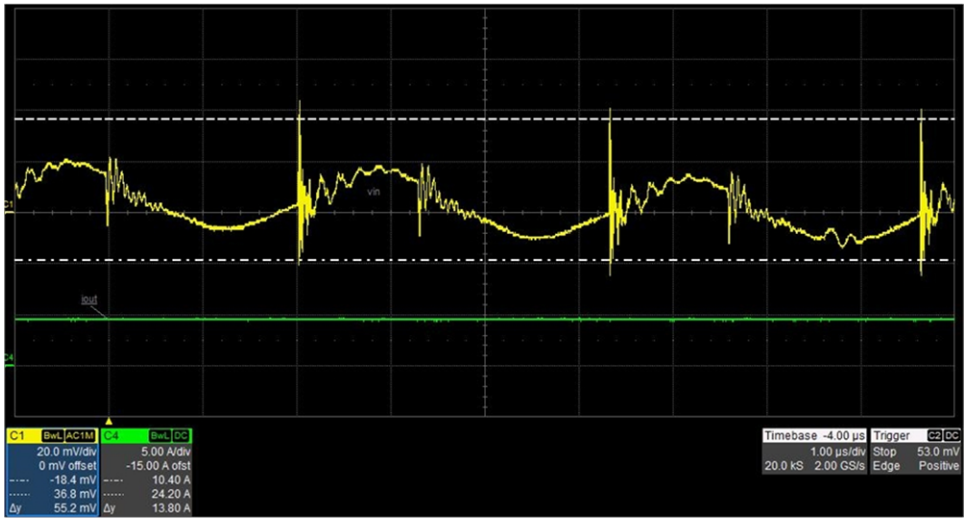
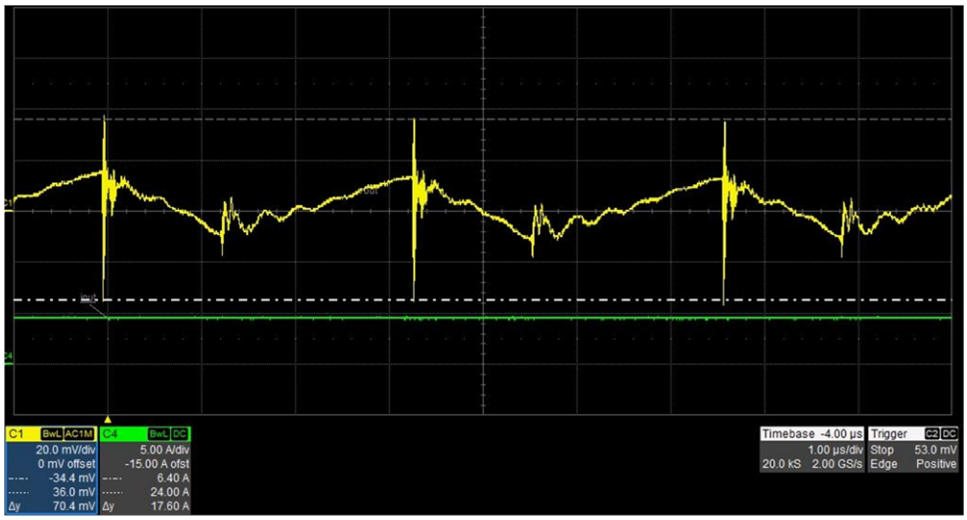


図 11. 12-V Ouput Ripple, 20 mV/div, 1 µs/div



3.2.2.5 Switching Waveforms

図 12 shows the V_{DS} voltage of primary switching MOSFET (Q5) and 図 13 shows the voltage across the secondary side rectifying diode (D18) at 3.7-A load. The input voltage is 48 V.

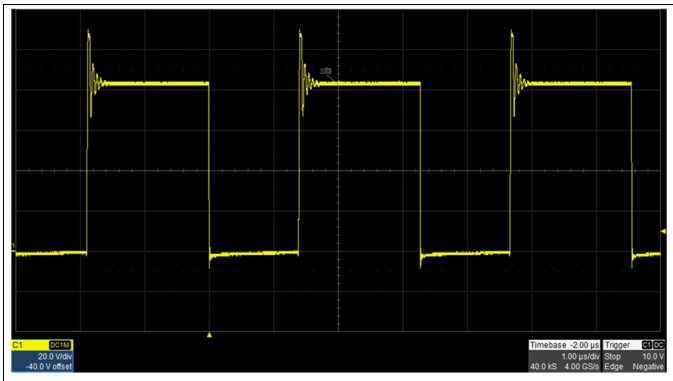


図 12. Primary MOSFET Voltage, 3.7-A Load, 20 V/div, 1 µs/div

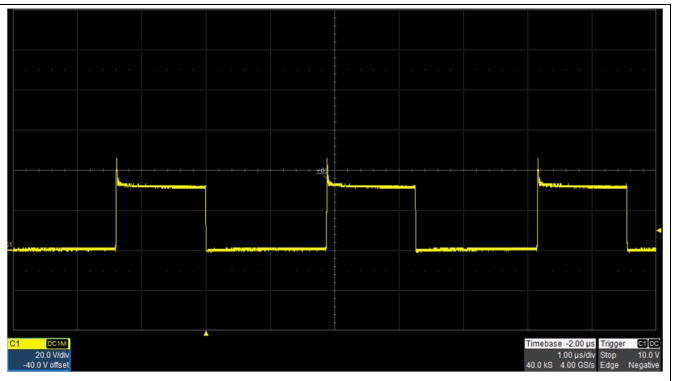
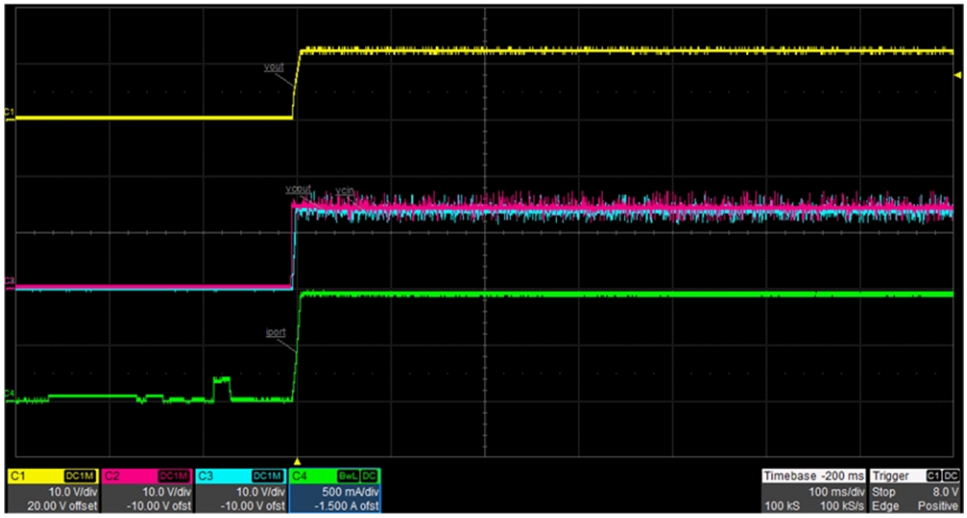


図 13. Secondary Diode Voltage, 3.7-A Load, 20 V/div, 1 µs/div

3.2.2.6 Start Up Response

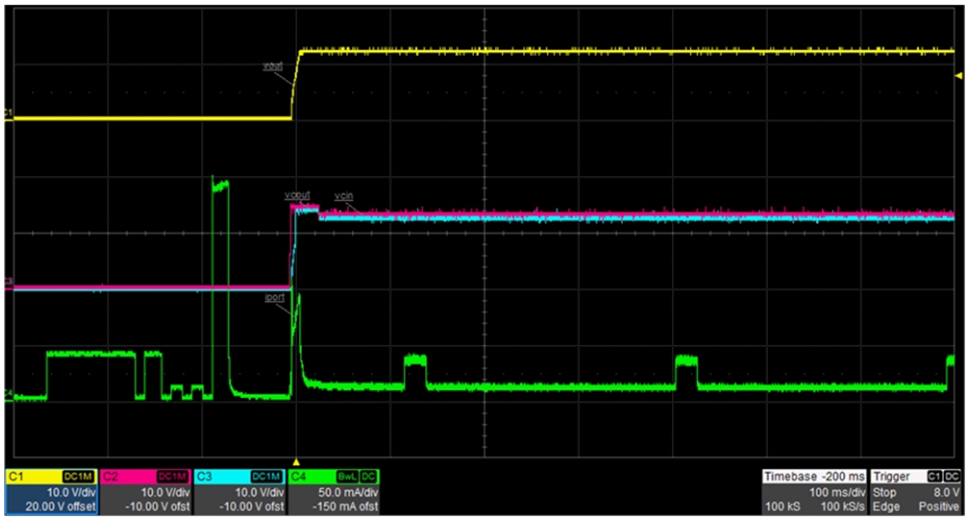
図 14 and 図 15 shows the 12-V output start up waveform after the application of 48 V at the PoE input (J1). The output was loaded to 3.7 A 図 14 and 5 mA 図 15. Both waveforms include the output voltage (yellow), V_{COUT} (pink), V_{CIN} (blue) and port current (green). Note that port current is 500 mA/div in 図 14 and 50 mA/div in 図 15.

図 14. Startup Waveforms at 3.7-A Load, 100 ms/div



The port current below shows the classification pulses classifying this as a Class 6 (51-W) Powered Device. The Maintain Power Signature (MPS) pulses which present a signal to the Power Sourcing Equipment (PSE) to maintain power at light load are also observed here.

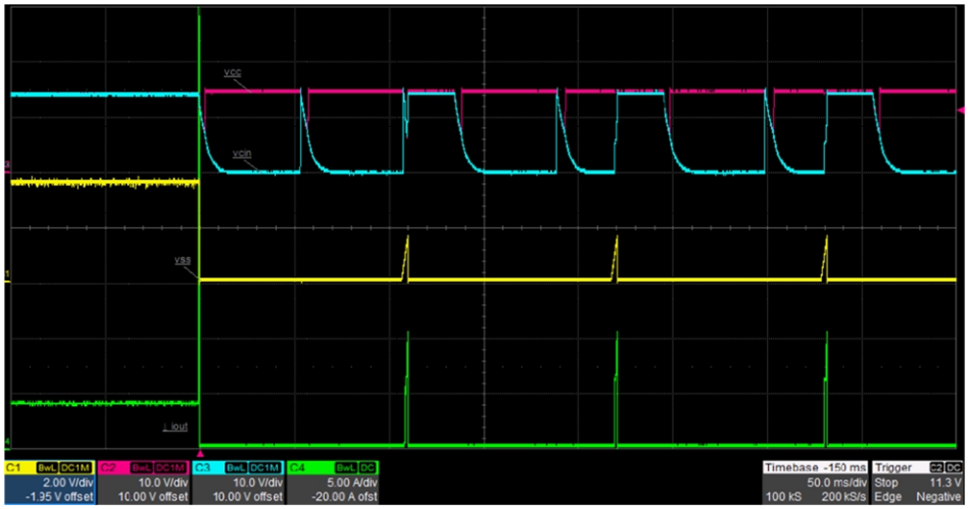
図 15. Startup Waveforms at 5-mA Load, 100 ms/div



3.2.2.7 Output Short Circuit Response

図 16 shows system response to a hot short at the 12-V output (J11). Due to the hiccup mode protection feature of the LM51551 PWM controller, the output will hiccup for 64 switching cycles in current limit and turn off for 32,768 cycles. Output voltage (yellow), V_{COUT} (pink), V_{CIN} (blue) and output current (green) are all shown in 図 16.

図 16. Short Circuit Hiccup Response, 50 ms/div



3.2.2.8 Thermal Performance

Top of board and bottom of board thermal measurements were taken at full PoE load (3.7-A), full adapter load (4.25 A) and output short circuit.

図 17 and 図 18 shows the resulting thermals at full PoE load of 3.7 A.

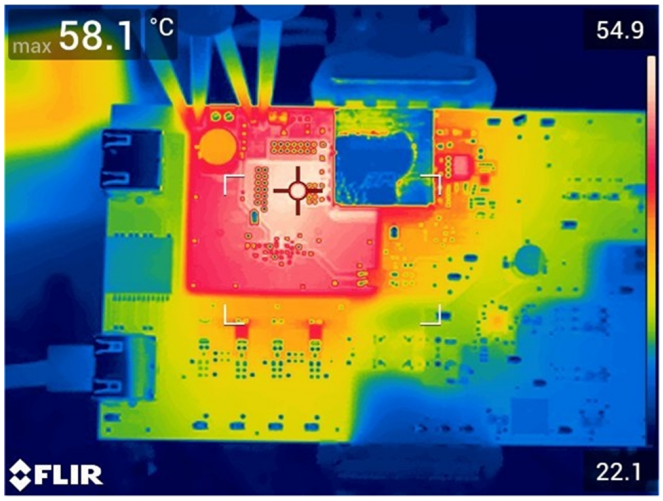


図 17. 3.7-A Load, Top of Board

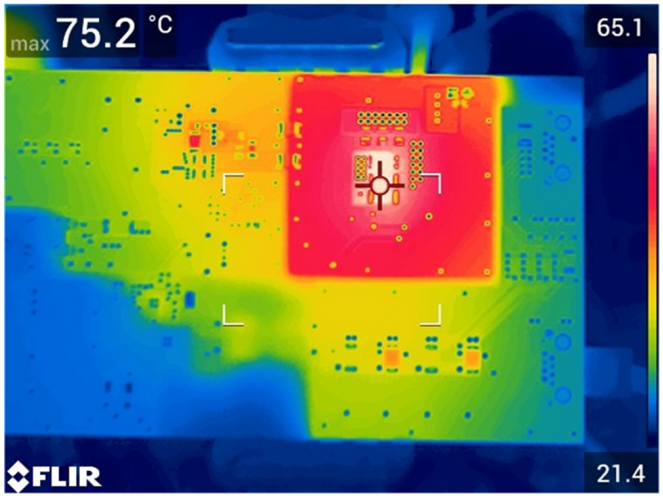


図 18. 3.7-A Load, Bottom of Board

図 19 and 図 20 shows the resulting thermals at full adapter load of 4.25 A.

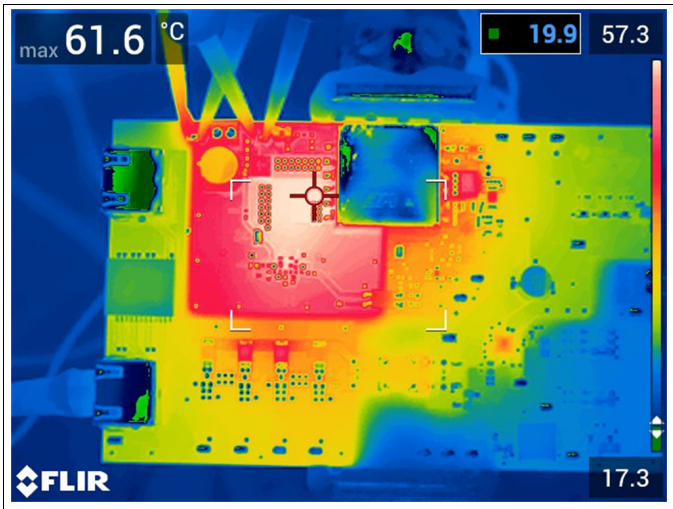


図 19. 4.25-A Load, Top of Board

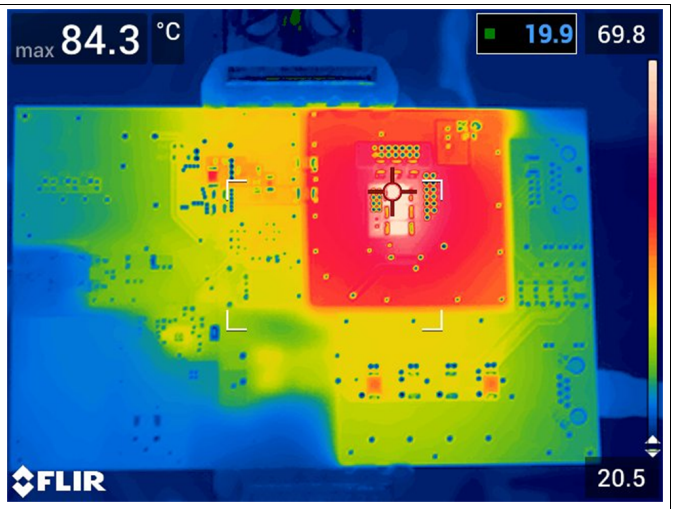


図 20. 4.25-A Load, Bottom of Board

図 21 and 図 22 shows the resulting thermals during a short circuit on the output.

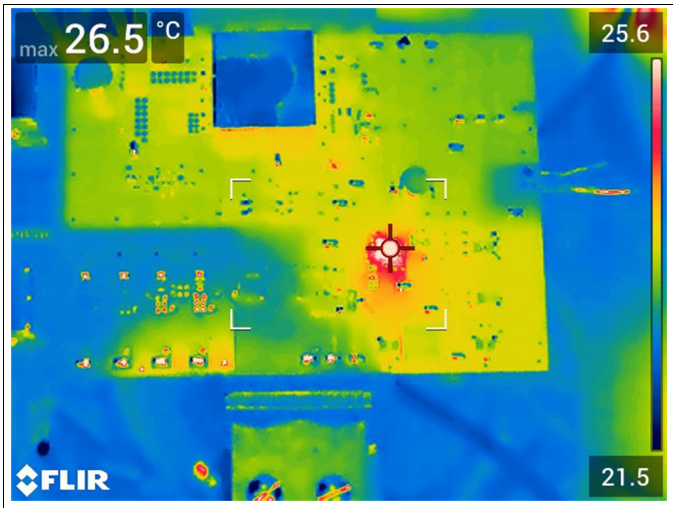


図 21. Short Circuit, Top of Board

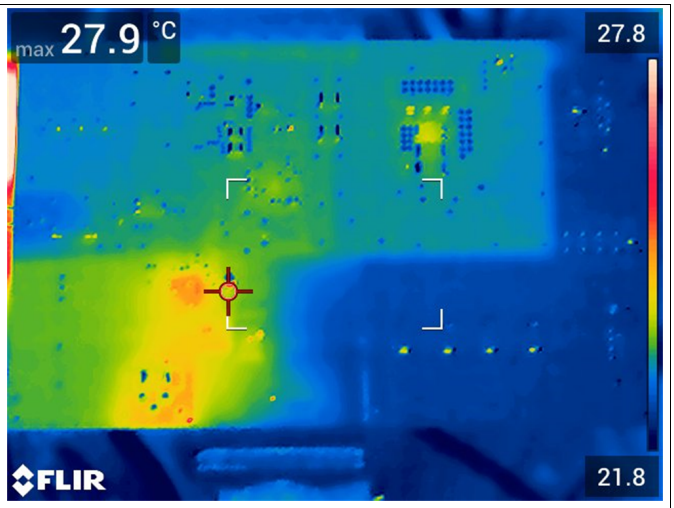


図 22. Short Circuit, Bottom of Board

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050023.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050023.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050023.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050023.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050023.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050023.

5 Related Documentation

- TPS2373-3 Product Folder
- LM51551 Product Folder
- TL431LI Product Folder

5.1 商標

5.2 Third-Party Products Disclaimer

6 Terminology

— PD: Powered Device
PSE: Power Sourcing Equipment
PoE: Power Over Ethernet

7 About the Author

Matthew Xiong is a Product Marketing and Applications Engineer in the Power Switches, Interface and Lighting Business Unit at Texas Instruments. Matt earned his Bachelor of Science in Electrical Engineering at the Universtiy of California, Los Angeles and his Master of Science in Systems Engineering and Management at the University of Texas at Dallas.

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