参考資料

デザイン・ガイド：TIDA-070002
20～ 40V V_{IN}、50W の宇宙グレード絶縁フライバック DC-DC 過電流保護のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

宇宙船用のバス電圧は、確立された 28V から、大電力の商用通信衛星で通常使用される 100V 超まで多岐にわたります。このリファレンス・デザインでは、過電流保護 (OCP) 制限機能を実装した宇宙グレードの 50W 絶縁型中間バス・コンバータを紹介します。このリファレンス・デザインでは、INA901-SP 耐放射線強化電流モニタ、LM139AQML-SP クワッド・コンパレータ、UC1901-SP を使用して電流センシングおよび過電流フラグを備えた絶縁型帰還フライバックを作成しています。フライバック・コンバータのローサイド MOSFET をスイッチングして電圧と電流を出力するために UC1843A-SP 電流モード PWM コントローラを使用し、出力電圧を検出するために UC1901-SP を使用して絶縁帰還ループを完成させています。INA901-SP は、LM139AQML-SP に供給される入力電流を検出し、過電流フラグを作成します。

リソース

TIDA-070002	デザイン・フォルダ
UC1843A-SP	プロダクト・フォルダ
UC1901-SP	プロダクト・フォルダ
INA901-SP	プロダクト・フォルダ
LM139AQML-SP	プロダクト・フォルダ

TI E2E™ Community

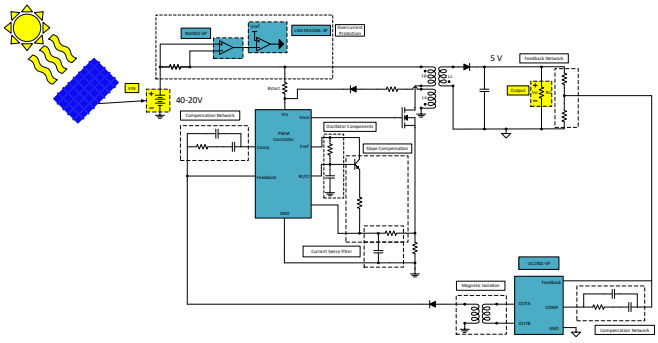
E2E™エキスパートに質問

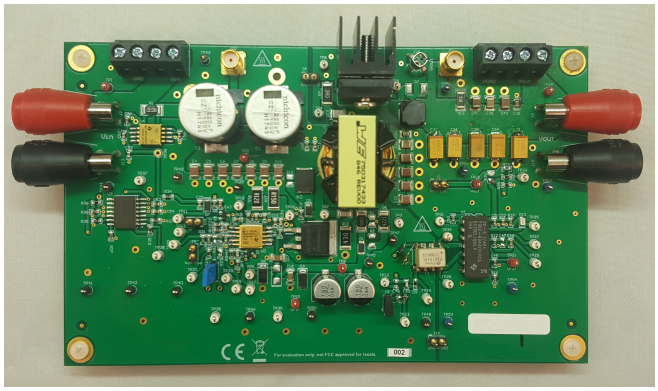
特長

- UC1901-SP を使用する絶縁磁気帰還
- INA901-SP を使用する電流センシング
- LM139AQML-SP を使用する過電流比較
- パルス単位の電流制限
- 二重パルスの抑制
- 複数の帰還パスをサポート

アプリケーション

- コマンドおよびデータ処理
- 衛星用電源システム (EPS)
- 光イメージングのペイロード
- レーダー・イメージング・ペイロード
- 通信ペイロード





1 System Description

The TIDA-070002 uses the UC1843A-SP, INA901-SP, LM139AQML-SP, and UC1901-SP to create an isolated feedback flyback with current sensing and overcurrent flags. The UC1843A-SP is used to switch the low side MOSFET of the flyback converter and provides voltage and current to the output. The system uses the UC1843A-SP to provide 5-V and 10-A outputs. These outputs are not dependent on the UC1843A-SP itself, and can be increased or decreased depending on the design. The UC1901-SP senses the output voltage and provides isolated feedback to the UC1843A-SP to complete the control loop. The INA901-SP senses the input current which is then provided to the LM139AQML-SP to create an overcurrent flag. In a full system, this flag could be used to shutdown the UC1843A-SP and turn off the converter.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input Power Supply	20 to 40 VDC	表 2
Output Voltage	5 VDC	表 2
Output Current	0 to 10 A	表 2
Output Current Pre-load	100 mA	表 2
Operating Temperature	25°C	表 2
Switching Frequency of UC1843A-SP	200 kHz	2.4.1
Switching Frequency of UC1901-SP	1 MHz	表 2
Peak Input Current Limit	12 A	2.4.7
Bandwidth	~2 kHz	3.2.2.3
Phase Margin	~70°	3.2.2.3

2 System Overview

2.1 Block Diagram

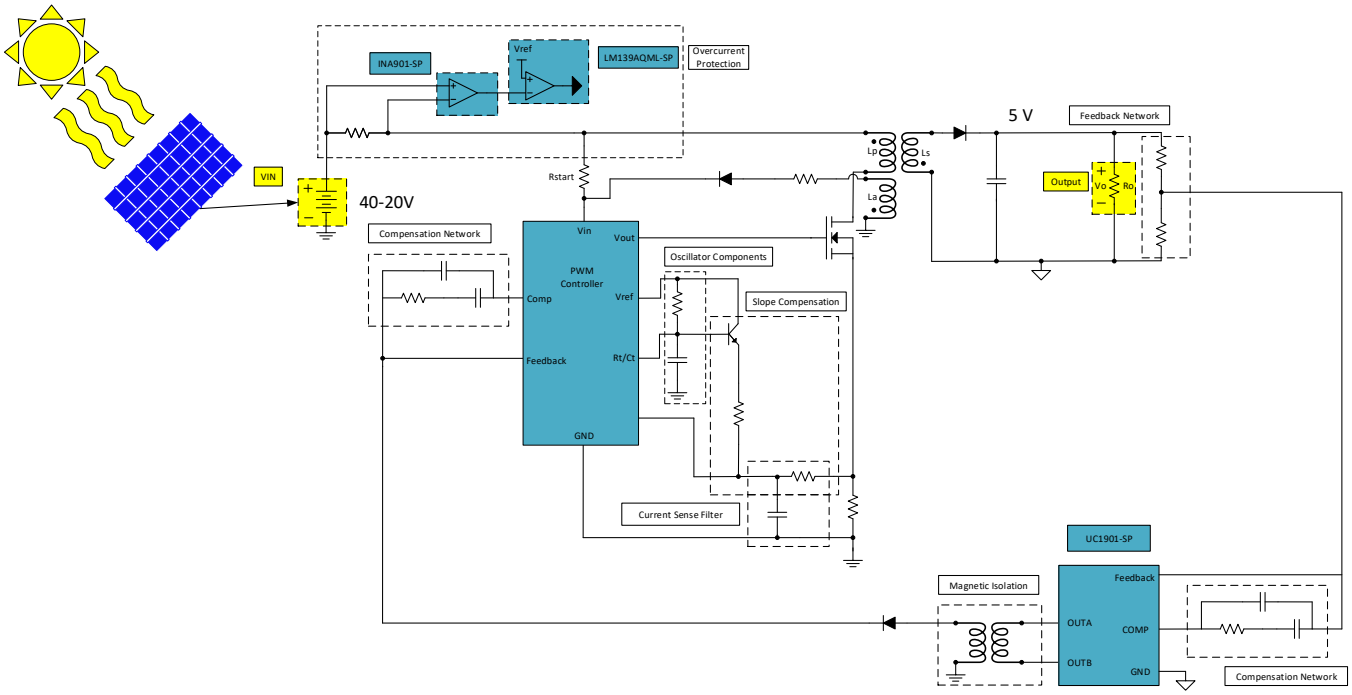


図 1. TIDA-070002 Block Diagram

2.2 Design Considerations

When using the INA901-SP and LM139AQML-SP as a way to implement an input overcurrent flag, care has to be taken to where the overcurrent point is set. Input current can vary widely due to duty cycle changes because of input voltage and efficiency changes over that input voltage. When using the UC1901-SP care has to be taken into account for the max minimum input voltage of 4.5 V. For low output voltages this can be a hard input voltage to maintain off of the output, so other methods may have to be used. One method is to charge pump the switch node and use diodes between that and the output voltage, while another method is simply have another source from a separate converter.

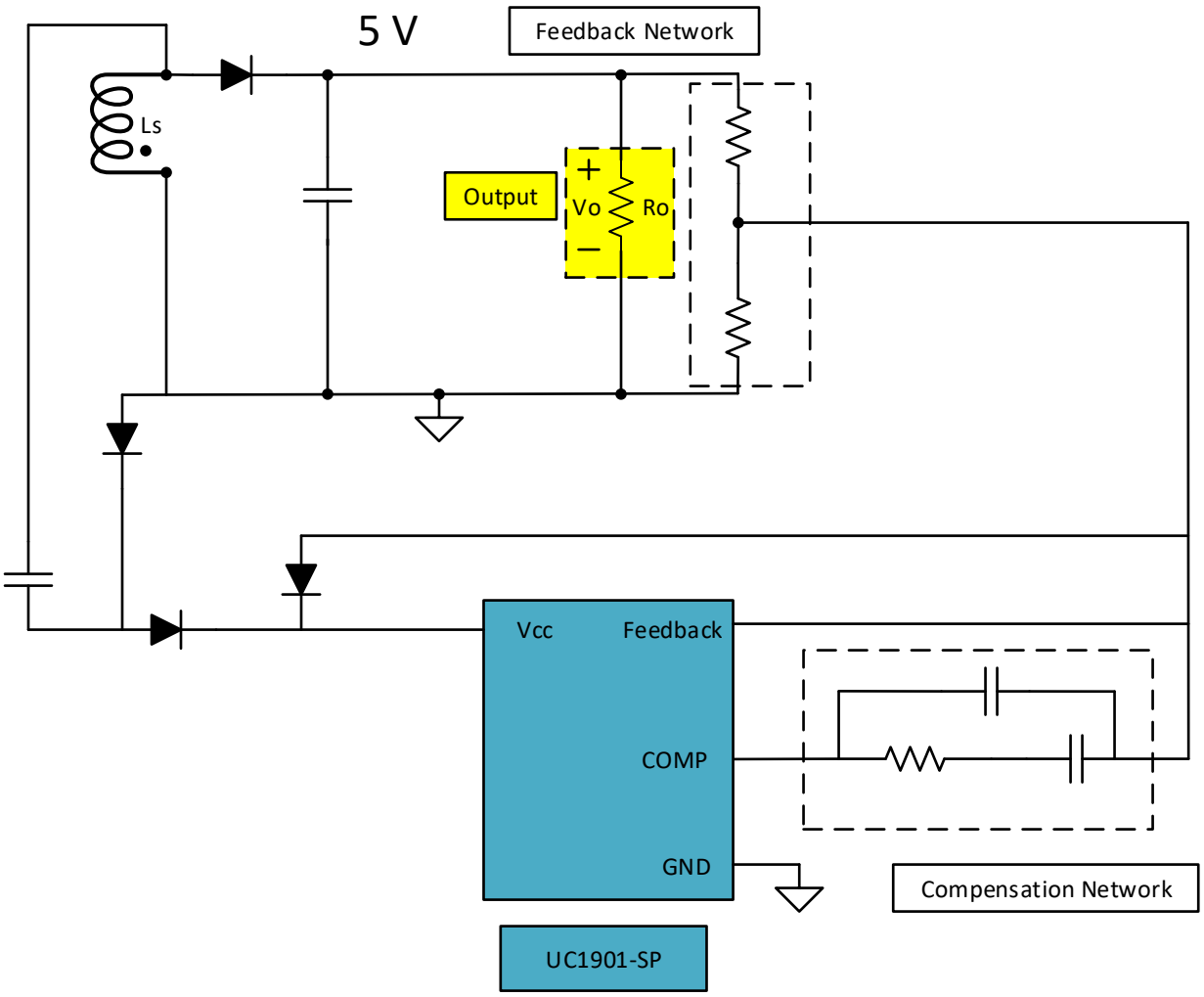


図 2. Alternative Method to Create V_{cc} for UC1901-SP

2.3 Highlighted Products

2.3.1 UC1843A-SP

- QML Class V (QMLV) Qualified, SMD 5962-86704
- 5962P8670409Vxx:
  - Radiation Hardness Assurance (RHA) up to 30-krad(Si) Total Ionizing Dose (TID)
  - Passes functional and specified post radiation parametric limits of 45 krad(Si) at LDR (10 mrad(Si)/s) per 1.5× over test as defined in MIL-STD-883 Test Method 1019.9 Paragraph 3.13.3.b
  - Exhibits LDR sensitivity but remains within the pre-radiation electrical limits at 30-krad(Si) Total Dose Level, as allowed by MIL-STD-883, TM1019
- Optimized for offline and DC-to-DC converters
- Low start-up current (< 0.5 mA)
- Trimmed oscillator discharge current
- Automatic feed forward compensation

- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lockout (UVLO) with hysteresis
- Double-pulse suppression
- High-current totem-pole output
- Internally-trimmed bandgap reference
- 500-kHz operation
- Low R_O error amplifier

2.3.2 UC1901-SP

- An amplitude-modulation system for transformer coupling an isolated feedback error signal
- Low-cost alternative to optical couplers
- Internal 1% reference and error amplifier
- Internal carrier oscillator usable to 5 MHz
- Modulator synchronizable to an external clock
- Loop status monitor

2.3.3 INA901-SP

- 5962-1821001
  - Radiation Hardness Assured (RHA) 100 krad(Si) at LDR
  - Single Event Latch-up (SEL) Immune to 93 MeV-cm^2 /mg at 125°C
  - Qualified over the Military Temperature Range (–55°C to 125°C)
  - High-performance 8-pin ceramic flat pack package (HKX)
- Wide common-mode range: –16 V to 80 V
- CMRR: 120 dB
- Accuracy:
  - ±0.5-mV offset
  - ±0.2% gain error
  - 2.5-μV/°C offset drift
  - 50-ppm/°C gain drift
- Bandwidth: Up to 130 kHz
- Gain: 20 V/V
- Quiescent current: 700 μA
- Power supply: 2.7 V to 18 V
- Provision for filtering

2.3.4 LM139AQML-SP

- Available with radiation ensured
  - TID 100 krad(Si)

  - ELDRS free 100 krad(Si)
- Wide supply voltage range
- LM139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- Very-low supply current drain (0.8 mA)
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±1 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

2.4 System Design Theory

2.4.1 Switching Frequency

Choosing a switching frequency has a trade off between efficiency and bandwidth. Higher switching frequencies will have larger bandwidth, but a lower efficiency than lower switching frequencies. A switching frequency of 200 kHz was chosen as a trade off between bandwidth and efficiency. Using equations provided by the datasheet for the UC1843A-SP, R_T and C_T were chosen to be 7.15 kΩ and 1200 pF, respectively. The equation from the datasheet are shown below:

$$f_{osc} \approx \frac{1.72}{R_{osc} \times C_{osc}} \tag{1}$$

$$f_{osc} \approx \frac{1.72}{7.15\ k\Omega \times 1200\ pF} = 200\ \ kHz \tag{2}$$

2.4.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. There is no minimum limit to the turns ratio of the transformer, just a maximum one. The equation below will give the turns ratio as a function of duty cycle which if you put in the maximum duty cycle of the converter will give you a maximum turns ratio. The UC1843A-SP design targeted a duty cycle of 50% which is somewhat low for this controller. The suggested value would be around 70% duty cycle to take advantage of the fact the UC1843A-SP has full duty cycle range. The equation of the turns ratio of the transformer is:

$$N_{psMAX} = \frac{V_{inMIN} \times D_{lim}}{(V_{out} + V_{Diode}) \times (1 - D_{lim})} \tag{3}$$

$$N_{psMAX} = \frac{20\ V \times 0.5}{(5\ V + 0.7\ V) \times (1 - 0.5)} = 3.5 \tag{4}$$

Often the turns ratio will slightly change in design due to how the transformer is manufactured. For the UC1843A-SP design a turns ratio of 3.33 was used. Another turns ratio that is important is the turns ratio of the auxiliary winding. The auxiliary winding is found by figuring out what positive voltage is needed from the auxiliary winding. Picking what voltage the auxiliary winding should have lets one pick the turns ratio from the secondary to the auxiliary winding, which in turn allows for the turns ratio from primary to auxiliary to be found.

$$N_{pa} = \frac{N_{ps} \times (V_{out} + V_{Diode})}{V_{aux}} \tag{5}$$

$$N_{pa} = \frac{3.33 \times (5\ V + 0.7\ V)}{13\ V} = 1.46 \tag{6}$$

An auxiliary winding of 1.43 was used for the UC1843A-SP design due to manufacturing constraints. The primary inductance of the transformer is found from picking an appropriate ripple current. A higher inductance will often mean reduced current ripple, thus lower EMI and noise, but a higher inductance will also increase physical size and limit the bandwidth of the design. A lower inductance will do the opposite, increasing current ripple, lowering EMI, lowering noise, decreasing physical size, and increasing the limited bandwidth of the design. The percent ripple current can be anywhere from 20% to 80% depending on the design. The equation for finding the primary inductance from the percentage ripple current is:

$$L_{PRI} = \frac{V_{inMAX}^{2} \times D_{MIN}^{2}}{V_{out} \times I_{out} \times f_{osc} \times \%_{Ripple}} \tag{7}$$

$$\frac{(40\ V)^2 \times 0.25^2}{5\ V \times 10\ A \times 200\ kHz \times 0.4} = 25\ \mu H \tag{8}$$

There are quite a few physical limitations when making transformers, so often this inductance will change slightly. For the UC1843-SP design a primary inductance of 21 µH. This corresponds to a percent ripple of around 0.475. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer, so equations are listed below.

$$I_{Ripple} = \frac{V_{out} \times I_{out} \times \%_{Ripple}}{V_{inMAX} \times D_{MIN}} \tag{9}$$

$$I_{Ripple} = \frac{5\ V \times 10\ A \times 0.475}{40\ V \times 0.25} = 2.375\ A \tag{10}$$

$$I_{PriPeak} = \frac{V_{out} \times I_{out}}{V_{inMIN} \times D_{MAX} \times \eta} + \frac{I_{Ripple}}{2} \tag{11}$$

$$I_{PriPeak} = \frac{5\ V \times 10\ A}{20\ V \times 0.5 \times 0.8} + \frac{2.375}{2} = 7.44\ A \tag{12}$$

$$I_{PriRMS} = \sqrt{D \times \left(\frac{V_{out} \times I_{out}}{V_{in} \times D}\right)^2 + \frac{I_{Ripple}^{2}}{3}} \tag{13}$$

$$I_{PriRMS} = \sqrt{0.5 \times \left(\frac{5\ V \times 10\ A}{20\ V \times 0.5}\right)^2 + \frac{(2.375\ A)^2}{3}} = 3.79\ A \tag{14}$$

$$I_{SecRMS} = \sqrt{\left(1 - D\right) \times I_{out}^{2} + \frac{(I_{Ripple} \times N_{ps})^2}{3}} \tag{15}$$

$$I_{SecRMS} = \sqrt{0.5 \times \left(10\ A\right)^2 + \frac{(2.375\ A \times 3.33)^2}{3}} = 8.42\ A \tag{16}$$

2.4.3 RCD and Diode Clamp

For the UC1843-SP design a Zener diode was used which will clamp, often called the snubber, the voltage to around what the breakdown voltage of the Zener diode plus the input voltage of the design. Since Zener diodes take time to switch, the actual clamped voltage will often be above the Zener diode breakdown voltage plus the input voltage. Since using a resistor and capacitor are commonly used for the clamp for flybacks, the design philosophy for how to pick resistor and capacitor values will be covered. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, one must first pick how much the node is allowed to overshoot. The equation for finding the voltage of the clamp is:

$$V_{clamp} = K_{clamp} \times N_{ps} \times (V_{out} + V_{Diode}) \tag{17}$$

Note that K_{clamp} is recommended to be 1.5 as this will allow for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the snubber voltage is allowed to change over the switching cycle, can allow one to figuring out starting values for the resistor and capacitor using the following equations:

$$R_{clamp} = \frac{V_{clamp}^{2}}{\frac{1}{2} \times L_{leakage} \times I_{PriPeak}^{2} \times \frac{V_{clamp}}{V_{clamp} - N_{ps} \times (V_{out} + V_{Diode})} \times f_{osc}} \tag{18}$$

$$C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp} \times V_{clamp} \times R_{clamp} \times f_{osc}} \quad (19)$$

A starting value of 10% is generally used for ΔV_{clamp}.

2.4.4 Output Diode

The voltage stress by the converter on the diode can be found with the following equation:

$$V_{DiodeStress} = V_{out} + \frac{V_{inMAX}}{N_{ps}} \quad (20)$$

$$V_{DiodeStress} = 5 \quad V + \frac{40 \ V}{3.33} = 17 \quad V \quad (21)$$

Note that any diode picked should have a voltage rating of well above this value as it does not include parasitic spikes in the equation. The UC1843-SP diode was picked to have a voltage rating of 60 V.

2.4.5 Output Filter and Capacitance

For most designs, a ripple voltage is picked and the output capacitance is figured out from that value. The UC1843A-SP design started similar to that using the equations:

$$C_{out} > \frac{I_{out} \times D_{MAX}}{V_{Ripple} \times f_{osc}} \quad (22)$$

$$C_{out} > \frac{10 \ A \times 0.5}{50 \ mV \times 200 \ kHz} = 500 \quad \mu F \quad (23)$$

$$C_{out} > \frac{\Delta I_{step}}{2\pi \times \Delta V_{out} \times f_{co}} \quad (24)$$

$$C_{out} > \frac{10 \ A}{2\pi \times 0.7 \ V \times 2.2 \ kHz} = 1 \quad mF \quad (25)$$

A value of around 1145 µF was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics will help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple will be attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. The equations below allow for finding the amount of attenuation that will come from a specific output filter inductance. An inductance of 500 nH was chosen to attenuate the output voltage ripple.

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{L_{Filter} \times C_{oBulk}}} \quad (26)$$

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{0.5 \ nH \times 1127 \ \mu F}} = 6.7 \quad kHz \quad (27)$$

$$F_{Zero} = \frac{1}{2\pi \times C_{oBulk} \times ESR_{oBulk}} \quad (28)$$

$$F_{Zero} = \frac{1}{2\pi \times 1127 \ \mu F \times 0.009 \ \Omega} = 15.69 \quad kHz \quad (29)$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{f_{osc}}{f_{resonant}}\right) - 20 \times \log_{10}\left(\frac{f_{osc}}{f_{zero}}\right) \quad (30)$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{200 \ kHz}{6.7 \ kHz}\right) - 20 \times \log_{10}\left(\frac{200 \ kHz}{15.69 \ kHz}\right) = 36.88 \quad dB \quad (31)$$

Sometimes the output filter can causing peaking at high frequencies, this can be damped by adding a resistor in parallel with the inductor. For the UC1843A-SP design 0.5 Ω was used as a very conservative value. The resistance needed to damp the peaking can be calculated using the following equations:

$$\omega_o = \sqrt{\frac{2(C_{oCerm} + C_{oBulk})}{L_{Filter} \times C_{oCerm} \times C_{oBulk}}} \quad (32)$$

$$\omega_o = \sqrt{\frac{2(19 \ \mu F + 1127 \ \mu F)}{500 \ nH \times 19 \ \mu F \times 1127 \ \mu F}} = 463 \quad kHz \quad (33)$$

$$R_{Filter} = \frac{R_o \times L_{Filter} \times \left(C_{oCerm} + C_{oBulk}\right) - \frac{L_{Filter}}{\omega_o}}{\frac{R_o \times (C_{oCerm} + C_{oBulk})}{\omega_o} - L_{Filter} \times C_{oCerm}} \quad (34)$$

$$R_{Filter} = \frac{0.5 \times 500\ nH \times \left(19\ \mu F + 1127\ \mu F\right) - \frac{500\ nH}{463\ kHz}}{\frac{0.5 \times (19\ \mu F + 1127\ \mu F)}{463\ kHz} - 500\ nH \times 19\ \mu F} = 0.232\ \Omega \quad (35)$$

2.4.6 Compensation

The poles and zeros of a flyback converter can be found with the following equations:

$$f_{ZESR} = \frac{1 + D}{2\pi \times C_{out} \times R_{ESR}} \quad (36)$$

$$f_{ZESR} = \frac{1 + 0.5}{2\pi \times 1146\ \mu F \times 0.009\ \Omega} = 23.15\ kHz \quad (37)$$

$$f_P = \frac{1}{2\pi \times C_{out} \times R_o} \quad (38)$$

$$f_P = \frac{1}{2\pi \times 1146\ \mu F \times 0.5} = 278\ Hz \quad (39)$$

$$f_{RHPZ} = \frac{R_{out} \times (1 - D_{MAX})^2}{2\pi \times \frac{L_{PRI}}{N_{ps}^2} \times D_{MAX}} \quad (40)$$

$$f_{RHPZ} = \frac{0.5 \times (1 - 0.5)^2}{2\pi \times \frac{21\ \mu H}{3.33^2} \times 0.5} = 21\ kHz \quad (41)$$

Type IIB compensation was selected to compensate the poles and zeros of the flyback converter. Since the RHPZ of the flyback converter is unable to be compensated, the crossover frequency of the converter should be between one fourth to a whole decade below the RHPZ of the converter. Type IIB compensation has 1 pole and 1 zero to help compensate the converter. The pole from the compensation is suggested to be placed by the RHPZ of the converter and the zero from compensation is suggested to be placed a decade before the expected crossover frequency. Using these guidelines the compensation values for the converter were picked for the converter. For the non-isolated portion of the board this means choosing the value of the compensation resistors and capacitors along these guidelines. For the UC1901-SP, the compensation was placed using the same guidelines, however the UC1901-SP adds a static gain of 12 to the feedback loop. This increase in gain can be compensated for by dividing the resistor from compensation down and increasing the values of the capacitors by the same amount. This allows for the gain to be controlled in the system without changing the poles and zeros of the system. Optimization is needed for compensation values, and those values can be validated through testing.

2.4.7 Sense Resistor and Slope Compensation

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is allowed to get too high. The voltage threshold of the CS pin is around 1 V, thus the equation to find the sense resistor from the peak current is:

$$R_{cs} = \frac{V_{CS\ \ Threshold} - V_{Slope\ \ Comp\ \ Offset}}{I_{limit}} \quad (42)$$

$$R_{cs} = \frac{1\ V - 0.1\ V}{12\ A} = 0.075\ \Omega \quad (43)$$

Note that I_{limit} should be greater than $I_{PriPeak}$, and that the voltage offset from the slope compensation will be dependant on the amount of slope compensation in the design. The value of 0.075 Ω for the sense resistance was found to be the optimum value adding some headroom for slope compensation offset of 0.1 V. Slope compensation was implemented with a BJT being turned off and on by the RC pin of the device. The BJT was placed between the REF pin and a resistor divider to the CS pin. The optimum slope compensation value can be found from the following equations after picking a value for the top of the divider:

$$S_c = \frac{V_{out} \times R_{cs} \times G_{cs}}{L_{PRI} \times N_{ps}} \quad (44)$$

$$S_c = \frac{5\ V \times 0.075\ \Omega \times 3}{21\ \mu H \times 3.33} = 16088 \quad (45)$$

$$S_{osc} = \frac{f_{osc} \times V_{oscpp}}{D_{MIN}} \quad (46)$$

$$S_{osc} = \frac{200\ kHz \times 1.7\ V}{0.25} = 1360000 \quad (47)$$

$$R_{csf} = \frac{R_{top}}{\frac{S_{osc}}{S_c} - 1} \quad (48)$$

$$R_{csf} = \frac{11.8\ k\Omega}{\frac{1360000}{16088} - 1} = 141\ \Omega \quad (49)$$

The UC1843A-SP design uses a much higher resistor of 1.47 kΩ, but this is an attempt to be very conservative. Note that the bottom resistor can be used as part of a filter to the CS pin as well, which is implemented in the design using a capacitor near the CS pin. Care was taken such that the RC filter would not filter the switching frequency by having the RC time constant be a decade less than the switching frequency.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

A power supply is needed to provide voltage to the input from 20 to 40 V at 4 A. The output load needs to sink up to 10 A of current at 5 V. The output of the device can reach 7 V during start up so the output load must be able to handle up to 7 V for small portions of time.

3.2 Testing and Results

3.2.1 Test Setup

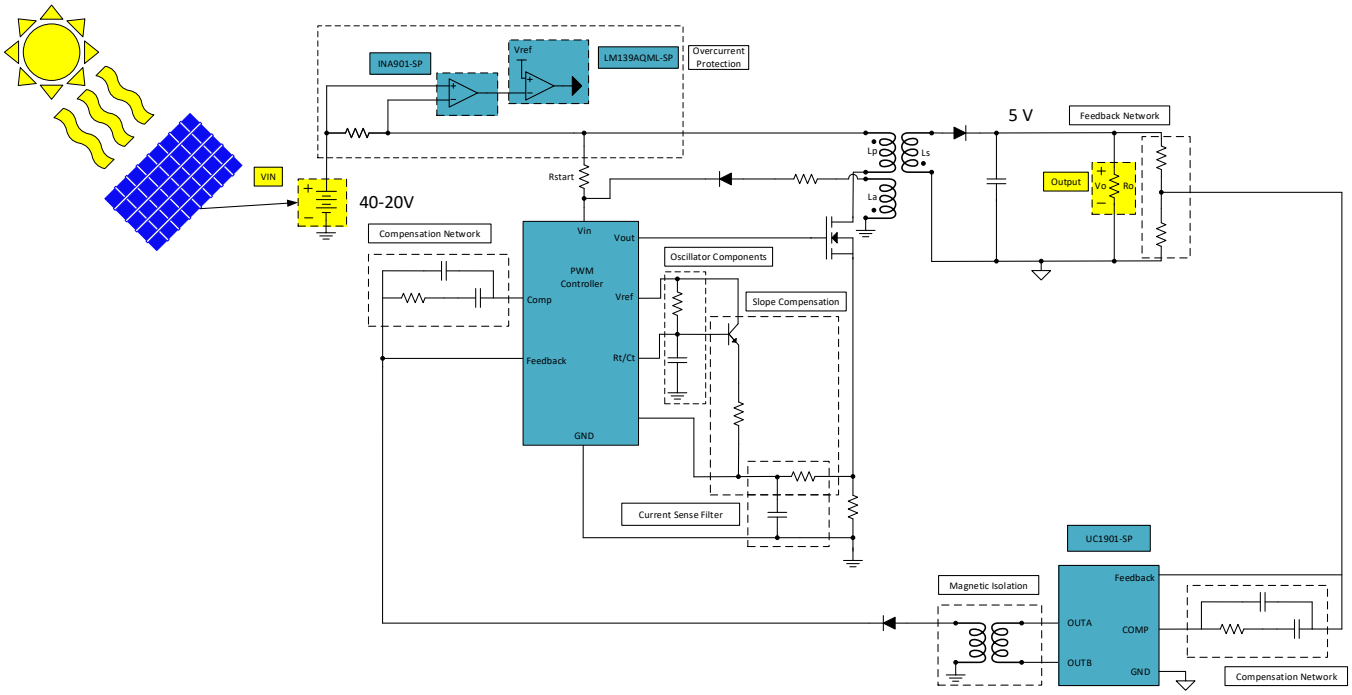


図 3. Test Setup

表 2. Test Parameters

PARAMETER	SPECIFICATIONS
Input Power Supply	20 to 40 VDC
Output Voltage	5 VDC
Output Current	0 to 10 A
Output Current Pre-load	100 mA
Operating Temperature	25°C
Switching Frequency of UC1843A-SP	200 kHz
Switching Frequency of UC1901-SP	1 MHz
Peak Input Current Limit	12 A
Bandwidth	~2 kHz
Phase Margin	~70°

3.2.2 Test Results

3.2.2.1 Efficiency

Efficiency measurement was taken after the board was run for 20 minutes at full output load. Values for input voltage, input current, output voltage, and output current were then taken starting at 10 A and decreasing the output load by 1 A down to no load. The output current does not include the 100-mA pre-load that is already included on the board.

表 3. Efficiency for 20 V_{in}

V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency
19.97	3.2	4.95	9.99	63.9	49.45	0.774
20	2.84	4.95	8.99	56.8	44.50	0.783
20.04	2.49	4.95	7.99	49.9	39.55	0.793
20.07	2.15	4.95	6.99	43.2	34.60	0.802
20.1	1.82	4.95	6	36.6	29.70	0.812
20.13	1.51	4.95	5	30.4	24.75	0.814
20.16	1.2	4.95	4	24.2	19.80	0.818
20.19	0.91	4.95	3	18.4	14.85	0.808
20.21	0.63	4.95	2	12.7	9.90	0.778
20.24	0.33	4.95	1	6.7	4.95	0.741
20.27	0.05	4.95	0	1.0	0.00	0.000

表 4. Efficiency for 40 V_{in}

V_{in}	I_{in}	V_{out}	I_{out}	P_{in}	P_{out}	Efficiency
40.39	1.5	4.95	9.99	60.59	49.45	0.816
40.4	1.34	4.95	8.99	54.14	44.50	0.822
40.42	1.19	4.95	7.99	48.10	39.55	0.822
40.43	1.04	4.95	6.99	42.05	34.60	0.823
40.45	0.89	4.95	6	36.00	29.70	0.825
40.46	0.75	4.95	5	30.35	24.75	0.816
40.45	0.61	4.95	4	24.67	19.80	0.802
40.49	0.46	4.95	3	18.63	14.85	0.797
40.5	0.32	4.95	2	12.96	9.90	0.764
40.52	0.18	4.95	1	7.29	4.95	0.679
40.53	0.03	4.95	0	1.22	0.00	0.000

3.2.2.2 Load Regulation

Load regulation was taken after output voltage settled and after decreasing load in 1-A increments.

表 5. 20-V_{in} Load Regulation

V_{out}	I_{out}
4.9495	9.99
4.9498	8.99
4.95	7.99
4.9504	6.99

表 5. 20-V_{in} Load Regulation (continued)

V_{out}	I_{out}
4.9507	6
4.509	5
4.9513	4
4.9516	3
4.952	2
4.9523	1
4.9526	0

表 6. 40-V_{in} Load Regulation

V_{out}	I_{out}
4.9495	9.99
4.9497	8.99
4.95	7.99
4.9503	6.99
4.9507	6
4.951	5
4.9513	4
4.9516	3
4.9519	2
4.9523	1
4.9526	0

3.2.2.3 *Frequency Response*

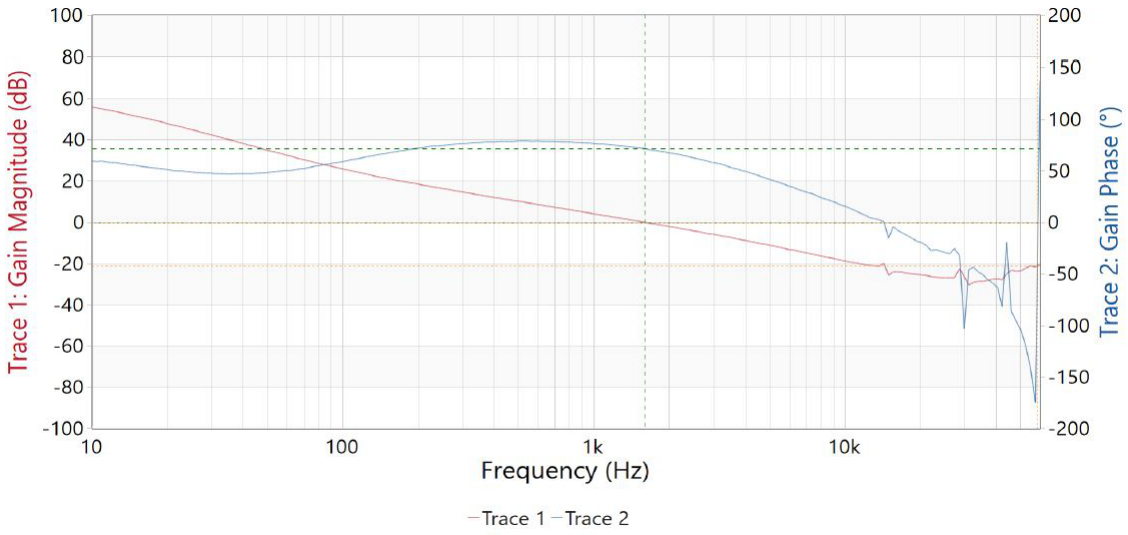


図 6. 20 V_{in} Frequency Response

Frequency response was taken with 10-A output current and 20 V_{in}.

表 7. Frequency Response Characteristics for 20 V_{in}

PARAMETER	VALUE
Crossover Frequency	1.61 kHz
Phase Margin	71.3°
Phase Crossover	58.9 kHz
Gain Margin	–20.95 dB

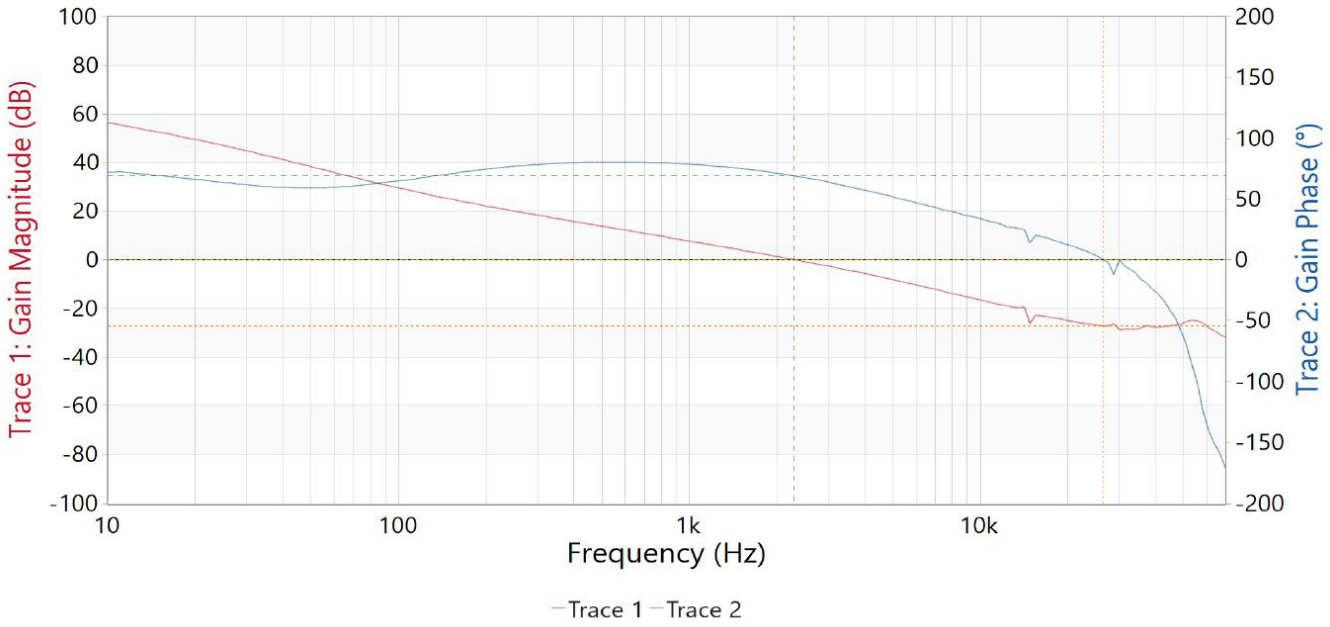


図 7. 40 V_{in} Frequency Response

Frequency response was taken with 10-A output current and 40 V_{in}.

表 8. Frequency Response Characteristics for 40 V_{in}

PARAMETER	VALUE
Crossover Frequency	2.31 kHz
Phase Margin	68.96°
Phase Crossover	26.6 kHz
Gain Margin	–27.2 dB

3.2.2.4 Thermal Characteristics

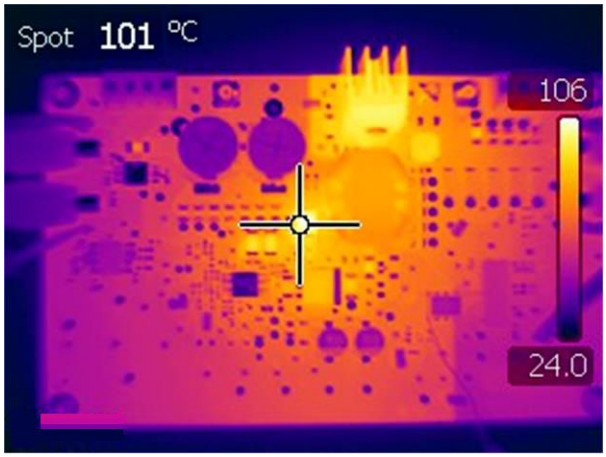


図 8. Thermal Characteristics for 20 V_{in}

Thermal measurement was done with 20 V_{in} after 20 minutes of running with full load on the output.

表 9. Notable Thermal Values for 20 V_{in}

Area	Temperature
Zener Diode Clamp (D4)	101°C
Output Diode (D2)	92.3°C
Output Filter Inductor (L1)	77.7°C
Main Switching MOSFET (Q1)	71.8°C
Sense Resistors (R17 and R18)	72.7°C
Transformer (T1)	61.7°C

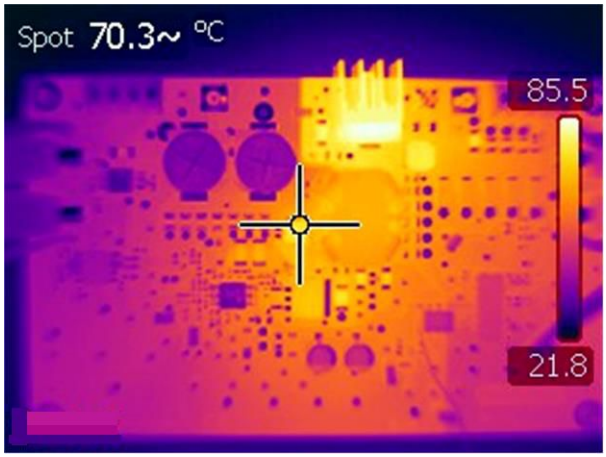


図 9. Thermal Characteristics for 40 V_{in}

Thermal measurement was done with 40 V_{in} after 20 minutes of running with full load on the output.

表 10. Notable Thermal Values for 40 V_{in}

Area	Temperature
Zener Diode Clamp (D4)	70.3°C
Output Diode (D2)	84.9°C

表 10. Notable Thermal Values for 40 V_{in} (continued)

Area	Temperature
Output Filter Inductor (L1)	73.8°C
Main Switching MOSFET (Q1)	61.4°C
Sense Resistors (R17 and R18)	54.7°C
Transformer (T1)	59.8°C

3.2.2.5 Output Voltage Ripple

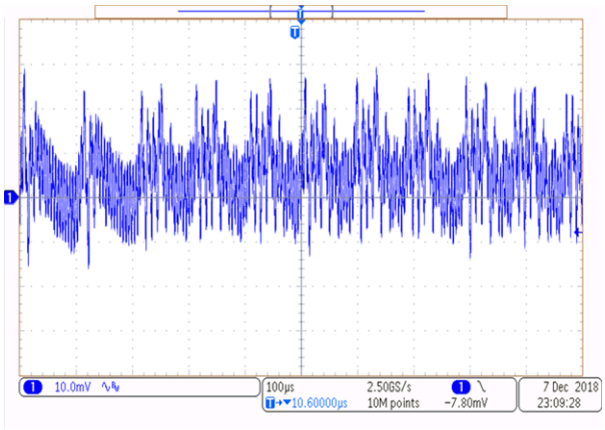


図 10. Output Voltage Ripple 20 V_{in}

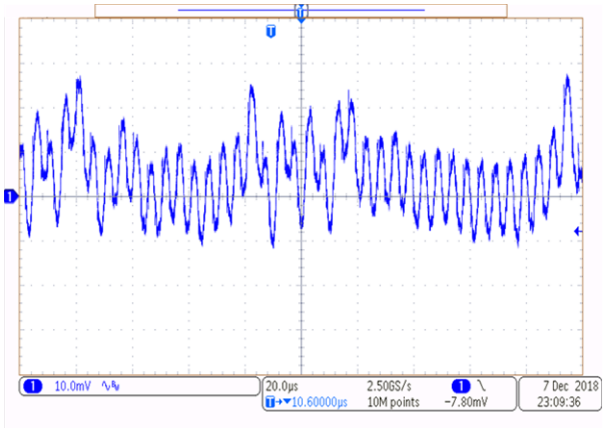


図 11. Output Voltage Ripple 20 V_{in} With Smaller Time Scale

Output voltage ripple was taken with 20 V_{in} and a fully loaded output. Ripple from the UC1843A-SP can be seen in 図 10 and ripple from the UC1901-SP can been seen in 図 11.

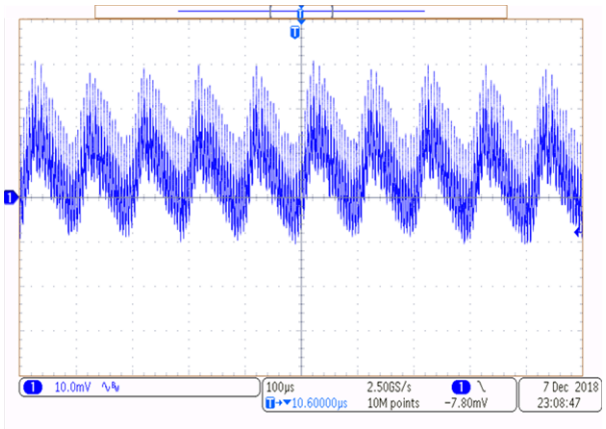


図 12. Output Voltage Ripple 40 V_{in}

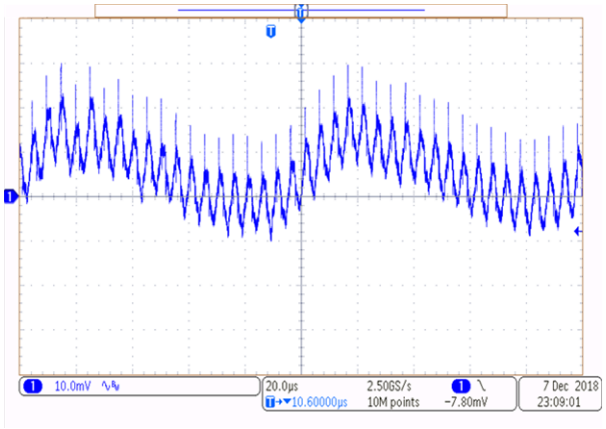


図 13. Output Voltage Ripple 40 V_{in} With Smaller Time Scale

Output voltage ripple was taken with 20 V_{in} and a fully loaded output. Ripple from the UC1843A-SP can be seen in 図 12 and ripple from the UC1901-SP can been seen in 図 13. The additional ripple from the output can be filtered out by POL converters that are supplied from the 5-V rail.

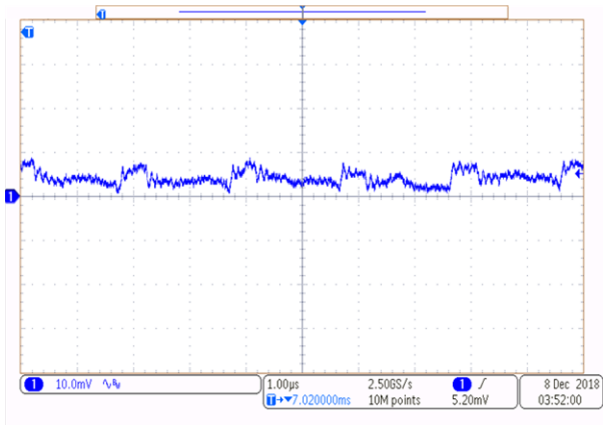


図 14. Output Voltage Ripple of TPS50601A-SP EVM Supplied From UC1843A-SP

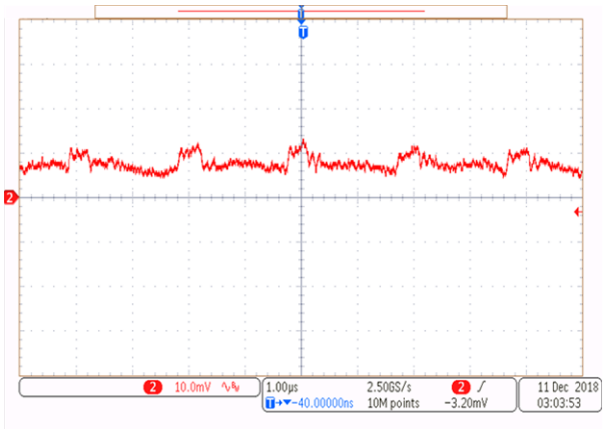


図 15. Output Voltage Ripple of TPS50601A-SP EVM Supplied From 5-V Power Supply

For the figure displayed in 図 14, the UC1843A-SP and UC1901-SP design supplied a TPS50601A-SP EVM using a 40-V rail. For the figure displayed in 図 15, the TPS50601A-SP EVM was supplied using a 5-V lab power supply. The additional ripple added to the line by the UC1843A-SP and the UC1901-SP had a negligible impact on the output ripple of the TPS50601A-SP EVM.

3.2.2.6 Load Step

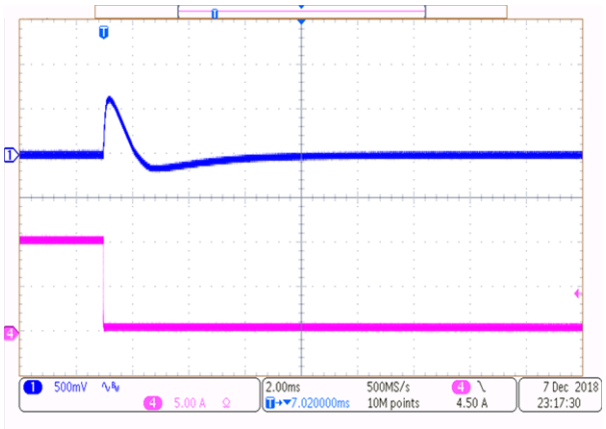


図 16. Partial Load Step Down With 20 V_{in}

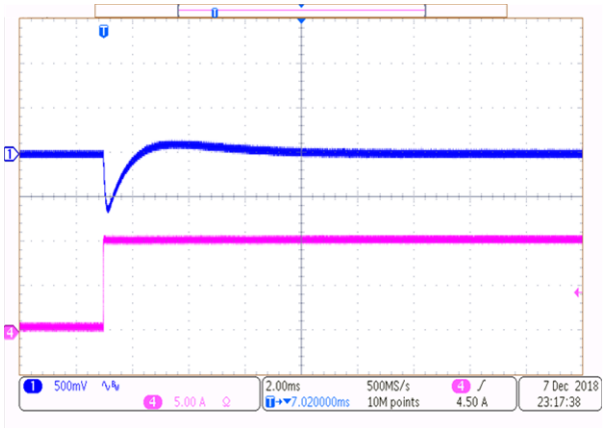


図 17. Partial Load Step Up With 20 V_{in}

For tests shown in 図 16 and 図 17, 20 V was applied to the input and a load step was applied to the output. The load step applied was from 0.6 A to 10 A and 10 A to 0.6 A. Note that those currents do not include the 0.1-A pre-load. The 0.6 A was found to be the minimum output current in order to avoid light load conditions with the design.

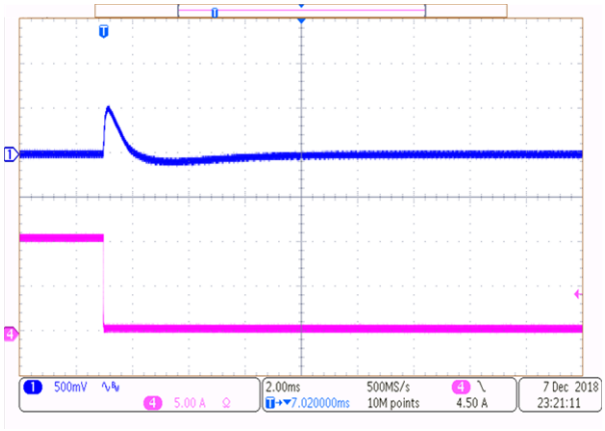


図 18. Partial Load Step Down With 40 V_{in}

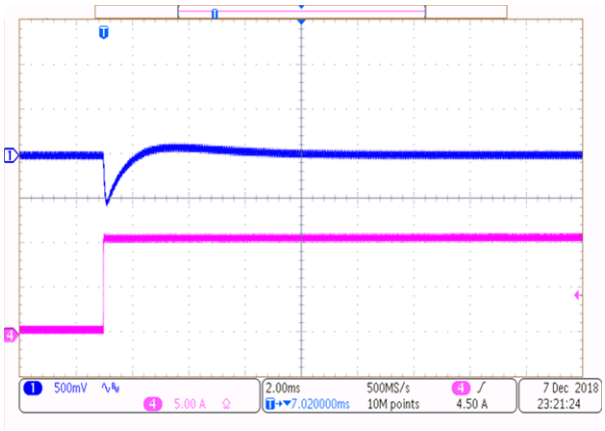


図 19. Partial Load Step Up With 40 V_{in}

For tests shown in 図 18 and 図 19, 40 V was applied to the input and a load step was applied to the output. The load step applied was from 0.5 A to 10 A and 10 A to 0.5 A. Note that those currents do not include the 0.1-A pre-load. The 0.5 A was found to be the minimum output current in order to avoid light load conditions with the design.

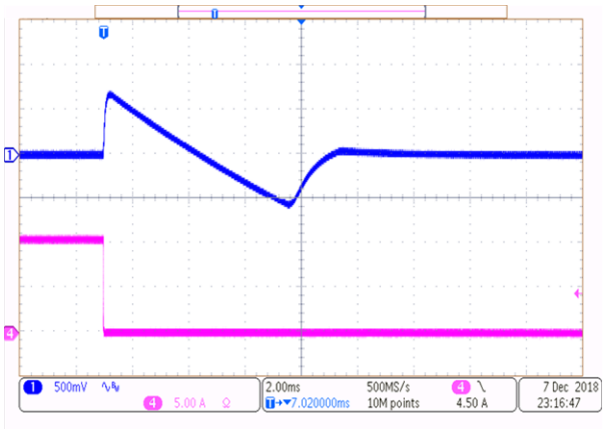


図 20. Load Step Down With 20 V_{in}

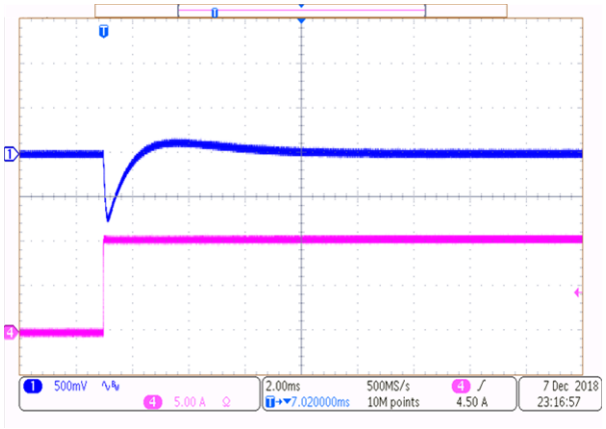


図 21. Load Step Up With 20 V_{in}

For tests shown in 図 20 and 図 21, 20 V was applied to the input and a load step was applied to the output. The load step applied was from 0 A to 10 A and 10 A to 0 A. Note that those currents do not include the 0.1-A pre-load.

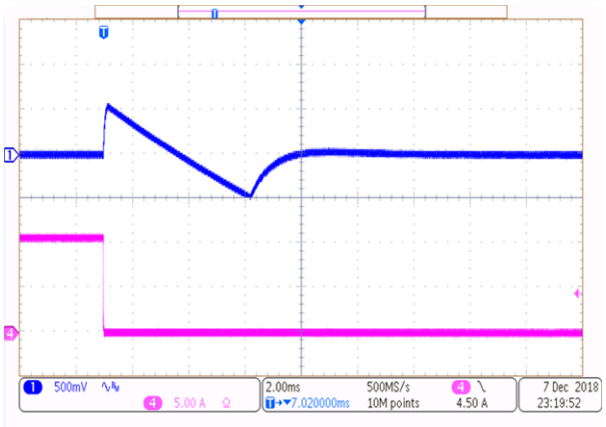


図 22. Load Step Down With 40 V_{in}

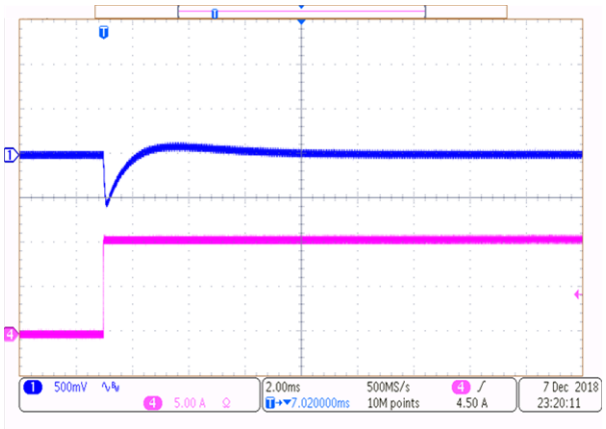


図 23. Load Step Up With 40 V_{in}

For tests shown in 図 22 and 図 23, 40 V was applied to the input and a load step was applied to the output. The load step applied was from 0 A to 10 A and 10 A to 0 A. Note that those currents do not include the 0.1-A pre-load.

3.2.2.7 Start-up

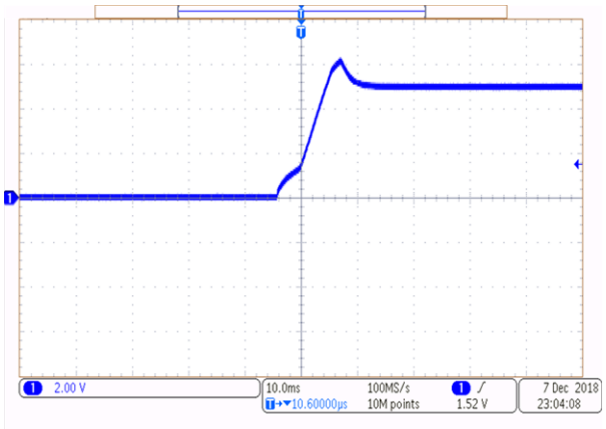


図 24. Start-up 20 V_{in} With Fully Loaded Output

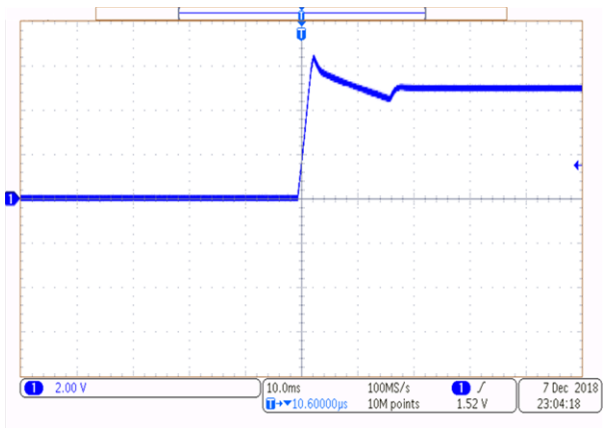


図 25. Start-up 20 V_{in} With No Load on Output

For tests shown in 図 24 and 図 25, 20 V was applied to the input from 0 V initially. The output was either loaded with 0 A on the output or 10 A. Note that those currents do not include the 0.1-A pre-load.

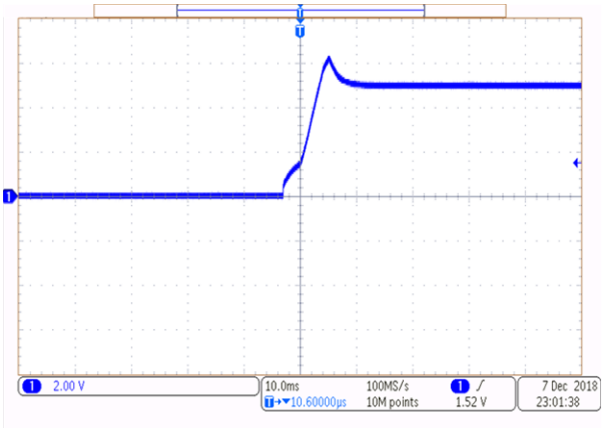


図 26. Start-up 40 V_{in} With Fully Loaded Output

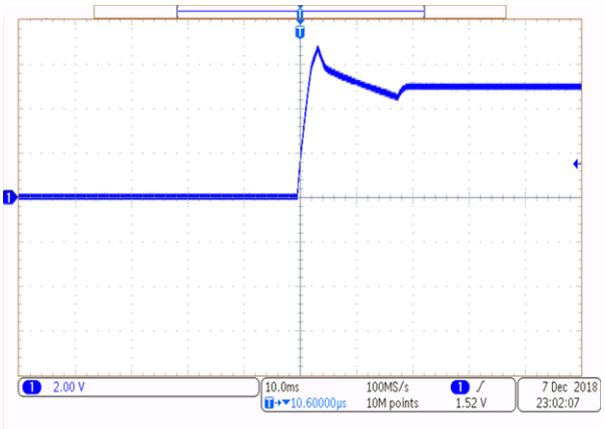


図 27. Start-up 40 V_{in} With No Load on Output

For tests shown in 図 26 and 図 27, 40 V was applied to the input from 0 V initially. The output was either loaded with 0 A on the output or 10 A. Note that those currents do not include the 0.1-A pre-load.

3.2.2.8 Shutdown

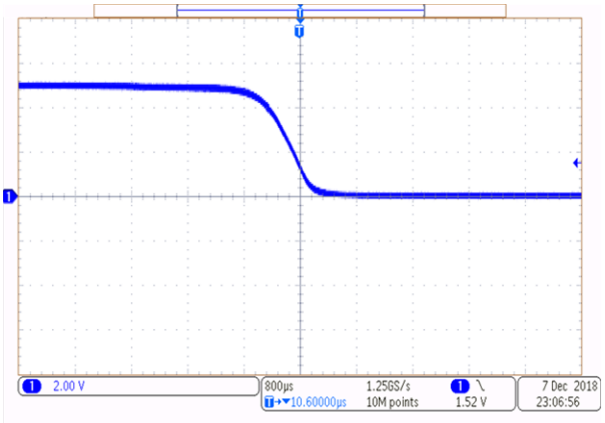


図 28. Start-up 20 V_{in} With Fully Loaded Output

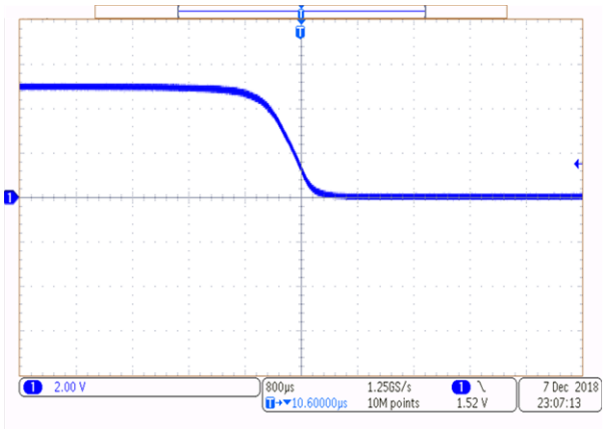


図 29. Start-up 40 V_{in} With Fully Loaded Output

For tests shown in 図 28 and 図 29, 20 V or 40 V was applied to the input and then disconnected. The output was loaded with 10 A on the output. Note that those currents do not include the 0.1-A pre-load.

3.2.2.9 Component Stresses

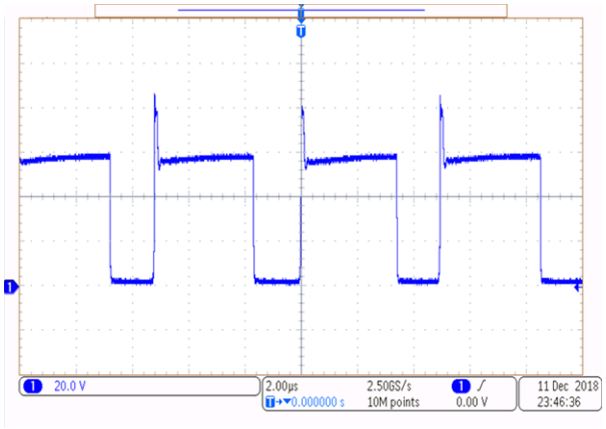


図 30. Voltage Stress on Main Switching MOSFET (Q1)

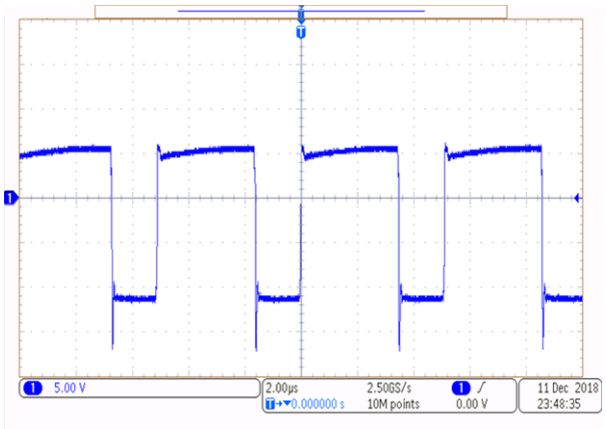


図 31. Output Diode Stress (D2)

For the test in 図 30 and 図 31, 40 V was applied to the input and 10 A was drawn from the output. For the output diode stress, the voltage was measured with respect to ground so the output voltage would have to be added to show the true stress on the output diode.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-070002.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-070002.

4.3 PCB Layout Recommendations

Make all of the power (high current) traces as short, direct, and thick as possible. It is good practice on a standard PCB to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close as possible to each other. This helps reduce the EMI radiated by the power traces due to the high-switching currents through them. This also reduces lead inductance and resistance, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. On multi-layer boards, vias are required to connect traces and different planes. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states: one state when the switch is on and one when the switch is off. During each state there is a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles and reduces radiated EMI.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-070002.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-070002.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-070002.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-070002.

5 Related Documentation

1. *Using The DRV3204EVM To Evaluate The DRV3203-Q1 application note*, SLVA559
2. *INA901-SP Radiation Hardened, –16-V to 80-V Common Mode, Unidirectional Current-Shunt Monitor data sheet*, SBOS938
3. *UC1843A-SP QML Class V, Radiation Hardened Current-Mode PWM Controller data sheet*, SLUSCI6

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2019) から **Revision B** に変更 **Page**

- タイトルを「過電流制限機能付きの 50W フライバック宇宙用のリファレンス・デザイン」から「20～40V V_{IN}、50W の宇宙グレード絶縁フライバック DC-DC 過電流保護のリファレンス・デザイン」に 変更 1
- 「概要」の段落 変更 1
- UC1843A-SP へのリンク 追加 1
- 人工衛星の絶縁型電源、放射線耐性を強化したアプリケーション、人工衛星のペイロード・アプリケーション 削除 1
- コマンドおよびデータ処理、衛星用電源システム (EPS)、光イメージングのペイロード、レーダー・イメージング・ペイロード、通信ペイロード・アプリケーションへのリンク 追加 1

2018年12月発行のものから更新 **Page**

- UCC1843-SP to UC1843-SP 変更 7
- UCC1843-SP to UC1843-SP 変更 8
- the Test Setup image 変更 12

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