参考資料

デザイン・ガイド：TIDA-010034
IP ネットワーク・カメラ向けポイント・オブ・ロードのリファレンス・デザイン、IEEE802.3at Type-1 PoE と 12V アダプタからの入力に対応

概要

PoE (Power over Ethernet) を使用すると、データと同じイーサネット・ケーブルで電力を供給でき、クロストーク、干渉、データ・ストリームの破損の危険はありません。このリファレンス・デザインでは、TI の DaVinci™デジタル・メディア・プロセッサまたは他のアプリケーション・プロセッサをベースとし、PoE または 12V アダプタで電力を供給する IP ネットワーク・カメラ用エンド・ツー・エンド電力ツリーを紹介します。この電力ツリーから、IP ネットワーク・カメラの各種ペリフェラル (例：イメージ・センサ、モータ制御、イーサネット PHY、RS485 インターフェイス、IR LED 照明、オーディオ、モーション・センシング、アラーム・インターフェイス) に必要なレールも得られます。

リソース

TIDA-010034	デザイン・フォルダ
TPS23755	プロダクト・フォルダ
TPS54202H	プロダクト・フォルダ
TPS561201	プロダクト・フォルダ
TPS562201	プロダクト・フォルダ
TPS561208	プロダクト・フォルダ
TPS562208	プロダクト・フォルダ
TLV62568	プロダクト・フォルダ
TLV62568A	プロダクト・フォルダ
TLV62569A	プロダクト・フォルダ
TPS54201	プロダクト・フォルダ
TPS2121	プロダクト・フォルダ
TLV742P	プロダクト・フォルダ

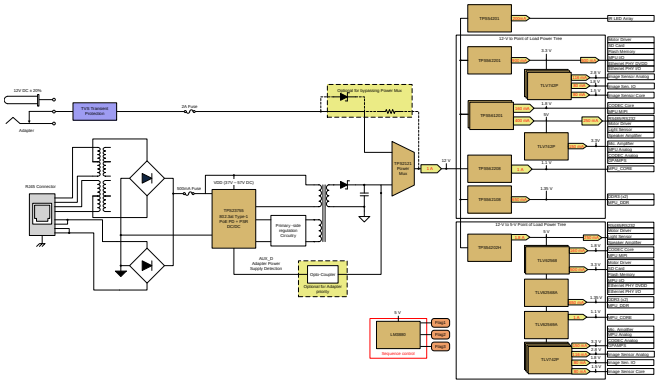
TI E2E™ Community　E2E™エキスパートに質問

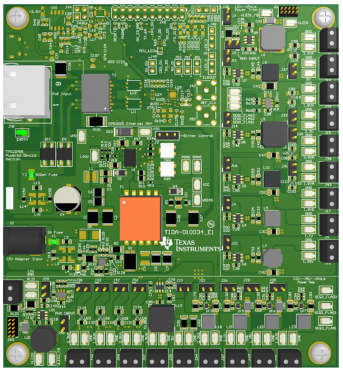
特長

- TPS23755：フォトカプラ不要のフライバック DC/DC コントローラ付き IEEE 802.3at PoE PD
  - タイプ 1 PoE 用の包括的な IEEE 802.3at PD ソリューション
  - 1 次側レギュレーション (PSR)、周波数ディザリング、高度なスタートアップ機能を持つ内蔵フライバック・コントローラ
  - 出力 12V、効率 89% の PoE 給電のフライバック電力段
  - スムーズな遷移で 2 次側アダプタを優先制御
- ダイオードの OR 処理なし：TPS2121 パワー・マルチプレクサで 2 次側 OR 処理を行い、アダプタ入力パスの消費電力を 88% 削減
- 2 つの電力ツリーを実装
  - 高効率優先：12V から PoL へ、中間入力範囲の降圧コンバータを使用
  - 低コスト優先：12V から 5V から PoL へ、低入力範囲の降圧コンバータを使用
- どちらの電力ツリーも FPWM モード付き降圧コンバータを使用
  - 高速過渡応答により、MPU コアおよび DDR RAM に電力を供給するレールで動的な負荷スイッチングに対応
  - MPU コアや DDR RAM など許容範囲が狭い電圧レールでも小さい出力電圧リップル

アプリケーション

- IP ネットワーク・カメラ





1 System Description

An IP based Ethernet network infrastructure is often already in place, which means the IP camera can easily be connected to the nearest network connection. Simply setup the IP address and you're up and running! Adding more IP cameras to a system is as easy as the first one. The ability to provide electrical power to an IP camera is an important aspect of IP video surveillance that is not available in analog security camera deployments. Analog cameras require some external power supply to meet the power requirements of the cameras. With the facility of Power over Ethernet (PoE) - supplying power directly over the network cable - an external power supply is optional, making installation much easier. Deploying IP cameras, whether indoor or outdoor, requires Power over Ethernet (PoE). Power over Ethernet technology saves time and cost of installing separate power cabling, AC outlets and wall warts, as well as eliminates the need for a dedicated UPS for individual devices. Most IP cameras in the market come with dual or triple power supply options for greater flexibility in terms of utilizing existing AC or DC power infrastructure in the buildings. The multiple power supply input options (PoE + DC input, PoE + AC input or PoE + DC + AC) also provides redundant power supply protection ensuring 24/7 reliability.

The IEEE802.3at type-1 PoE and 12-V adapter input to point-of-load reference design for IP network camera is a high efficiency, low cost and small form-factor complete power tree for an IP network camera. This reference design presents two most popular power tree implementations – first, PoE + 12V to POLs directly using mid-VIN range synchronous buck converters optimized for highest efficiency and second, PoE + 12V to 5V and then to POLs using one mid-VIN range buck converter followed by several low-VIN range buck converters optimized for low cost and reasonably high efficiency. This reference design takes care of complete power supply of an IP network camera based on the TI's DaVinci™ Digital Media Processor and different peripheral functions. This reference design system can also be adopted with minimal modifications for IP network cameras based on similar application processors. The power module also consists of rails required for different peripherals of an IP network camera like: Image sensor, motor control, Ethernet PHY, RS485 interface, IR LED illumination, audio, motion sensing and the alarm interface.

At a high level, this reference design consists of a Power-over-Ethernet (PoE) Powered Device (PD) with integrated DC/DC, Synchronous Buck Converters with Switch and low noise, high PSRR LDOs to generated different voltage rails required for an IP network camera. The Power-over-Ethernet (PoE) Powered Device (PD) is IEEE 802.3at Type-1 PD supporting up to 13-W with integrated current-mode DC-DC controller optimized for flyback topology. The synchronous step-down buck converters with forced PWM feature in SOT-563 package have been optimized for reduces output voltage ripple, fast transient response, high efficiency and compact solution size. This reference design provides a complete set of downloadable documents such as a comprehensive design guide, schematic, Altium PCB layout files, bill of materials (BOM), test results, and Gerber files that help system designers in the design and development of their end-equipment systems. The following subsections describe the various blocks within the reference design system and what characteristics are most critical to best implement the corresponding function.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATION					DETAILS
	Condition	Min	Typical	Max	Unit	
ELECTRICAL SPECIFICATION						
PoE input voltage		37	48	57	V	TPS23755 PoE PD with integrated DC-DC controller
Output voltage of PD stage		11.8	12	12.61	V	
Output current of PD stage		-	-	1	A	
Efficiency of PD stage	V_{IN} = 48-V before bridge rectifier, V_{OUT} = 12-V, I_{OUT} = 1-A	-	85	-	%	
	V_{IN} = 48-V after bridge rectifier, V_{OUT} = 12-V, I_{OUT} = 1-A	-	89	-	%	
Output ripple of PD stage	V_{OUT} = 12-V, I_{OUT} = 1-A	-	-	93.5	mV	
	V_{OUT} = 12-V, I_{OUT} = 100-mA	-	-	16.8	mV	
Input voltage to secondary side	I_{OUT_MAX}= 1-A	10	12	14	V	Adapter ORing with PD stage output
12-V TO POINT-OF-LOAD POWER TREE -- CONVERT 12-V FROM PD OUTPUT/ADAPTER INPUT DIRECTLY TO REQUIRED POWER RAILS						
DC-DC1 output voltage	V_{IN} = 12-V	5.062	5.075	5.118	V	TPS561201 DC-DC with pulse skip mode
DC-DC1 output current	V_{IN} = 12-V	-	400	-	mA	
DC-DC1 efficiency	V_{IN} = 12-V,V_{OUT} = 5-V, I_{OUT} = 400-mA	-	94.42	-	%	
DC-DC1 output ripple	V_{IN} = 12-V,V_{OUT} = 5-V	15.6	-	68	mV	
DC-DC2 output voltage	V_{IN} = 12-V	3.285	3.3	3.351	V	TPS562201 DC-DC with pulse skip mode
DC-DC2 output current	V_{IN} = 12-V	-	900	-	mA	
DC-DC2 efficiency	V_{IN} = 12-V,V_{OUT} = 3.3-V, I_{OUT} = 900-mA	-	93.65	-	%	
DC-DC2 output ripple	V_{IN} = 12-V,V_{OUT} = 3.3-V	4.6	-	17.4	mV	
DC-DC3 output voltage	V_{IN} = 12-V	1.781	1.8	1.814	V	TPS561201 DC-DC with pulse skip mode
DC-DC3 output current	V_{IN} = 12-V	-	160	-	mA	
DC-DC3 efficiency	V_{IN} = 12-V,V_{OUT} = 1.8-V, I_{OUT} = 160-mA	-	86.8	-	%	
DC-DC3 output ripple	V_{IN} = 12-V ,V_{OUT} = 1.8-V	16.8	-	35.6	mV	
DC-DC4 output voltage	V_{IN} = 12-V	1.349	1.35	1.357	V	TPS561208 DC-DC with forced PWM
DC-DC4 output current	V_{IN} = 12-V	-	650	-	mA	
DC-DC4 efficiency	V_{IN} = 12-V,V_{OUT} = 1.35-V, I_{OUT} = 650-mA	-	87.3	-	%	
DC-DC4 output ripple	V_{IN} = 12-V ,V_{OUT} = 1.35-V	11.2	-	11.2	mV	

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATION					DETAILS
DC-DC5 output voltage	V_{IN} = 12-V	1.096	1.1	1.109	V	TPS562208 DC-DC with forced PWM
DC-DC5 output current	V_{IN} = 12-V	-	1000	-	mA	
DC-DC5 efficiency	V_{IN} = 12-V,V_{OUT} = 1.1-V, I_{OUT} = 1000-mA	-	81.64	-	%	
DC-DC5 output ripple	V_{IN} = 12-V ,V_{OUT} = 1.1-V	11.2	-	11.2	mV	
LDO1 output current	V_{IN} = 5-V ,V_{OUT} = 3.3-V	-	150	-	mA	TLV742P
LDO2 output current	V_{IN} = 3.3-V ,V_{OUT} = 2.8-V	-	116	-	mA	TLV742P
LDO3 output current	V_{IN} = 3.3-V ,V_{OUT} = 1.8-V	-	80	-	mA	TLV742P
LDO4 output current	V_{IN} = 3.3-V ,V_{OUT} = 1.5-V	-	80	-	mA	TLV742P
12-V TO 5-V TO POINT-OF-LOAD POWER TREE -- CONVERT 12-V FROM PD OUTPUT/ADAPTER INPUT TO 5-V AND THEN STEP DOWN 5-V TO REQUIRED POWER RAILS						
DC-DC1 output voltage	V_{IN} = 12-V	4.986	5	5.011	V	TPS54202H DC-DC with pulse skip mode
DC-DC1 output current	V_{IN} = 12-V	-	1800	-	mA	
DC-DC1 efficiency	V_{IN} = 12-V,V_{OUT} = 5-V, I_{OUT} = 1800-mA	-	91.87	-	%	
DC-DC1 output ripple	V_{IN} = 12-V ,V_{OUT} = 5-V	7.44	-	20.8	mV	
DC-DC2 output voltage	V_{IN} = 5-V	3.296	3.3	3.336	V	TLV62568 DC-DC with pulse skip mode
DC-DC2 output current	V_{IN} = 5-V	-	500	-	mA	
DC-DC1 efficiency	V_{IN} = 5-V,V_{OUT} = 3.3-V, I_{OUT} = 500-mA	-	95.14	-	%	
DC-DC2 output ripple	V_{IN} = 5-V ,V_{OUT} = 3.3-V	7.6	-	38.4	mV	
DC-DC3 output voltage	V_{IN} = 5-V	1.778	1.8	1.803	V	TLV62568 DC-DC with pulse skip mode
DC-DC3 output current	V_{IN} = 5-V	-	160	-	mA	
DC-DC3 efficiency	V_{IN} = 5-V,V_{OUT} = 1.8-V, I_{OUT} = 160-mA	-	90.94	-	%	
DC-DC3 output ripple	V_{IN} = 5-V ,V_{OUT} = 1.8-V	5.52	-	22.4	mV	
DC-DC4 output voltage	V_{IN} = 5-V	1.336	1.35	1.343	V	TLV62568A DC-DC with forced PWM
DC-DC4 output current	V_{IN} = 5-V	-	650	-	mA	
DC-DC4 efficiency	V_{IN} = 5-V,V_{OUT} = 1.35-V, I_{OUT} = 650-mA	-	91.85	-	%	
DC-DC4 output ripple	V_{IN} = 5-V ,V_{OUT} = 1.35-V	6	-	6	mV	

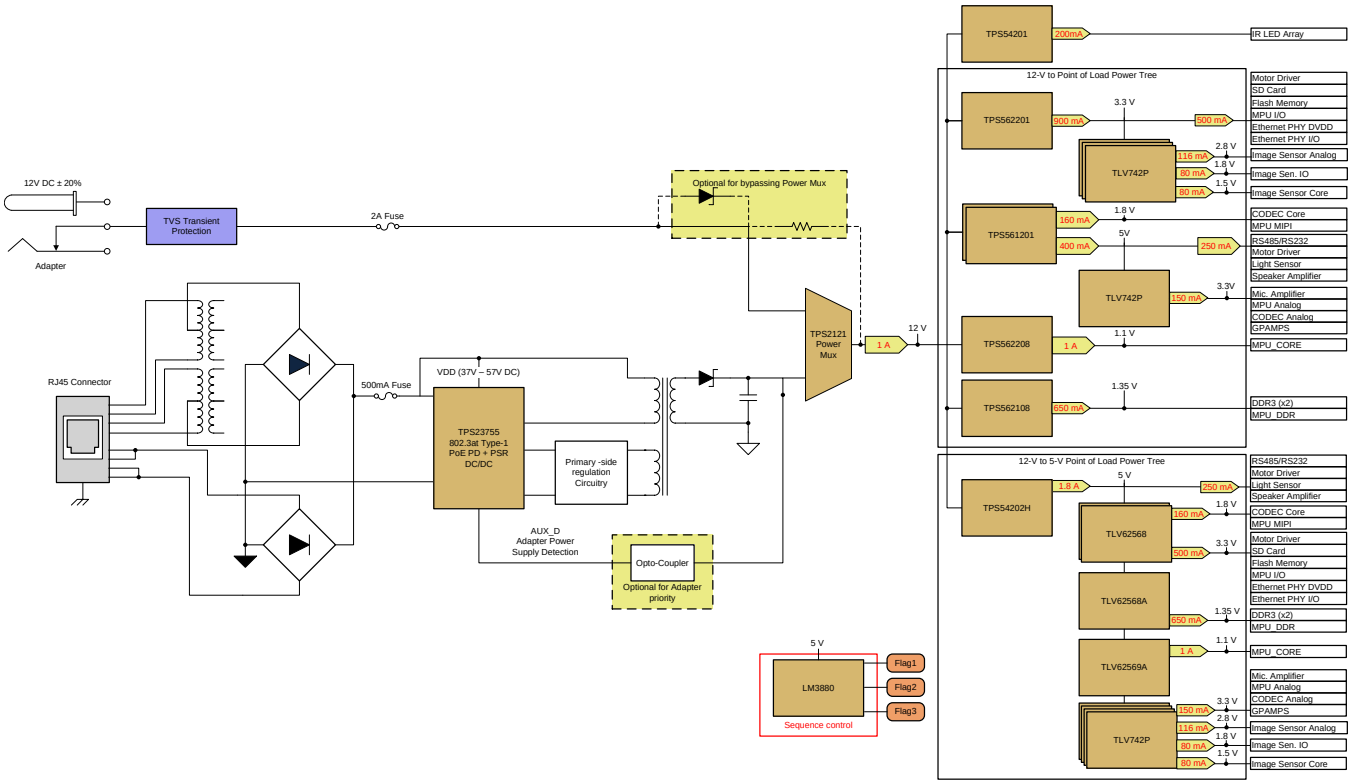
表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATION					DETAILS
DC-DC5 output voltage	V_{IN} = 5-V	1.08	1.089	1.09	V	TLV62569A DC-DC with forced PWM
DC-DC5 output current	V_{IN} = 5-V	-	1000	-	mA	
DC-DC5 efficiency	V_{IN} = 5-V,V_{OUT} = 1.1-V, I_{OUT} = 1000-mA	-	89.52	-	%	
DC-DC5 output ripple	V_{IN} = 5-V ,V_{OUT} = 1.1-V	8.4	-	8.4	mV	
LDO1 output current	V_{IN} = 5-V ,V_{OUT} = 3.3-V	-	150	-	mA	TLV742P
LDO2 output current	V_{IN} = 5-V ,V_{OUT} = 2.8-V	-	116	-	mA	TLV742P
LDO3 output current	V_{IN} = 5-V ,V_{OUT} = 1.8-V	-	80	-	mA	TLV742P
LDO4 output current	V_{IN} = 5-V ,V_{OUT} = 1.5-V	-	80	-	mA	TLV742P
ENVIRONMENTAL						
Operating temperature		-55	25	125	°C	

2 System Overview

2.1 Block Diagram

図 1. TIDA-010034 Block Diagram



2.2 Highlighted Products

2.2.1 TPS23755

The TPS23755 device is a 24-pin integrated circuit that contains all of the features needed to implement an IEEE802.3at type-1 powered device (PD), combined with a fully integrated 150-V switching power FET and a current-mode DC-DC controller optimized for flyback switching regulator designs using primary side control. The TPS23755 applies to single-output flyback converter applications where a secondary side diode rectifier is used.

Basic PoE PD functionality supported includes detection, hardware classification, and inrush current limit during startup. DC-DC converter features include startup function and current-mode control operation. The TPS23755 device integrates a low 0.36-Ω internal switch to support type-1 applications. The TPS23755 features secondary auxiliary power detect (AUX_D) capability, providing priority for a secondary side power adapter, while ensuring smooth transition (through AUX_V) to and from the PoE power input.

2.2.2 TPS54202H

The device is a 28-V, 2-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design. The TPS54202H's switching frequency is fixed to 500 kHz.

2.2.3 TPS561201, TPS561208

The TPS561201 and TPS561208 are 1-A synchronous step-down converters. The proprietary D-CAP2 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 mode control can reduce the output capacitance required to meet a specific level of performance.

2.2.4 TPS562201, TPS562208

The TPS562201 and TPS562208 are 2-A synchronous step-down converters. The proprietary D-CAP2 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 mode control can reduce the output capacitance required to meet a specific level of performance.

2.2.5 TPS54201

The TPS5420x device is a 1.5-A synchronous buck LED driver up to 28-V input. Current-mode operation provides fast transient response. The optimized internal compensation network minimizes the external component count and simplifies the control loop design. The TPS5420x device has a fixed 600-kHz switching frequency for a good tradeoff between efficiency and size. The integrated 150-mΩ high-side MOSFET and 70-mΩ low-side MOSFET allow for a high-efficiency LED driver with continuous output current up to 1.5 A.

The TPS5420x device supports deep dimming in both analog and PWM dimming modes. In analog dimming mode, the internal reference voltage is changed in proportion to the duty cycle of the PWM signal in the 1% to 100% range. In the PWM dimming mode, the LED turns on and off periodically according to the PWM duty cycle. For higher efficiency, the internal reference is halved to 100 mV.

2.2.6 TLV62568A,TLV62569A

These devices are high-efficiency, fixed switching frequency synchronous step-down converters with 1-A and 2-A output current. These devices operate with an adaptive off time with peak current control scheme and operate at typically 1.5-MHz frequency pulse width modulation (PWM) . Based on the VIN/VOUT ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

2.2.7 TLV62568,TLV62569

These devices are high-efficiency synchronous step-down converters with 1-A and 2-A output current. These devices operate with an adaptive off time with peak current control scheme. The devices operate at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate-to-heavy load currents. Based on the VIN/VOUT ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

2.2.8 TLV742P

The TLV742P device belongs to a family of LDOs. This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (VIN – VOUT) headroom, make this device ideal for portable RF applications.

2.2.9 LM3880

The LM3880 simple power supply sequencer provides a simple solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open-drain output flags. These flags permit connection to either a shutdown or enable pin of linear regulators and switchers to control the operation of the power supplies. This allows design of a complete power system without concern for large inrush currents or latch-up conditions that can occur

2.2.10 TPS2121

The TPS212x devices are dual-input, single-output (DISO) power multiplexer (MUX) that are well suited for a variety of systems having multiple power sources. The devices will automatically detect, select, and seamlessly transition between available inputs. Priority can be automatically given to the highest input voltage or manually assigned to a lower voltage input to support both ORing and source selection operations. A priority voltage supervisor is used to select an input source.

2.3 System Design Theory

This section explains the design theory (and equations, if required) for each of the devices used in the design. Video surveillance cameras such as analog security camera, IP network camera, pan tilt and zoom (PTZ) cameras typically consist of powerful processor interfacing with high-speed image sensor and video encoder. The processor also interfaces with SD RAM, flash memory, audio CODEC supporting two-way audio communication, Ethernet PHY and lens driver with IR cut filter sub circuitry.

From a power perspective, many different supply rails need to be generated to derive core voltage, I/O voltage and analog voltage for the peripherals.

2.3.1 TPS23755 Power Stage Design Considerations

The TPS23755 is optimized for primary-side-regulated diode rectified flyback topologies for 12-V outputs or higher due to its good balance of high efficiency and output voltage regulation. The TPS23755 integrates a DC-DC controller which can operate with feedback from an auxiliary winding of the flyback power transformer, eliminating the need for external shunt regulator and opto-coupler. It also operates with continuously connected feedback, enabling better optimization of the power supply and resulting in significantly lower noise sensitivity.

表 2. Design Parameters

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNIT
POWER INTERFACE					
Input voltage	Applied to the PoE input	37		57	V
	Applied to the secondary input		12		V
Input UVLO, POE input	Rising input voltage			36	V
	Falling input voltage	30			
Detection voltage	At device terminals	2.7		10.1	V
Classification voltage	At device terminals	14.5		20.5	V
Classification current	R_{CLASS} = 45.3 Ω	26.5		29.3	mA
Inrush current-limit				140	mA
Operating current-limit				550	mA

表 2. Design Parameters (continued)

PARAMETER	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNIT
DC-TO-DC CONVERTER					
Output voltage	V_{IN} = 48 V, I_{OUT} = 1-A		12		V
Output current	37-V ≤ V_{IN} ≤ 57-V		1		A
Maximum limit of duty cycle	D_{MAX}		78.5		%
Maximum duty cycle for design	D_{MAX_DESIGN}		50		
Output ripple voltage peak-to-peak	V_{IN} = 48-V, I_{OUT} = 1-A			80	mV
Efficiency, end-to-end	V_{IN} = 48-V, I_{OUT} = 100-mA		78		%
	V_{IN} = 48-V, I_{OUT} = 500-mA		86		
	V_{IN} = 48-V, I_{OUT} = 1-A		87		
Switching frequency				250	kHz

2.3.1.1 Input Bridge Rectifier (D9 and D11)

Using Schottky diodes instead of PN junction diodes for the PoE input bridges reduces the power dissipation in these devices by about 30%. The IEEE standard specifies a maximum backfeed voltage of 2.8 V. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet.

Increasing R_{DEN} slightly may also help meet the requirement. Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. In this design, a 0.8-A, 100-V rated PN junction diode bridge is used for the input rectifiers.

2.3.1.2 TVS for Protection (D10)

D10 is used to protect the powered-device (PD) controller front-end from overvoltage due to line transients, hotplug into 48-V sources, and output faults. A transient suppressor diode, such as the SMAJ58A, must be connected from V_{DD} to V_{SS}.

2.3.1.3 Input Capacitor (C14)

The IEEE802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 µF to 0.12 µF. A 0.1-µF, 100-V, 10% ceramic capacitor is used in this design.

2.3.1.4 Detection Resistor (R12)

A resistor from CLS to V_{SS} programs the classification current according to the IEEE802.3at standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to 表 3.

表 3. Class Resistor Selection

CLASS	POWER AT PD PI		RESISTOR (Ω)
	MINIMUM (W)	MAXIMUM (W)	
0	0.44	12.95	649
1	0.44	3.84	121
2	3.84	6.49	68.1

表 3. Class Resistor Selection (continued)

CLASS	POWER AT PD PI		RESISTOR (Ω)
3	6.49	12.95	45.3

Class 0 and R_{CLS} = 649 Ω is chosen for this design.

2.3.1.5 Output Voltage Feedback Divider (R14, R15, R18 and R21)

R14, R15, and R18 set the output voltage of the bias winding of the converter. TPS23755's unique auxiliary power detect capability provides priority to a secondary side power adapter, while ensuring smooth transition to and from the PoE power. Whenever the auxiliary power is present, a signal (AUX_D) tells the PD PWM to lower its output voltage slightly below the auxiliary voltage to ensure that auxiliary has priority to power the main output. When the auxiliary power goes away, the DC-DC converter increases back its output voltage, to ensure seamless transition. 式 1

式 1 can be used to set output voltage on the bias winding when auxiliary power is not present.

$$V_{BIAS} = \frac{V_{REFC}\left\{\left(R14+R15\right)\times R18+\left(R14+R15\right)\times R21+R21\times R18\right\}}{R21\times R18} \quad (1)$$

式 2 can be used to set output voltage on the bias winding when auxiliary power is present.

$$V_{BIAS} = \frac{V_{REFC}\left(R14+R15+R21\right)}{R21} \quad (2)$$

Where,

- V_{BIAS} is output voltage on bias winding of DC-DC stage
- V_{REFC} is feedback regulation voltage (minimum 1.723 V, typical 1.75 V, maximum 1.777 V)

In this design, R14 = 49.9 ohm, R15 = 24.9 Kohm, R18 = 8.66 Kohm, and R21 = 6.49 Kohm are selected for V_{BIAS} = 13.4 V when auxiliary power is not present and V_{BIAS} = 8.5 V when auxiliary power is present.

注: For applications that do not use auxiliary power detection functionality, R21 can be de-populated.

2.3.1.6 Setting Switching Frequency (R28)

The converter switching frequency in PWM mode is set by connecting resistor R28 from the FRS pin to RTN. For 250-KHz switching frequency, the resistor value is selected using the following equation:

$$R28\left(K\Omega\right) = \frac{15000}{f_{SW}\left(KHz\right)} = \frac{15000}{250} = 60\ K\Omega \quad (3)$$

Where,

- f_{SW} is the desired switching frequency

A standard 60.4-kΩ resistor is used in this design.

2.3.1.7 Frequency Dithering (R24 and C24)

The frequency dithering feature in the TPS23755 can be used to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements.

The oscillator frequency can be dithered by connecting a capacitor from DTHR to RTN and a resistor from DTHR to FRS. An external capacitor, C24, is selected to define the modulation frequency fm. This capacitor is being continuously charged and discharged between slightly less than 0.5 V and slightly greater than 1.5 V by a current source/sink equivalent to approximately 3 times the current through FRS pin. C24 capacitor value is defined according to the following equation:

$$C24(nF) = \frac{3 / R28(\Omega)}{2.052 \times f_m(Hz)} = \frac{49.6\ \mu A}{2.052\ V \times 11000\ Hz} = 2.2\ nF \quad (4)$$

Where,

- fm is the modulation frequency: fm should always be greater than 9 kHz, which is the resolution bandwidth applied during conducted emission measurement. Typically, fm should be set to around 11 kHz to account for component variations.

The resistor R24 is used to determine Δf, which is the amount of dithering, and its value is determined according to 式 5.

$$R24(\Omega) = \frac{0.513 \times R28(\Omega)}{\%DTHR} = \frac{0.513 \times 60.4\ K\Omega}{0.132} = 235\ K\Omega \quad (5)$$

Where,

- %DTHR is the dithering with a nominal switching frequency set by resistor R28

In this case, 13.2% dithering with a nominal switching frequency of 250 kHz results in frequency variation of ±33 kHz. A standard 237-kΩ resistor and 2.2-nF capacitor are used in this design.

2.3.1.8 Transformer Design (T1)

The turns ratio and primary inductance are important parameters to consider in a flyback transformer. The turns ratio act to limit the maximum duty cycle and reduce stress on the secondary components while the primary inductance sets the current ripple. In CCM operation, the higher inductance allows for a reduced current ripple which can help with EMI performance and noise. For primary-side regulated flyback converters, the transformer construction is important to maintain good regulation on the secondary output.

REQUIRED TRANSFORMER TURNS RATIOS

Assumed maximum duty cycle for design, D_{MAX_DESIGN} = 0.50. 式 6 yields a maximum primary to secondary turns ratio at $V_{FLYBACK\_MIN}$ and D_{MAX_DESIGN}.

$$N_{PS} = \frac{D_{MAX\_DESIGN}}{1 - D_{MAX\_DESIGN}} \times \frac{V_{FLYBACK\_MIN}}{V_{OUT} + V_{DIODE}} = 2.71 \quad (6)$$

$V_{FLYBACK\_MIN}$ is the minimum voltage at transformer primary winding calculated by using 式 7.

$$V_{FLYBACK\_MIN} = V_{INPUT\_MIN} - 2 \times I_{IN\_MAX} \times DCR_{WINDING} - (2 \times V_{BRIDGE}) - V_{FUSE\_DROP} - \left[I_{IN\_MAX} \times \left\{ (2 \times DCR_{FERRITE\_BEAD}) + DCR_{FILTER} + R_{CURRENT\_SENSE} + R_{DS\_MAX} \right\} \right] \quad (7)$$

$$V_{FLYBACK\_MIN} = 37\ V - 2 \times 0.35\ A \times 0.65\ \Omega - (2 \times 0.7\ V) - 0.125\ V - \left[0.35\ A \times \left\{ (2 \times 0.07\ \Omega) + 0.138\ \Omega + 0.55\ \Omega + 1.28\ \Omega \right\} \right] = 34.38\ V \quad (8)$$

Where,

- V_{INPUT_MIN} is the minimum voltage applied at PoE input = 37 V
- I_{IN_MAX} is the maximum allowable current from PoE input = 350 mA
- $DCR_{WINDING}$ is the maximum DC resistance of winding of Ethernet transformer (T1) = 0.65 ohm
- V_{BRIDGE} is the maximum voltage drop of diode in bridge rectifier (D9 and D11) = 0.7 V
- V_{FUSED_ROP} is the maximum voltage drop across a 500-mA fuse (F2) = 125 mV
- $DCR_{FERRITE\_BEAD}$ is the maximum DC resistance of ferrite beads in input and return path (L12 & L15) = 0.7 ohm
- DCR_{FILTER} is the maximum DCR of input filter inductor (L1) = 0.138 ohm
- R_{DS_MAX} is the maximum drain-to-source resistance of 150-V Power FET integrated in TPS23755 = 1.28 ohm
- V_{DIODE} is the maximum forward voltage of rectifier diode (D1) used on the secondary side = 0.62 V

The equations yield a maximum primary to bias turns ratio at $V_{FLYBACK\_MIN}$ and D_{MAX_DESIGN}.

$$N_{PB} = \frac{D_{MAX\_DESIGN}}{1 - D_{MAX\_DESIGN}} \times \frac{V_{FLYBACK\_MIN}}{V_{BIAS}} = 2.55 \quad (9)$$

PRIMARY INDUCTANCE

The following equation yields a minimum primary inductance required to keep the peak current below that in 式 10.

$$L_P = \frac{D_{MAX\_DESIGN}}{f_{SW\_NOM}} \times \frac{V_{FLYBACK\_MIN}}{\Delta I_L} = 137\ \mu H \quad (10)$$

Where,

- ΔIL is assumed to be 50% of primary side peak current.

The LDT0950 transformer is used in this design with 2.58 primary-to-secondary winding turns ratio (N_{PS_ACTUAL}), 2.25 primary to bias winding turns ratio (N_{PB_ACTUAL}), and 150-uH primary inductance (L_{P_ACTUAL}).

ACTUAL DUTY CYCLE AT VOLTAGE USING SELECTED TRANSFORMER

$$D_{MAX\_ACTUAL} = \frac{\left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}}{V_{FLYBACK\_MIN} + \left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}} = 0.487 \quad (11)$$

$$D_{MIN\_ACTUAL} = \frac{\left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}}{V_{FLYBACK\_MAX} + \left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}} = 0.363 \quad (12)$$

Where $V_{FLYBACK\_MAX}$ is assumed to be 57 V.

$$D_{NOM\_48V} = \frac{\left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}}{48\ V + \left(V_{OUT} + V_{DROP\_SECONDARY}\right) \times N_{PS\_ACTUAL}} = 0.404 \quad (13)$$

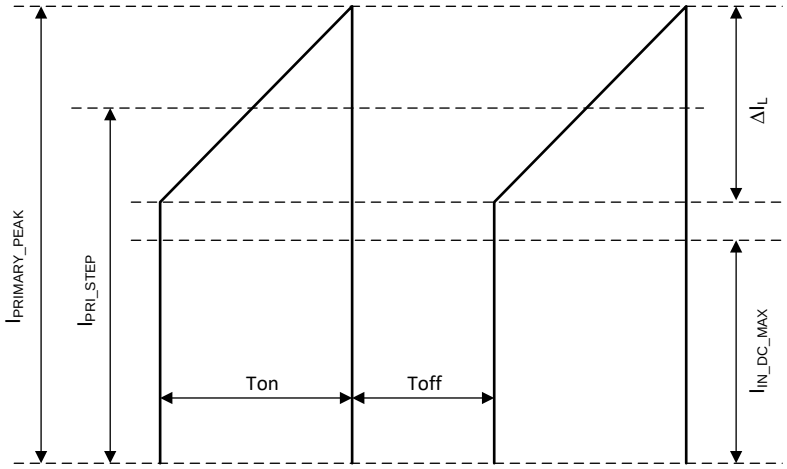
2.3.1.9 Bulk Capacitance (C4) and Input Filter (L1, C5 and C6)

The input capacitance must furnish the transient switching current, and the bulk capacitance furnishes input transients during heavy loads and long cable length conditions. It also helps with stability on the DC-DC converter. An inductor, L1 provides another layer of filtering and reduces the requirements on C5 and C6 which provide switching energy absorption.

CALCULATE PRIMARY CURRENTS

An example of the primary current waveform is shown in 図 2.

図 2. Primary Current Waveform



Low line average DC input current:

$$I_{IN\_DC\_MAX} = \frac{P_{OUT\_MAX}}{V_{FLYBACK\_MIN} \times \eta_{FB}} = \frac{12\ W}{34.28\ V \times 0.85} = 0.411\ A \quad (14)$$

Where η_{FB} is the assumed efficiency for DC-DC converter stage

On-state step current:

$$I_{PRI\_STEP} = \frac{I_{IN\_DC\_MAX}}{D_{MAX\_ACTUAL}} = 0.847\ A \quad (15)$$

Ramp current:

$$\Delta I_L = \frac{D_{MAX\_ACTUAL}}{f_{SW\_NOM}} \times \frac{V_{FLYBACK\_MIN}}{L_{P\_ACTUAL}} = 0.445\ A \quad (16)$$

Peak current:

$$I_{PRIMARY\_PEAK} = I_{PRI\_STEP} + \frac{\Delta I_L}{2} = 1.07\ A \quad (17)$$

Target input ripple voltage, V_{IN_RIPPLE} » 0.4V

$$C_{IN\_MIN} = \frac{\left(I_{PRI\_STEP} - I_{IN\_DC\_MAX}\right) \times D_{MAX\_ACTUAL}}{f_{SW\_NOM} \times V_{IN\_RIPPLE}} \quad (18)$$

For this design, Two capacitors with capacitance 1-µF, X7R ceramic, 100-V, 10-m ESR at 100 + kHz 2ARMS ripple current rating are selected.

$$\Delta V_{IN\_C_{IN}} = \frac{\left(I_{PRI\_STEP} - I_{IN\_DC\_MAX}\right) \times D_{MAX\_ACTUAL}}{f_{SW\_NOM} \times C_{IN\_SELECTED}} + I_{PRI\_STEP \times ESRC_{IN\_SELECTED}} = 0.197\ V \quad (19)$$

A common-type aluminum electrolytic capacitor for C_{BULK} is selected and then inductor sizing is done to achieve the additional attenuation of the ripple voltage.

Choosing C1 = 10-µF, aluminum electrolytic, 100-V, 0.9-Ω ESR and 85-mA ripple current rating as per datasheet targeting: ΔI_{CIN1} < 0.085 A so $\Delta V_{IN1} = \Delta I_{CIN1}$ x ESR_{CIN1} = 76m V

$$L_{IN} = \frac{\Delta V_{IN\_C_{IN}} + \Delta V_{CIN1}}{I_{PRI\_STEP} - I_{IN\_DC\_MAX} - \Delta I_{CIN1}} \times \frac{D_{MAX\_ACTUAL}}{f_{SW\_NOM}} = 1.52\ \mu H \quad (20)$$

A 3.3-µH, 1.5-ARMS, 138-mΩ inductor is selected.

2.3.1.10 Primary FET Clamping (R1, C3 and D2)

The stored energy in the leakage inductance of the power transformer can cause ringing during the primary FET turnoff. The snubber is chosen to mitigate primary FET overshoot and oscillation while maintaining high overall efficiency.

Without a snubber, the stored energy in the leakage inductance rings with the transformer inter-winding (C_{WDG}) and MOSFET output capacitance (C_{OSS}) at MOSFET turnoff. The transformer winding capacitance can be several hundred picofarads.

$$V_{SPIKE} = I_{PRIMARY\_PEAK} \times \sqrt{\frac{L_{LKG}}{C_{CWG} + C_{COSS}}} = 1.07\ A \times \sqrt{\frac{1.3\ \mu H}{100\ pF}} = 114\ V \quad (21)$$

Where

- L_{LKG} is leakage inductance (value from the transformer datasheet).

For V_{SPIKE_NEW} = 10 V so C3 should be selected as per the following equation.

$$C3 > \left(\frac{V_{SPIKE}}{V_{SPIKE\_NEW}}\right)^2 \times \left(C_{CWG} + C_{COSS}\right) = 12.9\ nF \quad (22)$$

R1 is chosen so that the snubber time constant is much larger (for example, 500 times larger) than the switching period.

$$R1 = \frac{500}{f_{SW} \times C3} = 20\ k\Omega \quad (23)$$

A 39-kΩ (125-mW) resistor and 0.1-uF (100-V) capacitor are used in this design. Diode D2 is an ultra-fast diode with a short forward recovery time allowing the snubber to turn on quickly.

2.3.1.11 Current Sense Resistor (R10 and R11)

The current sense resistor should be chosen based on the peak primary current at the desired output current limit.

$$R_{CURRENT\_SENSE} = \frac{V_{CSMAX}}{I_{PRIMARY\_PEAK}} = 0.55\ \Omega \quad (24)$$

Where,

- V_{CSMAX} is the maximum threshold voltage (minimum 0.5 V, typical 0.55 V, maximum 0.6 V)

Two 0.91-ohm resistors (R10 and R11) are connected in parallel for 1-A peak primary current.

2.3.1.12 Current Slope Compensation (R13)

The slope compensation resistor is used when internally provided slope compensation is not enough. The down slope of the reflected secondary current through the current sense resistor at each switching period is determined and a percentage (typically 50%-75%) of it will define V_{SLOPE}. Using the LDT0950, TI recommends starting with 251 mV and using the following equation:

$$R13(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(\frac{V_{SLOPE}(mV)}{D_{MAX}}\right)\right]}{\frac{I_{SL\_EX}(\mu A)}{D_{MAX}}} \times 1000 = \frac{\left[251\,mV - \left(\frac{155\ mV}{78.5\%}\right)\right]}{\frac{42\ \mu A}{78.5\%}} = 1\,K\Omega \quad (25)$$

2.3.1.13 Bias Supply Requirements (D4 and C16)

Advanced startup in the TPS23755 allows for relatively low capacitance on the bias circuit. A 1-uF, 10%, 25-V ceramic capacitor and MMSD4148 diode (100 V, 200 mA) are used on bias winding output.

2.3.1.14 Switching Transformer Considerations (R3 and C11)

R3 helps to reduce peak charging from the bias winding. Reduced peak charging becomes especially important when tuning hiccup mode operation during output overload. A 1-uF, 10%, 25-V ceramic capacitor and 10-ohm resistor are used in this design.

2.3.1.15 Internal Control Rail Capacitor (C25)

VB pin is bypassed with a 0.1-µF ceramic capacitor to RTN. The switching MOSFET gate driver draws current directly from the VB pin, which is the output of an internal 5-V regulator fed from VCC.

2.3.1.16 Secondary Output Diode Rectifier (D1)

The output rectifier diode should have low forward voltage drop at secondary peak current. Consideration must be given to a safe operating area during output overload conditions. For a 12-V output, PDS360-13 in a high thermal performance package (60 V reverse voltage, 3-A continuous current maximum, V_f = 0.62 V maximum at 3 A) is used in this design.

2.3.1.17 Output Capacitance (C7, C8)

The output capacitor is considered as part of the overall stability of the converter, output voltage ripple, and load transient response. The minimum capacitance is typically determined by the output voltage ripple as shown in 式 26.

$$C_{OUT} > \frac{I_{OUT}(A) \times D_{MAX\_ACTUAL}}{V_{Ripple}(V) \times f_{SW}(Hz)} = \frac{1A \times 0.468}{0.05\ V \times 250\ KHz} = 37.4\ \mu F \quad (26)$$

In this design, two 22-µF ceramic capacitors are used in parallel at the DC-DC converter output.

2.3.1.18 Slew Rate Control (R23 and R26)

R23 and R26 minimize primary drain-source oscillations and help optimize EMI performance at high frequencies. This design also has provisions for R22 and R25 potentiometers which can be adjusted during bench and EMI testing.

2.3.1.19 Shutdown at Low Temperatures (D6 and C13)

For applications operating near –10°C or less, there may be some extra switching cycles during removal of the PoE input or during shutdown. It is acceptable for most applications, however, for a more monotonic shutdown of the output voltage during power removal.

2.3.2 ORing With Adapter Input

The adapter configuration bypasses the flyback transformer by applying the adapter voltage directly to the secondary side of the TPS23755 converter section. This reference design uses the TPS2121 priority power MUX for ORing 12-V adapter input and flyback stage output. The TPS2121 has a maximum 100-mohm on-state resistance (-40°C to 125°C) which helps to reduce power dissipation in adapter input path. Power MUX also helps to achieve seamless switch over between PoE and adapter supply within 5 us (typical) and maintains power signature (MPS) with power sourcing equipment (PSE) irrespective of adapter presence and absence. An Ideal Diode operation is used to seamlessly transition between input sources. During switchover, the voltage drop is controlled to block reverse current before it happens and provide uninterrupted power to the load with minimal hold-up capacitance.

This design also has provision for traditional ORing implementation using Schottky diodes.

2.3.3 Buck DC-DC Regulator

The buck converter has two sections that impact the performance. One section is the power stage, and the other is the control topology. Power stage remains the same for all control topology. The inductor value is computed based on the preferred mode of switching operation whereas the control loop effects the loop response time, undershoot and overshoot in output voltage, output voltage ripple, and full- and light-load efficiency.

TI offers devices with 12 different types of control architectures. Most commonly used are output voltage control, peak current control, and hysteric or adaptive or fixed on time. Application requirements are driving factors for selecting the control topology. In this application, fast output response, low voltage ripple, high DC voltage accuracy with minimum external components, and seamless transition from PWM to power save mode are required. The DCS-Control architecture is selected for high current demanding rail such as MPU core voltage and DDR rail. This architecture offers benefits of both voltage control loop for high DC accuracy and hysteric control loop for seamless transition, fast response with minimum external components with only trade off of wide variation of switching frequency as function of load current.

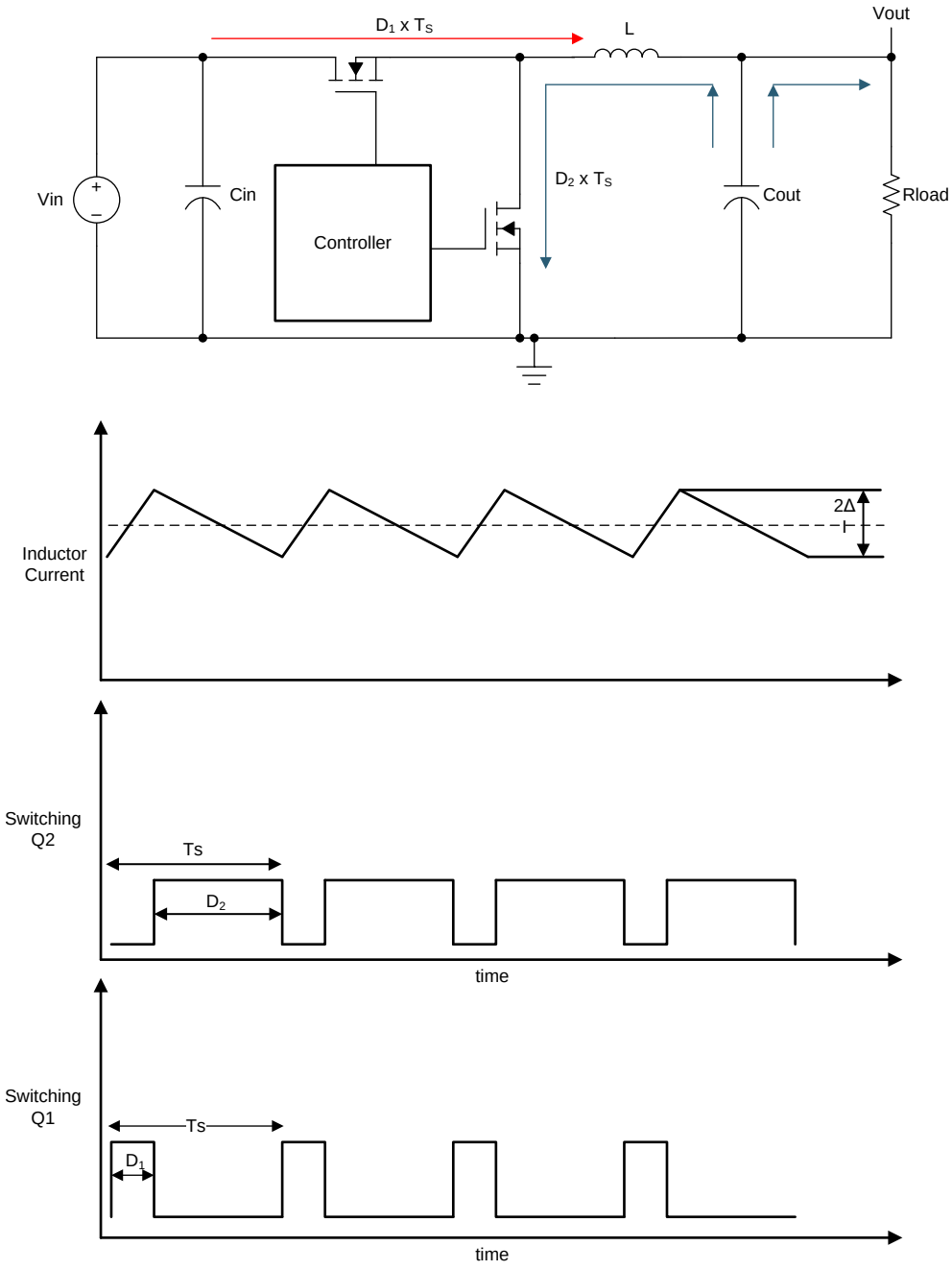
2.3.3.1 Buck Power Stage Design Consideration

Before computing the power stage inductor and capacitor values, the operating mode for the maximum period of operation needs to considered. The rails which operate most of time in moderate to full load,CCM mode is preferred (core voltage and 3.3 V) whereas rails which operate most of time in light to moderate load, DCM mode is considered (DDR3 and sensor voltage).

2.3.3.2 Inductor Ripple Current CCM Mode

In CCM mode, the inductor ripple is a non-zero AC triangular ripple waveform with DC offset equal to output current as shown in 図 3.

図 3. CCM Mode Current and Switching Waveforms



CCM mode reduces AC core loss for moderate to full load. For the flux swing in inductor core to be less than one half of maximum flux density, ripple current should be chosen between 20% - 40% of output DC current. In this mode, there are two events in one switching cycle. To reduce DC loss and thermal hotspot for full load current, it is required that the DCR of inductor should be as low as possible. To achieve very small DCR, a lower number of turns is required, which results into smaller inductance value. For lower switching frequency, the ripple current will increase, dominating core and AC losses.

The operating duty cycle and power stage inductor can be computed using 式 27 and 式 28.

$$D = \frac{V_{OUT} + V_{DS\_LOW}}{V_{IN\_MIN} - V_{DS\_HIGH} + V_{DS\_LOW}} \quad (27)$$

$$L = \frac{\left(V_{IN\_MIN} + V_{OUT}\right) \times D}{\left(0.2 \text{ to } 0.4\right) \times I_{OUT\_MAX} \times f_{SW}} \quad (28)$$

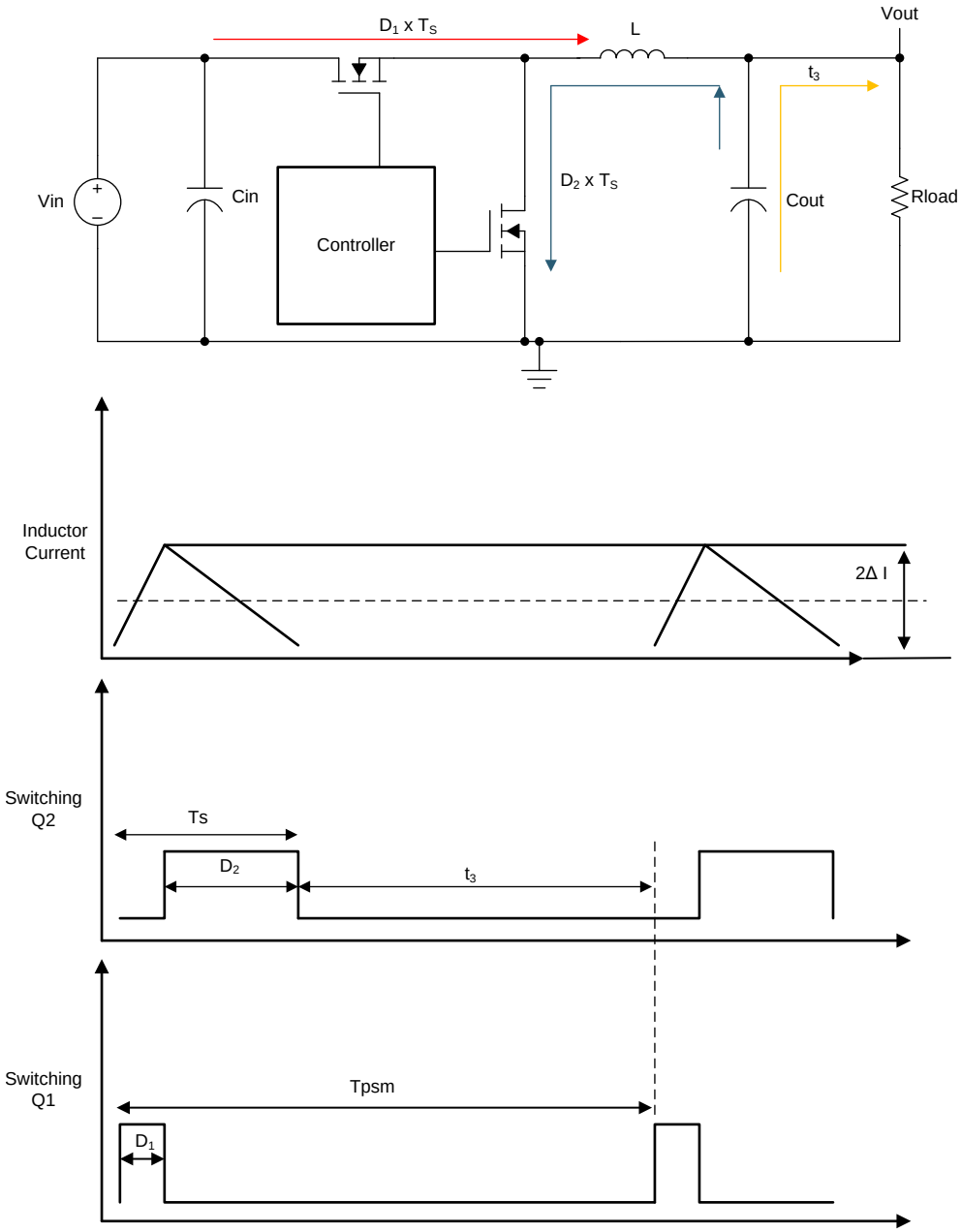
Where,

- V_{IN_MIN} is the minimum input voltage to power stage
- V_{OUT} is the desired output voltage
- V_{DS_LOW} and V_{DS_HIGH} are voltage drops across low and high side FETs, respectively

2.3.3.3 Inductor Ripple Current DCM Mode

In DCM mode, the inductor ripple is an AC triangular ripple waveform with zero crossing in each switching period as shown in 図 4.

図 4. DCM Mode Current and Switching Waveforms



There are three events in one switching cycle described as on time (D_1TS), off time (D_2TS), and dead time (t_3). Dead time is a function of output load current and output capacitor value. To operate in DCM mode, the duty cycle and power stage inductor can be calculated using 式 29 and 式 30 for minimum load resistor.

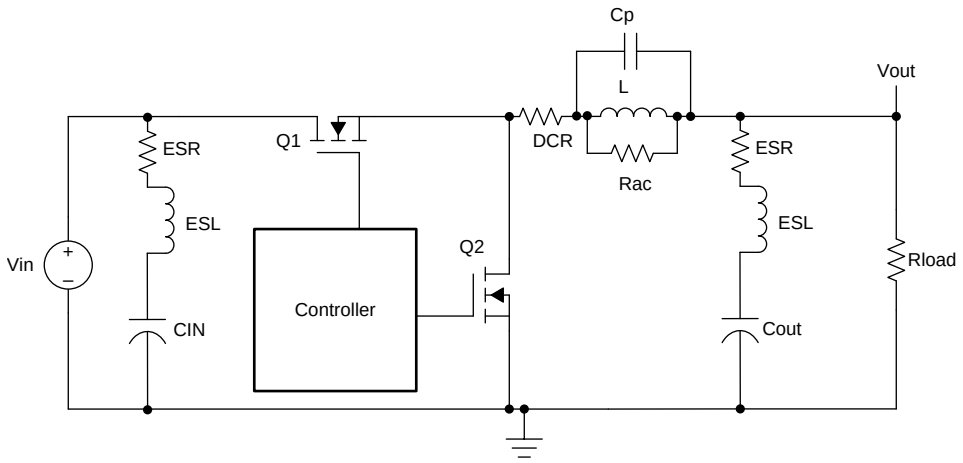
$$L < \frac{D' \times R_L}{2 \times f_{SW}} \tag{29}$$

$$D = \frac{1}{\sqrt{\frac{2 \times V_{IN\_MIN}}{V_{OUT}} \left(\frac{2 \times V_{IN\_MIN}}{V_{OUT}} \right)}} \times \sqrt{\frac{8 \times L \times f_{SW}}{R_L}} \tag{30}$$

2.3.3.4 Output Capacitor

The output capacitor with power inductor forms a second order low pass filer, attenuating switching output, and also acts as an energy storage for fast transient loads above close-loop bandwidth. At a higher switching frequency, there is also capacitance lead inductance, which is also known as ESL and ESR of the capacitor as shown in 図 5.

図 5. Output Capacitor Block



For expected output ripple voltage in CCM mode, output capacitor can be calculated using 式 31.

$$C_{OUT} = \frac{1}{8 \times f_{SW} \times \left(\left(\frac{\Delta V - \left(ESL \times \frac{V_{in} - V_{out}}{L} \right)}{di} \right) - ESR \right)} \tag{31}$$

注: Capacitor with low ESR and ESL reduce output ripple voltage. For ESL in the range of pico Hernias (pH), it factor can be ignored.

In DCM mode, the output ripple voltage is slightly higher than in CCM mode based on dead time and output current which can re-trigger the internal comparator of the DC-DC converter when ripple voltage is lower than the threshold. Capacitor current can be integrated to derive the output voltage ripple in DCM mode during turn on and take twice of its value to get peak-to-peak ripple voltage. Capacitor current during turn on pulse is calculated as follows:

$$I_c = \frac{\left(V_{IN} - V_{OUT}\right) \times t_{ON}}{L} - I_{OUT} \tag{32}$$

Solving integration during the turn on period for capacitor current and capacitor voltage can be expressed as shown in 式 33:

$$V_C = \int_0^{D \times Ts} \frac{\left(V_{IN\_MIN} - V_{OUT}\right) \times t_{ON}}{L} - I_{OUT\_MAX} = \frac{\left(D \times T_S \times \left(di - I_{OUT\_MAX}\right)^2\right)}{2 \times di} \tag{33}$$

Ripple voltage, when considering additional ESR voltage, can be expressed as shown in 式 34:

$$\Delta V = \frac{\left[\left(D \times T_S \times \left(di - I_{OUT\_MAX}\right)^2\right)\right]}{di} + 2 \times R_{ESR} \times \left(di - I_{OUT\_MAX}\right) \quad (34)$$

$$I_{COUT}\left(A\ rms\right) = \frac{1}{\sqrt{12}} \frac{V_{OUT}\left(V_{IN\_MAX} - V_{OUT}\right)}{L \times f_{SW} \times V_{IN\_MAX}} \quad (35)$$

2.3.3.5 Input Capacitor

Due to a switching event, ripple can be observed at the input side of the buck converter. Using a capacitor at the input side, the ripple voltage can be kept within expected limits. 式 36 can be used to calculate input capacitor using expected ripple voltage as the input parameter.

$$Cin = \frac{V_{OUT}}{f_{SW} \times V_{IN\_MIN} \times \left(\left(\frac{\Delta V_{IN}}{I_{OUT\_MAX}}\right) - ESR\right)} \quad (36)$$

$$I_{CIN}\left(A\ \ rms\right) = \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \left\{ {I_{OUT\_MAX}}^2 \left(1 - \frac{V_{OUT}}{V_{IN\_MIN}}\right) + \frac{1}{12} {\Delta I_L}^2 \right\}} \quad (37)$$

2.3.3.6 Power Stage Calculations

Using equations shown in 2.3.3, required power stage inductor, and capacitor for DC/DC rail is calculated as shown in 表 4.

表 4. Power Stage Calculation Parameters

PARAMETER/RAIL	UNIT	DC-DC 1.1-V	DC-DC 3.3-V	DC-DC 5-V	DC-DC 1.35-V	DC-DC 1.8-V
12-V TO POINT-OF-LOAD POWER TREE -- CONVERT 12-V FROM PD OUTPUT/ADAPTER INPUT DIRECTLY TO REQUIRED POWER RAILS						
Operating output current	mA	1000	900	400	650	160
Max output current(1)	A	2	2	1	1	1
Inductor	uH	4.7	15	4.7	10	2.2
Output capacitor	uF	47	47	47	47	47
Input capacitor	uF	10	10	10	10	10
Switching frequency at maximum output current	kHz	580	580	580	580	580
Switching frequency at operating output current	kHz	580	300	360	580	250
Feedback resistor R1	kOhms	4.42	33.2	56.2	7.68	13.3
Feedback resistor R2	kOhms	10	10	10	10	10
12-V TO 5-V TO POINT-OF-LOAD POWER TREE -- CONVERT 12-V FROM PD OUTPUT/ADAPTER INPUT TO 5-V AND THEN STEP DOWN 5-V TO REQUIRED POWER RAILS						
Operating output current	mA	1000	500	1.8	650	160
Maximum output current(1)	A	2	1	2	1	1
Inductor	uH	1	2.2	10	1	2.2
Output capacitor	uF	22	10	94	22	10
Input capacitor	uF	4.7	4.7	20	4.7	4.7
Switching frequency at maximum output current	kHz	1500	1500	500	1500	1500
Switching frequency at operating output current	kHz	1500	1400	500	1500	1400

表 4. Power Stage Calculation Parameters (continued)

PARAMETER/RAIL	UNIT	DC-DC 1.1-V	DC-DC 3.3-V	DC-DC 5-V	DC-DC 1.35-V	DC-DC 1.8-V
Feedback resistor R1	kOhms	100	442	100	124	196
Feedback resistor R2	kOhms	120	97.6	13.7	100	97.6

(1) All DC-DC stages are designed considering maximum output current rating of converter.

2.3.4 Buck LED Driver

The TIDA-01586 board has provisions of buck LED drivers to test IR LED illumination typically required in video imaging applications. For more information, see the IR LED illumination and ICR control reference design for IP network cameras with day/night vision.

2.3.5 LDO and Power Sequencing

In this design, image sensor analog voltage, audio codec analog voltage, and MPU I/O voltage are powered using LDO. TI's TLV742P LDO offers excellent high PSRR up to –45 dB at 1 MHz and very low noise output voltage noise to meet the critical specification of analog peripherals. The TLV742P device requires an input and output capacitor and at a minimum of external components with internal feedback and a compensation circuit.

The LM3880 three-rail simple power sequencer controls power up sequencing and power down sequencing of multiple independent voltage rails.

3 Getting Started With the Hardware

Before powering up the board, check for input and output connectors as shown in the following tables. See 表 5 and 表 6 for more information on connectors provided on the board.

表 5. 12-V to Point-of-Load DC-DC and LDOs Output Connectors

CONNECTOR NUMBER	DESCRIPTION
J1	12-V PD controller DC-DC output
J13	5-V DC-DC output
J15	3.3-V DC-DC output
J17	1.8-V DC-DC output
J9	1.1-V DC-DC output
J12	1.35-V DC-DC output
J8	Low current IR LED output
J34	1.8-V LDO output
J39	2.8-V LDO output
J40	3.3-V LDO output
J43	1.5-V LDO output

表 6. 12-V to 5-V to Point-of-Load DC-DC and LDOs Output Connectors

CONNECTOR NUMBER	DESCRIPTION
J25	5-V DC-DC output
J27	1.1-V DC-DC output
J29	1.35-V DC-DC output
J31	1.8-V DC-DC output
J24	3.3-V DC-DC output
J60	High current IR LED output
J36	1.8-V LDO output
J54	2.8-V LDO output
J55	3.3-V LDO output
J57	1.5-V LDO output

Required test points with designator are populated for measuring signals at each interface point of the design.

注: This design also has provision for disconnecting DC-DC stage or LDO from power path by depopulating jumpers.

表 7. Jumpers for Disconnecting DC-DC or LDO From Power Path

CONNECTOR NUMBER	DESCRIPTION
12-V TO POINT-OF-LOAD POWER TREE	
J7	Disconnect low current IR LED DC-DC
J11	Disconnect 5-V DC-DC
J14	Disconnect 3.3-V DC-DC
J16	Disconnect 1.8-V DC-DC
J10	Disconnect 1.35-V DC-DC
J4	Disconnect 1.1-V DC-DC
J32	Disconnect 1.8-V LDO
J35	Disconnect 2.8-V LDO

表 7. Jumpers for Disconnecting DC-DC or LDO From Power Path (continued)

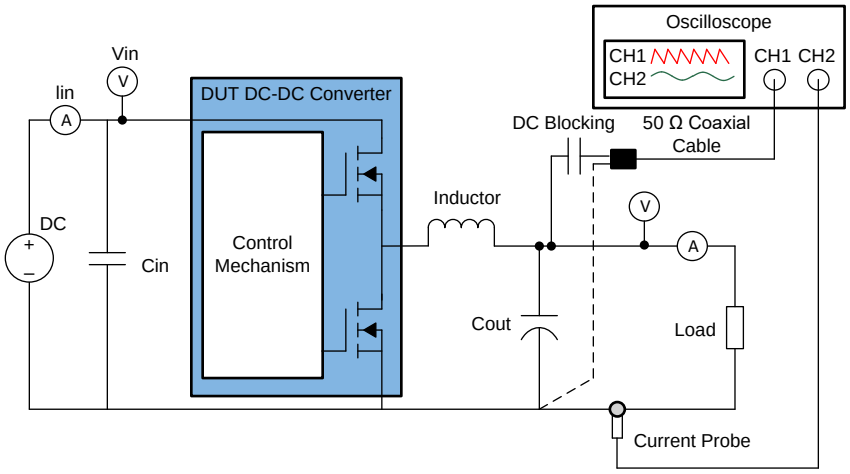
CONNECTOR NUMBER	DESCRIPTION
12-V TO POINT-OF-LOAD POWER TREE	
J37	Disconnect 3.3-V LDO
J41	Disconnect 1.5-V LDO
12-V TO 5-V TO POINT-OF-LOAD POWER TREE	
J23	Disconnect 5-V DC-DC
J22	Disconnect 3.3-V DC-DC
J30	Disconnect 1.8-V DC-DC
J28	Disconnect 1.35-V DC-DC
J26	Disconnect 1.1-V DC-DC
J59	Disconnect high current IR LED DC-DC
J33	Disconnect 1.8-V LDO
J42	Disconnect 2.8-V LDO
J38	Disconnect 3.3-V LDO
J56	Disconnect 1.5-V LDO

3.1 Testing and Results

3.1.1 Test Setup

The test setup consists of the TIDA-010034 board, DC Supply, digital multimeter, electronic load, and current probe as shown in 図 6.

図 6. Test Setup



The tests to be conducted for this design are:

- Device efficiency and system efficiency at various loads
- Ripple voltage, ripple frequency at full- and light-load conditions, output voltage accuracy
- Load transient response

To test conditions mentioned previously, the 6½ DMM is set with the following settings to average the source and instrument error.

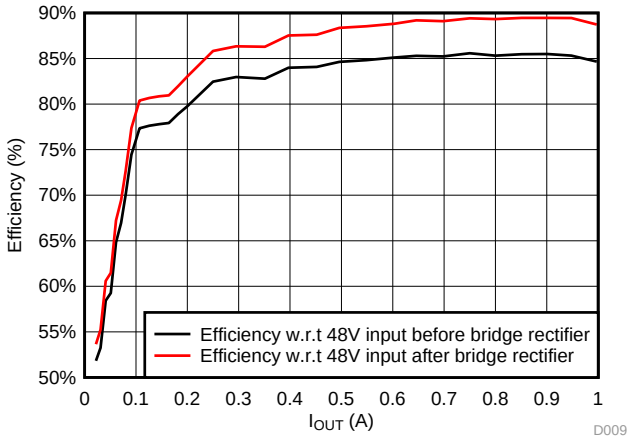
- Slow filter – 7 seconds / reading
- No samples – 50 (approximately 6 minutes)

3.1.2 Test Results

This section comprises of test data for efficiency over full scale load variation, output voltage regulation, output ripple, and transient load response waveforms, as well as thermal performance of both power tree implementations.

3.1.2.1 Efficiency Over Load Variation

図 7. Efficiency Over Load Variation for TPS23755-Based Powered Device (PD) With 12-V Output Voltage



3.1.2.1.1 Efficiency Curves for 12-V to Point-of-Load Power Tree

図 8. Efficiency Over Load Variation for TPS561201 With 5-V Output Voltage

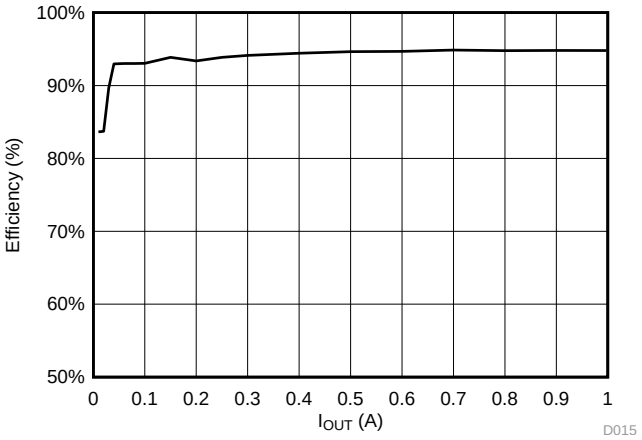


図 9. Efficiency Over Load Variation for TPS562201 With 3.3-V Output Voltage

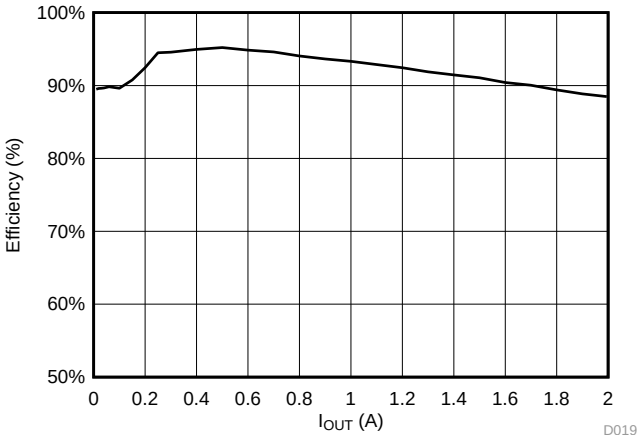


図 10. Efficiency over Load Variation for TPS561201 With 1.8-V Output Voltage

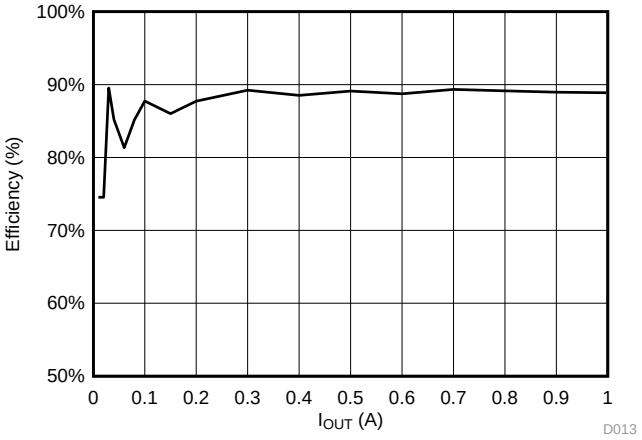


図 11. Efficiency Over Load Variation for TPS561208 With 1.35-V Output Voltage

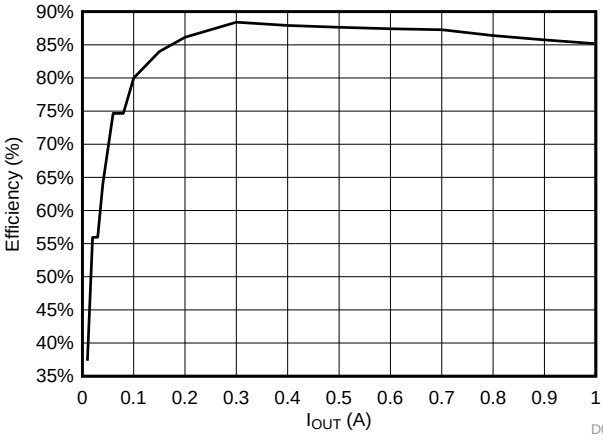
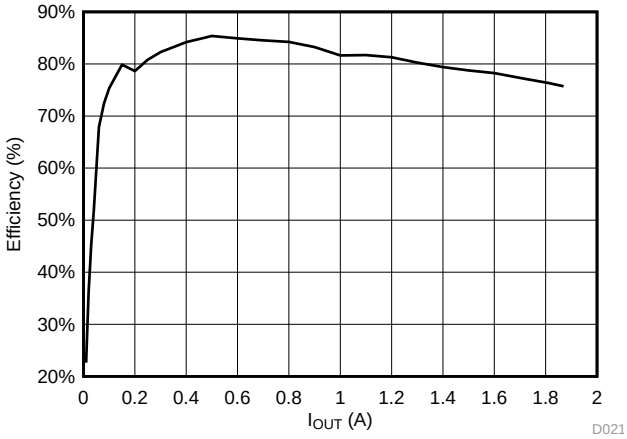


図 12. Efficiency Over Load Variation for TPS562208 With 1.1-V Output Voltage



3.1.2.1.2 Efficiency Curves for 12-V to 5-V to Point-of-Load Power Tree

図 13. Efficiency Over Load Variation for TPS54202H With 5-V Output Voltage

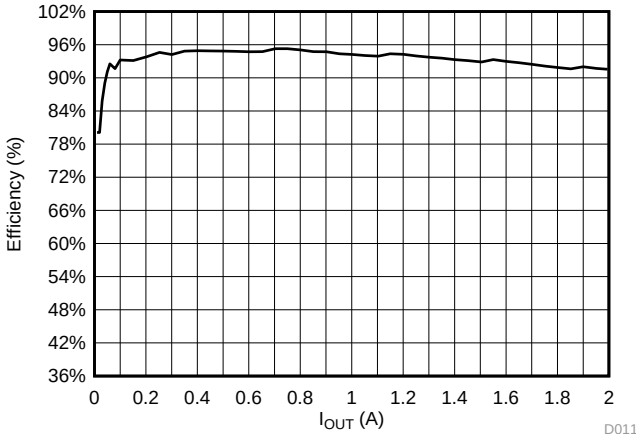


図 14. Efficiency Over Load Variation for TLV62568 With 3.3-V Output Voltage

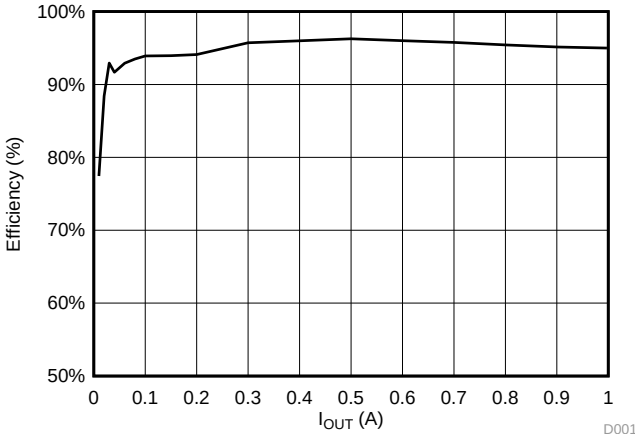


図 15. Efficiency Over Load Variation for TLV62568 With 1.8-V Output Voltage

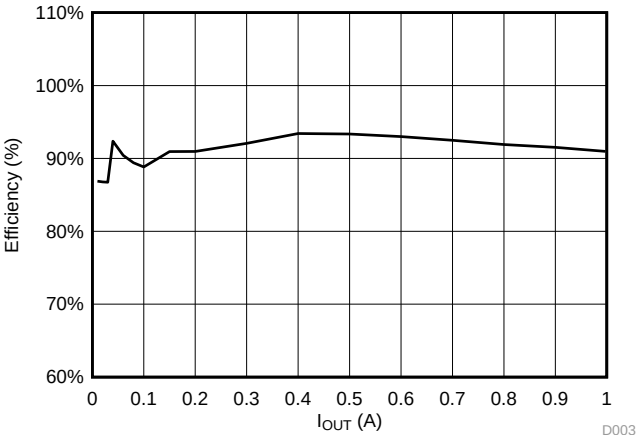


図 16. Efficiency Over Load Variation for TLV62568A With 1.35-V Output Voltage

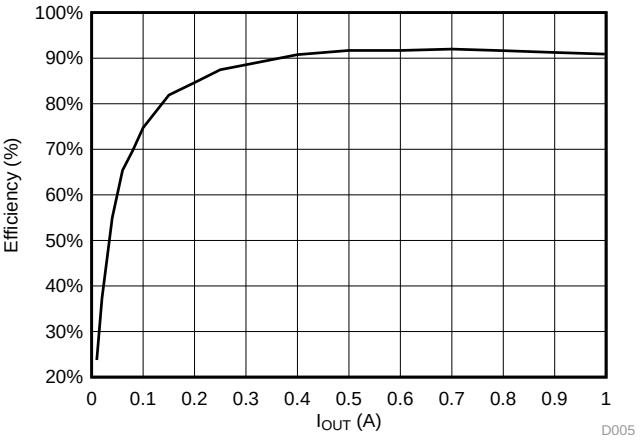
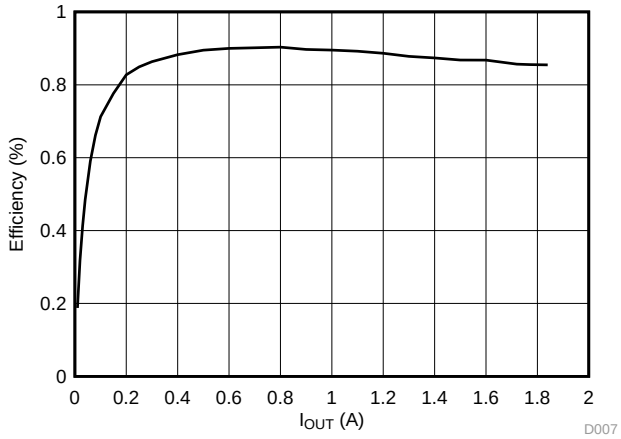
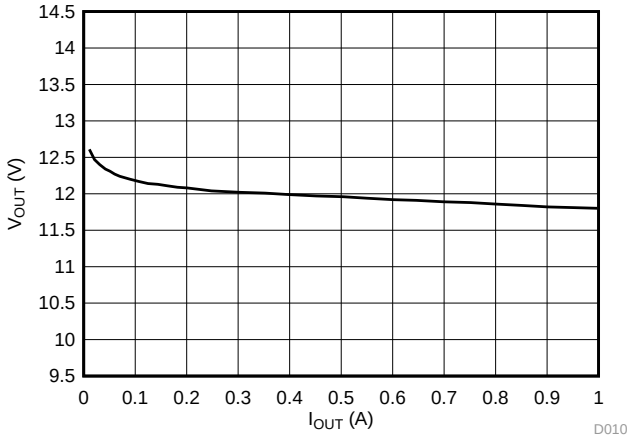


図 17. Efficiency Over Load Variation for TLV62569A With 1.1-V Output Voltage



3.1.2.2 Voltage Accuracy

図 18. Voltage Regulation for TPS23755-Based Powered Device (PD) With 12-V Nominal Output Voltage



3.1.2.2.1 Voltage Regulation Curves for 12-V to Point-of-Load Power Tree

図 19. Voltage Regulation for TPS561201 With 5-V Nominal Output Voltage

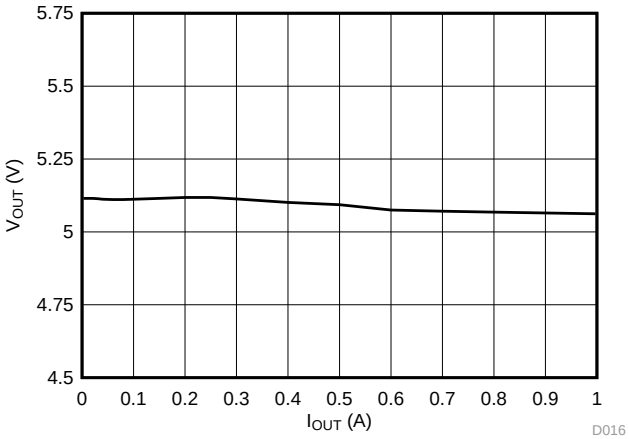


図 20. Voltage Regulation for TPS562201 With 3.3-V Nominal Output Voltage

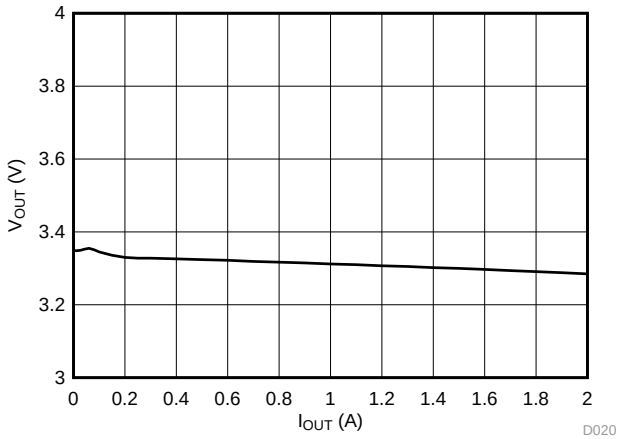


図 21. Voltage Regulation for TPS561201 With 1.8-V Nominal Output Voltage

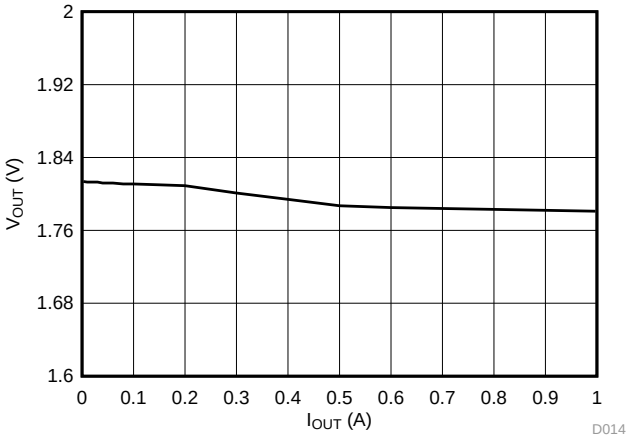


図 22. Voltage Regulation for TPS561208 With 1.35-V Nominal Output Voltage

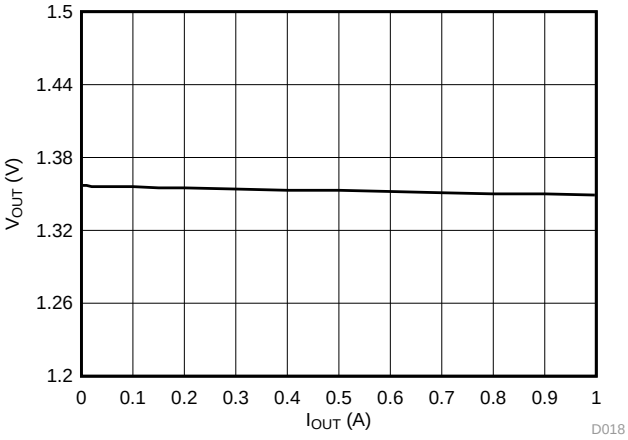
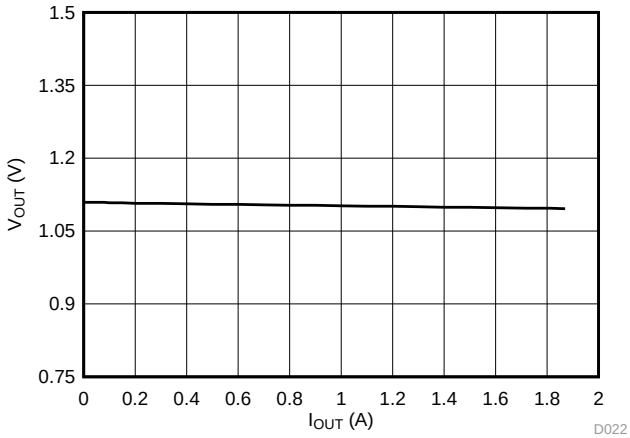


図 23. Voltage Regulation for TPS562208 With 1.1-V Nominal Output Voltage



3.1.2.2.2 Voltage Regulation Curves for 12-V to 5-V to Point-of-Load Power Tree

図 24. Voltage Regulation for TPS54202H With 5-V Nominal Output Voltage

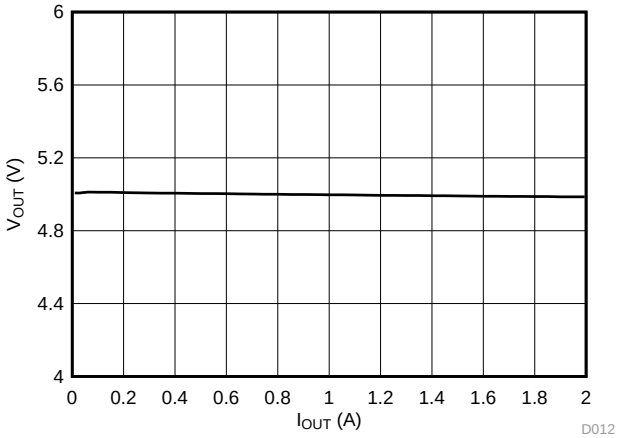


図 25. Voltage Regulation for TLV62568 With 3.3-V Nominal Output Voltage

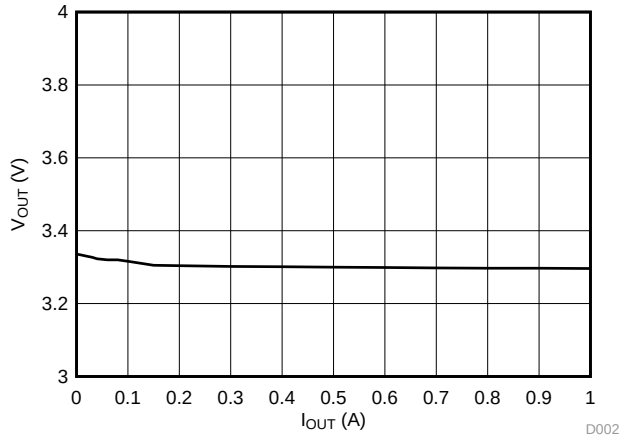


図 26. Voltage Regulation for TLV62568 With 1.8-V Nominal Output Voltage

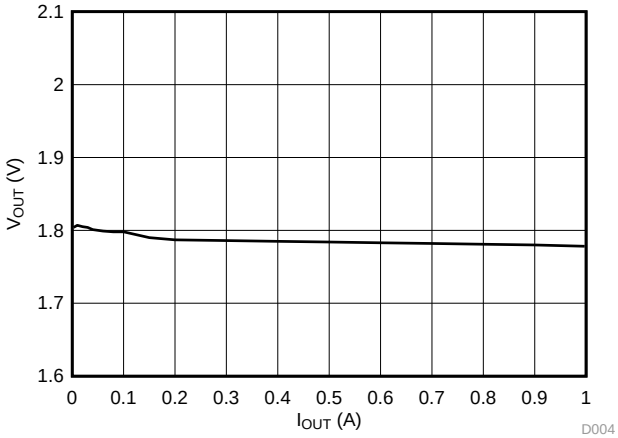


図 27. Voltage Regulation for TLV62568A With 1.35-V Nominal Output Voltage

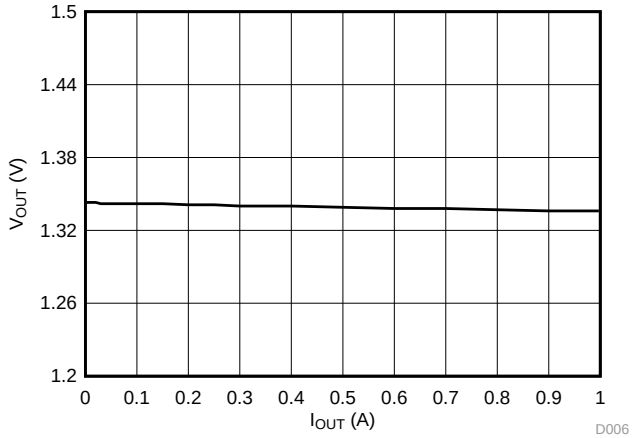
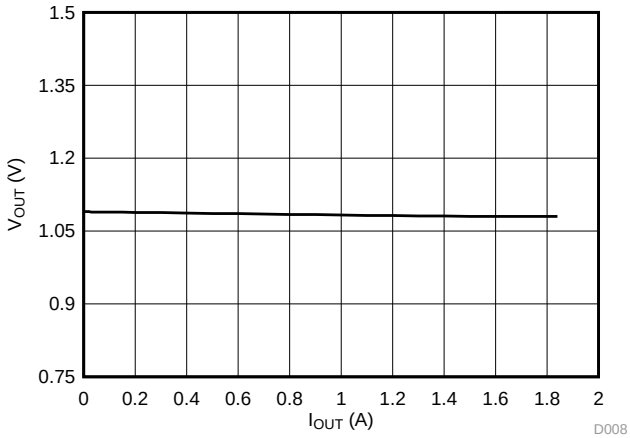


図 28. Voltage Regulation for TLV62569A With 1.1-V Nominal Output Voltage



3.1.2.3 Output Ripple Waveforms

In 1x AC probe, as shown in 図 6, the output ripple has been captured for all DC-DC rails to validate very low ripple output and harmonic-free spectrum to achieve higher ENOB with respect to power supply spur and noise floor.

図 29. Output Ripple of TPS23755-Based Powered Device (PD) With 12-V Output Voltage at 100-mA Load

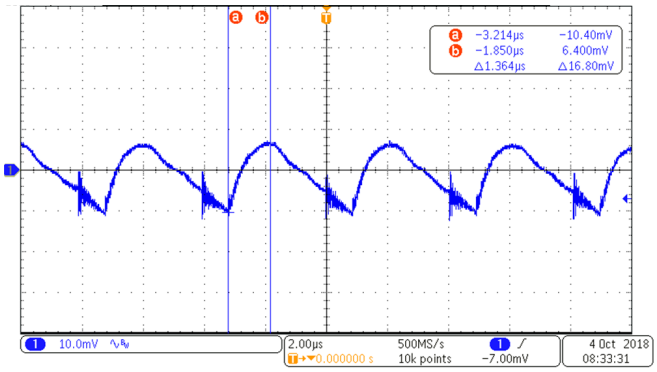
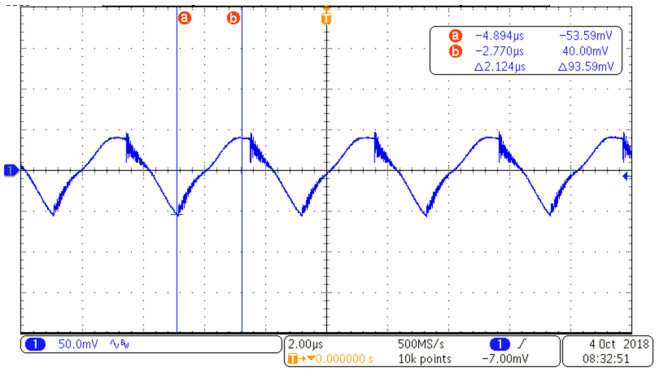


図 30. Output Ripple of TPS23755-Based Powered Device (PD) With 12-V Output Voltage at 1-A Load



3.1.2.3.1 12-V to Point-of-Load Power Tree Output Ripple Waveforms

図 31. Output Ripple of TPS561201 With 5-V Output Voltage at No Load

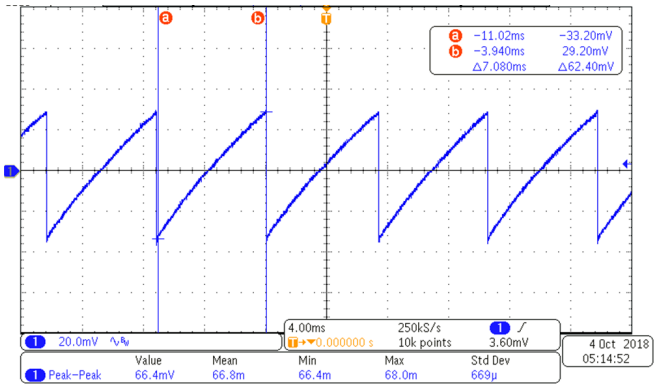


図 32. Output Ripple of TPS561201 With 5-V Output Voltage at 1-A Load

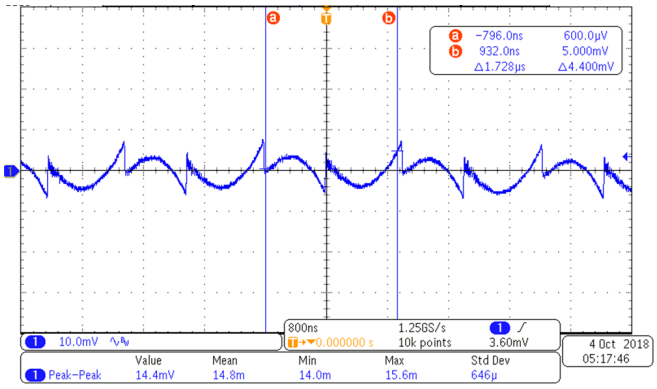


図 33. Output Ripple of TPS562201 With 3.3-V Output Voltage at No Load

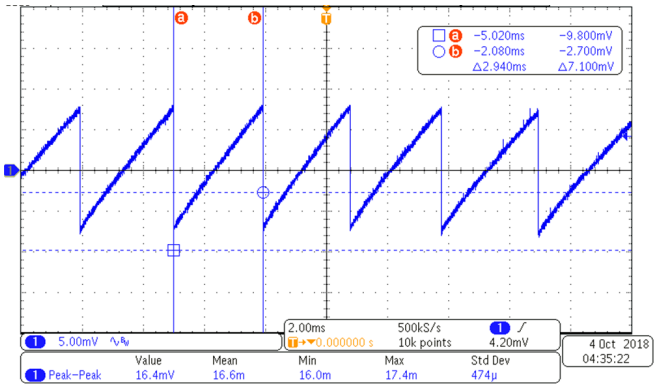


図 34. Output Ripple of TPS562201 With 3.3-V Output Voltage at 2-A Load

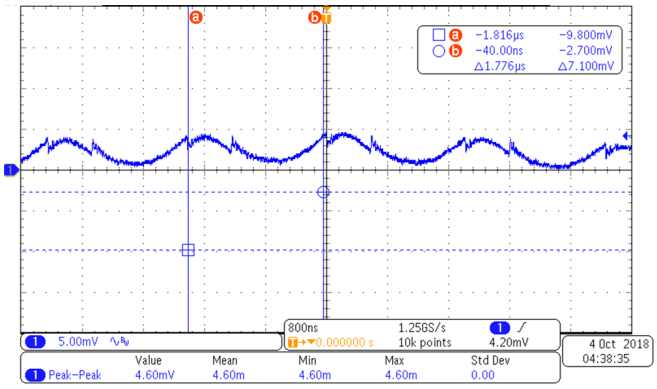


図 35. Output Ripple of TPS561201 With 1.8-V Output Voltage at No Load

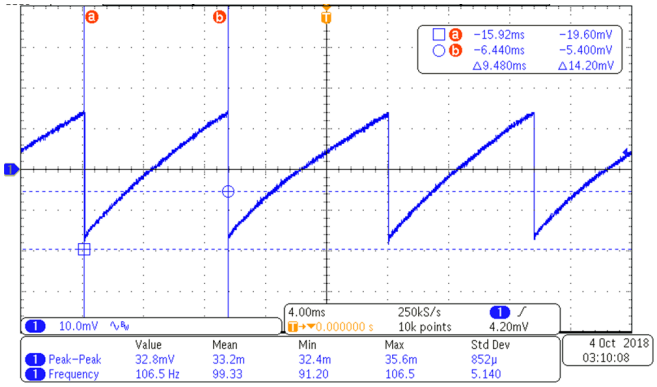


図 36. Output Ripple of TPS561201 With 1.8-V Output Voltage at 1-A Load

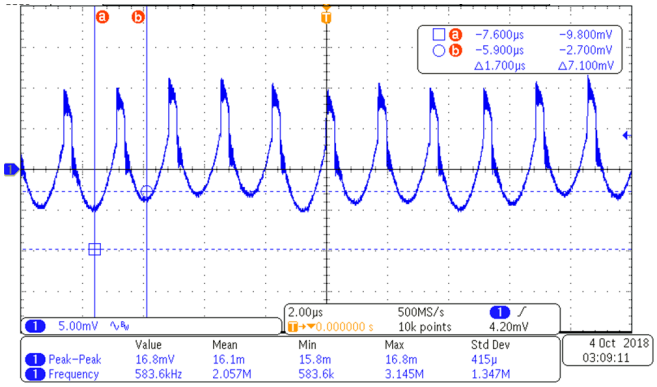


図 37. Output Ripple of TPS561208 With 1.35-V Output Voltage at No Load

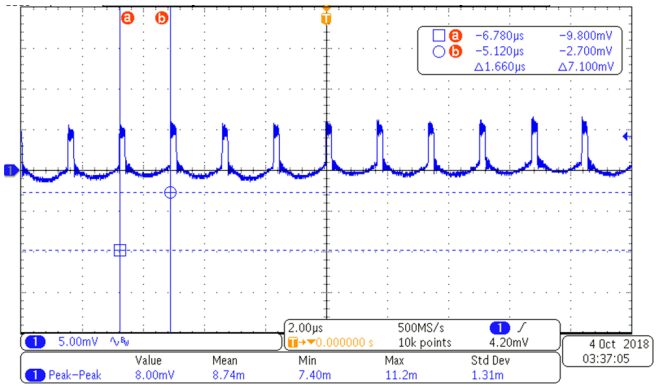


図 38. Output Ripple of TPS561208 With 1.35-V Output Voltage at No Load With FFT

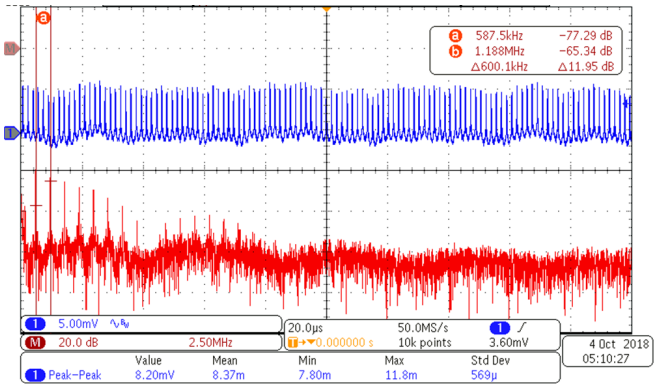


図 39. Output Ripple of TPS561208 With 1.35-V Output Voltage at 1-A Load

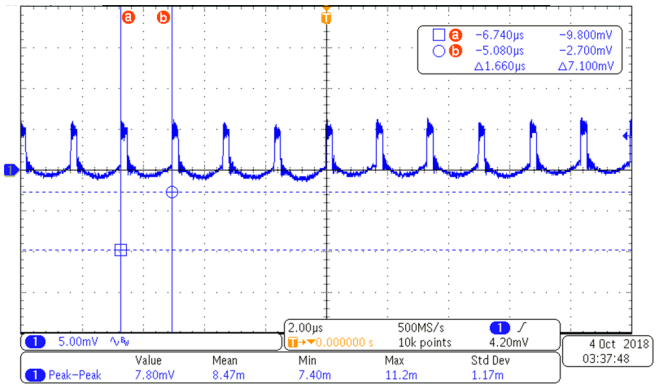


図 40. Output Ripple of TPS561208 With 1.35-V Output Voltage at 1-A Load With FFT

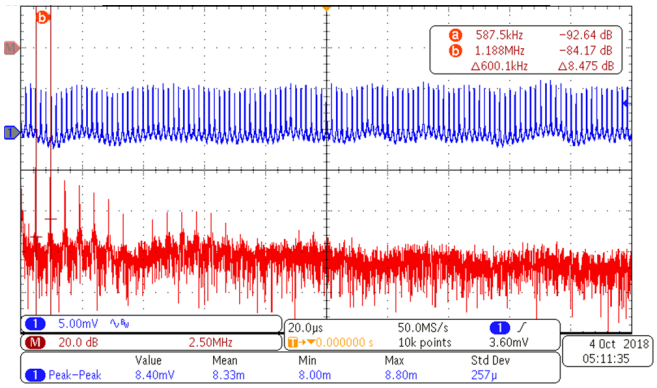


図 41. Output Ripple of TPS562208 With 1.1-V Output Voltage at No Load

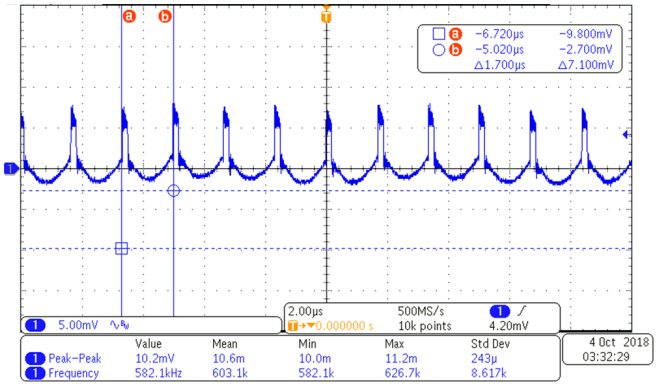


図 42. Output Ripple of TPS562208 With 1.1-V Output Voltage at No Load With FFT

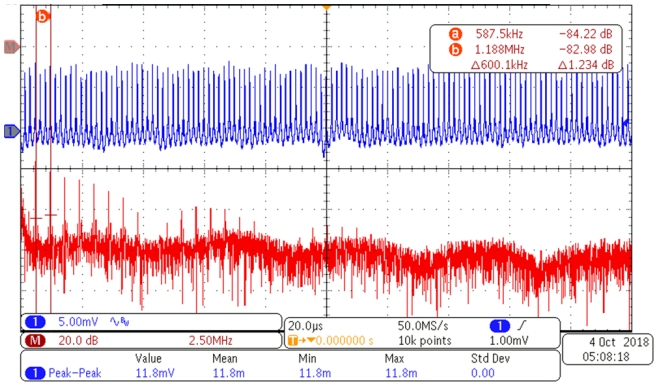


図 43. Output Ripple of TPS562208 With 1.1-V Output Voltage at 2-A Load

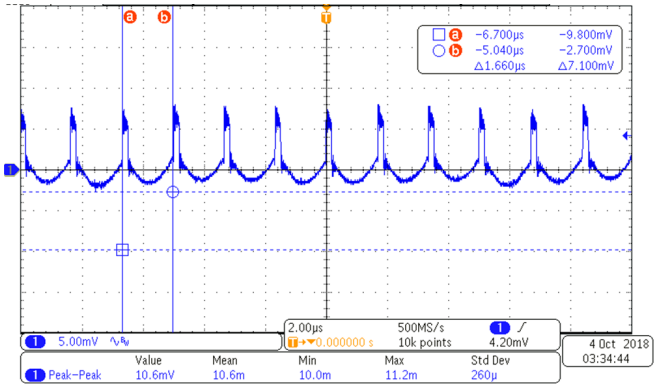
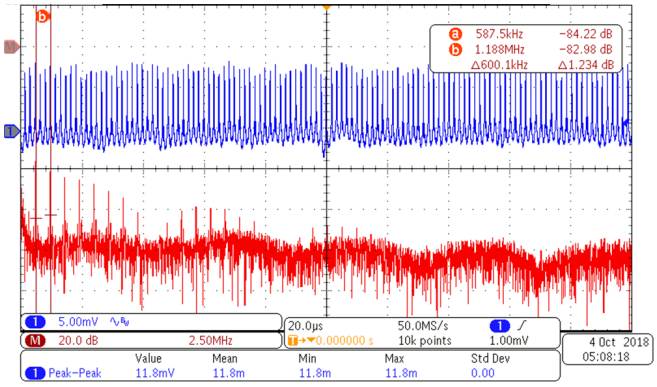


図 44. Output Ripple of TPS562208 With 1.1-V Output Voltage at 2-A Load With FFT



3.1.2.3.2 12-V to 5-V to Point-of-Load Power Tree Output Ripple Waveforms

図 45. Output Ripple of TPS54202H With 5-V Output Voltage at No Load

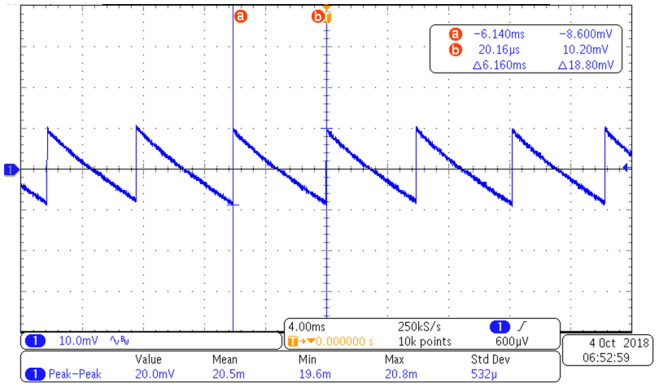


図 46. Output Ripple of TPS54202H With 5-V Output Voltage at 2-A Load

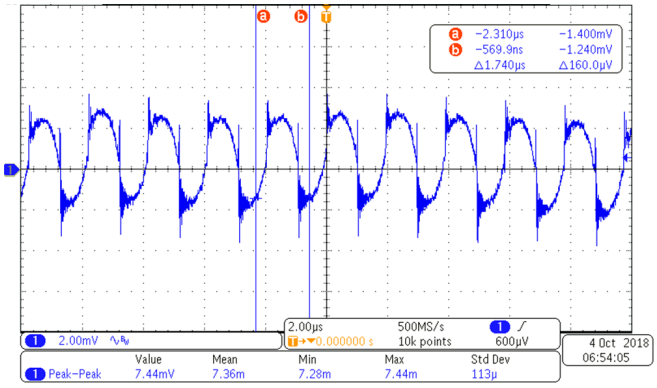


図 47. Output Ripple of TLV62568 With 3.3-V Output Voltage at No Load

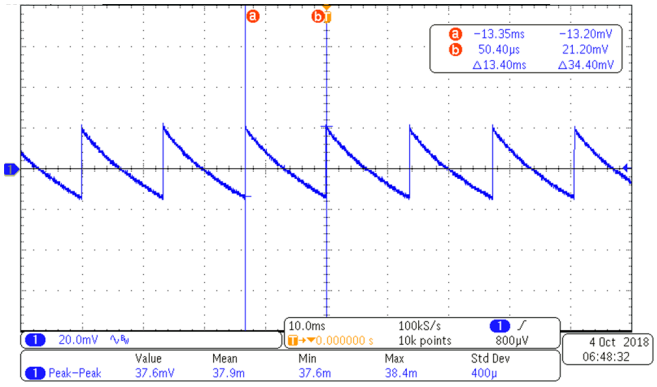


図 48. Output Ripple of TLV62568 With 3.3-V Output Voltage at 1-A Load

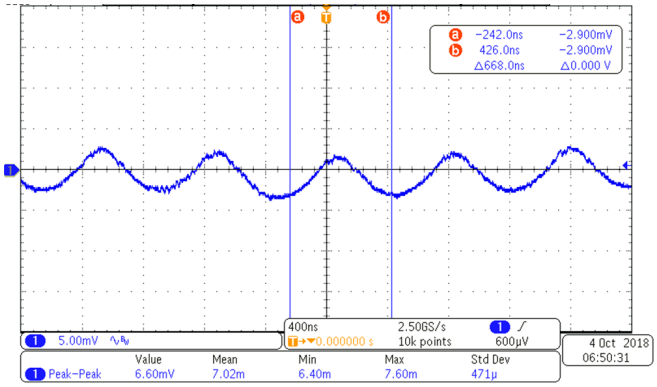


図 49. Output Ripple of TLV62568 With 1.8-V Output Voltage at No Load

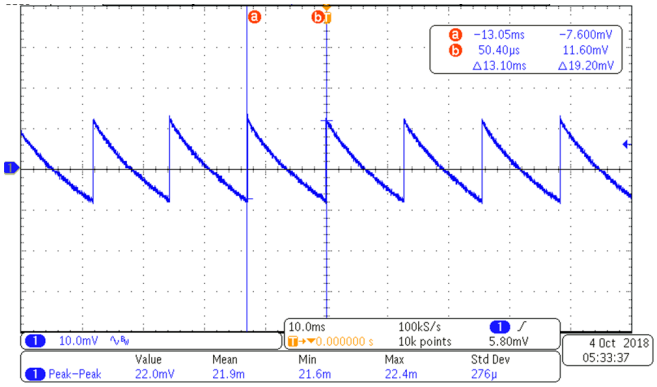


図 50. Output Ripple of TLV62568 With 1.8-V Output Voltage at 1-A Load

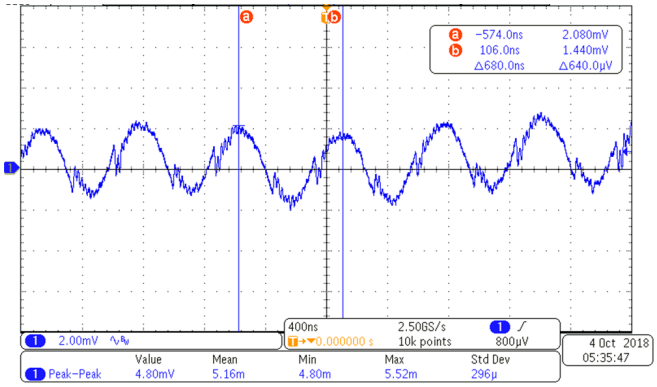


図 51. Output Ripple of TLV62568A With 1.35-V Output Voltage at No Load

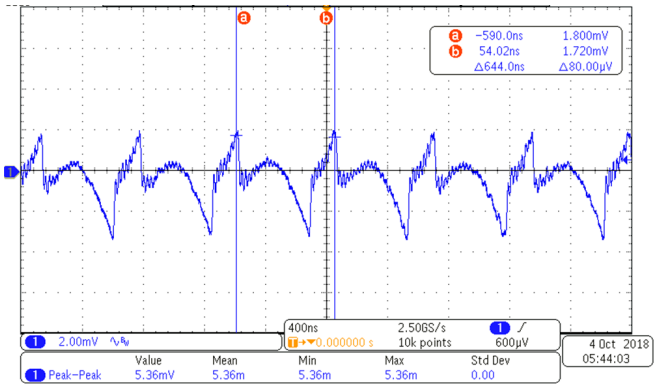


図 52. Output Ripple of TLV62568A With 1.35-V Output Voltage at No Load With FFT

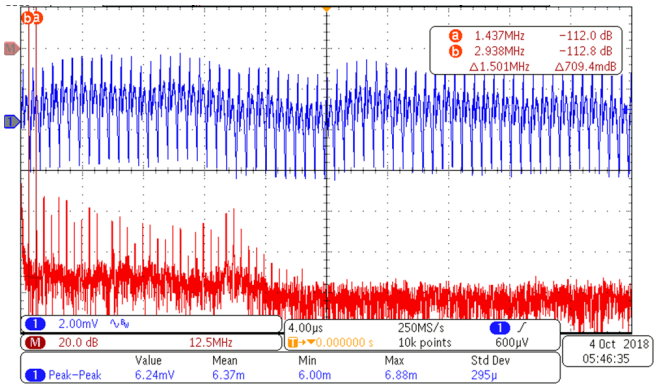


図 53. Output Ripple of TLV62568A With 1.35-V Output Voltage at 1-A Load

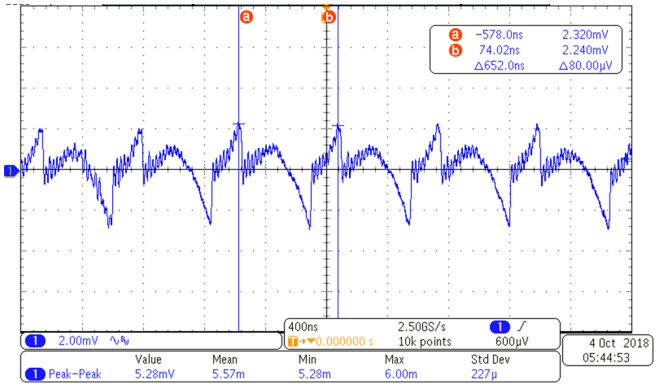


図 54. Output Ripple of TLV62568A With 1.35-V Output Voltage at 1-A Load With FFT

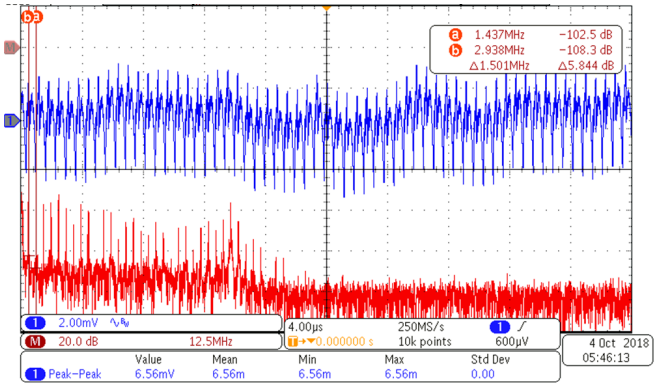


図 55. Output Ripple of TLV62569A With 1.1-V Output Voltage at No Load With FFT

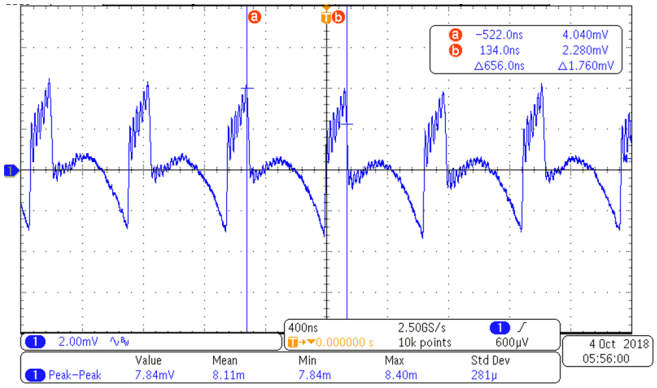


図 56. Output Ripple of TLV62569A With 1.1-V Output Voltage at No Load With FFT

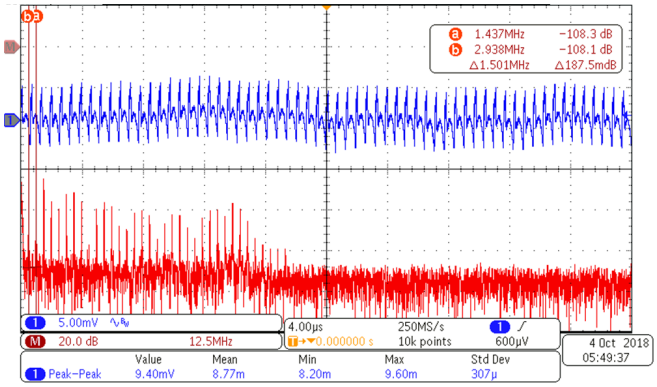


図 57. Output Ripple of TLV62569A With 1.1-V Output Voltage at 2-A Load

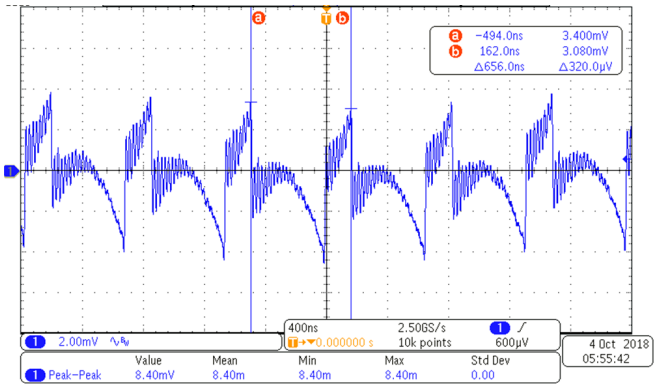
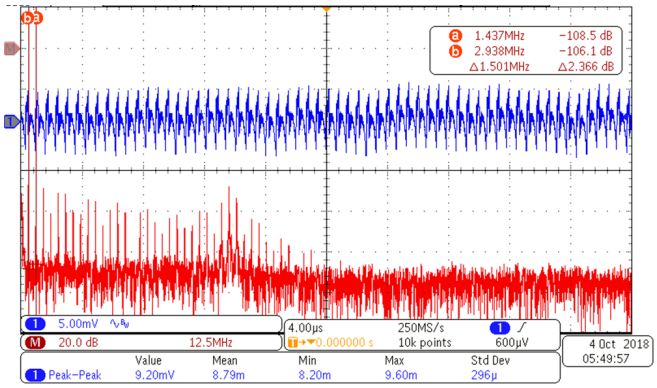


図 58. Output Ripple of TLV62569A With 1.1-V Output Voltage at 2-A Load With FFT



注: Output ripple has been captured for all DC-DC rails using 1x AC probe as shown in 3.1.1.

3.1.2.4 Transient Load Response

Each DC-DC rail has been tested for transient load condition ranging from 10 mA to 1 A/2 A using DC electronic load with 10-kHz switching frequency, 50% duty cycle, and 250 mA/µs slew rate to capture overshoot, undershoot in output voltage, and validate fast transient response.

図 59. Transient Response of TPS23755-Based Powered Device (PD) With 12-V Nominal Output Voltage

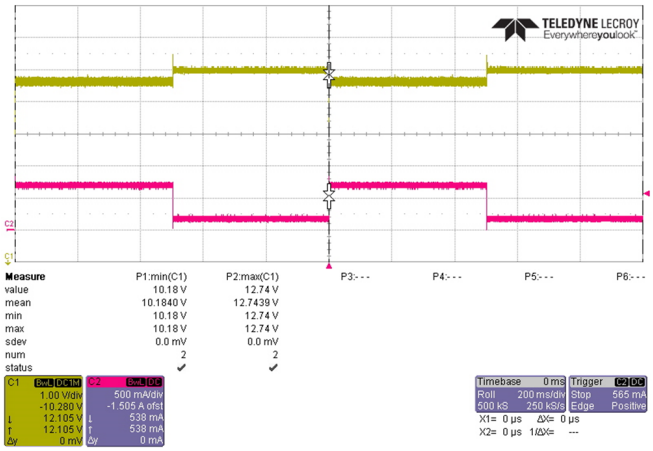


図 60. Undershoot on 12-V Nominal Output Voltage Rail of TPS23755-Based Powered Device (PD)

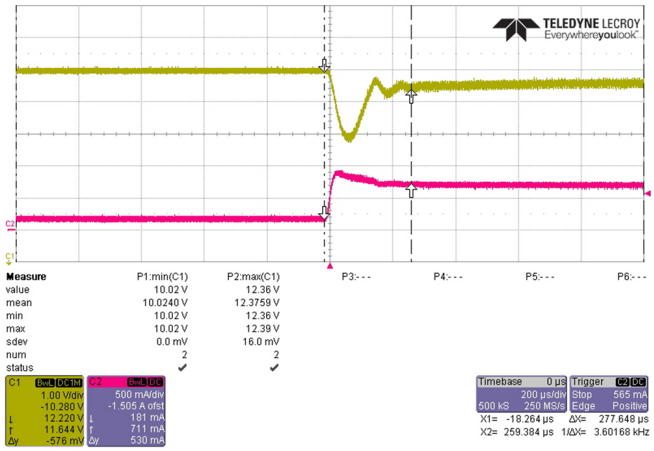


図 61. Undershoot on 12-V Nominal Output Voltage Rail When Main Power Switches From PoE to 12-V Adapter

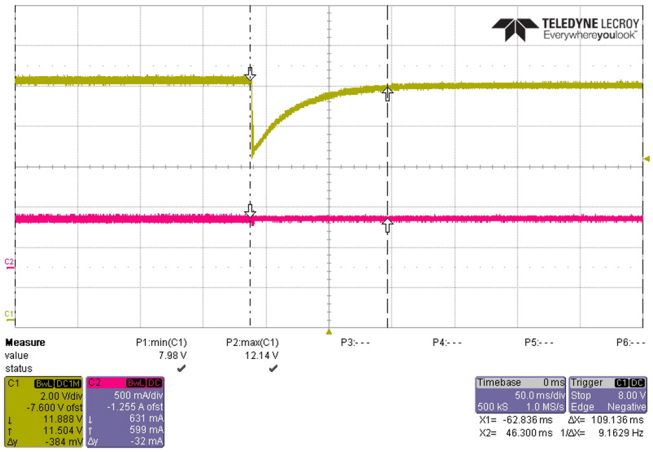
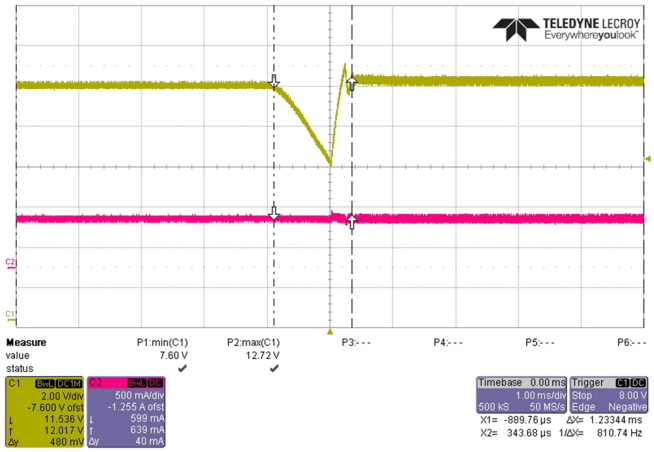


図 62. Undershoot on 12-V Nominal Output Voltage Rail When Main Power Switches From 12-V Adapter to PoE



3.1.2.4.1 12-V to Point-of-Load Power Tree Transient Waveforms

図 63. Transient Response of TPS561201 With 5-V Nominal Output Voltage

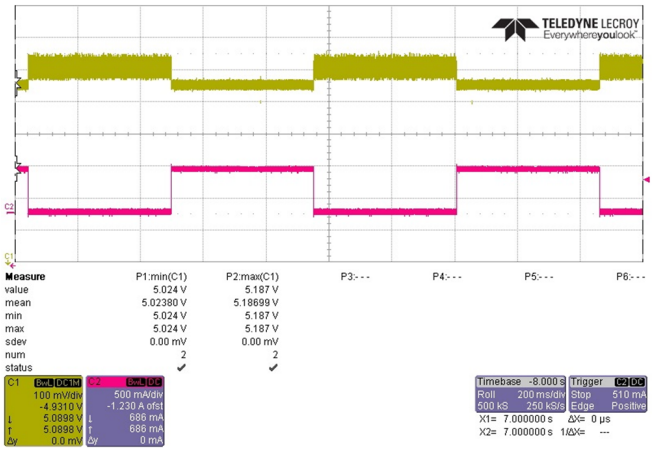


図 64. Transient Response of TPS562201 With 3.3-V Nominal Output Voltage

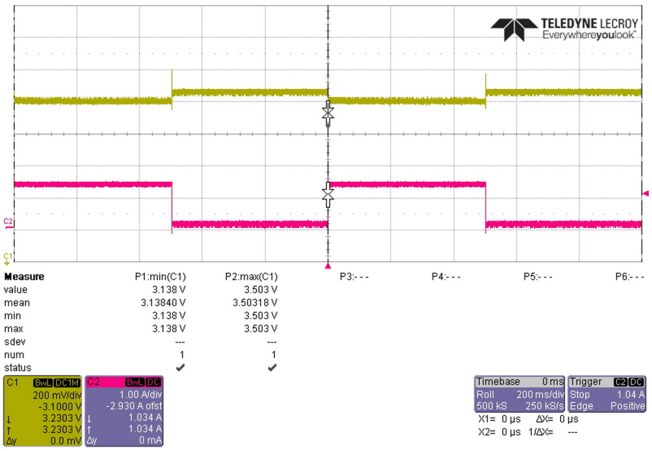


図 65. Transient Response of TPS561201 With 1.8-V Nominal Output Voltage

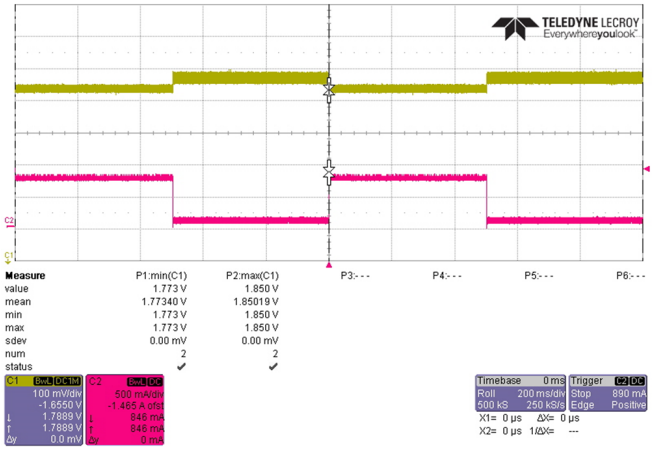


図 66. Transient Response of TPS561208 With 1.35-V Nominal Output Voltage

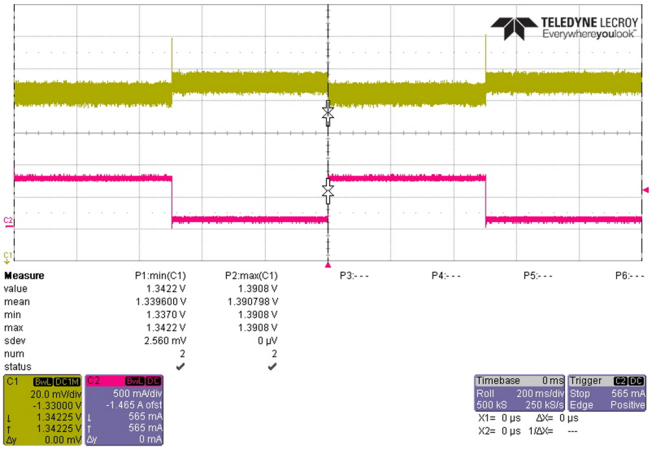
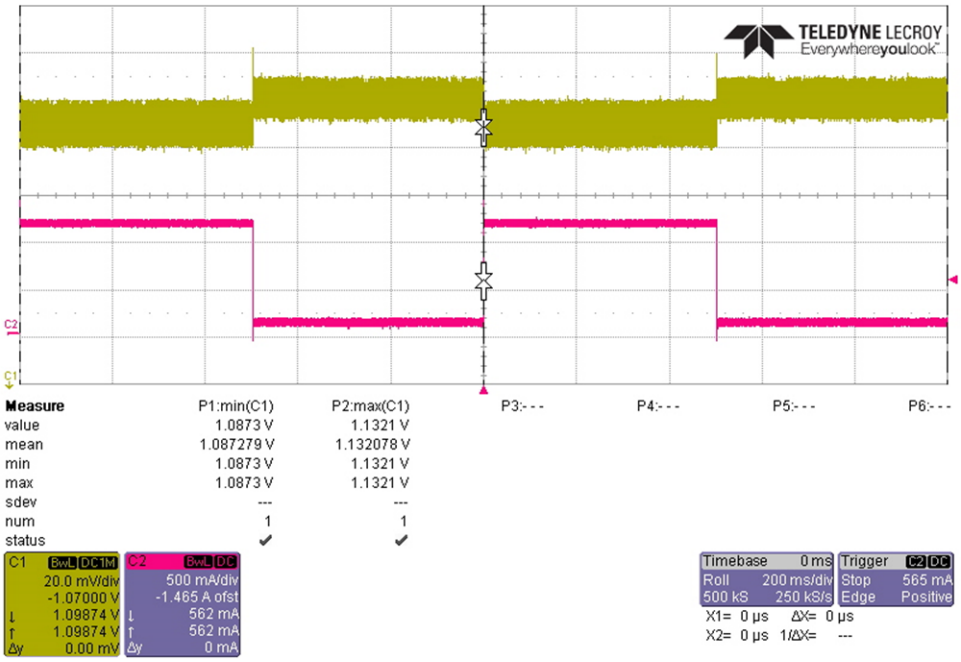


図 67. Transient Response of TPS562208 With 1.1-V Nominal Output Voltage



3.1.2.4.2 12-V to 5-V to Point-of-Load Power Tree Transient Waveforms

図 68. Transient Response of TPS54202H With 5-V Nominal Output Voltage

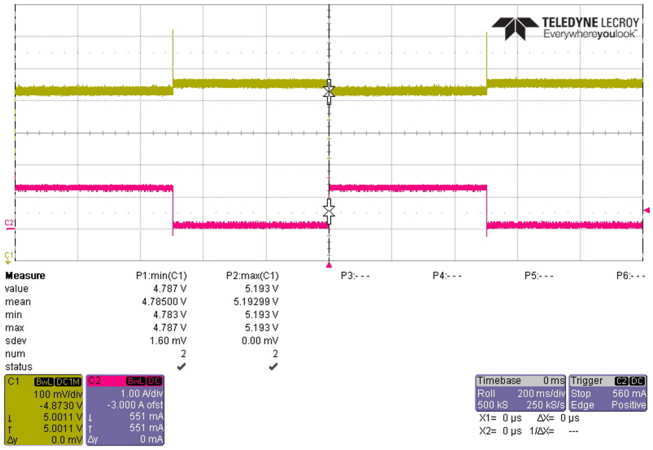


図 69. Transient Response of TLV62568 With 3.3-V Nominal Output Voltage

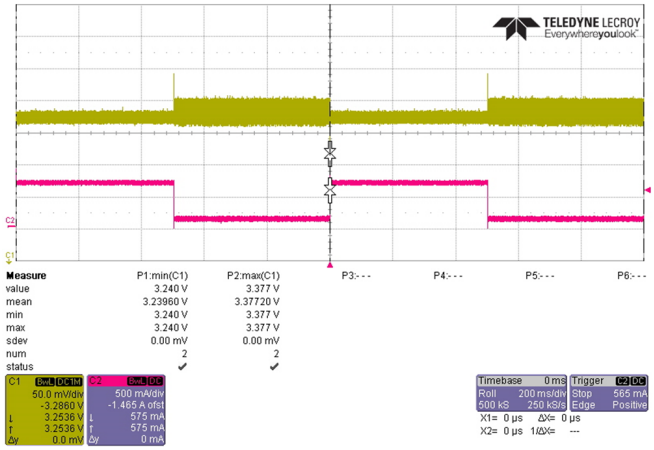


図 70. Transient Response of TLV62568 With 1.8-V Nominal Output Voltage

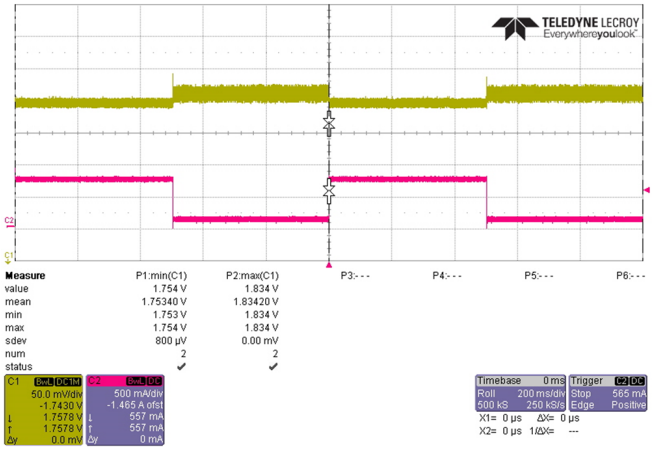


図 71. Transient Response of TLV62568A With 1.35-V Nominal Output Voltage

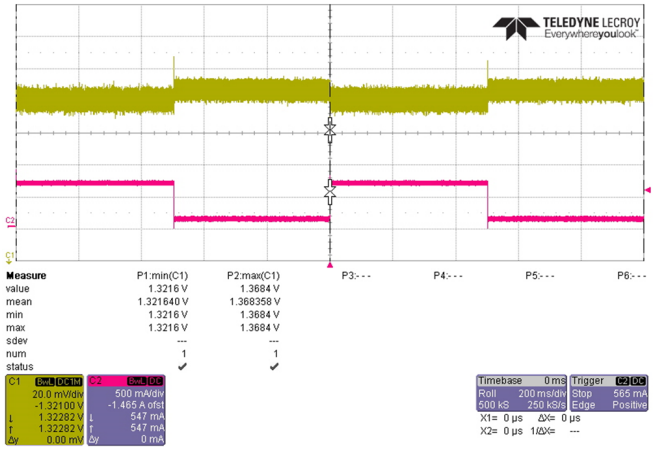
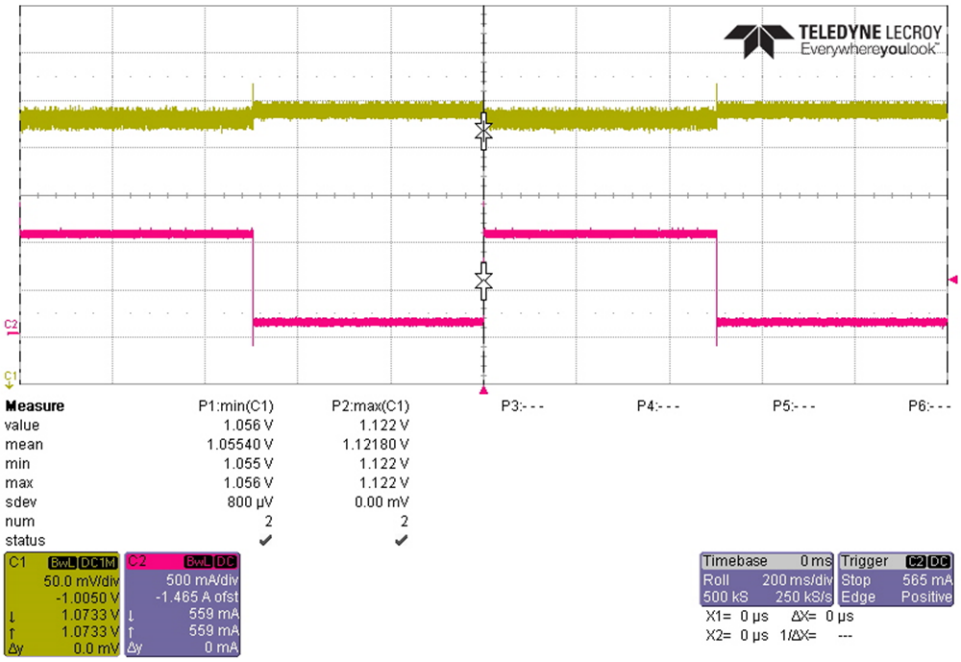


図 72. Transient Response of TLV62569A With 1.1-V Nominal Output Voltage



3.1.2.5 Thermal

This design has been targeted to achieve very low thermal dissipation in small form factor. 図 73 and 図 74 show thermal performance of both power tree implementations.

図 73. Thermal Image of Main Power Derived From PoE and Delivered to Point-of-Load Using 12-V as Intermediate Rail

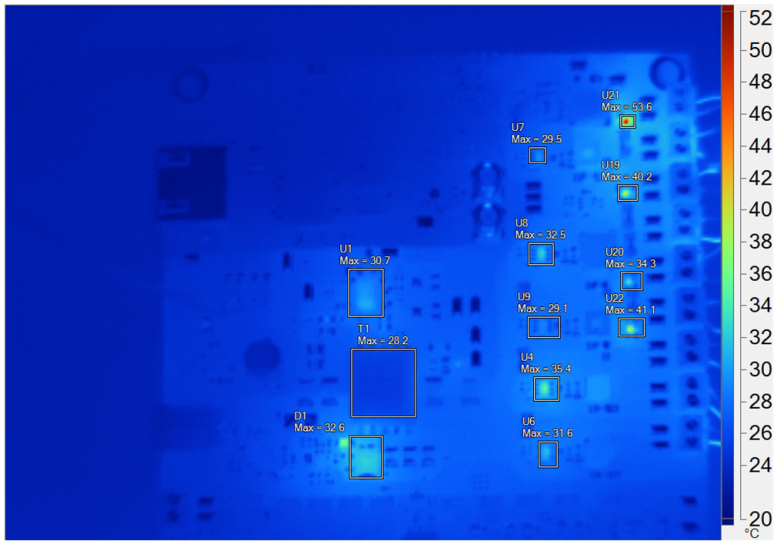
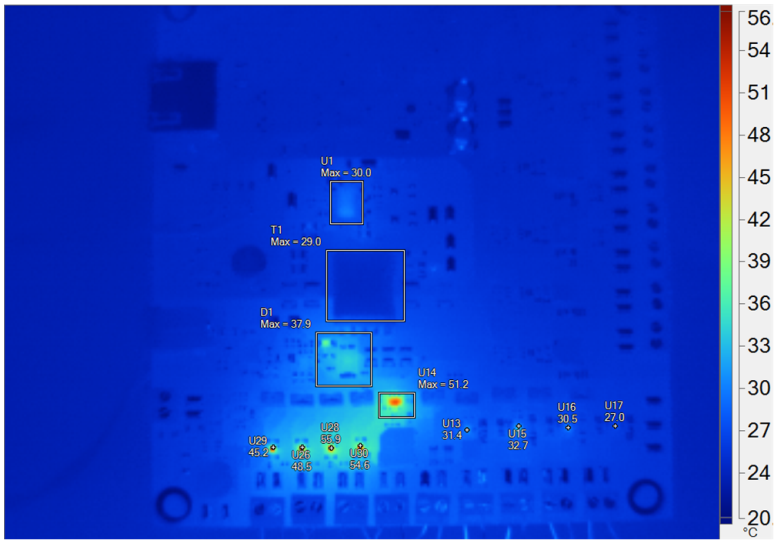


図 74. Thermal Image of Main Power Derived From PoE and Delivered to Point-of-Load Using 12-V and 5-V as Intermediate Rail



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010034.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010034.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010034.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010034.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010034.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010034.

5 Software Files

To download the software files, see the design files at TIDA-010034.

6 Related Documentation

1. Texas Instruments, *Advanced adapter ORing solutions using the TPS23753 application report*

6.1 商標

6.2 デベロッパー・ネットワークの製品に関する免責事項

7 About the Author

SURYA MISHRA is a systems engineer at Texas Instruments where he is responsible for designing sub-system solution, developing TI Designs and other collaterals for Building Security & Video Surveillance market. Surya earned his bachelor of electronics and communication engineering from the Motilal Nehru National Institute of Technology (MNNIT), Allahabad.

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