参考資料

デザイン・ガイド: TIDA-050020
PMBus™ 電圧レギュレータのリファレンス・デザイン、Xilinx® Ultrascale+™ FPGA 向け

概要

このリファレンス・デザインは、TPS53681 マルチフェーズ・コントローラと CSD95490Q5MC スマート電力段を使用し、Xilinx™ Viretex Ultrascale+ FPGA の 0.85V、200A、VCCINT レールに給電するための高性能設計を実装します。コントローラの 2 次側出力を使用して、FPGA の補助レールに給電します。スマート電力段と、内蔵の PMBus™ により、出力電圧の設定と主要なデザイン・パラメータの遠隔測定を簡単に行えます。このデザインにより、構成、VID 調整、および電源補償の調整が可能になるとともに、入力と出力の電圧、電流、電力、温度を監視できます。TI の Fusion Digital Power™ Designer を使用して、システムのプログラミング、監視、検証、特性設定を行います。

リソース

TIDA-050020	デザイン・フォルダ
TPS53681	プロダクト・フォルダ
CSD95490Q5MC	プロダクト・フォルダ
Fusion Digital Power Designer	ツール・フォルダ
TPS53681EVM-002	ツール・フォルダ

TI E2E™ Community

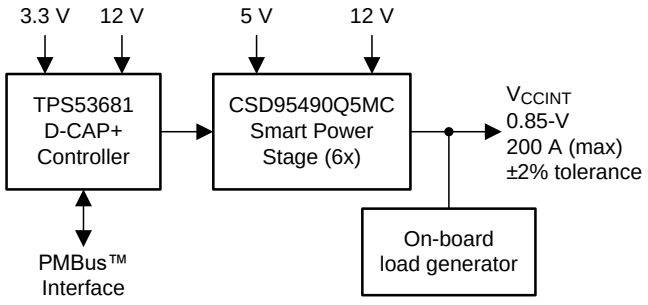
E2E™エキスパートに質問

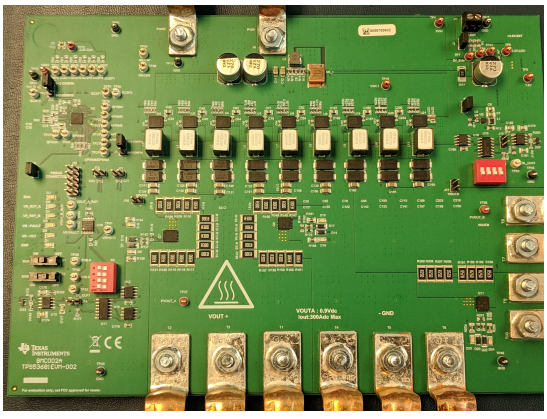
特長

- 大電力のメイン FPGA コア・レールを目的を対象とした 6 相の設計
- D-CAP+ 変調器による優れた電流共有能力と過渡応答
- PMBus 互換性による出力電圧設定、および V_{IN}、V_{OUT}、I_{OUT}、温度の遠隔測定
- デュアル・レール温度監視機能により、独立した熱性能トラッキングを実現
- PMBus による完全な補償調整
- V_{OUT} = 0.85V において、VCCINT レールのピーク効率 92% (公称値)

アプリケーション

- ハードウェア・アクセラレータ・カード
- データ・センター向けスイッチ
- キャンパスおよび支店のスイッチ





1 System Description

This is a power-dense, high-performance design targeted at powering Xilinx Ultrascale+ FPGAs commonly found in demanding datcenter switches and hardware accelerator card applications. These processors require excellent thermal performance, efficiency, and a fast transient response from their voltage regulators while also requiring on-the-fly optimization through PMBus. This design meets all the criteria with a simple thermal solution and minimal number of output capacitors despite an extremely tight regulation window thanks to the performance of TI's D-CAP+ modulator. The dual-output multiphase controller and TI's proprietary smart power stages allow for an integrated design, which, when compared to more traditional discrete designs, eliminates a number of passive components and reduces the printed-circuit board (PCB) layout area.

1.1 Key System Specifications

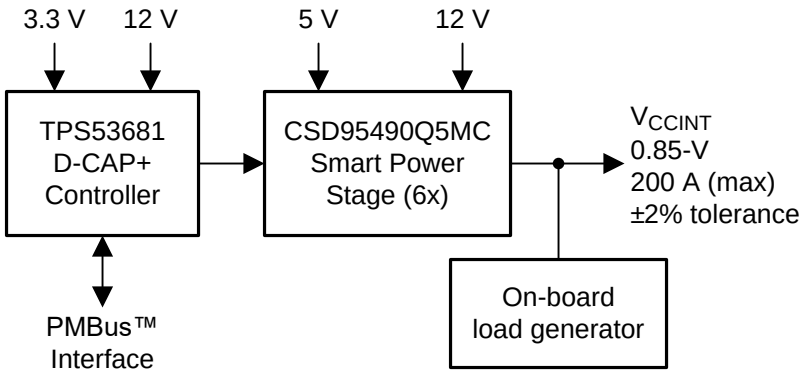
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input supply	12 V, ±5%
AC+DC tolerance	±2%
Output voltage	0.72 V, 0.85 V (nominal), 0.90 V
Maximim output current	200 A
DC load line	n/a
Maximim load step	100 A at 100 A/µs
Switching frequency	500 kHz
Number of phases	6
$C_{OUT, Bulk}$	17 x 470 µF, 2V, 3mΩ
$C_{OUT, MLCC}$	30 x 100 µF, 4V, X5R, 1206

2 System Overview

2.1 Block Diagram

図 1. TIDA-050020 Block Diagram



2.2 Highlighted Products

2.2.1 TPS53681 - Dual-Channel (6-Phase + 2-Phase) or (5-Phase + 3-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™

- Easily configurable for a wide range of dual-output voltage scenarios
- Programmable loop compensation through PMBus
- Configurable with non-volatile memory (NVM) for low external component counts
- Dynamic phase shedding with programmable current threshold for optimizing efficiency at light and heavy loads
- PMBus system interface for telemetry of voltage, current, power, temperature, and fault conditions
- Dual-rail temperature monitoring
- 5-mm × 5-mm, 40-pin, QFN PowerPad™ package

2.2.2 CSD95490Q5MC - 75-A Synchronous Buck NexFET™ Power Stage With DualCool™ Packaging

- 75-A continuous current capability
- 95% system efficiency at 25 A
- Up to 1.25-MHz switching frequencies supported
- Temperature-compensated bidirectional current sense signal
- Analog temperature output and fault monitoring
- High-density, low-inductance, SON 5-mm × 6-mm package

2.3 System Design Theory

The D-CAP+ modulator of the TPS53681 controller is integral to the high-performance of this reference design. This modulator allows the control loop to remain stable over a wide range of operating conditions as its transfer function is insensitive to variations in input voltage, load current, and phase number. A phase margin of 81.6° was measured for the V_{CCINT} rail with a crossover frequency of 99.5 kHz. Placing the unity gain frequency higher than 1/10 the switching frequency allows for a faster transient response. This faster transient response allows V_{OUT} to remain within its regulation limits during large load steps, such as the 100-A step specified by Xilinx. The output maintains stability even as the load current duty cycle and frequency vary. A faster transient response directly reduces the number of output capacitors required as compared to older regulation topologies such as peak current mode and voltage mode control.

Loop compensation can be adjusted easily using the PMBus interface through TI's Fusion Graphical User Interface (GUI). The GUI allows the user to tune the design for a wide range of output filters, including using all ceramic output capacitors, in case the design requirements change. At high load currents, the D-CAP+ modulator can maintain an even balance of all phase currents to avoid thermally stressing or damaging either the field-effect transistors (FETs), inductors, or FPGA while maintaining tight output voltage regulation.

The CSD95490Q5MC smart power stage features an optimized driver-FET solution in a thermally-efficient package which provides high efficiency up to 75 A of DC load current. The design process for the thermal solution becomes much simpler than using less efficient power stages or discrete FETs. The lower switching and conduction losses lead to higher efficiency and thus excellent thermal performance. The excellent thermal performance allows for smaller heat sink requirements and less airflow to be implemented in the final system design. Integrated temperature and fault monitoring from the power stage to the TPS53681 controller allows for operational telemetry, debug, validation, and configuration of the design through PMBus. On-chip, temperature compensated, bidirectional current sensing offers increased accuracy over operational corners compared to older, potentially uncompensated, DCR sense methods.

The regulator layout and output capacitor selection for this design received special consideration. Common bulk capacitors with 6 mΩ or 9 mΩ ESR values do not meet the tight regulation tolerances for this design during transient events. Instead 3-mΩ capacitors ensure a low-output impedance and specification compliance while maintaining a resonable component count..

These bulk capacitors, along with additional ceramic capacitors, are placed as close as possible (within 2 to 3 inches) to the load to maintain minimal board impedance and optimal performance. This layout also includes wide output and ground planes on multiple PCB layers to help minimize board parasitics. With no DC load line and a ±2% tolerance on V_{OUT} every millivolt matters. Proper layout and component selection becomes even more of a priority for these types of high-performance designs.

3 Hardware, Software, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The hardware requirements for this design are the same as those listed in the TPS53681 EVM User Guide on page 12.

3.1.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.2 Testing and Results

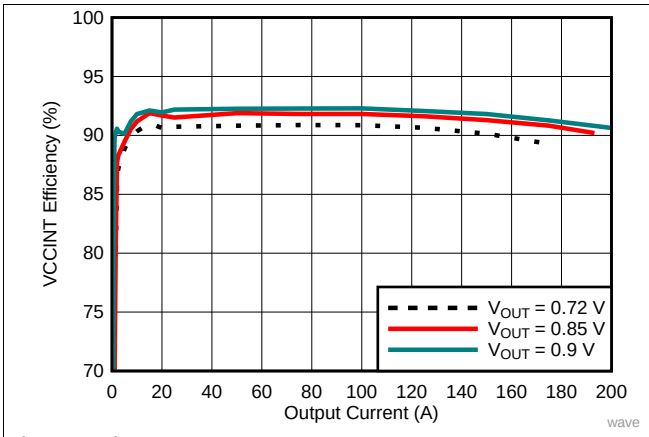
3.2.1 Test Setup

The setup for testing this design follows the guidelines set forth in the TPS53681 EVM User Guide.

3.2.2 Test Results

3.2.2.1 Efficiency and Power Loss

Efficiency and loss curves were measured, with inductor and 5-V loss included, for the nominal, minimim, and maximiu output votlages. Due to dropout limitations with the electronic load, 200-A could not be achieved at output voltages of 0.72 V and 0.85V, so the results show only up to the maximum load that was sustainedat each voltage.



f_{SW} = 500 kHz

図 2. VCCINT Efficiency

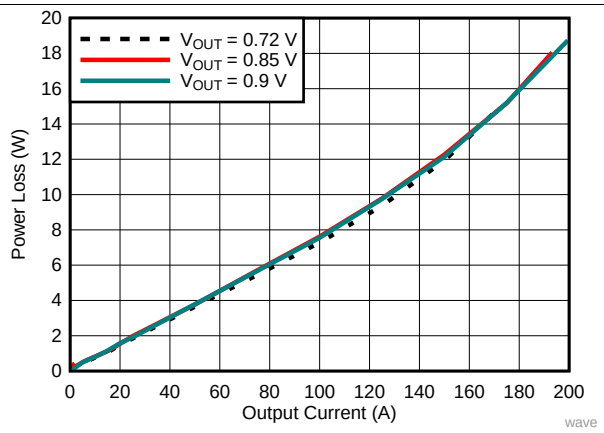
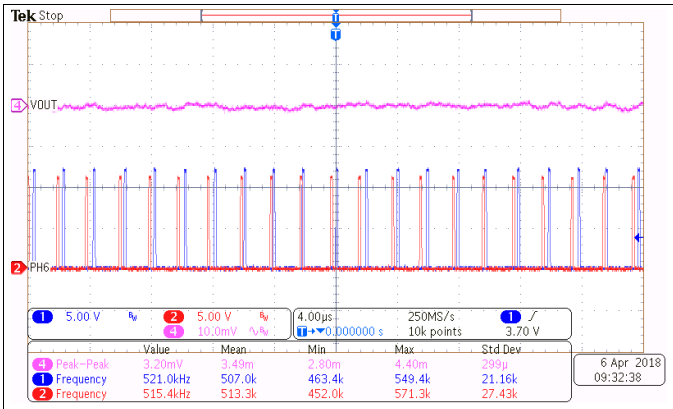


図 3. VCCINT Power Loss

OUTPUT VOLTAGE (V)	PEAK EFFICIENCY AND POWER LOSS	MAXIMUM CURRENT EFFICIENCY AND POWER LOSS
0.72	91.1%, 1.1 W @ 15 A	89.3%, 15.3W @ 175A
0.85	91.9%, 1.1 W @15 A	90.2%, 18.0W @ 193A
0.92	92.3%, 7.6 W @ 100 A	90.6%, 18.8W @ 200A

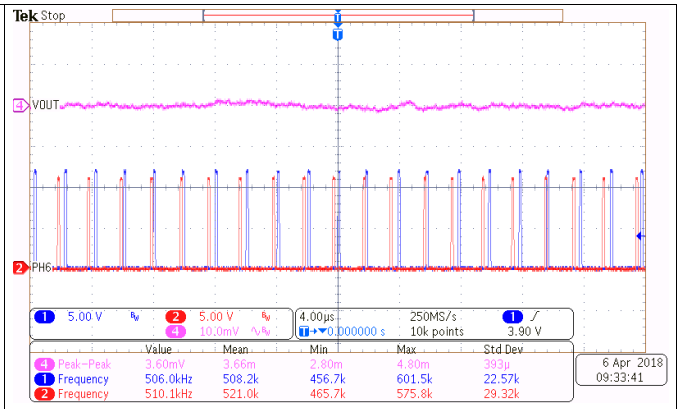
3.2.2.2 Steady-State Regulation and DC Accuracy

The output voltage was tested for steady-state stability across the entire load range without recording any failures or anomalies. DC ripple remained within the design targets and the measured switching frequency was within the data sheet limits.



I_{LOAD} = 100 A

図 4. Steady State

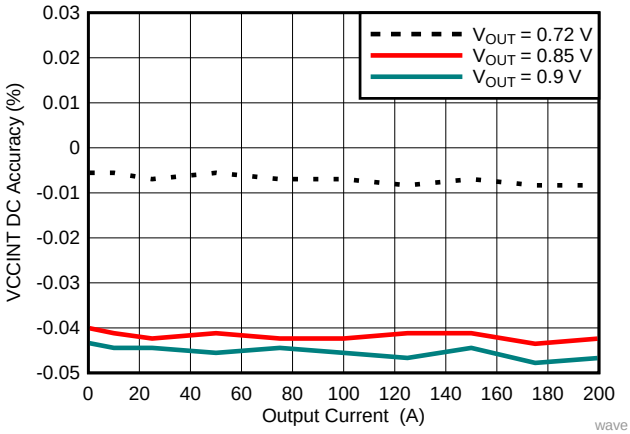


I_{LOAD} = 200 A

図 5. Steady State

表 2. DC Ripple and Switching Frequency

VCCINT RAIL OUTPUT VOLTAGE(V)	OUTPUT CURRENT (A)	OUTPUT RIPPLE (mVpp)	SWITCHING FREQUENCY (f_{SW}) (kHz)	
			PHASE 1	PHASE 6
0.85	100	3.49	507	513
	200	3.66	508	521

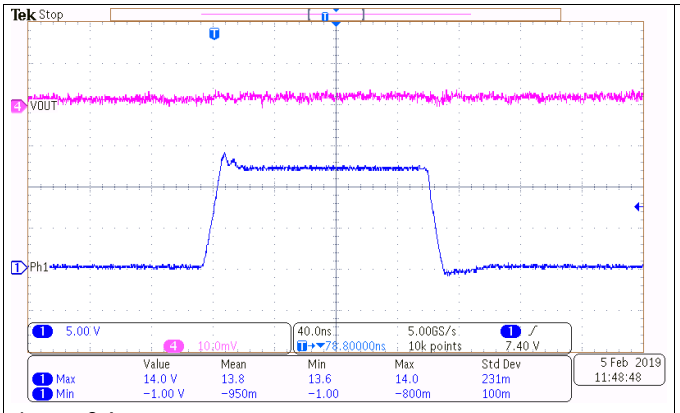


Nominal, minimum, and maximum, the DC accuracy remained within ±0.05% of the desired voltage across the entire load range.

図 6. VCCINT DC Accuracy

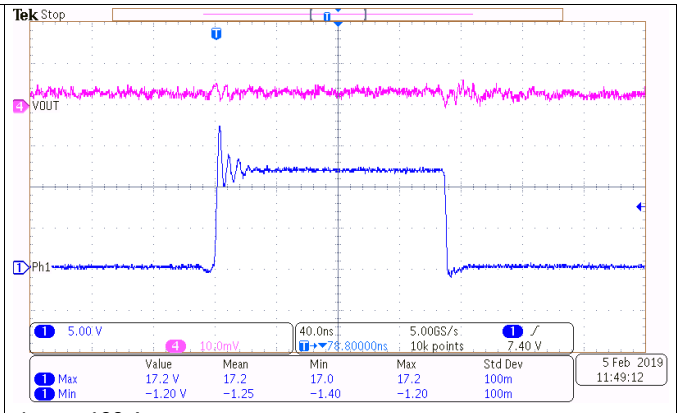
3.2.2.3 Switch Node Ringing

Switch node ringing of this design was checked to ensure long term robustness. Ringing above or below the CSD95490Q5MC datasheet limits could damage the power MOSFETs inside the power stage over time. Eventually, performance would decline and complete failure is possible.



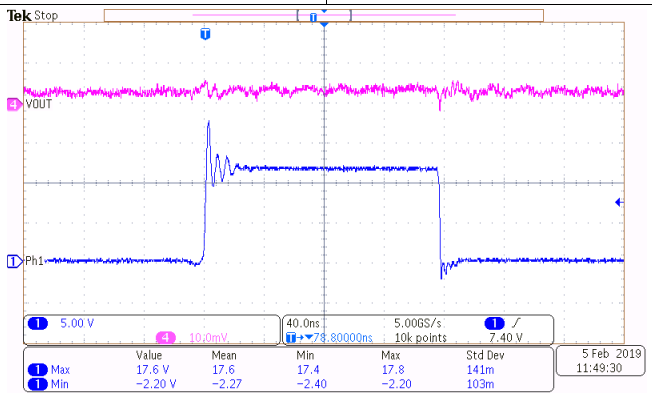
I_{LOAD} = 0 A

図 7. Switch Node Ringing



I_{LOAD} = 100 A

図 8. Switch Node Ringing



I_{LOAD} = 200

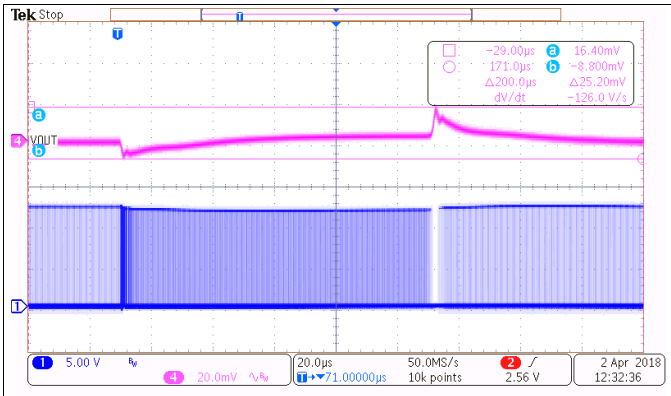
図 9. Switch Node Ringing

Over the full load range, the ringing on the rising and falling edge of the switch nodes was observed to be within the Absolute Maximum Ratings of the power stage datasheet without the use of a boot resistor or snubber on each phase. Only a small 0402 sized 4700 pF input decoupling capacitor was placed close to the V_{IN} pins of each power stage to help reduce ringing. However, switch node ringing is highly dependent on PCB layout and so placeholders for boot resistors and snubbers are recommended for every design in case differences between the end application board and the board used for these measurements increases ringing.

LOAD CURRENT (A)	HIGH-SIDE RINGING (V)	LOW-SIDE RINGING (V)
0	14.0	–1.0
100	17.2	–1.2
200	17.6	–2.2
CSD95490Q5MC 10-ns limits	23.0	–7.0

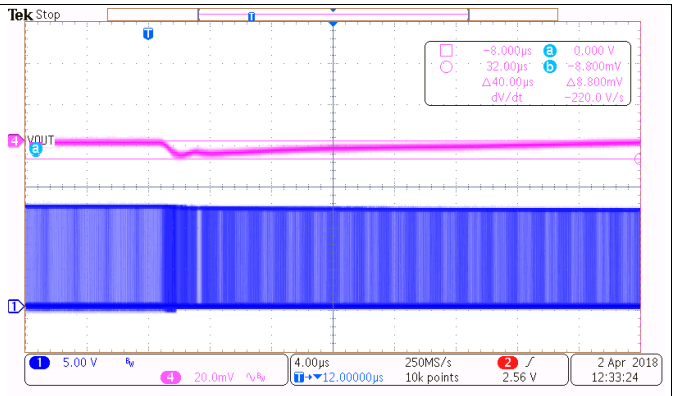
3.2.2.4 Transient Response

A load transient circuit placed on the board close to the output of the VCCINT rail was used to generate the 100-A step at the slew rate of 100A/µs. The single-step response showed little to no undershoot and the overshoot was less than the allowable 17 mV.



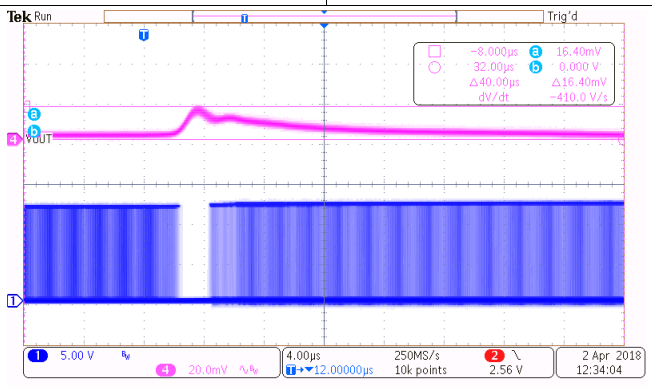
Transient 0 A to 100 A Duty Cycle = 10%

図 10. Overall Trasient Response



Transient 0 A to 100 A Duty Cycle = 10%

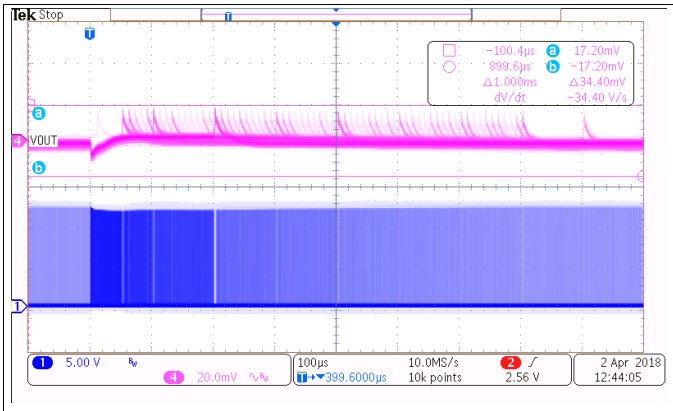
図 11. Undershoot Transient



Transient 0 A to 100 A Duty Cycle = 10%

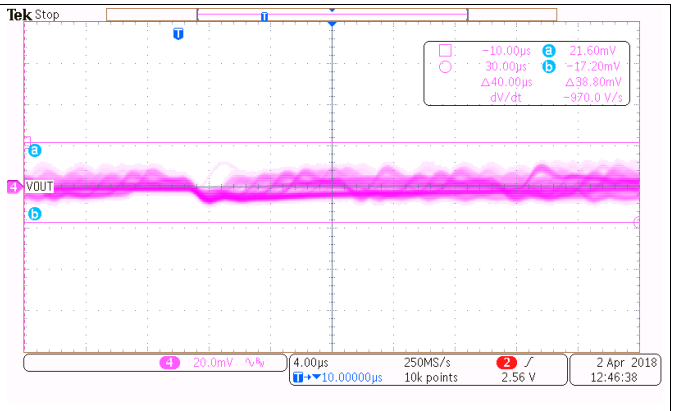
図 12. Transient Overshoot

The output voltage remained stable as the load duty cycle sweeps from 5% to 80%. Minimal undershoot was measured and the overshoot was less than 17 mV. While the transient circuit was able to hit the quick slew rate, it could not handle load frequencies above 150 kHz and so a beat frequency check at 500 kHz could not be performed. However, 図 13 shows no instabilities as the frequency of the load step rises to 150 kHz.



Transient from 0 A to 100 A Duty cycle from 5% to 80%

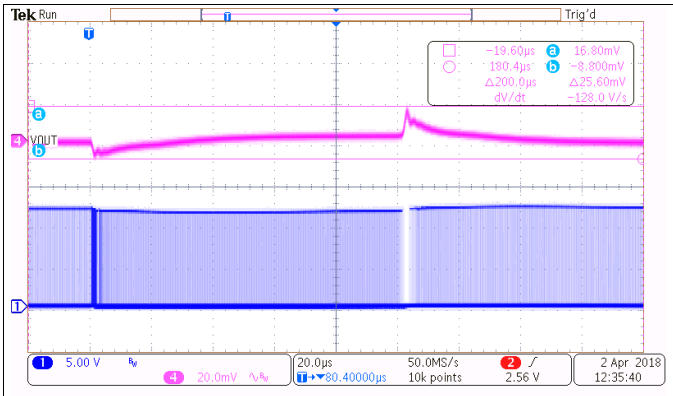
図 13. Transient



Transient from 0 A to 100 A Load frequency 10 kHz to 150 kHz

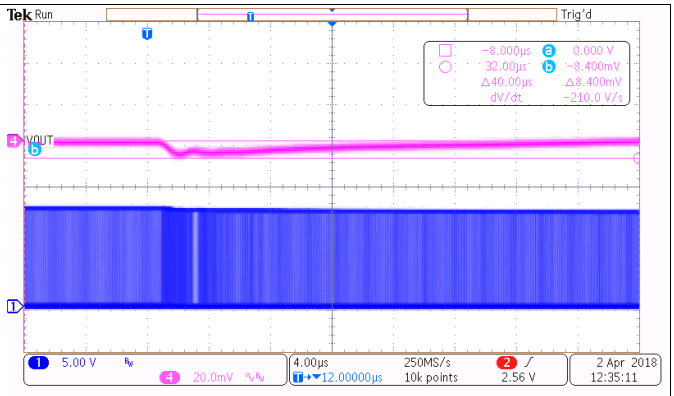
図 14. Transient and Load Frequency Change

Identical results occur when aa 100 A to 200 A load step is applied to the regulator output. The peak-to-peak excursions, overshoot, and undershoot all remain within the allowable ±2% window.



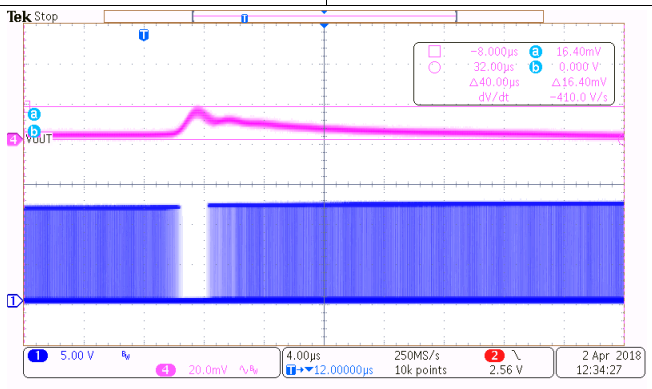
Transient from 100 A to 200 A Duty cycle = 10%

図 15. Transient Overall Response



Transient from 100 A to 200 A Duty cycle = 10%

図 16. Transient Undershoot



Transient from 100 A to 200 A Duty cycle = 10%

図 17. Transient Overshoot

3.2.2.5 Additional Small Signal Stability Testing

Because high frequency transients can not be generated for this design, a network analyzer is used generate a Bode plot of the loop transfer function and confirm the stability of the regulator. 図 18 shows a unity gain frequency of 99.5 kHz with a phase margin of 81.6°, indicating good stability with plenty of margin.

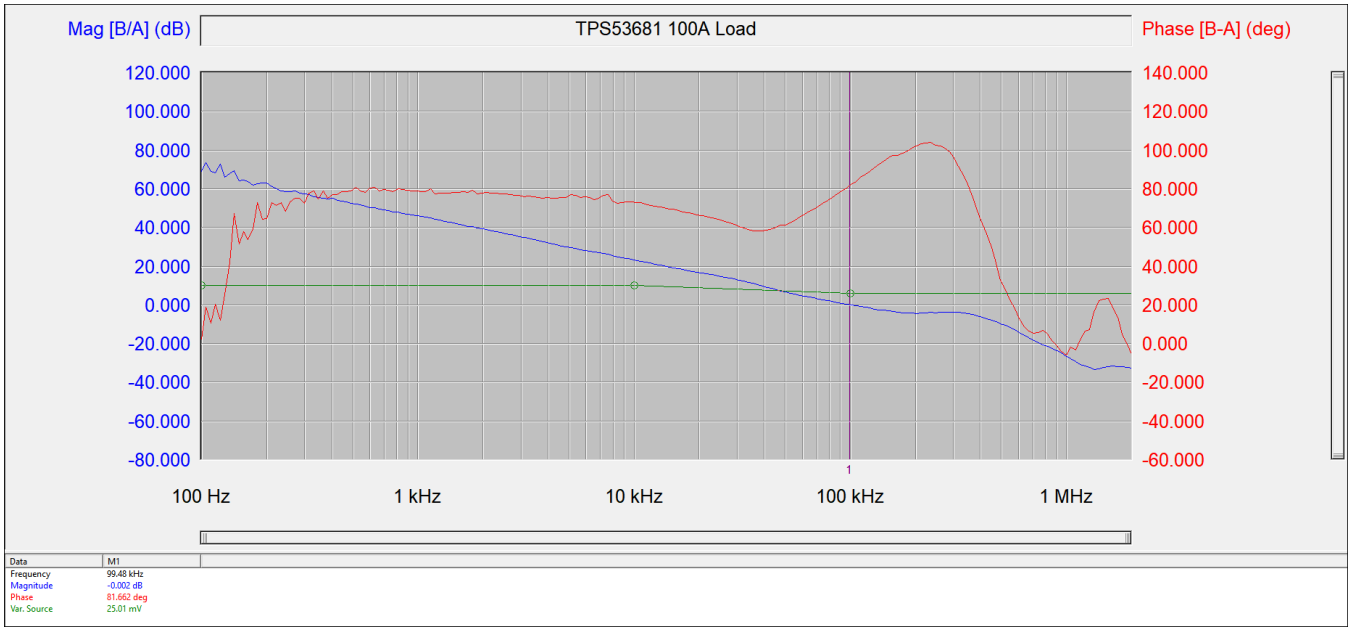
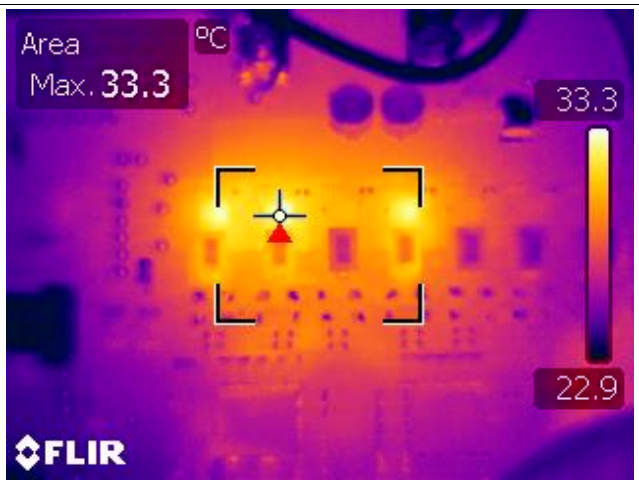


図 18. VCCINT Bode Plot at 100 A

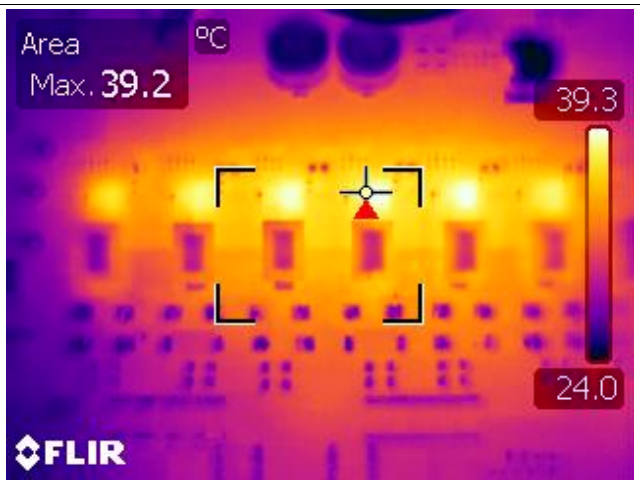
3.2.2.6 Thermal Performance

The thermal performance of the VCCINT rail is tested for 50 A, 100 A, 150 A, and 200 A loads at the nominal output voltage. The ambient temperature is 22°C for each test case and the design was allowed to soak for 5 minutes under load to reach thermal equilibrium. Airflow across the boards is 200 LFM.



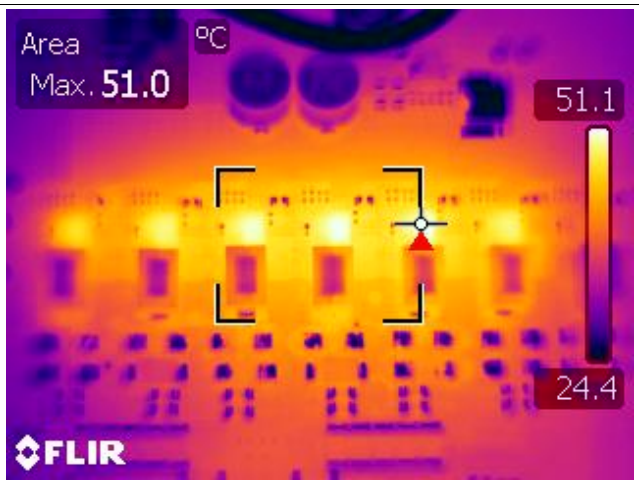
I_{LOAD} = 50 A

図 19. VCCINT Power Stage Temperature



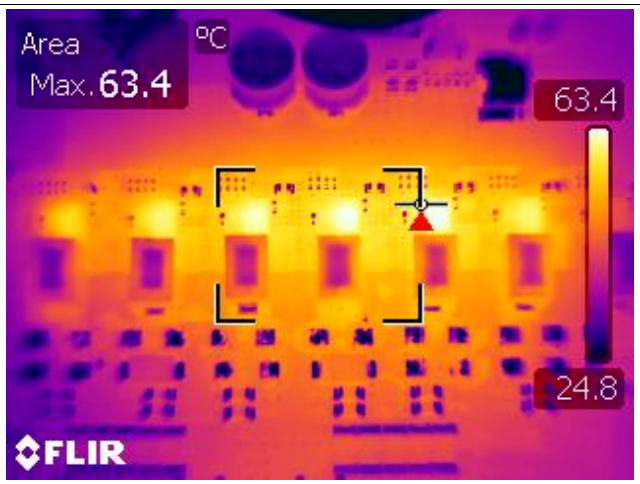
I_{LOAD} = 100 A

図 20. VCCINT Power Stage Temperature



I_{LOAD} = 150 A

図 21. VCCINT Power Stage Temperature



I_{LOAD} = 200 A

図 22. VCCINT Power Stage Temperature

3.2.2.7 Output Voltage Probing Techniques

Due to the tight output voltage tolerances associated with this application, standard passive and differential probes do not suffice when validating the design. Instead, solder a cut down coaxial cable from the oscilloscope BNC input directly across either an output capacitor near the feedback line sense point, or the feedback lines. (see 図 23). This procedure yields a much clearer of the output voltage on the oscilloscope when measuring DC ripple and confirming transient response.

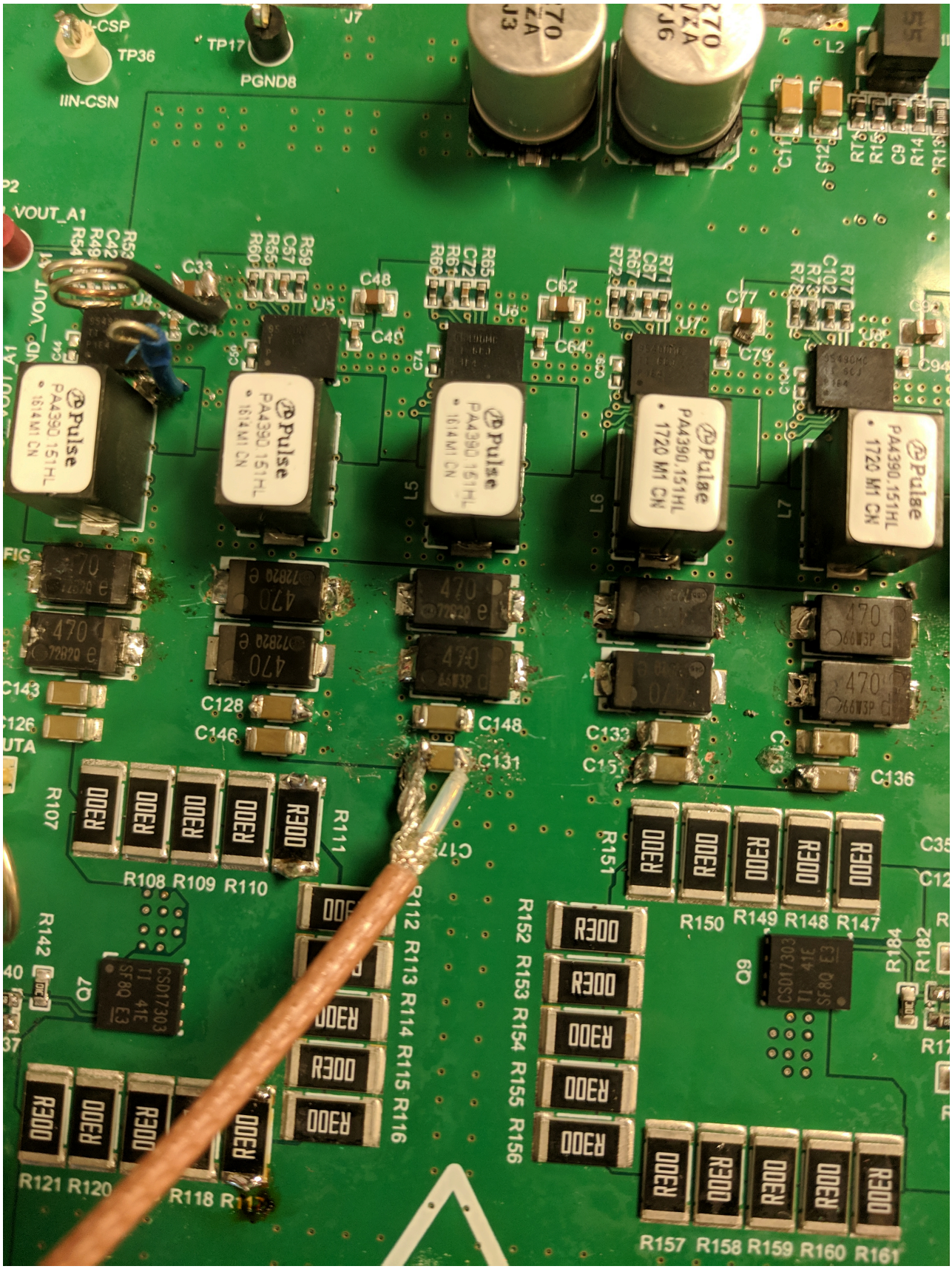


図 23. Proper BNC Cable Placement on V_{OUT}

To show the impact that probe type can make, 図 24 shows a direct connection with a BNC cable compared with passive and differential probes as a load transient is applied to the design.

Using a passive probe (blue trace) slows down the response when compared to the BNC probe by misrepresenting the overshoot upon load release. At the same time, the ringback after the load step is over exaggerated and there is more noise during the steady state portion of the waveform. With this waveform, a designer might incorrectly assume compensation is an issue and make changes that could hurt loop stablity while also undersizing the value of output capacitance (C_{OUT}).

Probing the output voltage (V_{OUT}) with a differential probe instead (magenta trace) shows significantly more noise than the BNC probe which falsely reports a peak-to-peak excursion that is 6.4 mV higher than the true value. Using this probing technique, significantly more output capacitance would be needed to keep V_{OUT} within the speficiation range, if it is even possbile. The noise injection from the differential probe might simply be too high, making a passing result unobtainable given the tight tolerances required.

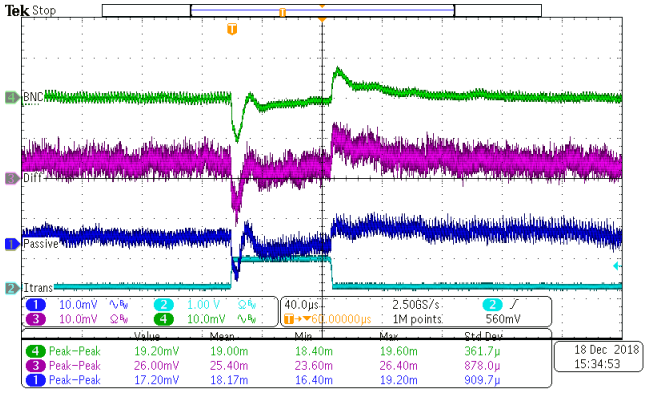


図 24. Probe Comparison Results

Probe Method	Transient Peak-to-Peak Voltage Swing (±17mV Target)
BNC	19.00mV
Differential	25.40mV
Passive	18.17mV

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050020.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050020.

4.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective data sheet for each part when laying out a design using the TPS53681 controller and CSD95490 smart power stage. Some other guidelines to consider include:

- Use an identical layout for all six phases on the core rail to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as pulse-width modulation (PWM) and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, CSP, VREF, and so forth.
- Use quality decoupling capacitors for both the input and output sides of the regulator to obtain the maximum performance possible with respect to DC ripple and transient response. Ceramic capacitors must be rated to at least 16 V for input decoupling and 2 V for output decoupling with a dielectric rating of X5R or better.
- Ensure that the V_{OUT} and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for a maximum amount of heat to flow out of the power stages and inductors into the board.
- Place output capacitors as close as possible to the load to ensure the least amount of board parasitics and optimal transient performance.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050020.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050020.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050020.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050020.

5 Software Files

To download the Fusion Digitial Power Designer Software, go to the product page on TI's website.

6 Related Documentation

1. Texas Instruments, TPS53681 Dual-Channel (6-Phase + 2-Phase) or (5-Phase + 3-Phase) D-CAP+™

Step-Down Multiphase Controller with NVM and PMBus™ Datasheet
2. Texas Instruments, CSD95490Q5MC Synchronous Buck NexFET™ Smart Power Stage Datasheet
3. Texas Instruments, Using the TPS53681EVM-002, Dual Multiphase DC-DC Step-Down Analog Controller with PMBus™ Interface, User Guide

6.1 商標

6.2 デベロッパー・ネットワークの製品に関する免責事項

7 About the Author

Carmen Parisi is a Senior Applications Engineer working in the Multiphase and Control Solutions (MCS) group at TI developing reference designs and application notes. He has seven years of experience in power electronics working on mobile, desktop, and server V_{CORE} applications; battery chargers; and system PMICs. Carmen earned a combined BS/MS degree in electrical engineering from the Rochester Institute of Technology.

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