参考資料

デザイン・ガイド：TIDA-050029
車載照明向け 45W、15W デュアル SEPIC LED ドライバのリファレンス・デザイン

概要

このリファレンス・デザインは、TPS92682-Q1 デュアルチャネル LED コントローラを車載フロントライト・アプリケーションに使用して、ハイビーム (HB) とロービーム (LB)、日中走行用ライト (DRL) とポジション (POS) ライトの機能をサポートするものです。TPS92682-Q1 を 1 個使用して 1 段構成の電源ソリューションを実装し、コントローラ・エリア・ネットワーク (CAN) インターフェイスを介して HB と LB、DRL と POS の各チャネルを駆動します。従来はコントローラを 2 個使用していましたが、このシンプルな設計により部品点数を削減し、ソリューションを小型化できます。TPS92682-Q1 は柔軟性が高く、内部および外部 PWM 調光に対応するほか、内蔵された監視機能によるフォルト検出と連続 LED 電流の保護も実現しています。電磁干渉 (EMI) フィルタも搭載し、CISPR-25 Class 5 の伝導性放射要件に適合するように設計されています。

リソース

TIDA-050029	デザイン・フォルダ
TPS92682-Q1	プロダクト・フォルダ
TPS92682EVM-070	ツール・フォルダ
TPS92682EVM-069	ツール・フォルダ

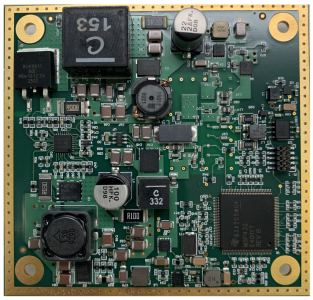
E2E™エキスパートに質問

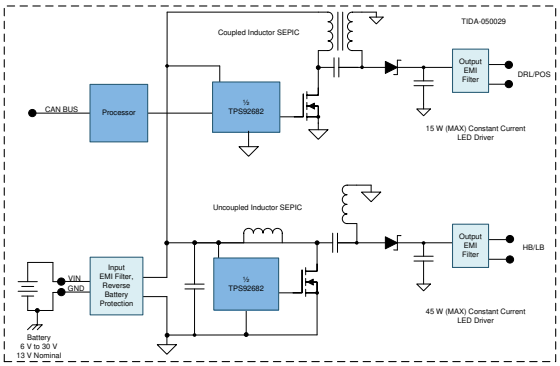
特長

- デュアル・コントローラ・モード
  - DRL および POS 用結合 SEPIC
  - HB および LB 用非結合 SEPIC
- CISPR-25 Class 5 EMI ソリューション
- AM帯域外のスイッチング周波数
- 拡散スペクトラム周波数変調
- ウォーム・クランクおよびロード・ダンプ時も動作
- CAN インターフェイス
- 過電圧保護と入力低電圧誤動作防止

アプリケーション

- ボディ・エレクトロニクスとライティング
  - ヘッドライト
- 先進運転支援システム (ADAS)
  - ドライバー監視システム





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1 System Description

This reference design describes a high-power LED driver for automotive front lighting applications. The design uses a dual-channel controller and power stage solution for driving both the high beam and low beam (HB/LB) and daytime running lights and positioning (DRL/POS). Traditional implementation uses two separate controllers and power stages. This new approach minimizes cost and circuitry while providing high-quality lighting solutions in terms of electromagnetic interference, thermal efficiency, and light quality. The design uses a CAN interface to control the module.

The design gives a simple, ease-to-adopt implementation for a high-power and output accuracy LED driver. This design uses the TPS92682 dual multi-topology controller for an input voltage range from 6 V to 40 V. This design meets CISPR-25 Class 5 EMI standards with shielding, and the switching frequency of the controller operates outside the AM frequency band. The TPS92682 controller offers SPI communication interface with spread spectrum frequency modulation as well as PWM dimming features that can be used along with this reference design for a variety of other automotive lighting applications.

The LED current for HB/LB is set to 1.2 A nominal and DRL/POS is set to 1 A nominal. The switching frequency set at 320 kHz. For POS mode, the current will be PWM dimmed at 10%. For HB mode, both HB and LB will be ON. All these parameters can be modified to different user requirements.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN} input voltage (nominal)	V_{IN} ≥ 9 V: full functionality. For V_{IN} < 9 V: Current is reduced linearly from 100% to 50% at 6 V	9	13	16	V
V_{IN} input voltage (min or max)	Warm crank or load dump	6		40	V
V_{IN} undervoltage lockout			4.5		V
OUTPUT CHARACTERISTICS					
LED forward voltage			3.2		V
V_{LED} output voltage		7		40	V
HB/LB: I_{LED} output current		400		1200	mA
DRL/POS: I_{LED} output current		100		1000	mA
HB/LB: Output power		2.8		45	W
DRL/POS: Output power		0.7		15	W
PWM dimming range (200 Hz–400 Hz)		5		100	%
SYSTEM CHARACTERISTICS					
Output overvoltage protection level			60		V
Overvoltage hysteresis			3		V
f_{SW} switching frequency			320		kHz
HB/LB Efficiency	V_{IN} = 13.5 V, I_{OUT} = 1.2 A , V_{OUT} = 34.3 V		88%		
DRL/POS Efficiency	V_{IN} = 13.5 V, I_{OUT} = 1 A , V_{OUT} = 14 V		88%		
EMI (conducted)		CISPR-25 Class 5			
BASE BOARD CHARACTERISTICS					
Form factor		3.0" L × 3.15" W			

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表 **1. Key System Specifications (continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Number of layers			6		
Height	Including heat sink and shield		0.9"		

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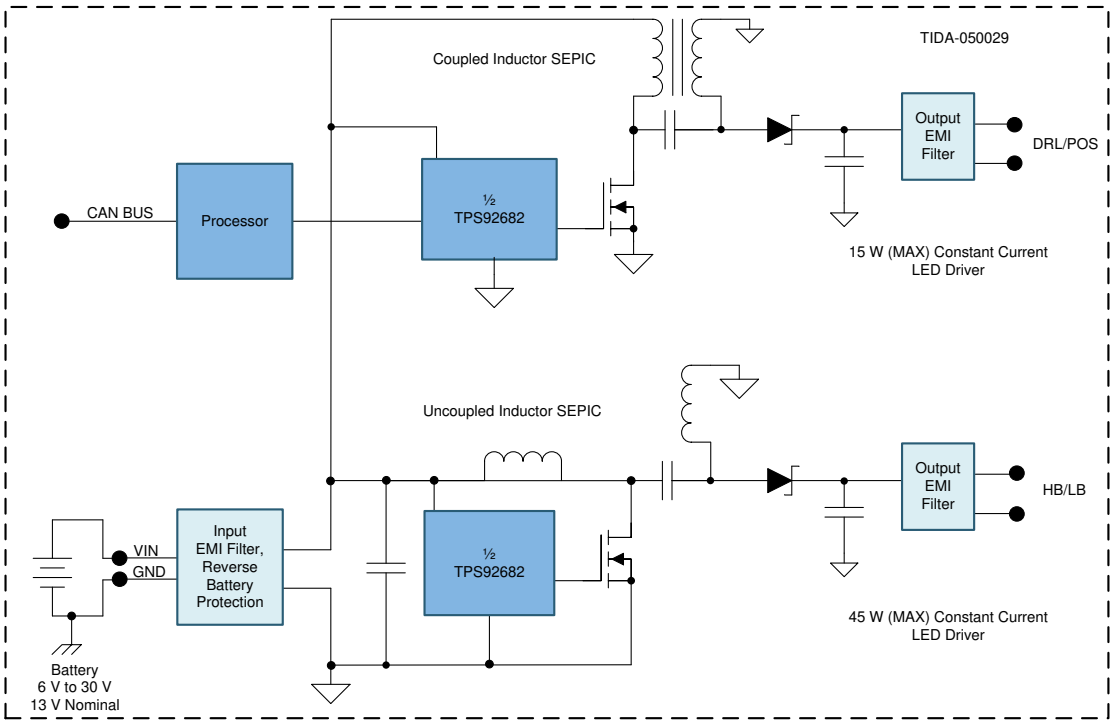
2 System Overview

2.1 Block Diagram

図 1. TIDA-050029 Block Diagram



2.2 Design Considerations

This reference design uses the TPS92682-Q1 dual-channel LED controller in an automotive front lighting application. The design powers the HB/LB for a maximum of 43 W along with the DRL/POS for 15 W maximum. The module communicates with a CAN interface. The CAN interface is used to command the module to either enable the HB or LB along with enabling the DRL or POS. When the high beam is enabled, both the HB and LB are enabled. It can also change register settings to the TPS92682-Q1 device to optimize for different configurations or LEDs. The key system specifications are listed in 表 1.

2.3 Highlighted Products

2.3.1 TPS92682-Q1

The TPS92682 device is a versatile dual LED controller that can support a range of topologies. It is a peak current controller with SPI communication interface. The device is programmable to operate in constant-voltage (CV) or constant-current modes (CC). The device is intended for high-brightness LED lighting applications where efficiency, high accuracy, high power, and PWM or analog dimming (or both) are important. The device includes gate drivers for an external LED string disconnect FET to enable faster turn-on and turn-off of the LED string for high contrast ratios. In addition, it has the capability for Spread Spectrum Frequency Modulation (SSFM) for improved EMI performance.

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A low-offset rail-to-rail current sense amplifier improves the steady-state accuracy. This amplifier directly measures LED current using either a high-side or a low-side series current sense resistor. The device modulates LED current using either analog dimming, PWM dimming, or both simultaneously. Other features include comprehensive programmable fault detection circuitry, undervoltage lockout (UVLO), wide input voltage operation, open and overvoltage protection (OVP) operation, and a wide-operating temperature range with thermal shutdown.

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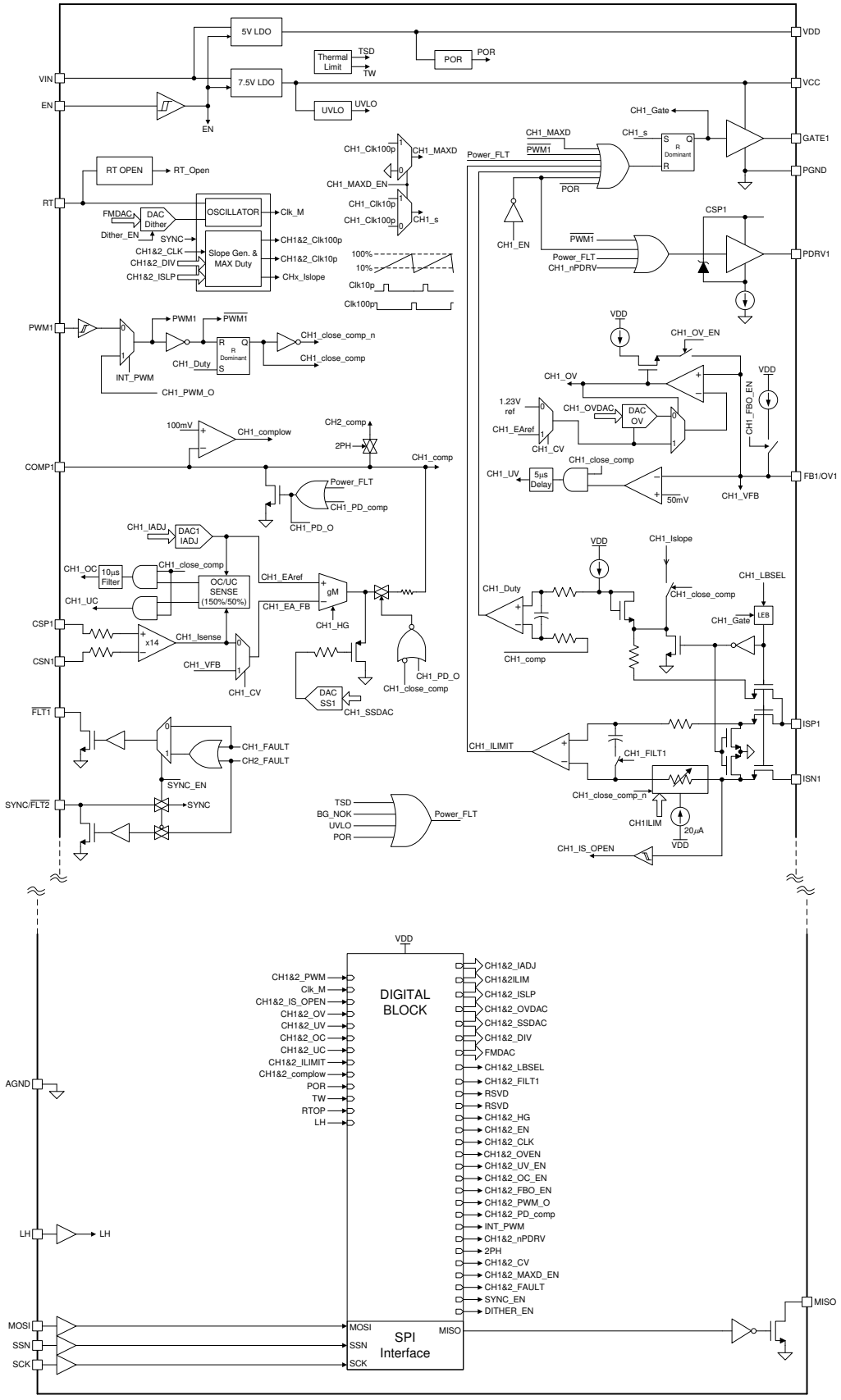
図 2. TPS92682 Block Diagram



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The TPS92682 device operates at an input range up to 65 V in a thermally enhanced wettable flank (VQFN) package.

Key features of this device include:

- TPS92692-Q1: AEC-Q100 Grade 1 qualified
- Wide input voltage range: 4.5 V to 65 V
- ±4% LED current accuracy over –40°C to 150°C junction temperature range
- SPI programmable features:
  - Better than ±4% LED current accuracy over –40°C to 150°C junction temperature range
  - Compatible with high-side and low-side current sense implementations
  - SSFM for improved EMI
  - Soft-start timing
  - ILED current and output voltage settings
  - Current limit, overvoltage, fault-timer
  - Single vs dual phase
  - CV and CC mode configuration
- Dual-channel peak-current-mode (PCM) controller
- Low input offset rail-to-rail current sense amplifier
- Analog dimming
- External series FET PWM dimming with integrated P-channel driver interface
- Open drain fault flag indicator per channel
- Up to 1-MHz programmable switching frequency with external clock synchronization capability
- Comprehensive programmable fault protection circuitry

2.4 LM74700

The LM74700 diode controller operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low-loss reverse polarity protection. The wide input range of 3 V to 65 V allows the control of the battery input voltage. With a low $R_{DS(on)}$ external N-channel MOSFET, a very low forward voltage drop can be achieved while minimizing the power loss.

2.5 MSP432E401Y

The MSP432401Y microcontroller is used as a communication interface between the CAN and the TPS92682 device. The microcontroller initializes the TPS92682 device for constant-current mode with register settings to regulate the LED current per the system specification. The microcontroller monitors the temperature of the HB/LB and DRL/POS and will lower the effective current by PWM dimming the current if the temperature is above 100°C. This thermal fold-back function prevents thermal runaway of the LED. It also monitors the onboard temperature of the power stage through the R20 thermistor and will perform the same PWM'ing function to protect the power stage from overtemperature. Note that the MSP432401Y MCU is not automotive grade and it is used here as a demonstration for the capability of the TPS92682 device.

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2.6 System Design Theory

This reference design consists of a high-performance LED controller configured in both a coupled-inductor and non-coupled inductor SEPIC topology. It uses EMI filtering and a load disconnect FET for high slew rate PWM dimming (see 図 3). The input voltage range from 9 V to 16 V for nominal operation with the capability to run as low as 6 V and for warm crank operation. It can operate as high as 40 V for load dump operation. This design supports up the HB/LB function to 1.2 A of output current and an output power rating of 45 W. It will support DRL/POS for up to 1 A of output current and output of up to 15 W. However, multiple combinations of input supplies and LED loads along with an external CAN interface can be created and optimized using this reference design as a starting point. Standard recommended component values (such as the VCC capacitor) are not covered in this section.

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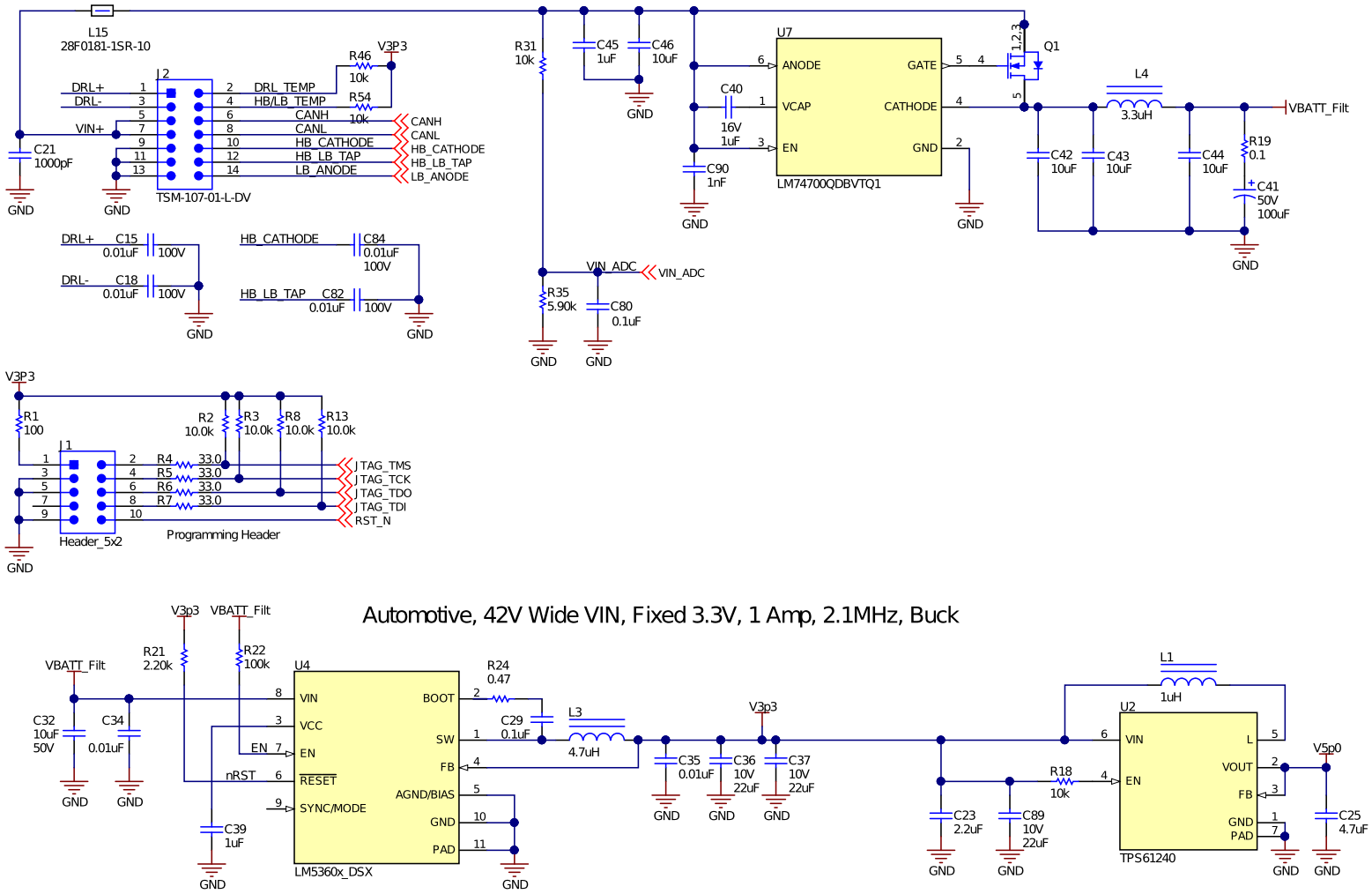
図 3. Schematic Sheet 1: Input Filter and Regulators for Microcontroller



R18 is populated to allow for PWM dimming.

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図 4. Schematic Sheet 2: TPS92682 Main Power Stage

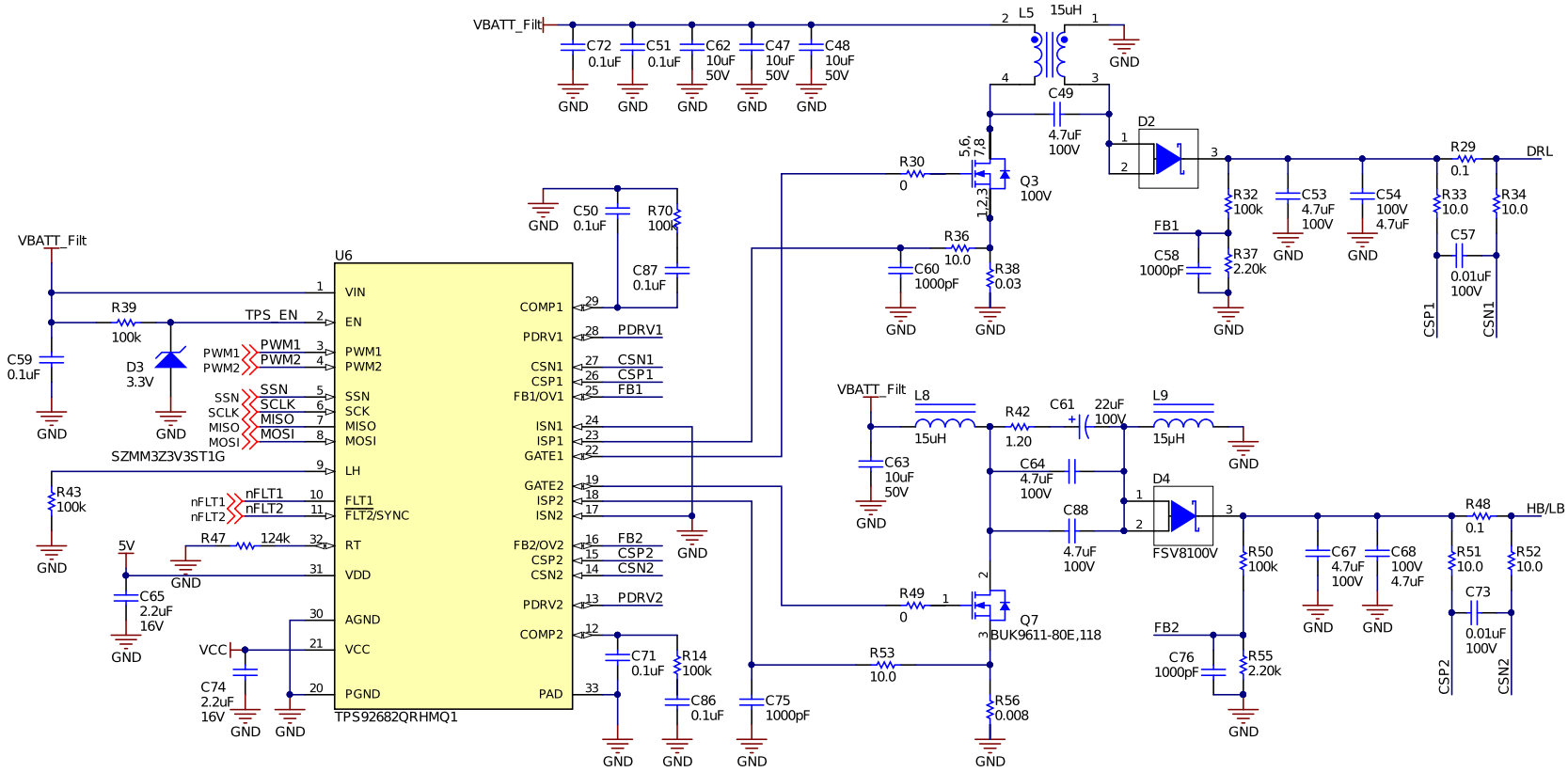

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図 5. Schematic Sheet 3: Output Stages and CAN Interface

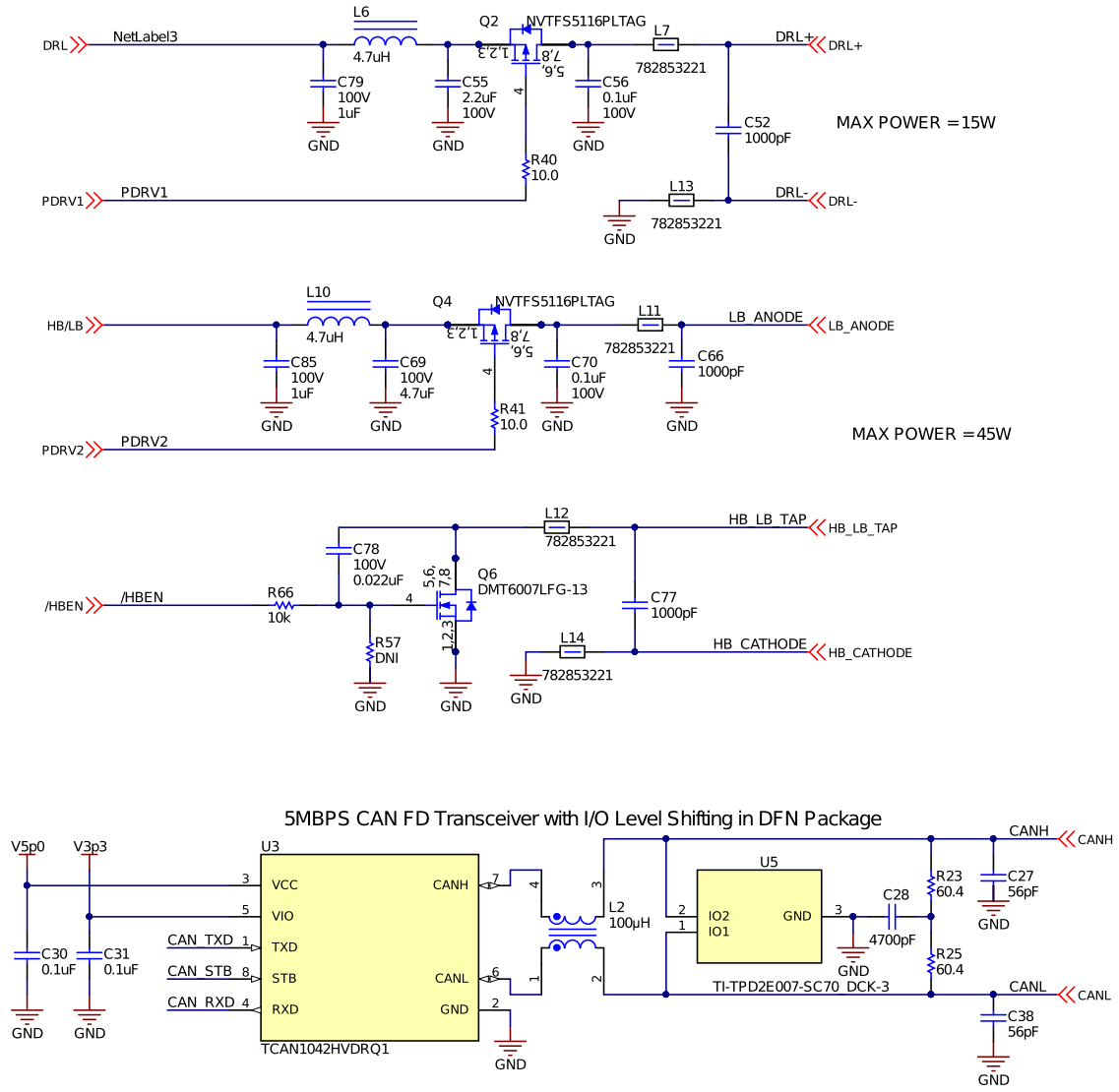

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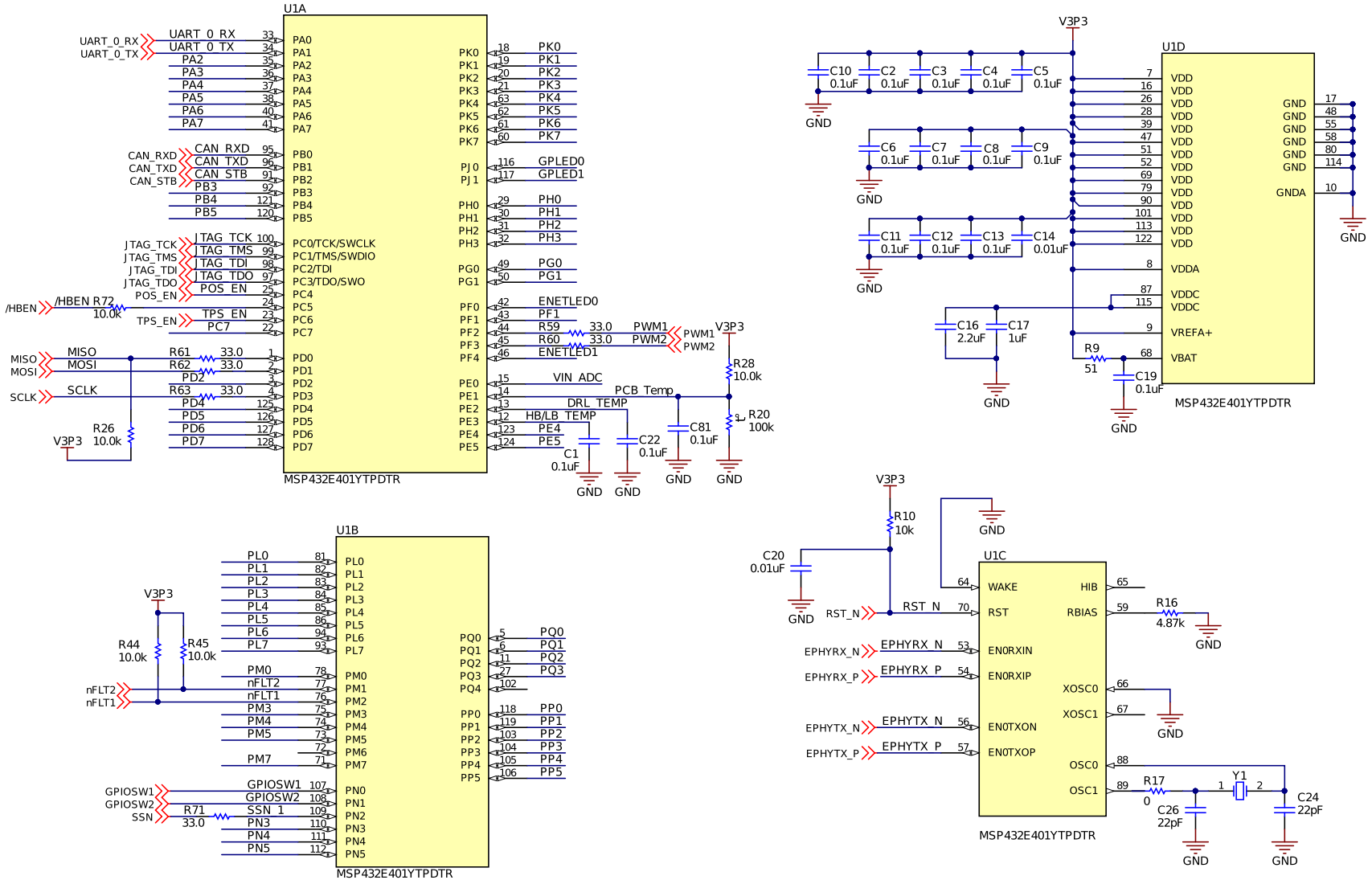
図 6. Schematic Sheet 4: MSP432E401 Microcontroller



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2.6.1 Design Procedure:

The input power is received from the J1 connector and is supplied to U7 (LM74700) which is an ideal diode rectifier that is used for reverse battery protection. The voltage then goes to the U6 (TPS92682) along with U4 to generate the 3.3-V supply for the microcontroller (U1). The microcontroller interface to the TPS92682 and CAN interface lines via U3 (TCAN1042HVDRQ1). Upon power up, the microcontroller will initialize the TPS92682 device with the appropriate register settings. The CAN interface is use to command the module to either enable the HB or LB along with enabling the DRL or POS. When the high beam is enabled, both the HB and LB are enabled. When in POS mode, the TPS92682device will lower the output current to the DRL via PWM dimming the current to 10% of the set point. This design guide focuses on the power stage design for the TPS92682 device and not the microcontroller and its associated circuitry. Note that the microcontroller (MPS432E401YTPDTR) is not rated for automotive and is used as a communication interface device for the CAN interface and the TPS92682 device. The following subsections help calculate component values and ratings. These equations are based on the key specifications listed in 表 1. The calculation for the component is done for both power stages operation in SEPIC mode. The lower power DRL/POS design is done with a coupled inductor design while the higher power level HB/LB design is done with an uncoupled inductor design. The reason for the two separate inductors for HB/LB is due to the fact that there is a limited number of coupled inductors for the high power levels.

2.6.1.1 Setting the Switching Frequency

For this design, a switching frequency of 320 kHz is selected to keep the fundamental switching noise out of the AM band and reduce the switching power loss for thermal reasons on the HB/LB because of the high output power (45 W). The RT resistor (R47) can be calculated for 320 kHz using 式 1:

$$R_T = \frac{10^{12}}{12.5 \times SW_{DIV} \times f_{sw}} = \frac{10^{12}}{12.5 \times 2 \times 330\,kHz} = 125\ k\Omega \quad (1)$$

where

- SW_{DIV} is 2. This is the default division factor in SW_{DIV} register 03h of the TPS92682 device
- f_{SW} is the switching frequency of the circuit

A value of 124 kΩ is selected for R47.

2.6.1.2 Uncoupled SEPIC 45 W: Operating Parameters, Duty Cycle for HB/LB

The typical operating duty cycle (D), the maximum operating duty cycle (D_{MAX}), and the minimum operating duty cycle (D_{MIN}) are required to calculate the inductor values. These values can be calculated using the following equations:

$$D = \frac{V_{OUT} + V_f}{V_{IN} + V_{OUT} + V_f} = \frac{23\ V + 0.6\ V}{13\ V + 23\ V + 0.6\ V} = 0.64 \quad (2)$$

$$D_{MAX} = \frac{V_{OUT(MAX)} + V_f}{V_{IN(MIN)} + V_{OUT(MAX)} + V_f} = \frac{40\ V + 0.6\ V}{6 + 40\ V + 0.6\ V} = 0.87 \quad (3)$$

$$D_{MIN} = \frac{V_{OUT(MIN)} + V_f}{V_{IN(MAX)} + V_{OUT(MIN)} + V_f} = \frac{7\ V + 0.6\ V}{40\ V + 7\ V + 0.6\ V} = 0.16 \quad (4)$$

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2.6.1.3 Uncoupled SEPIC 45 W: Inductor Value Calculation for HB/LB

The power stage is designed to run down to 6-V input for the warm cranking condition. The inductor value is calculated to ensure the circuit operates in continuous conduction mode (CCM) for a certain range of output currents at the typical operating points. In this design, the CCM to DCM boundary is set to about 1/3 of the maximum output power of 45 W, or a 1.2-A LED current with a 37.5-V LED load. As a result, this power boundary ($P_{O(BDRY)}$) is set for 15 W and the inductor values can be calculated using the following equations for the SEPIC regulator:

$$\Delta I_L = I_{IN} \times 33\% = \frac{P_{O(MAX)}}{V_{IN(NOM)}} = 33\% = \frac{44\ W}{13\ V} \times 33\% = 1.15\ A \tag{5}$$

$$L1 = L2 = \frac{V_{IN,MIN}}{\Delta I \times f_{SW}} \times D_{MAX} = \frac{6}{1.15 \times 320\ kHz} \times 0.87 = 14.2\ \mu H$$

where

- f_{SW} is the switching frequency of the circuit (6)

A value of 15 µH is selected for both L8 and L9.

2.6.1.4 Uncoupled SEPIC 45-W Peak Primary Inductor Current for HB/LB

To determine the minimum saturation rating of the inductor current, the peak inductor current at the minimum input voltage must be known and the inductor sized accordingly. This peak inductor current can be calculated using the following equations for average current (I_L) and peak current ($I_{L(peak)}$):

$$I_{L1(peak)} - I_{IOUT(max)} \times \frac{V_{OUT,max} + V_f}{V_{IN,min}} \times \left(1 + \frac{33\%}{2}\right) = 1.2\ A \times \frac{40\ V + 0.6\ V}{6\ V} \times 1.165 = 9.5\ A \tag{7}$$

The current calculated in 式 7 is for steady-state operation. Set the current limit and inductor saturation current rating 30% above the steady state 9.5 A for a transient condition. Use an inductor with a minimum current rating of 12.5 A.

2.6.1.5 Uncoupled SEPIC 45 W: Peak Secondary Inductor Current for HB/LB

To determine the minimum saturation rating of the inductor current, the peak inductor current at the minimum input voltage must be known and the inductor sized accordingly. This peak inductor current can be calculated using the following equations for average current (I_L) and peak current ($I_{L(peak)}$):

$$I_{L2(peak)} - I_{IOUT(max)} \times \left(\frac{1 + 33\%}{2}\right) = 1.2\ A \times 1.165 = 1.4\ A \tag{8}$$

Set the current limit and inductor saturation current rating 30% above 1.4 A for transient and efficiency loss. Use an inductor with a minimum current rating of 1.82 A.

2.6.1.6 Calculating Uncoupled SEPIC R_{IS} (R9)

Due to the relatively high peak switch currents in this design, the equation based on the current limit results in a much lower value. A $VI_{IS(LIMIT)}$ value of 75 mV is used both for high current demand during load switching from low beam to high beam and for power dissipation purposes. Find the value using 式 9:

$$R_{IS} = \frac{V_{IS(LIMIT)}}{I_{L(PEAK)}} = \frac{0.075}{9.5} = 0.008\ \Omega \tag{9}$$

For this design, a value of 0.008 Ω is selected for R56.

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2.6.1.7 Coupled SEPIC 15 W: Operating Parameters, Duty Cycle for DRL/POS

The typical operating duty cycle (D), the maximum operating duty cycle (D_{MAX}), and the minimum operating duty cycle (D_{MIN}) are required to calculate the inductor values. These values can be calculated using the following equations:

$$D = \frac{V_{OUT} + V_f}{V_{IN} + V_{OUT} + V_f} = \frac{23\ V + 0.6\ V}{13\ V + 23\ V + 0.6\ V} = 0.64 \quad (10)$$

$$D_{MAX} = \frac{V_{OUT(MAX)} + V_f}{V_{IN(MIN)} + V_{OUT(MAX)} + V_f} = \frac{40\ V + 0.6\ V}{6 + 40\ V + 0.6\ V} = 0.87 \quad (11)$$

$$D_{MIN} = \frac{V_{OUT(MIN)} + V_f}{V_{IN(MAX)} + V_{OUT(MIN)} + V_f} = \frac{7\ V + 0.6\ V}{40\ V + 7\ V + 0.6\ V} = 0.16 \quad (12)$$

2.6.1.8 Coupled SEPIC 15 W: Inductor Value Calculation for DRL/POS

The inductor value is calculated to ensure the circuit operates in continuous conduction mode (CCM) for a certain range of output currents at the typical operating points. In this design, the CCM to DCM boundary is set to about 1/3 of the maximum output power of 15 W. As a result, this power boundary ($P_{O(BDRY)}$) is set for 5 W and the inductor values can be calculated using 式 13 for the coupled SEPIC regulator: Note the factor of 2, different in the denominator of the equation for the coupled inductor case versus the uncoupled inductor SEPIC.

$$\Delta I_L = I_{IN} \times 33\% = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times 33\% = \frac{15\ W}{6\ V} \times 33\% = 0.83\ A \quad (13)$$

$$L1 = L2 = \frac{V_{IN,MIN}}{2 \times \Delta I \times f_{sw}} \times D_{MAX} = \frac{6\ V}{2 \times 0.83\ A \times 320\ kHz} \times 0.87 = 9.8\ \mu H$$

where

- f_{sw} is the switching frequency of the circuit (14)

Use a value greater than 9.8 µH: 15 µH is selected for L5.

2.6.1.9 Coupled SEPIC Peak Inductor Current for DRL/POS

To determine the minimum saturation rating of the inductor current, the peak primary and secondary current at the minimum input voltage must be known and the inductor sized accordingly. This peak inductor current is the sum of the primary and secondary current and can be calculated using the following equations ($I_{PRIMARY}$) and peak current ($I_{L(PEAK)}$):

$$I_{L(PRIM)} = I_{OUT(MAX)} \times \frac{V_{OUT(MAX)} + V_f}{V_{IN(MIN)}} \times \left(1 + \frac{33\%}{2}\right) = \frac{15\ W}{13\ V} \times \left(1 + \frac{33\%}{2}\right) = 2.91\ A \quad (15)$$

$$I_{L(SEC)} = I_{OUT(MAX)} \times \left(1 + \frac{33\%}{2}\right) = 1 \times \left(1 + \frac{33\%}{2}\right) = 1.165\ A \quad (16)$$

$$I_{L(PEAK)} = I_{L(PRIM)} + I_{L(SEC)} = 2.91 + 1.165 = 4.075\ A \quad (17)$$

Set the current limit and inductor saturation current rating 30% above 4.075 A for transient and efficiency loss. Use an inductor with a minimum current rating of 5.3 A.

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2.6.1.10 Calculating Coupled SEPIC R_{IS} (R38)

Due to the relatively high peak switch currents in this design, the equation based on current limit results in a lower value. A $VI_{IS(LIMIT)}$ value of 120 mV is used both for high current demand during load switching and input transient and for power dissipation purposes. Find the value using 式 9:

$$R_{IS} = \frac{V_{IS(LIMIT)}}{I_{L(PEAK)}} = \frac{0.120}{4.075} = 0.029\,\Omega \tag{18}$$

For this design, a value of 0.03 Ω is selected for R38.

2.6.1.11 Setting the LED Current

To lower the current sense resistor power dissipation and still keep a potential analog dimming range, the current sense resistor value (R2) can be calculated using 式 19:

$$R_{CS} = \frac{V_{IADJ(MAX)}}{14 \times I_{LED(MAX)}} = \frac{2.1}{14 \times 1.3} = 0.115\,\Omega \tag{19}$$

A 0.1-Ω resistor is chosen.

2.6.1.12 Main N-Channel MOSFET Selection

The main switching FET (Q2) needs to be able to stand off the input voltage plus the output voltage, even during output OVP events. This FET must also have a sufficient current rating for this application. The minimum transistor voltage and current rating can be calculated using the following equations:

$$V_{DS} < V_{O(OV)} \times 1.1 = 62 \times 11 = 69.2\,V \tag{20}$$

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} \times \sqrt{\left(\frac{V_{OUT(MAX)}}{V_{O(MAX)} + V_{IN(MIN)}} \right)} = \frac{45}{6} \times \sqrt{\frac{40}{40+6}} = 7\,A \tag{21}$$

An 80-V, D2PAK Q-grade FET is chosen for the switching FET (Q3). This FET is chosen for low gate charge along with a good thermal dissipation package.

2.6.1.13 Thermal Protection

Internal thermal protection circuitry protects the controller in the event of exceeding the maximum junction temperature. At 175°C, the converter typically shuts down, thus protecting the TPS92682 circuitry in the reference design. In addition, the design monitors temperature inputs to the microcontroller from board temperature, HB/LB temperature, and DRL/POS temperature. If the temperature on the board is above 100°C then the microcontroller will start issuing a lower PWM dimming duty cycle for the output current of both power stages to limit the heat dissipation. If temperature feedback from the HB/LB is above 100°C the microcontroller will start PWM dimming the output current to HB/LB to lower the effective power for thermal fold-back. The same is done with DRL/POS. The maximum junction temperature is a function of the system operating points (that is, efficiency, ambient temperature, and thermal management), component choices, and switching frequency. The example of this design, along with the microcontroller give the end-user flexibility when there are different thermal fold-backs and break points.

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2.6.2 Designing for Low EMI

2.6.2.1 EMI Performance

図 8 shows the passing conducted EMI scan for this design at a nominal 13-V input voltage. This is done with HB at 1.2 A while the DRL is at 1 A and the output power is 45 W and 15 W, respectively. The blue trace is the peak scan, and the line labeled C25Px denotes the peak limits for CISPR-25 Class 5. The black trace is the average scan. The scan covers the entire conducted frequency range from 150 kHz to 108 MHz.

This performance is with full shielding, see 図 7. This pre-compliance test scan is used for engineering development and evaluation and is not a certified EMI test result. If an official EMI test result is required, it is the responsibility of the end-user to submit any design based on this reference design to a certified EMI lab.

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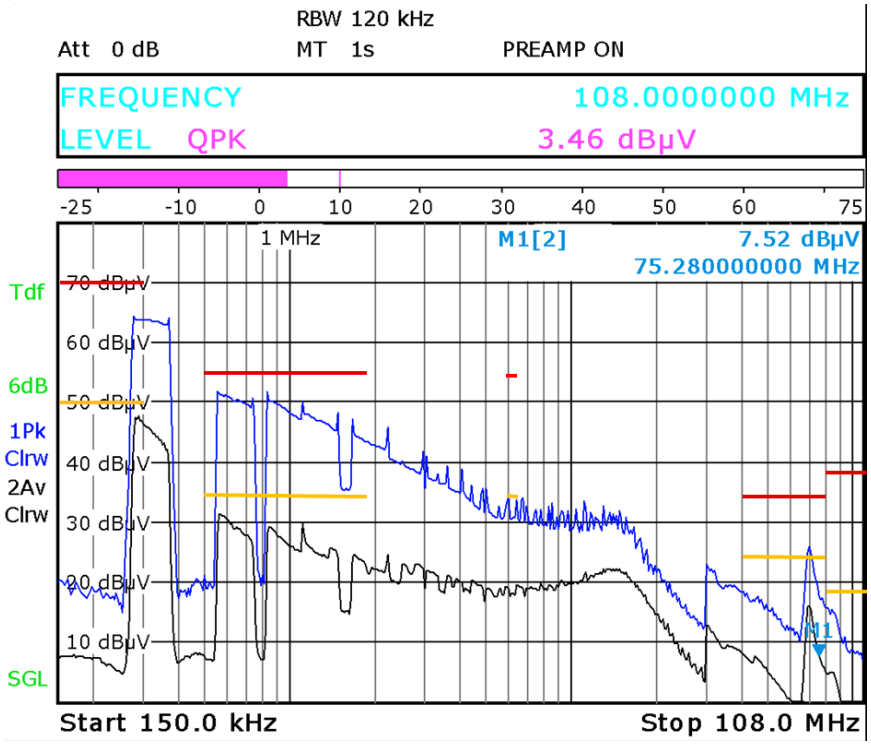
図 7. Shielding or Housing is Required on Switching Components to Pass CISPR-25 Class 5 Conducted EMI

図 8. CISPR-25 Class 5 Conducted EMI Scan (C25Px: Peak Limits, C25Ax: Average Limits) V_{IN} = 13 V, $V_{HB/LB}$ = 37 V, I_{LED} = 1.2 A, $V_{DRL/POS}$ = 15 V, I_{LED} = 1 A (Pre-Compliance Data)



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2.6.2.2 EMI Filter Design

The input EMI filter consists of a PI filter formed by the input capacitors (C42, C43, C44, and C41) and the input inductor (L1). The primary purpose of the filter is to minimize EMI conducted from the circuit to prevent it from interfering with the electrical network supplying power to the LED driver. Frequencies in and around the switching frequency of the LED driver (fundamental and harmonics) are primarily addressed with this filter, and the filter cutoff frequency is determined by the inductor and capacitor resonance. An input ferrite filter (L15) is also included to reduce high-frequency noise at 10 MHz and above.

Sufficient differential mode noise filtering on the output is generally provided by the output capacitor assuming low equivalent-series-resistance (ESR) ceramics are used as in this reference design for CISPR-25 class 5 conducted limits. A common-mode filter has also been added to the output (L4) to account for high frequencies with unknown loads. This filtering may not be required in an end application depending on the load. This LED driver was designed with the assumption that a connection to chassis ground is not available.

For more information on EMI filter design, see the application notes *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* and *Input Filter Design for Switching Power Supplies*.

2.6.2.2.1 Additional EMI Considerations

- Higher power levels may likely require increased EMI filtering to pass CISPR-25 class 5 limits. For lower power levels, EMI filtering can also be reduced for cost reduction.
- Options include increasing input capacitance or output capacitance (or both), adding ferrite bead resistance to mitigate high-frequency EMI, or include input chokes for common-mode noise reduction

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This reference design requires software and hardware from the host to communicate through the CAN interface. The CAN interface is used to command the module to enable the HB/LB and DRL/POS. The CAN interface also has the ability to communicate with the TPS92682 device to change any internal settings.

The register of the TPS92682 device is initialized with the following values at initial power up:

図 9. TPS92682 Register Setting

```
readWriteSPI(1, 0x01, 0x00, 0);
readWriteSPI(1, 0x02, 0x00, 0);
readWriteSPI(1, 0x03, 0x00, 0);
readWriteSPI(1, 0x04, 0x22, 0);
readWriteSPI(1, 0x05, 0x34, 0);
readWriteSPI(1, 0x06, 0xFF, 0);
readWriteSPI(1, 0x07, 0x90, 0);
readWriteSPI(1, 0x08, 0xB4, 0);
readWriteSPI(1, 0x09, 0x01, 0);
readWriteSPI(1, 0x0B, 0x03, 0);
readWriteSPI(1, 0x0A, 0xFF, 0);
readWriteSPI(1, 0x0D, 0x03, 0);
readWriteSPI(1, 0x0C, 0xFF, 0);
readWriteSPI(1, 0x0E, 0x0F, 0);
readWriteSPI(1, 0x0F, 0x0A, 0);
readWriteSPI(1, 0x10, 0x99, 0);
readWriteSPI(1, 0x13, 0x3C, 0);
readWriteSPI(1, 0x14, 0x0F, 0);
readWriteSPI(1, 0x15, 0x00, 0);
readWriteSPI(1, 0x16, 0x22, 0);
readWriteSPI(1, 0x17, 0x3C, 0);
readWriteSPI(1, 0x18, 0x00, 0);
readWriteSPI(1, 0x19, 0x00, 0);
readWriteSPI(1, 0x1A, 0x00, 0);
readWriteSPI(1, 0x1B, 0x00, 0);
readWriteSPI(1, 0x1C, 0x00, 0);
readWriteSPI(1, 0x1D, 0x00, 0);
readWriteSPI(1, 0x1E, 0x0F, 0);
readWriteSPI(1, 0x1F, 0x0A, 0);
readWriteSPI(1, 0x20, 0x99, 0);
readWriteSPI(1, 0x21, 0x3C, 0);
readWriteSPI(1, 0x22, 0x0F, 0);
readWriteSPI(1, 0x23, 0x00, 0);
readWriteSPI(1, 0x24, 0x22, 0);
readWriteSPI(1, 0x25, 0x00, 0);
```


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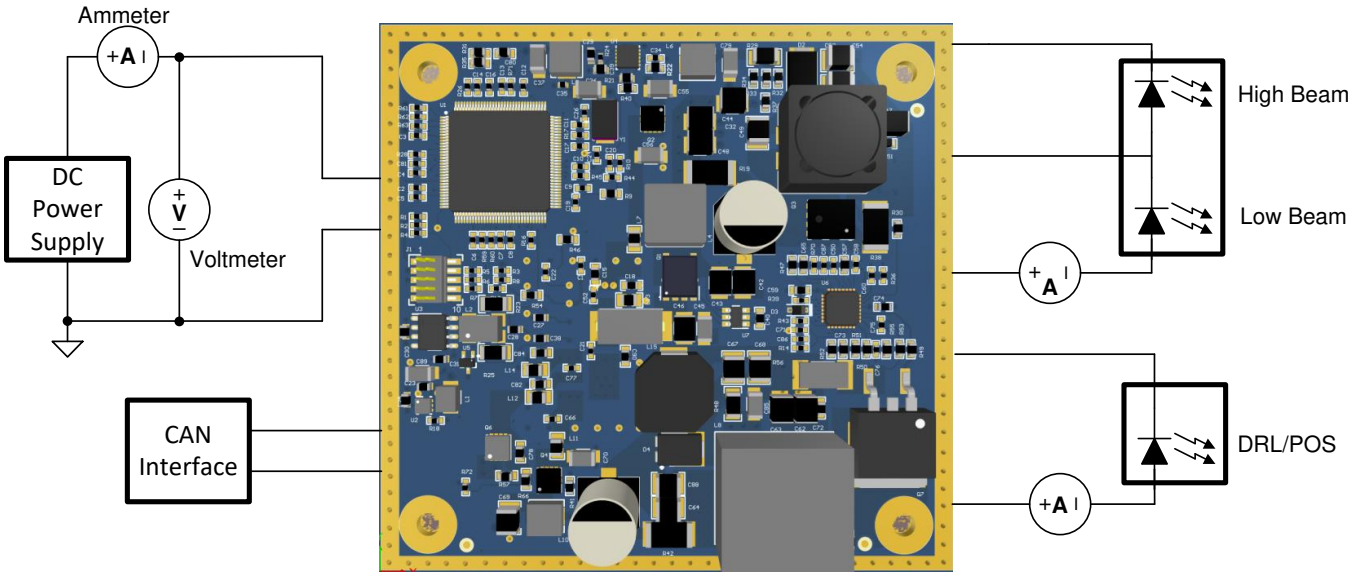
3.1.1 Hardware

3.2 Testing and Results

3.2.1 Test Setup

図 9 shows the test setup. The input voltage was supplied by a DC power supply connected to the connector J2. The LED loads are connected to the board also using the J2 connector. Four digital multimeters (DMMs), scope probes, or current probes measure input voltage, input current, output voltage, and output current.

図 10. Test Setup Connections



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3.2.2 Test Results

The test setup described in 図 9 generates the following data for efficiency, analog dimming, and PWM dimming measurements.

Unless otherwise noted, these conditions apply to 図 11 through 図 27.

- V_{IN} = 13 V
- Number of LEDs for high beam: 6
- Number of LEDs for low beam: 6
- HB/LB: I_{LED} = 1.2 A
- Number of LEDs DRL/POS: 5
- HB/LB: I_{LED} = 1 A

3.2.2.1 Nominal Operation Waveforms

図 11. Soft-Start Into Normal Operation

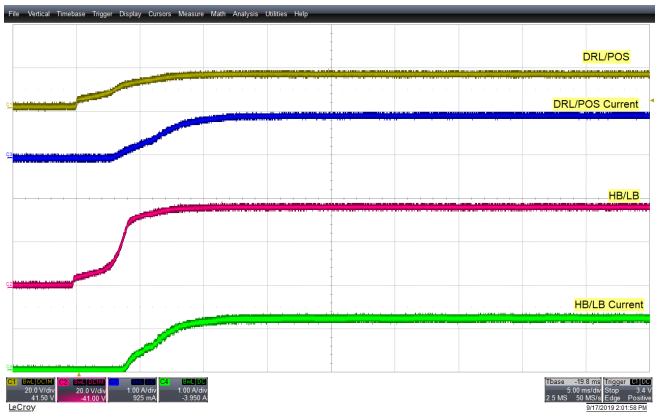

図 12. High Beam to Low Beam Transition

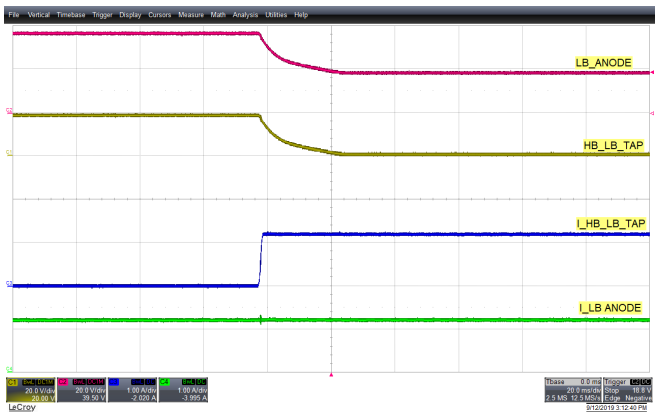

図 13. Low Beam to High Beam Transition

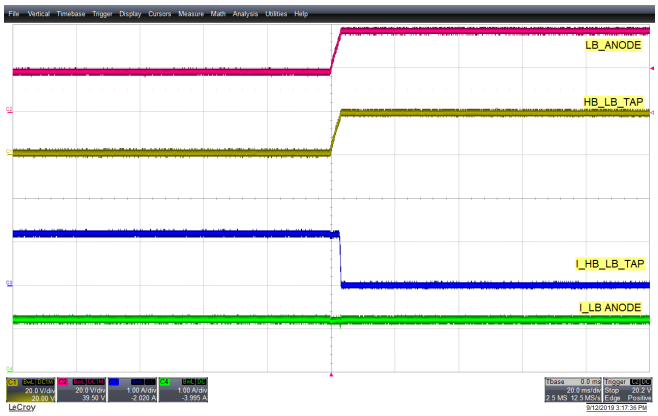

図 14. DRL to POS Transition

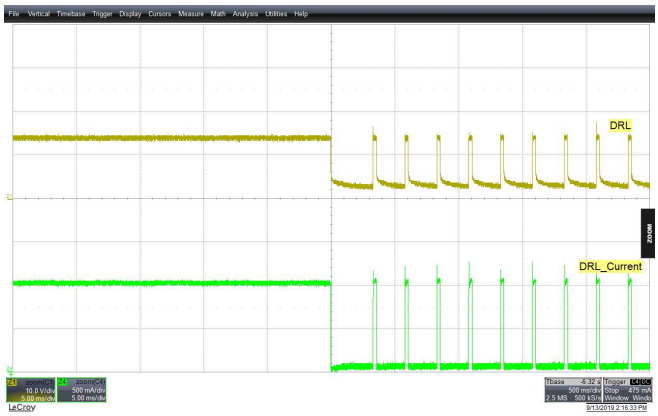

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図 15. POS to DRL Transition

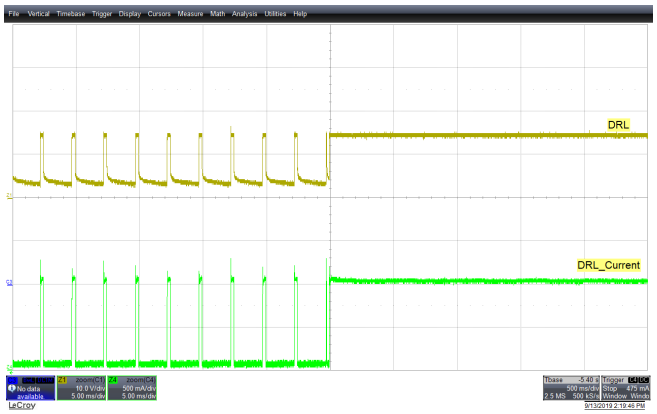

図 16. 90% PWM'ing at High Power

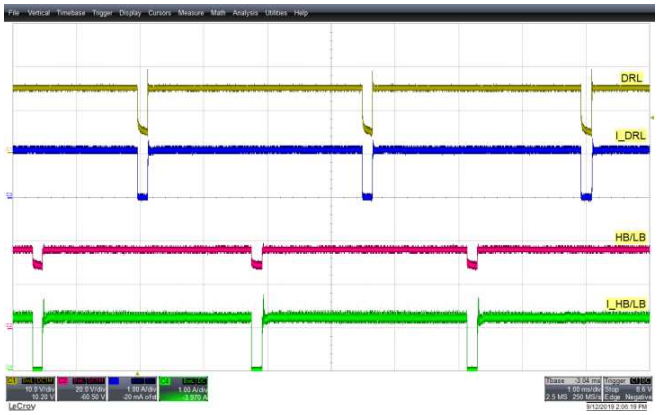

図 17. 50% PWM'ing at High Power

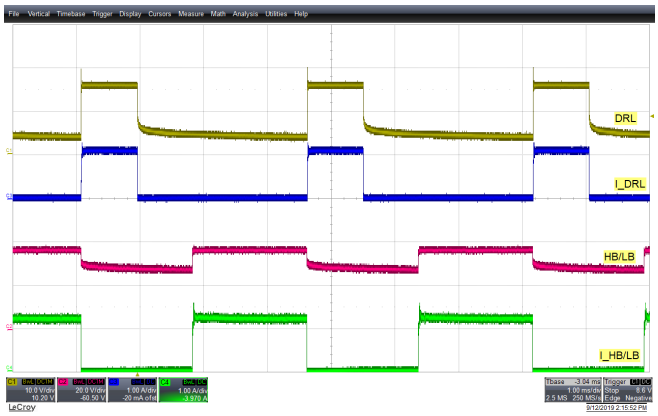

図 18. 10% PWM'ing at High Power

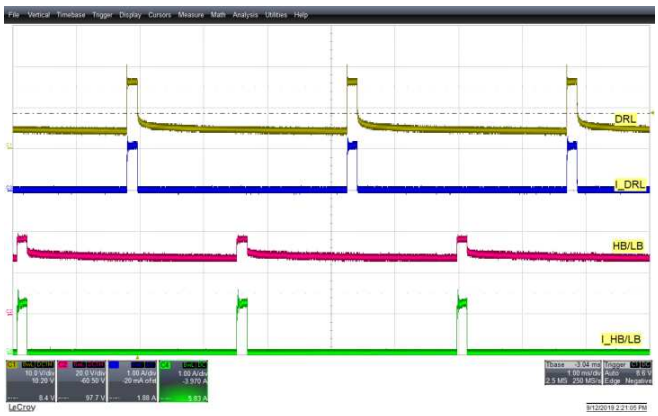

図 19. 90% PWM'ing at Low Power

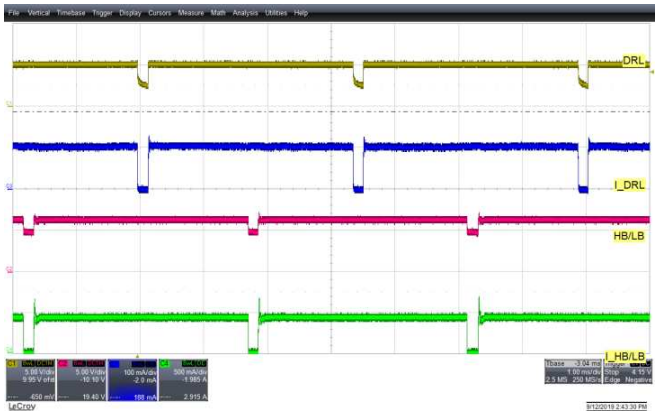

図 20. 50% PWM'ing at Low Power

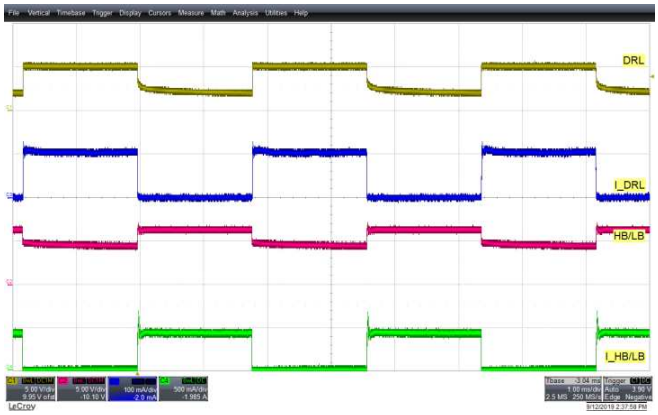

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図 21. 10% PWM'ing at Low Power

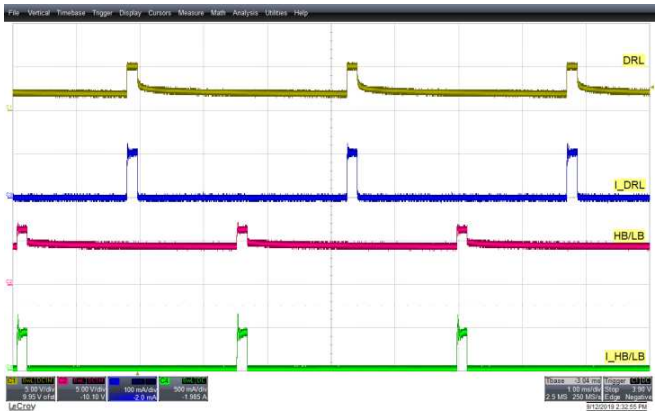

図 22. High Power Warm-Crank

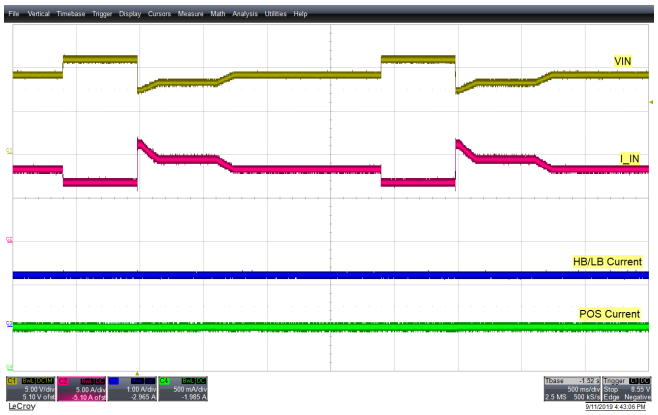

図 23. Low Power Warm Crank

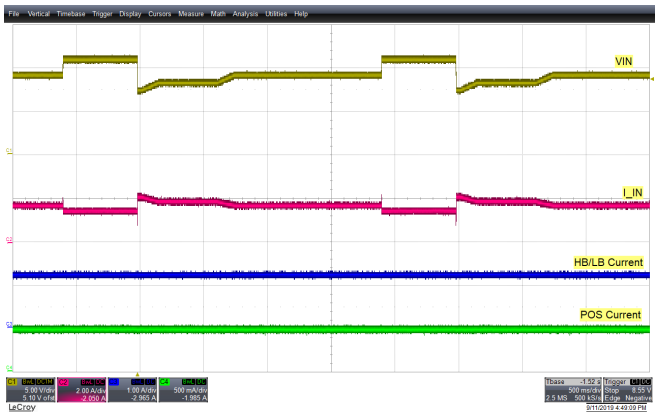

図 24. DRL/POS Open Protection

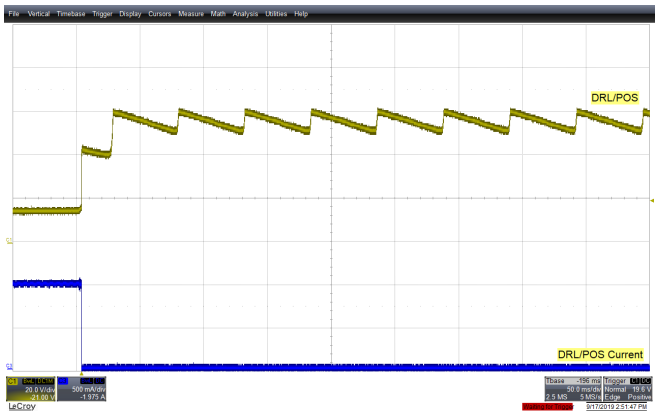

図 25. DRL/POS Short Protection

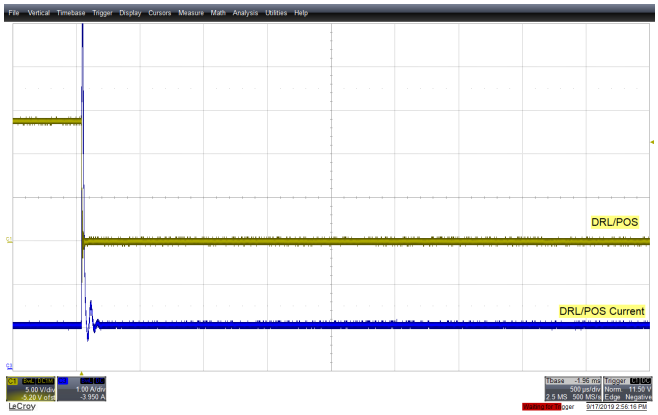

図 26. High Beam and Low Beam Open Protection

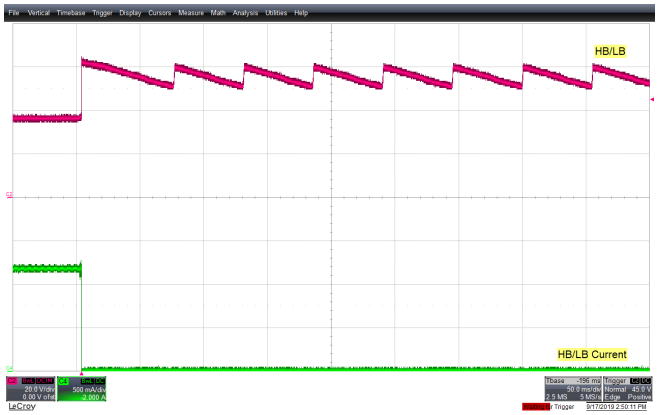

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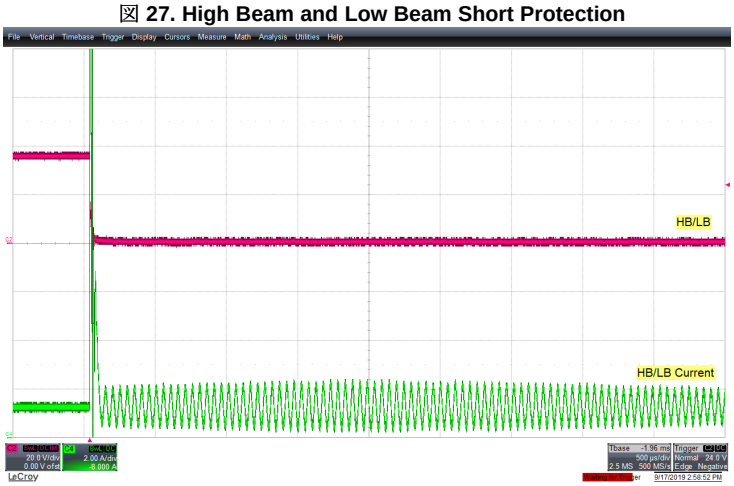
図 27. High Beam and Low Beam Short Protection



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3.2.2.2 Efficiency: Done for Different Power Levels

図 28 through 図 31 illustrate efficiency graphs at different power levels. Note that the measurements are done considering only the power stage power while the microcontroller is disabled.

図 28. HB/LB (ILED = 1.2 A) Efficiency vs P_{OUT} (W)

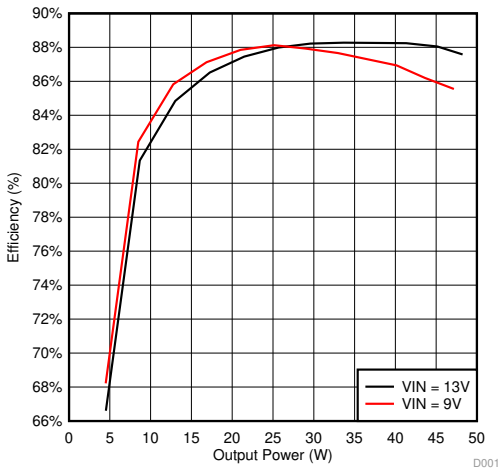


図 29. DRL (ILED = 1 A) Efficiency vs P_{OUT} (W)

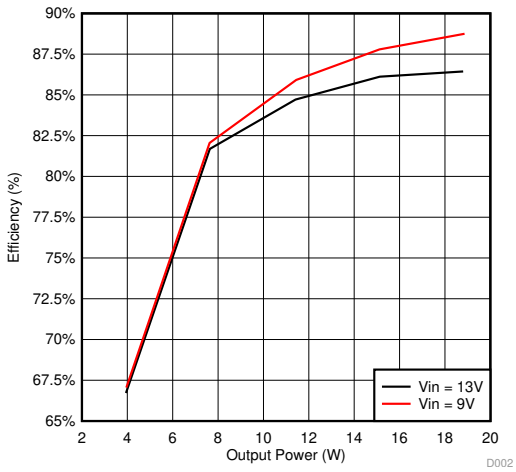


図 30. DRL (ILED = 0.5 A) Efficiency vs P_{OUT} (W)

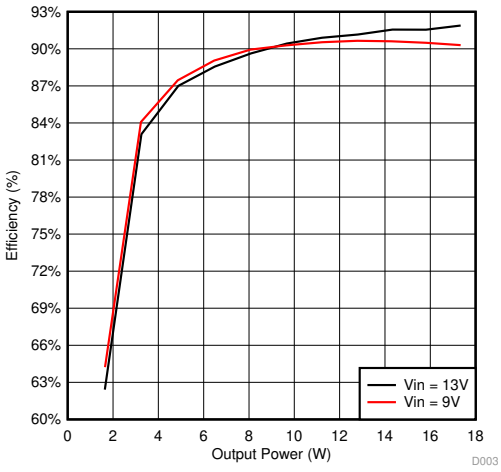
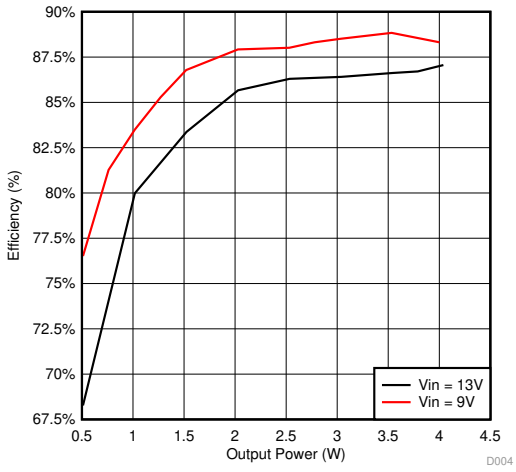


図 31. DRL (ILED = 0.1 A) Efficiency vs P_{OUT} (W)



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3.2.2.3 Thermal Scan

図 33 shows a thermal scan of the board running at room temperature (≈ 25°C) with no air flow. 表 2 lists the measured temperatures of key components.

図 32. Picture of Housing and Heatsink

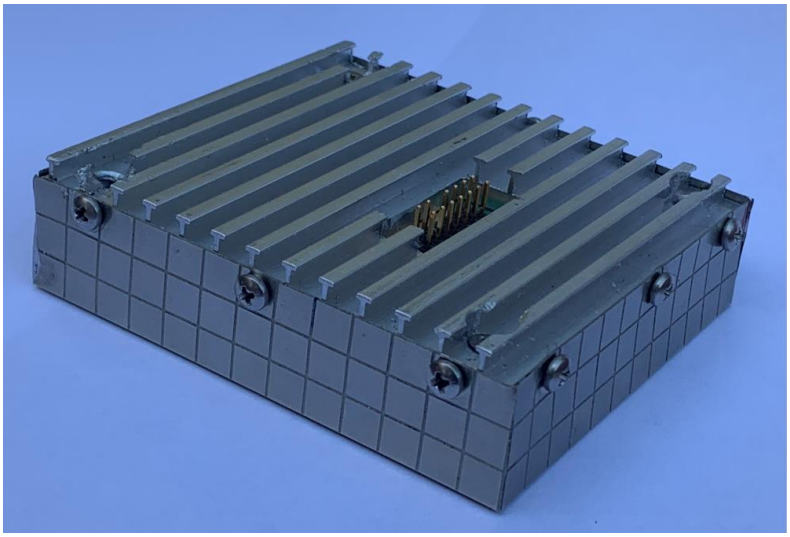

図 33. Thermal Scan With Heat Sink—Top-View (Power Components): V_{IN} = 13 V, HB/LB Mode (45 W), I_{LED} = 1.2 A

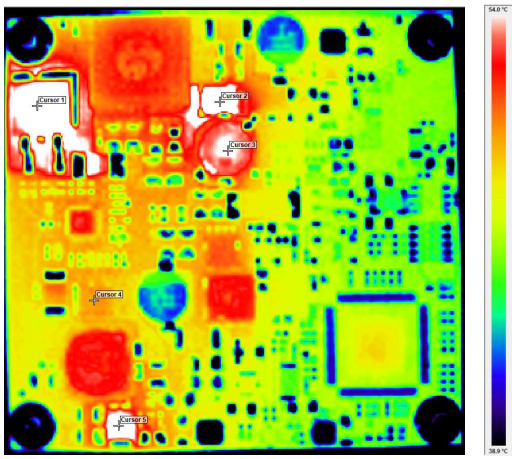

表 2. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	Q7	57.0
2	D4	59.0
3	L9	54.7
4	Q3	49.9
5	L5	55.9

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図 34 shows a thermal scan of the board running at an elevated temperature (≈ 70°C) with no air flow. 表 3 lists measured temperatures of key components.

図 34. Thermal Scan—Top-View (Power Components): V_{IN} = 13 V, HB/LB (45 W), DRL (15 W)

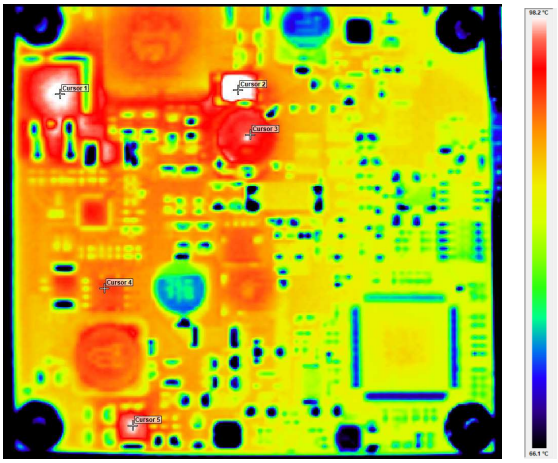

表 3. Component Temperatures

CURSOR	COMPONENT	TEMPERATURE (°C)
1	Q7	98.4
2	D4	100.7
3	L8	96.8
4	Q3	92.2
5	D2	97.5

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050029.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050029.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050029.

図 35. Top Layer

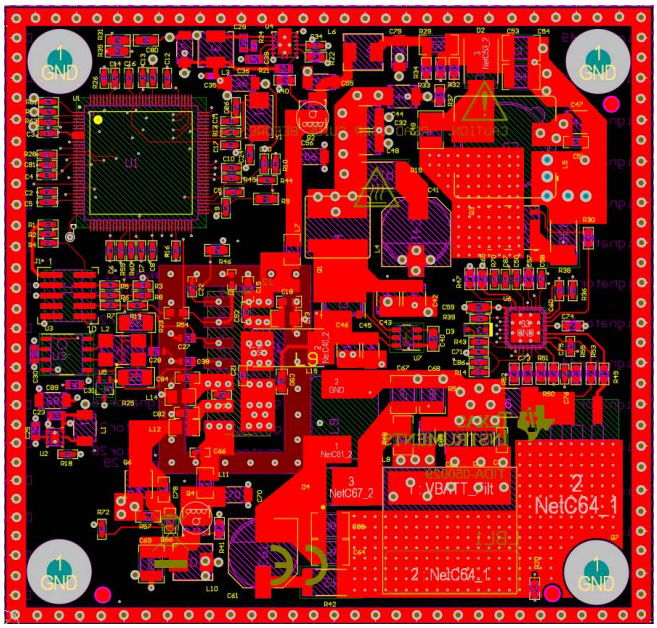
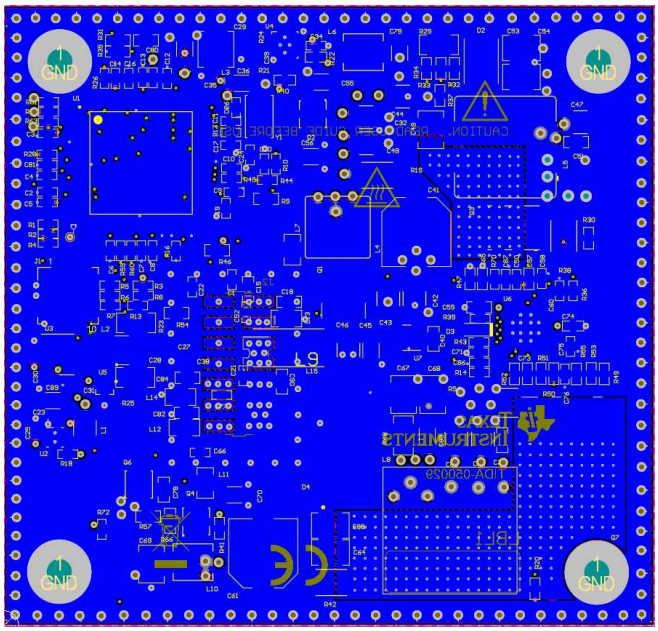


図 36. Bottom Layer



4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-050029.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050029.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050029.

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5 Related Documentation

1. Texas Instruments, *TPS92682-Q1 Dual-Channel Constant-Voltage and Constant-Current Controller With SPI*
2. Texas Instruments, *TPS92682EVM Constant Current Two-channel Boost And Boost-to-Battery User's Guide*
3. Texas Instruments, *TPS92682EVM-069 CV 2-Phase Boost Controller Evaluation Module User's Guide*

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