参考資料

デザイン・ガイド：TIDA-010070
低電圧サーボ・ドライブ向け保護機能搭載 DC バス入力電力 / 制御電源のリファレンス・デザイン

概要

このリファレンス・デザインは、低電圧 DC サーボ・ドライブ用の保護機能搭載 DC バス電源を示しています。このデザインは、OR コントローラである LM5050-1 を使用して、逆極性と逆電流に対する保護を実現しています。さらに、過電流、過電圧、低電圧に対する保護と、突入電流の制限を目的として、ホット・スワップ・コントローラ LM5069 も組み合わせて使用しています。また、ゲート・ドライバ、エンコーダ、マイコン (MCU) などの制御系電子回路用に、複数の電源レールを搭載しています。

リソース

TIDA-010070	デザイン・フォルダ
LM5050-1	プロダクト・フォルダ
LM5069	プロダクト・フォルダ
LM5164	プロダクト・フォルダ
TPS560430	プロダクト・フォルダ
TPS22919	プロダクト・フォルダ
LP38691	プロダクト・フォルダ
TPS2121	プロダクト・フォルダ
TPS26624	プロダクト・フォルダ

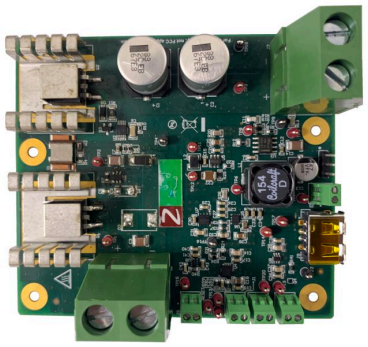
E2E™エキスパートに質問

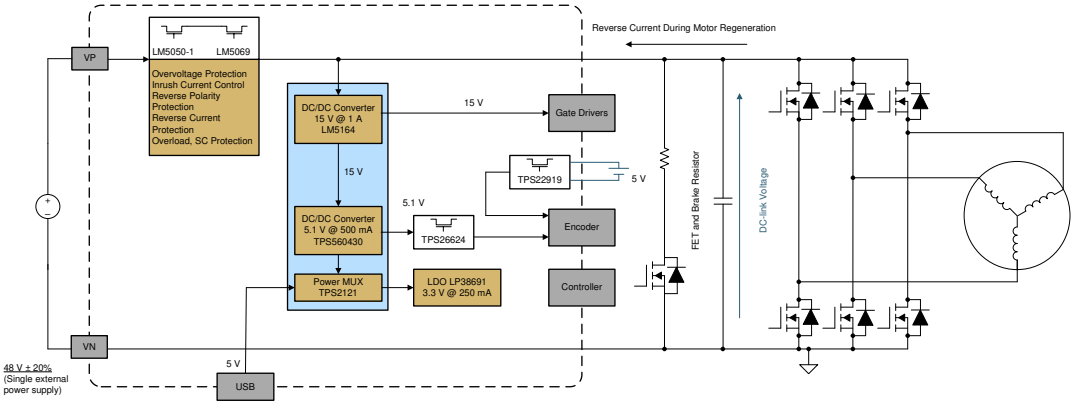
特長

- 過電圧、逆極性、過電流、突入電流から DC バス電圧を保護
- モーターのブレーキ (制動) 時に逆電流が DC バス電圧ラインに逆流することを防止
- DC リンク (公称 48V) で最大 100V の過渡耐性
- DC バス入力が存在しない構成で USB を使用して MCU に電力を供給するオプション
- (DC バスと外部バックアップ・バッテリ両方の) 短絡障害からエンコーダの電圧ラインを保護

アプリケーション

- サーボ CNC とロボット
- ブラシレス DC ドライブ

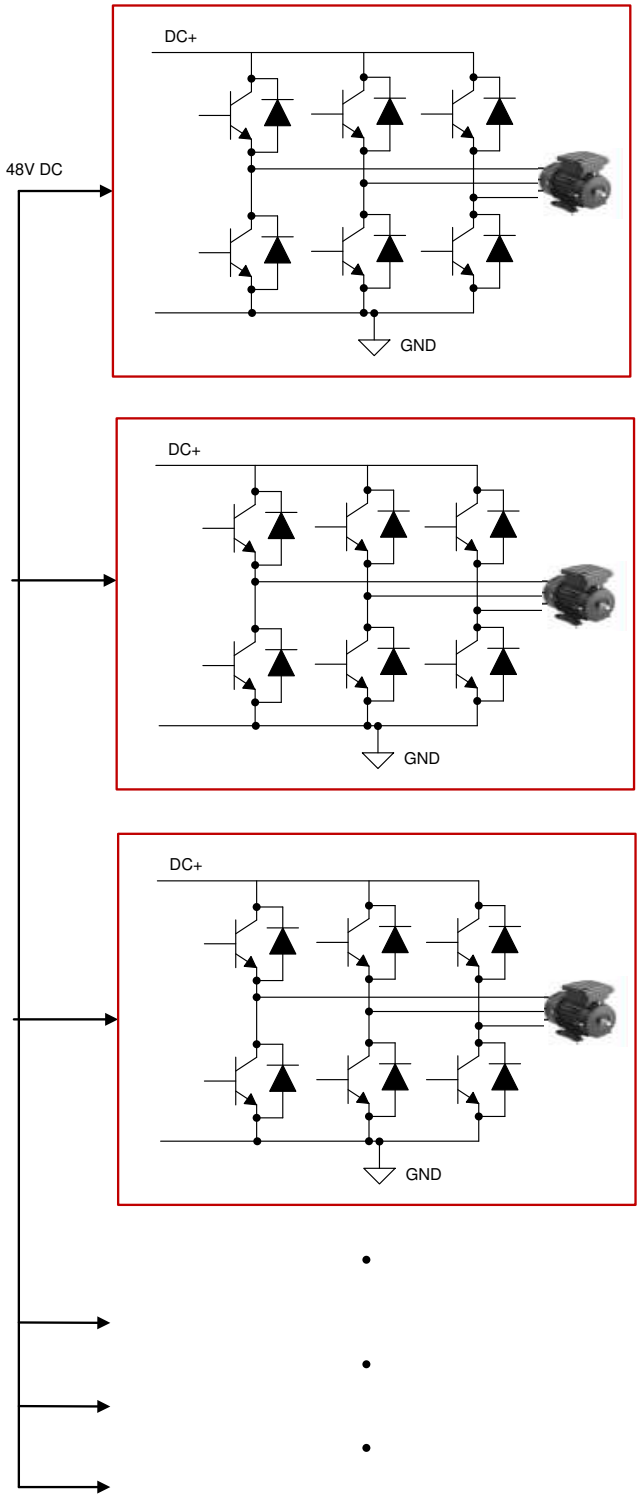




1 System Description

Servo drives consist of a power stage, controller, position sensor and feedback, analog and digital I/Os, communication module, and display. Multiple voltage rails are required for the operation of all the control electronics in the drive which can be generated from the DC link voltage as 図 1 shows.

図 1. System Block Diagram



When the control electronics are getting powered up by the DC link voltage, its protection from unwanted conditions become desirable. Input reverse polarity, reverse current flow, overvoltage, undervoltage, overcurrent on the DC link voltage, and so forth, are some of the undesirable situations that cause the control electronics to fail. The power supply for the control electronics should also be compact, cost effective, and efficient. In a servo drive, the control electronics power supply can be further classified into the following categories:

1. Gate drive power supply – The three-phase inverters use semiconductor switches (IGBT, MOSFET, SiC) to convert the DC bus voltage to three-phase AC voltage with adjustable magnitude and frequency depending on the application. The fundamental frequency of the three-phase output generated by the inverter is controlled by the PWM signals generated by the MCU and driven by the gate drivers. A 15-V supply voltage is often used for powering up the gate drivers.
2. Encoder power supply – Various position encoders are available for industrial applications from different vendors with vendor-specific or open-source interface standards. The supply voltage range is encoder-specific and typically depends on the analog and digital interface standard it supports. Encoders with TTL or analog Sin/Cos interface are typically offered with a 5-V input.
3. MCU power supply – A continuous and regulated supply voltage for the MCU is extremely crucial in any system. The MCU should remain active even if the bus voltage shuts off in case of an undesirable event. This design uses dual-channel architecture for supplying power to the MCU. The stepped down voltage from the DC bus and the external USB supply are combined using power MUX to automatically provide a seamless transition.

1.1 Key System Specifications

表 1 describes the system specifications.

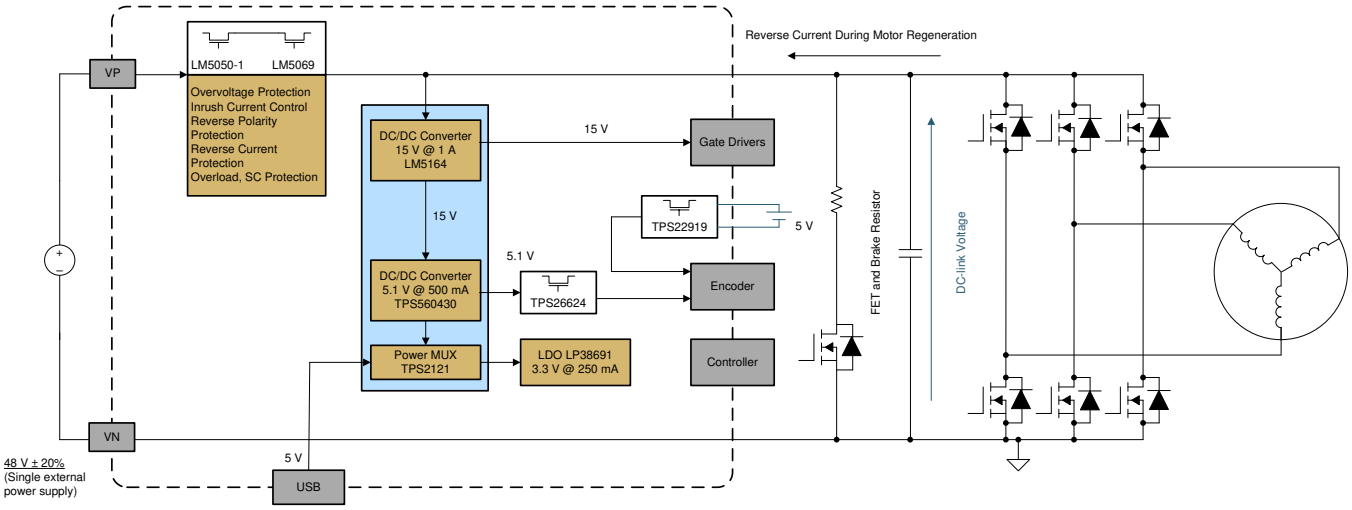
表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
DC input motor supply	48 VDC
DC input overvoltage threshold	60 VDC
DC input undervoltage threshold	36 VDC
DC link voltage (continuous)	70 VDC
DC input current	20 A
Inrush current limit	23 A
Protections	Reverse polarity at input, reverse current from output, overvoltage and undervoltage, overcurrent, inrush current
Logic supply	Non-isolated 15 V for gate drivers (2% regulation); 5 V for encoders (current limit at 250 mA); 3.3 V for MCU (< 1% regulation)
Provision	Powering MCU using USB and encoder, using external battery if DC bus is powered down

2 System Overview

2.1 Block Diagram

図 2. TIDA-010070 Block Diagram



2.2 Design Considerations

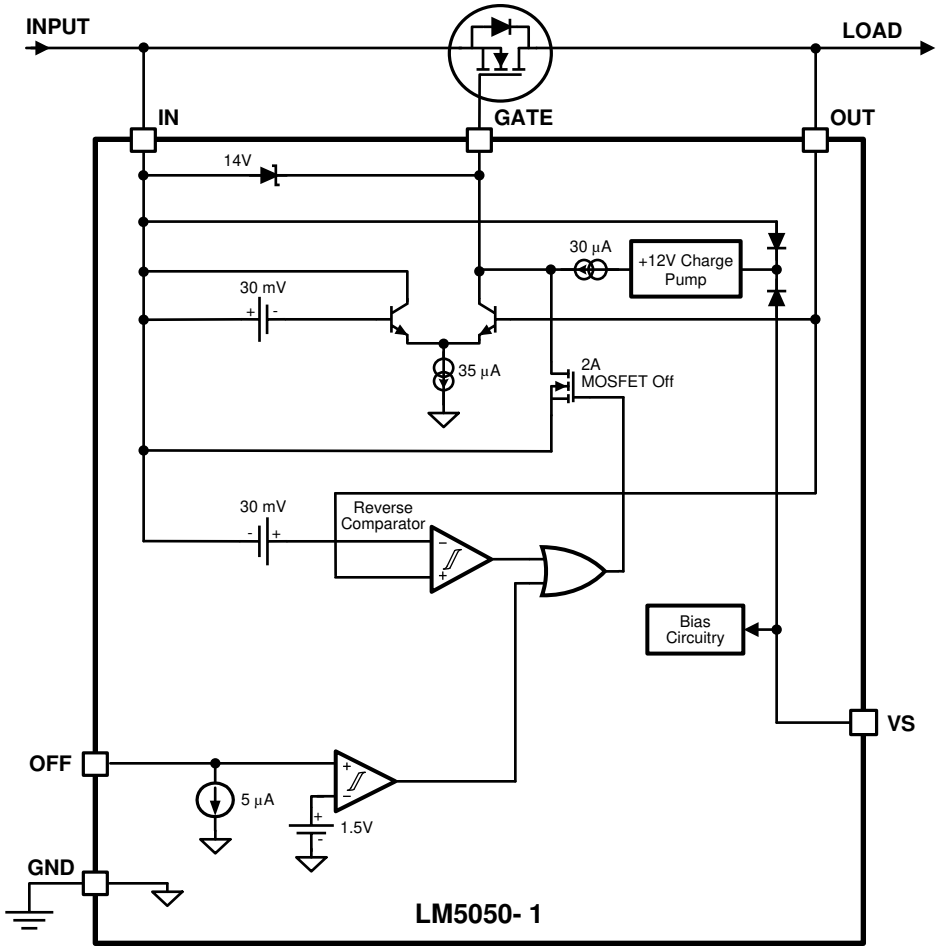
図 2 shows the block diagram of the TIDA-010070 design. This design is capable of operating at 48-V nominal input. The protection circuitry consists of the LM5050 and LM5069 devices. The 48-V input is fed through the MOSFETs controlled by the ORing controller LM5050 and hot swap controller LM5069. Further, this protected 48 V is available at the output for the inverter. The 48-V input is stepped down further to 15 V by the LM5164 device. This 15 V is available at the output for the gate drivers. The encoder supply typically requires 5 V, so the 15 V is further down-converted to 5 V using the TPS560430 device which is then provided to the eFuse TPS26624 device for protecting the encoder supply rail. Redundant supply on the encoder is needed so that the position information is not lost even if the DC link fails. This design resolves such situations and uses a secondary voltage source as battery followed by the TPS22919 load switch, to power the encoder. The USB provides the backup supply for the controller in case the 48-V mains fail. The 5-V USB is ORed with 5 V from DC link using the TPS2121 power MUX. The 5 V at the output of the TPS2121 device is further converted to 3.3 V using the LP38691 LDO to power the MCU.

2.3 Highlighted Products

2.3.1 LM5050-1

The LM5050-1 high-side ORing FET controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

図 3. LM5050-1 Functional Block Diagram



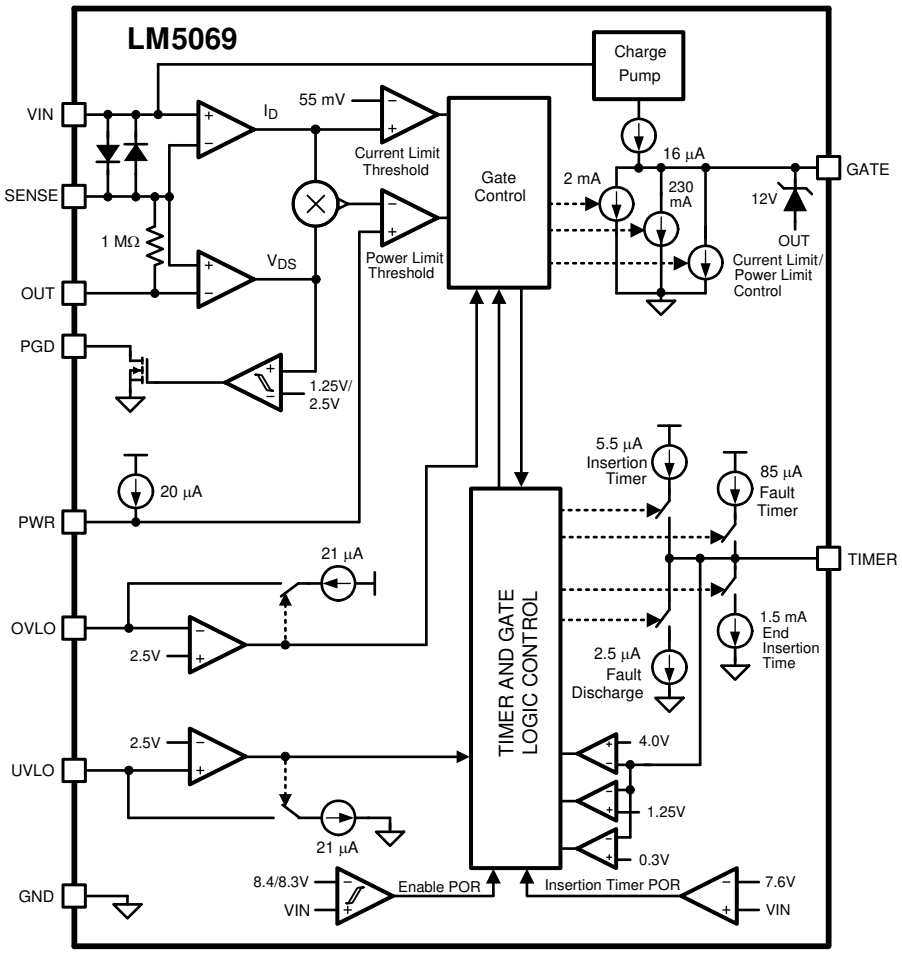
The LM5050-1 device in the current design aids in the input reverse polarity protection and reverse current blocking from the load. If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5050-1 IN and OUT pins is more negative than the VSD (REV) voltage of –28 mV (typical), the LM5050-1 will quickly discharge the MOSFET gate through a strong GATE to IN pin discharge transistor.

2.3.2 LM5069

The LM5069 positive hot swap controller provides intelligent control of the power supply connections during insertion and removal of circuit cards from a live system backplane or other hot power sources. The LM5069 device provides in-rush current control to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-channel MOSFET are programmable, ensuring operation within the Safe Operating Area (SOA). The Power Good output indicates when the output voltage is within 1.25 V of the input voltage. The input undervoltage and overvoltage lockout levels and hysteresis are programmable, as well as the initial insertion delay time and fault detection time.

The features of inrush current control, undervoltage lockout (UVLO) and overvoltage lockout (OVLO) of the LM5069 controller are used in the current design for the protection. The UVLO and OVLO are set through the resistor divider networks and inrush current limit is employed with the help of a shunt resistor. The dv/dt startup is used to turn on the MOSFET in SOA.

図 4. LM5069 Functional Block Diagram

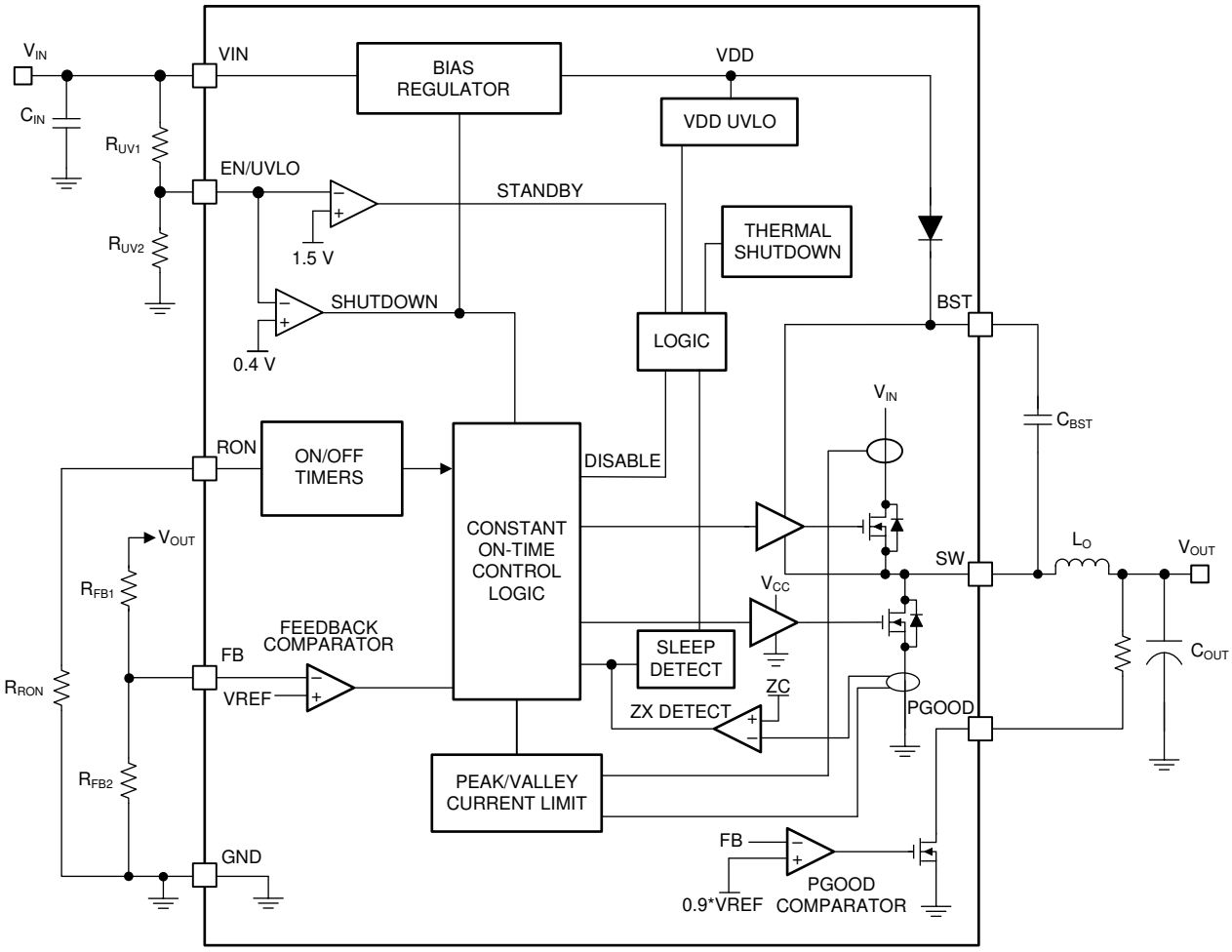


2.3.3 LM5164

The LM5164 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge-suppression components. A minimum controllable on-time of 50 ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48-V nominal input to low-voltage rails for reduced system complexity and solution cost. The LM5164 operates during input voltage dips as low as 6 V, at nearly 100% duty cycle if needed, making it an excellent choice for wide input supply range industrial applications.

The need for wide input comes from the fact that during motor braking the DC-link line can go high up to 80 V, so to accommodate that variation, wide-V_{IN} DC/DC converter is used. With integrated high-side and low-side power MOSFETs, the LM5164 converter delivers up to 1 A of output current. Constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. In the current design, the LM5164 device steps down 48-V DC input to 15-V DC.

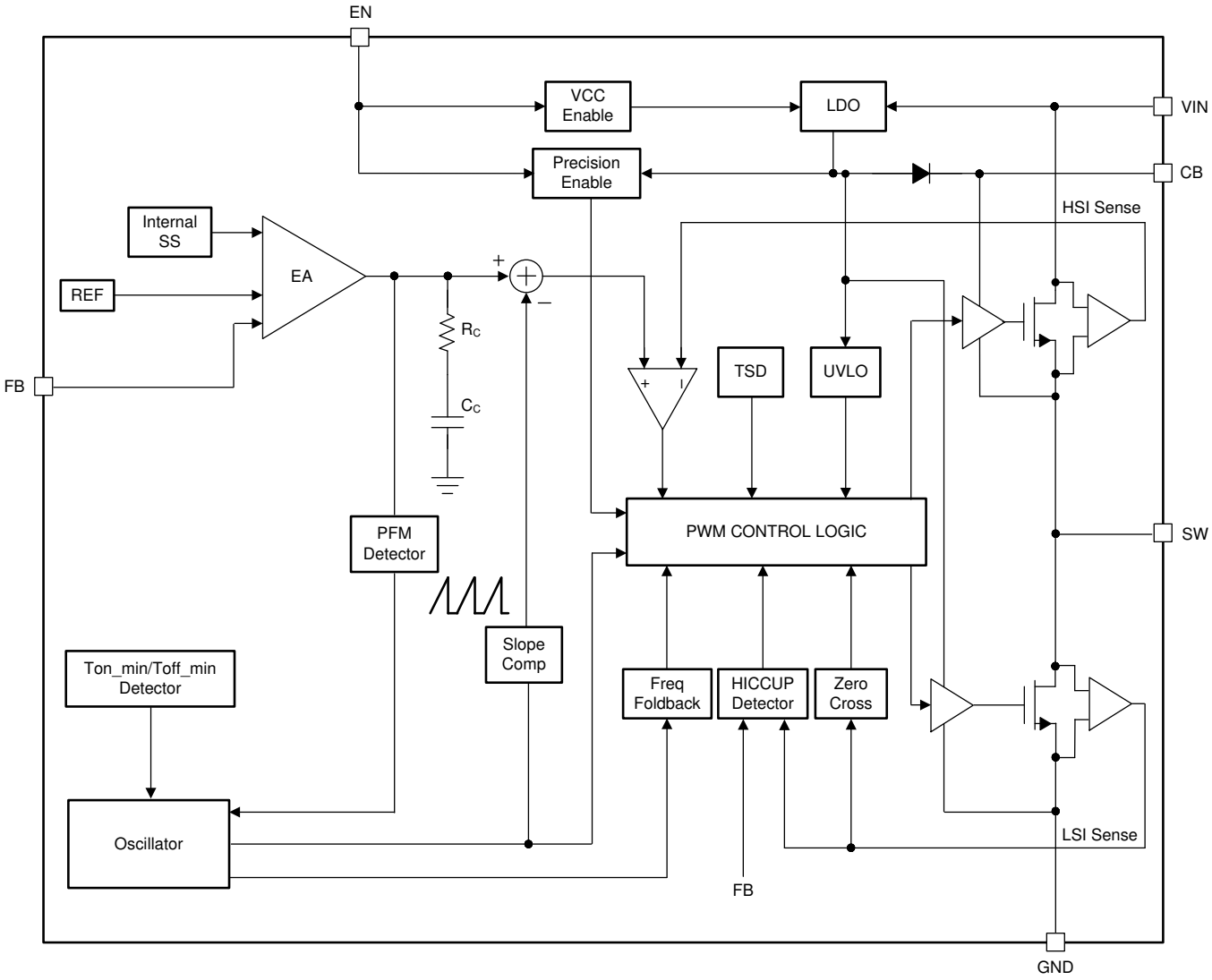
図 5. LM5164 Functional Block Diagram



2.3.4 TPS560430

The TPS560430 device is a synchronous step-down DC/DC converter capable of driving up to 600-mA load current. With a wide input range of 4 V to 36 V, the device is suitable for a wide range of applications from industrial to automotive for power conditioning from an unregulated source. The TPS560430 device has 1.1-MHz and 2.1-MHz operating frequency versions for either high efficiency or small solution size. The TPS560430 device also has a FPWM (forced PWM) version to achieve constant frequency and small output voltage ripple over the full load range. Soft-start and compensation circuits are implemented internally which allows the device to be used with minimum external components. In this design, the TPS560430 converter is used to generate 5-V output from 15-V input.

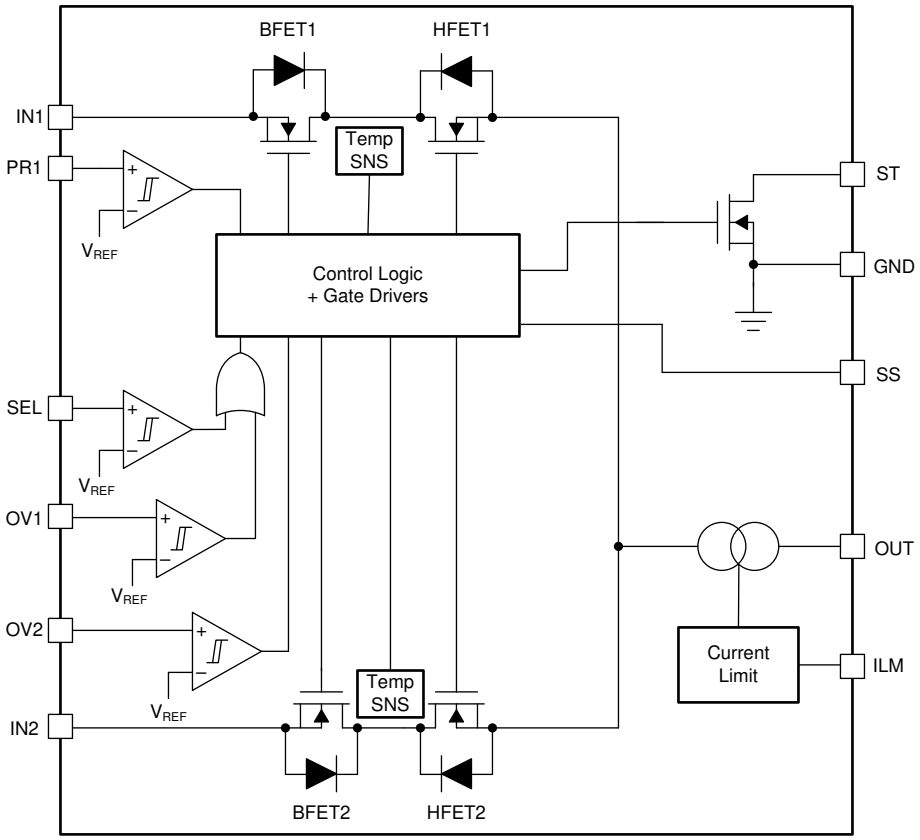
図 6. TPS560430 Functional Block Diagram



2.3.5 TPS2121

The TPS2121 device is a dual-input, single-output (DISO) power multiplexer (MUX) that is well suited for systems having multiple power sources. The device will automatically detect, select, and seamlessly transition between available inputs. Priority is automatically given to the highest input voltage or manually assigned to a lower voltage input to support both ORing and source selection operations. A priority voltage supervisor is used to select an input source. An ideal diode operation is used to seamlessly transition between input sources. During switchover, the voltage drop is controlled to block reverse current before it happens and provide an uninterrupted power to the load with minimal hold-up capacitance. Here the priority is set to the main DC link voltage, the output of the TPS2121 device is powered by 5 V from the TPS560430 converter until it falls below 4.5 V, then the USB 5 V takes over the output.

図 7. TPS2121 Functional Block Diagram

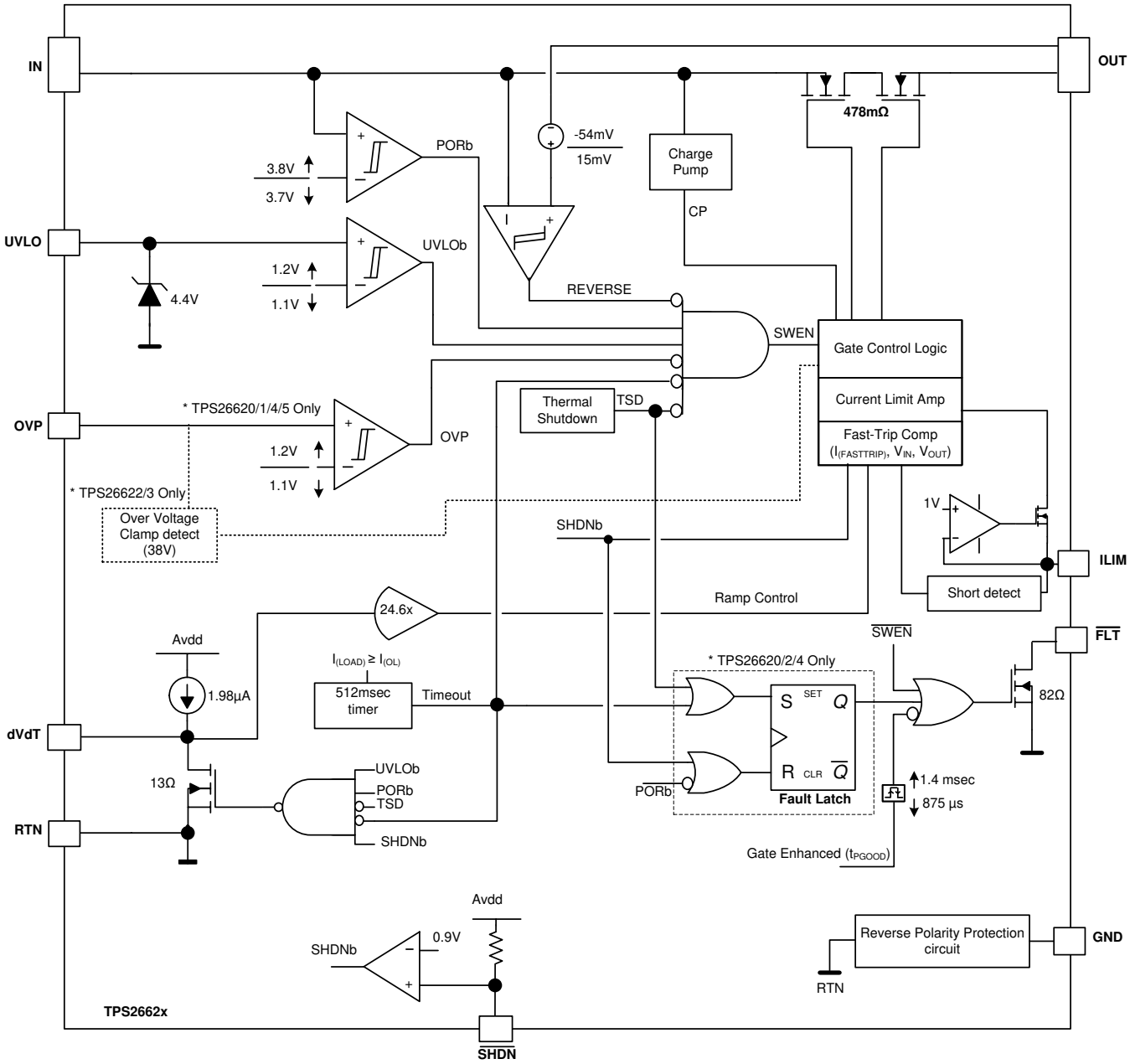


2.3.6 TPS26624

The TPS26624 device is high-voltage eFuse with protection features. The wide supply input range of 4.5 V to 57 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. The TPS26624 device has both an input and output reverse polarity protection feature. Integrated back-to-back FETs provide a reverse current blocking feature making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source, and device protection are provided with many adjustable features including overcurrent, output slew rate, and overvoltage, undervoltage thresholds.

The TPS26624 eFuse in the current design is used to protect the 5-V output encoder power supply for the miss-wire protection.

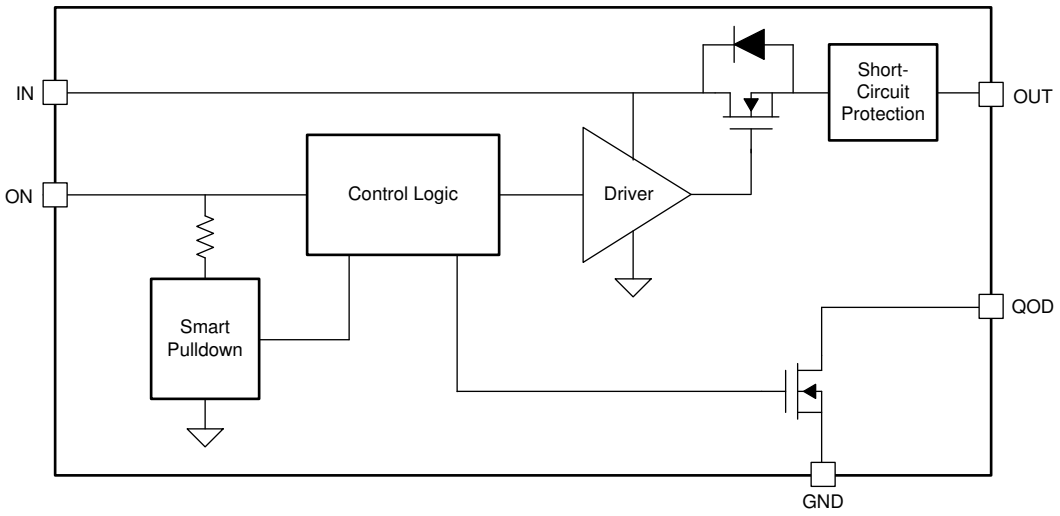
図 8. TPS26624 Functional Block Diagram



2.3.7 TPS22919

The TPS22919 device is a small, single-channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6 V to 5.5 V and can support a maximum continuous current of 1.5 A. The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a *Smart Pull Down* is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven high (> VIH), the *Smart Pull Down* will be disconnected to prevent unnecessary power loss. The TPS22919 switch is used to provide the protected encoder supply of 3.6 V from the battery. The device turns on only when the main DC link is disabled.

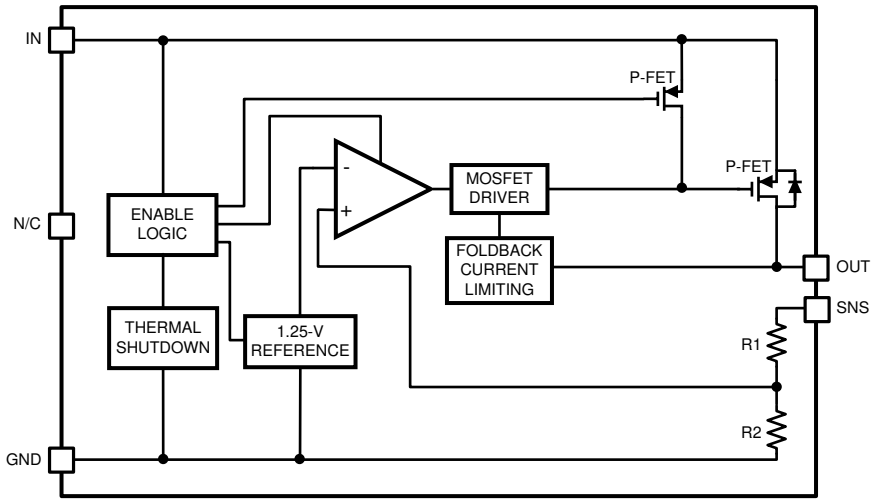
図 9. TPS22919 Functional Block Diagram



2.3.8 LP38691

The LP38691 device is a low-dropout CMOS linear regulator which provides tight output tolerance (2% typical), extremely low dropout voltage (250 mV at 500-mA load current, V_{OUT} = 5 V), and excellent AC performance using ultra-low equivalent series resistance (ESR) ceramic output capacitors. The LP38691 regulator is used to generate 3.3-V processor supply from the 5-V input.

図 10. LP38691 Functional Block Diagram



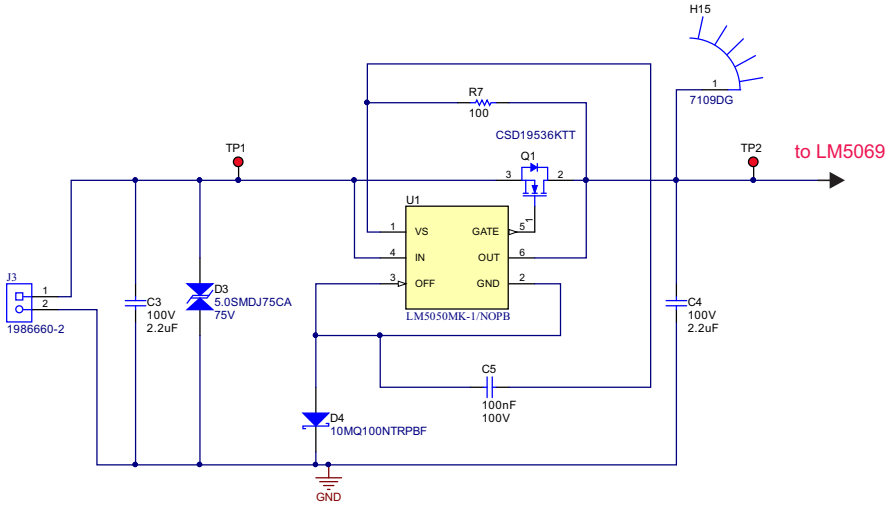
2.4 System Design Theory

2.4.1 Input Power Protection – LM5050-1 and LM5069

2.4.1.1 Reverse Current and Reverse-Polarity Protection

The LM5050-1 ORing controller with external FET provides the reverse current protection from output to input and also reverse polarity protection at the input as 図 11 shows.

図 11. LM5050-1 Schematic

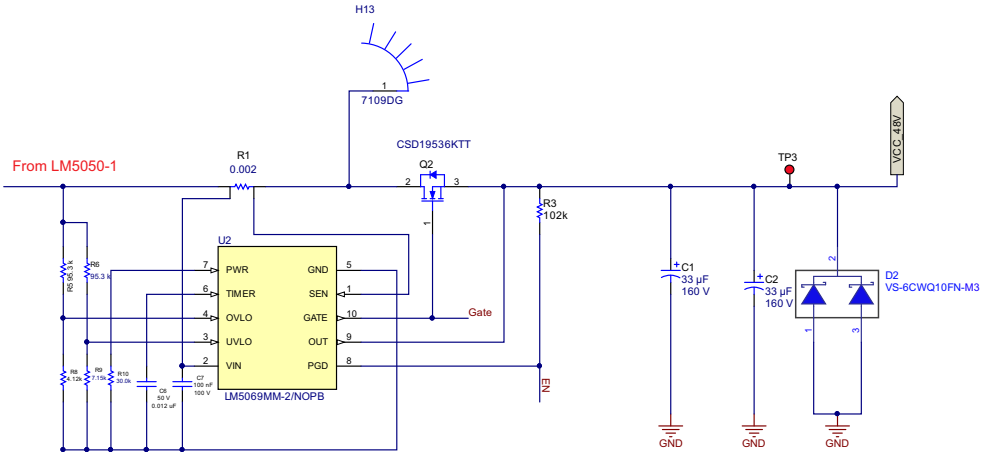


At the input, the TVS diode D3 provides the transient suppression for input voltages above the maximum recommended voltage at IN pin (75 V). The diode D4 placed between device ground and input ground aids in the protection of the devices from the reverse input voltage.

2.4.1.2 Setting up UVLO and OVLO at the Input

The UVLO and OVLO are set at the input of the LM5069 device as 図 12 shows. The UVLO and overvoltage trip points are set using an external voltage divider network.

図 12. LM5069 Schematic



The operating range at the input is from 36 V to 60 V. The upper OVLO threshold is 60 V with a hysteresis of 2 V. The lower UVLO threshold is 36 V with hysteresis of 2 V. Set the overvoltage threshold using 式 1 and 式 2. Set the undervoltage threshold by using 式 1 through 式 4.

$$R5 = \frac{V_{OVH} - V_{OVL}}{21\,\mu A} = \frac{60\ V - 58\ V}{21\,\mu A} = 95.3\ k\Omega \quad (1)$$

$$R8 = \frac{2.5\ V \times R5}{V_{OVH} - 2.5\ V} = \frac{2.5\ V \times 95.3\ k\Omega}{60\ V - 2.5\ V} = 4.12\ k\Omega \quad (2)$$

$$R6 = \frac{V_{UVH} - V_{UVL}}{21\,\mu A} = \frac{60\ V - 58\ V}{21\,\mu A} = 95.3\ k\Omega \quad (3)$$

$$R9 = \frac{2.5\ V \times R6}{V_{OVL} - 2.5\ V} = \frac{2.5\ V \times 95.3\ k\Omega}{36\ V - 2.5\ V} = 7.11\ k\Omega \quad (4)$$

Solving these equations gives R5 = 95.3 kΩ, R8 = 4.12 kΩ, R6 = 95.3 kΩ and R9 = 7.11 kΩ.

2.4.1.3 Input Current Limit

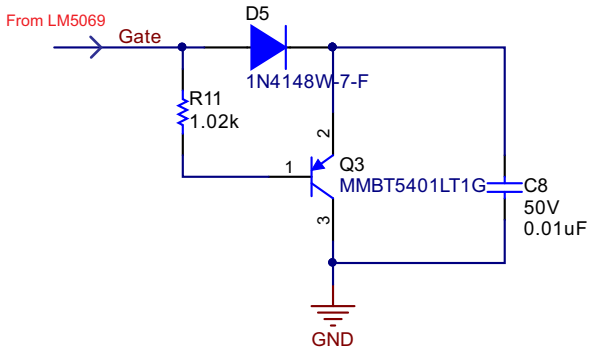
The input current limit is set through the LM5069 hotswap controller. The current limit threshold is reached when the voltage across the sense resistor R1 (VIN to SENSE) reaches 55 mV. Here, the input current limit is set to 23 A. RSENSE (R1) is calculated based on 式 5.

$$R1 = \frac{V_{CL}}{I_{LIM}} = \frac{55\ mV}{27\ A} = 0.002\ \Omega \quad (5)$$

Hence, sense resistor R1 is selected to be 2 mΩ.

2.4.1.4 Startup Based on dv/dt

図 13. Start up Based on dv/dt



To reduce the stress on the FET during the initial startup and operate it in the safe operating area during initial turn on, dv/dt start-up is employed. The V_{OUT} slew rate is set to 4 V/ms, based on this, C8 (Cdv/dt) is calculated using 式 6:

$$C_{\frac{dv}{dt}} = \frac{I_{Source,Max}}{V_{out\ Slew\ rate}} = \frac{40\ \mu A}{4\ V/ms} = 10\ nF \quad (6)$$

Here, Cdv/dt = 10 nF is selected.

2.4.1.5 FET Selection

The device must meet the following requirements:

- The VDS rating must be sufficient to handle the maximum system voltage along with any ringing

caused by transients

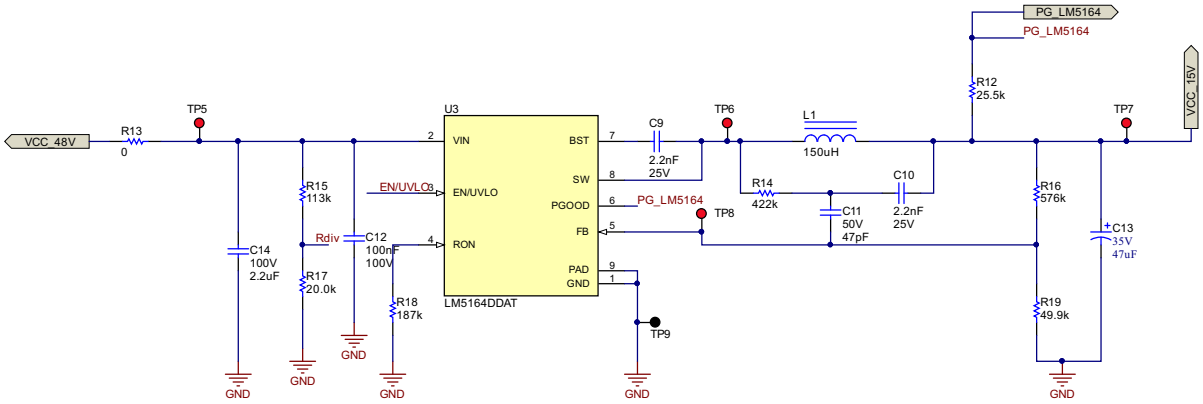
- The SOA of the FET must be sufficient to handle all usage cases: start-up, hot-short, start into short.
- $R_{DS(on)}$ must be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, TI recommends keeping the steady state FET temperature below 125°C to allow margin to handle transients.
- The maximum continuous current rating must be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements also pass these two.

The calculations for the FET and the Hot swap controller are easily made using the following tool: FET and hot swp controller calculations.

2.4.2 Designing Gate Driver Power Supply - LM5164

図 14 shows the LM5164 schematic.

図 14. LM5164 Schematic



2.4.2.1 LM5164 Switch Frequency

The switching frequency of the LM5164 device is set by the on-time programming resistor placed at R_{on}. The R_{on} is related to switching frequency and is calculated using 式 7:

$$R_{on}\left(k\frac{dv}{dt}\right)=\frac{V_{OUT}(V)\times 2500}{F_{SW}(kHz)}=\frac{15\ V\times 2500}{200\ kHz}=187\ k\Omega \tag{7}$$

R_{on} is calculated to be 187 kΩ, setting the switching frequency to 200 kHz.

2.4.2.2 Inductor Calculation

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by 式 8 and 式 9.

$$\Delta I_L=\frac{V_{OUT}}{F_{SW}\times L_O}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)=\frac{15\ V}{200\ kHz\times 150\ \mu H}\times\left(1-\frac{15}{48}\right)=343\ mA \tag{8}$$

$$I_{L(peak)}=I_{OUT(max)}+\frac{\Delta I_L}{2}=20+\frac{0.343}{2}=20.17\ A \tag{9}$$

The inductor L is calculated using 式 10:

$$L_O=\frac{V_{OUT}}{F_{SW}\times\Delta I_L}\times\left(1-\frac{V_{OUT}}{V_{IN(nom)}}\right)=\frac{15\ V}{200\ kHz\times 350\ mA}\times\left(1-\frac{15}{48}\right)=147\ \mu H \tag{10}$$

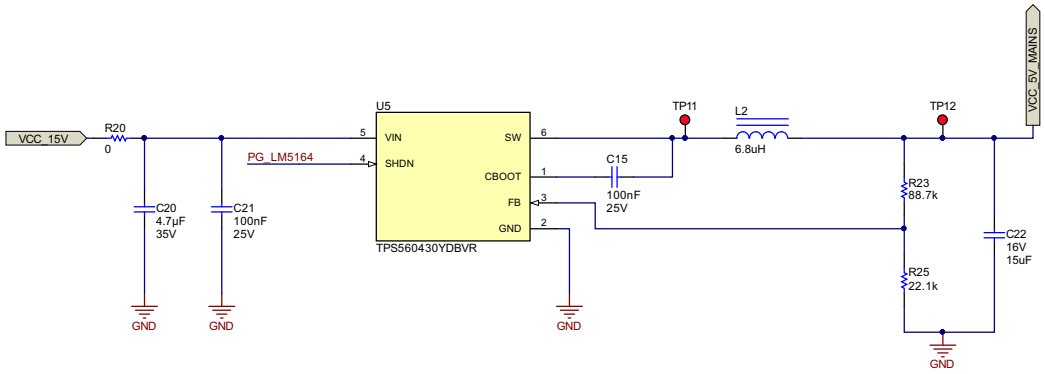
However, inductor L is selected to be 150 µH which results in the ripple of approximately 350 mA.

2.4.3 Designing Encoder Supply - TPS560430, TPS22919, and TPS22625

2.4.3.1 Designing DC/DC Converter - TPS560430

The 5-V supply for the encoder is obtained either from the 48 V main bus or from 5 V external USB. The TPS560430 device is used to generate 5 V from 15-V input as 図 15 shows. The device operates at 2.1-MHz frequency, which helps to reduce the inductor size. The external resistor divider is used to set the output voltage. The inductor L2 and the output capacitor C22 form the output low-pass filter. The inductor value is calculated based on the maximum current under static load conditions. For the switching frequency of 2.1 MHz, to convert 15 V to 5 V the inductor value is calculated to be 6.8 µH and the output capacitance of 15 µF is selected.

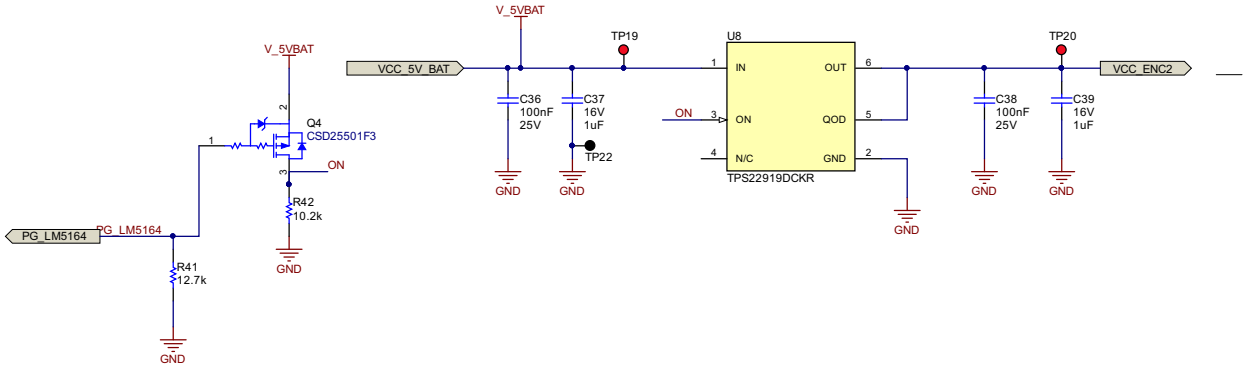
図 15. TPS560430 Schematic



2.4.3.2 Designing Self-Protected Load for Connecting External Battery - TPS22919

図 16 shows the TPS22919 schematic. Calculate the slew rate of the load switch using 式 11.

図 16. TPS22919 Schematic



$$\text{Slew rate} = \frac{I_{RUSH}}{C_{OUT}} = \frac{250\ \text{mA}}{1\ \mu\text{F}} = 250\ \text{mV}/\mu\text{s} \quad (11)$$

where

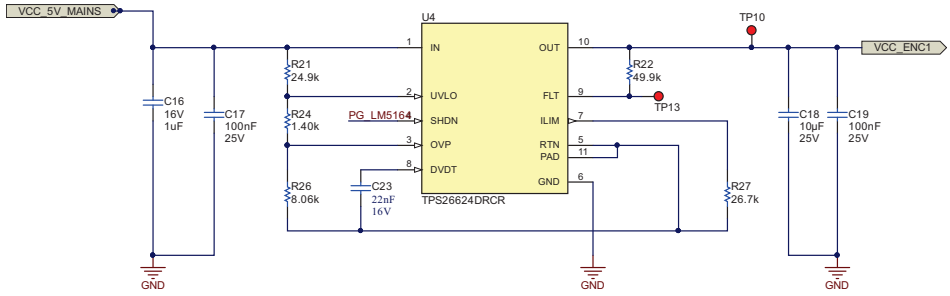
- I_{RUSH} = maximum acceptable inrush current (mA)
- C_{OUT} = capacitance on VOUT (µF)
- Slew rate = Output slew rate during turn on (mV/µs)

For I_{RUSH} of 250 mA, using C_{OUT} of 1 µF gives a slew rate of 250 mV/µs. The TPS22919 switch has a slew rate of 2.7 mV/µs.

This device has an active high switch control input, ON. This pin is connected to the PG of the LM5164 device as 図 16 shows, so that whenever the mains supply is unavailable PG goes down and ON gets activated thereby supplying the encoder from the battery.

2.4.3.3 Designing Protection for Encoder - TPS22624

図 17. TPS22625 Schematic



In the TPS26624 device, the current limit is set to 250 mA using the external resistor connected to ILIM pin. The resistor value is calculated using 式 12:

$$R_{ILIM} = \frac{6.636}{I_{OL}} = \frac{6.636}{250\ mA} = 26.5\ k\Omega$$

where

- I_{OL} is the current limit, that is, 250 mA in the design. Therefore, R_{ILIM} = 26.7 kΩ (12)

The OVP and UVP are set using the resistive divider network derived from the input using 式 13 and 式 14.

$$V_{(OVPR)} = \frac{R3}{R1 + R2 + R3} \times V_{(OV)} \quad (13)$$

$$V_{(UVLOR)} = \frac{R3}{R1 + R2 + R3} \times V_{(UV)} \quad (14)$$

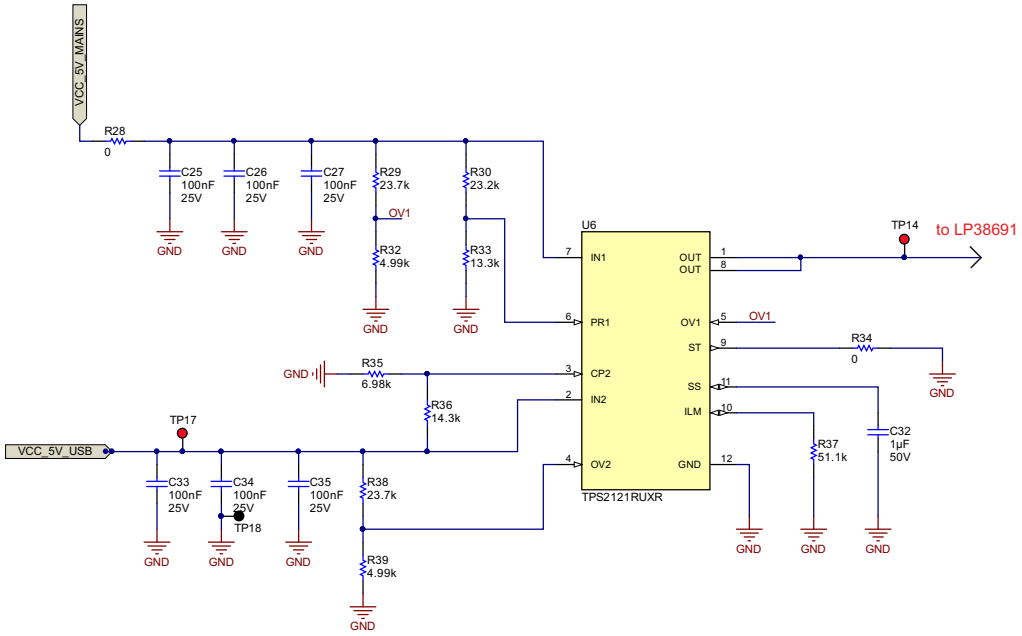
From device electrical specifications, $V_{(OVPR)}$ = 1.19 V and $V_{(UVLOR)}$ = 1.19 V. The OVP is set to 5.25 V and UVP to 4.75 V, hence resistors R21 = 24.9 kΩ, R24 = 1.40 kΩ, and R26 = 8.06 kΩ.

2.4.4 Designing Controller Power Supply - TPS2121

2.4.4.1 Designing Power MUX - TPS2121

図 18 shows the TPS2121 schematic.

図 18. TPS2121 Schematic



The TPS2121 device can operate in manual switchover, automatic switchover, and highest voltage operation. In this design, the device is operated in automatic switchover with priority set to supply 1 (mains supply) and switches to supply 2 (USB supply) when supply 1 goes down. The design involves accurate selection of resistors at OV, PRI, and CP inputs. In this design, the device will switch from IN1 to IN2 when the voltage on IN1 drops below 4.5 V. Therefore, the voltage on PR1 needs to remain higher than the voltage on CP2 until this condition exists. The resistor divider configured the voltage on CP2 to be 1.64 V using 式 15:

$$V_{CP2} = 5\ V \times \frac{6.98\ k\Omega}{14.3\ k\Omega + 6.98\ k\Omega} = 1.64\ V \tag{15}$$

To calculate the necessary resistor divider on PR1, the voltage on PR1 needs to drop below 1.64 V when IN1 reaches 4.5 V as 式 16 shows.

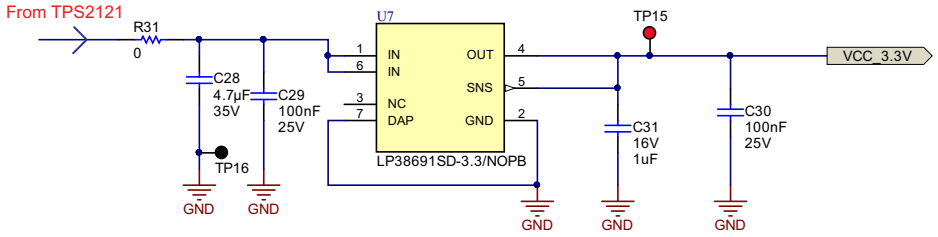
$$V_{PR1} = 4.5V \times \frac{13.3\ k\Omega}{23.2\ k\Omega + 13.3\ k\Omega} = 1.64\ V \tag{16}$$

Hence for V_{CP2}: R36 = 14.3 kΩ and R35 = 6.98 kΩ. Similarly for V_{PR1}: R30 = 23.3 kΩ, R33 = 13.3 kΩ.

2.4.4.2 Designing LDO - LP38691

The value of input and output capacitors are 4.7 µF and 1 µF as 図 19 shows.

図 19. LP38691 Schematic



Foldback current limiting is built into the LP38691 regulator which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between the IN and OUT pins. Typically, when this differential voltage exceeds 5 V, the load current limits at about 350 mA.

Output SNS pin of the LP38691 device allows remote sensing at the load which eliminates the error in output voltage due to voltage drops caused by the resistance in the traces between the regulator and the load.

The actual power dissipated is calculated by using 式 17:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} = \left(5\ V - 3.3\ V\right) \times 200\ mA = 340\ mW \tag{17}$$

The maximum allowable power dissipation for the device in a given package is calculated using 式 18:

$$P_{D-MAX} = \frac{\left(T_{J-MAX} - T_A\right)}{R_{\theta JA}} = \frac{125°C - 25°C}{50.6°C/W} = 1.97\ W \tag{18}$$

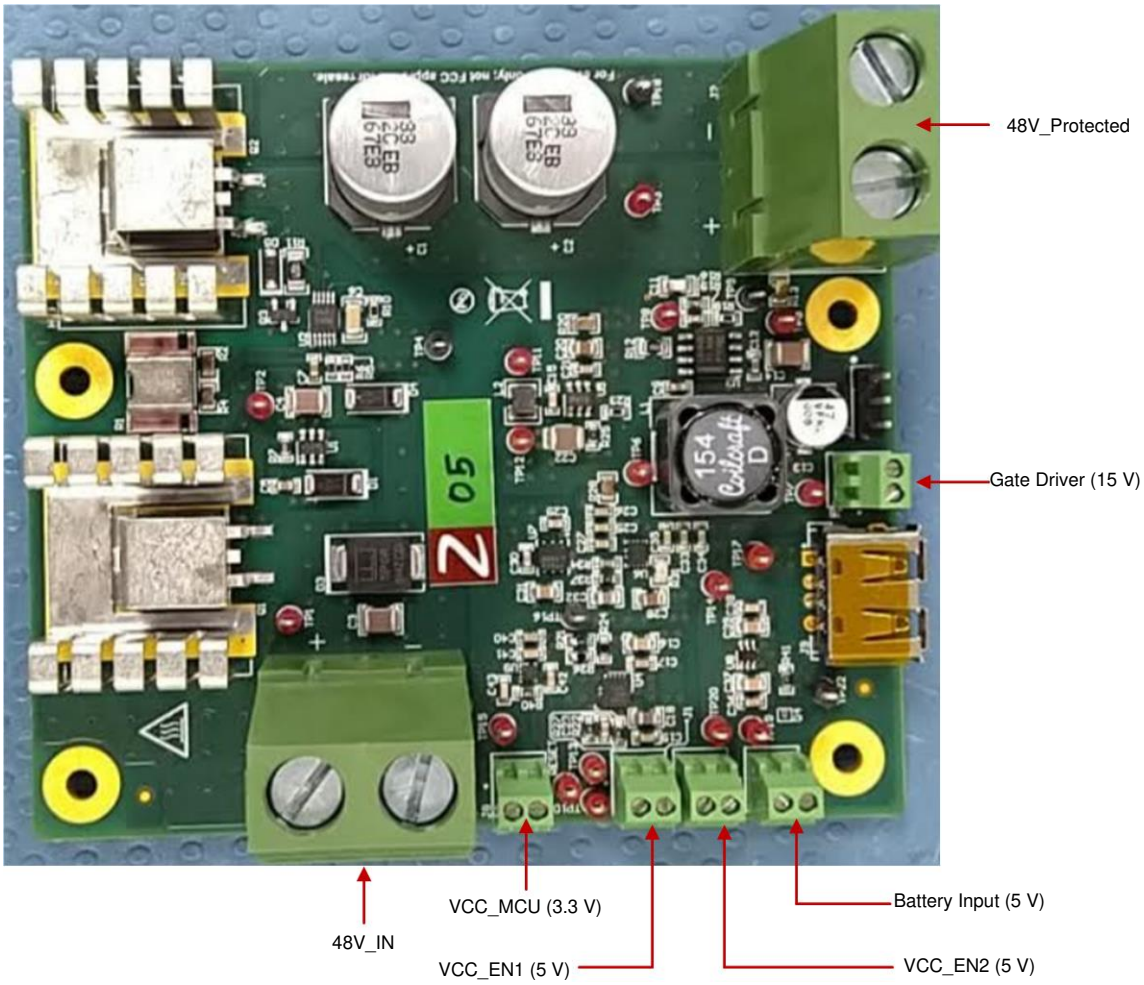
This gives enough margins to operate at a higher ambient temperature.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

The TIDA-010052 design is very compact, with 81.89-mm × 92.53-mm dimensions.

図 20. TIDA-010070 Board



J3 is a 2-pin connector which supplies the 48-V input voltage. J6 is the connector for supplying redundant power input to the encoder through the battery. J9 is the input port for the USB. 表 2 specifies the other connectors with their description.

表 2. Connector Description

CONNECTOR	FUNCTION
J1	Output 5-V encoder power supply
J2	Output protected 48-V supply to the inverters
J3	Input 48-V nominal power supply
J4	Output encoder power supply from external battery
J5	Output 15-V gate drive supply
J6	Input encoder power supply from external battery
J8	Output 3.3-V controller supply
J9	Input USB port

3.2 Testing and Results

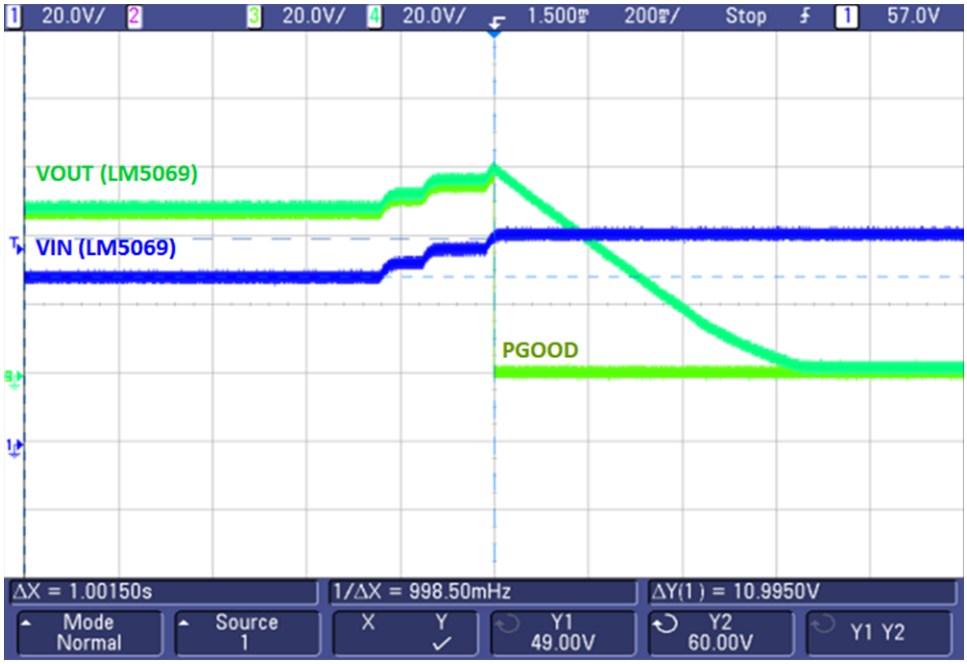
3.2.1 Test Results

3.2.1.1 Input Power Protection

3.2.1.1.1 Overvoltage Protection

The overvoltage threshold at the input is set with the LM5069 controller. As the input voltage rises to 60 V, the power good signal goes low and the output of the LM5069 device decreases to 0 V, depending upon the load, as 図 21 shows.

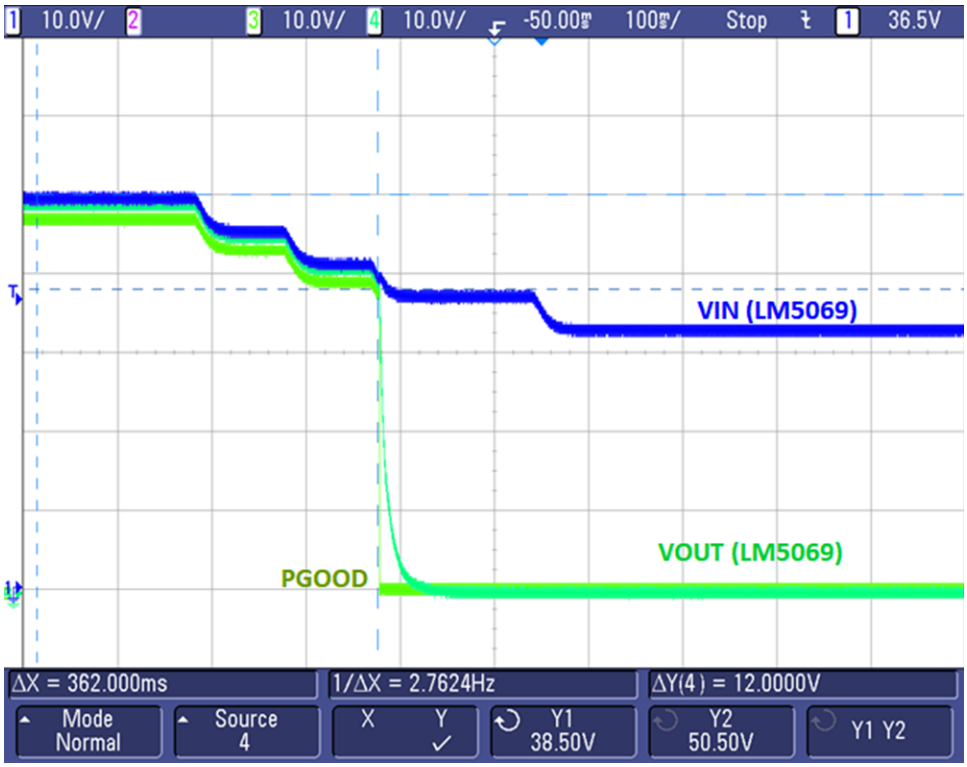
図 21. Overvoltage Protection at 60 V



3.2.1.1.2 Undervoltage Protection

The undervoltage threshold at the input is set with the LM5069 controller. As the input voltage decreases to 38.5 V, the power good signal goes low and the output capacitor of the LM5069 device discharges to 0 V, depending upon the load, as 図 22 shows.

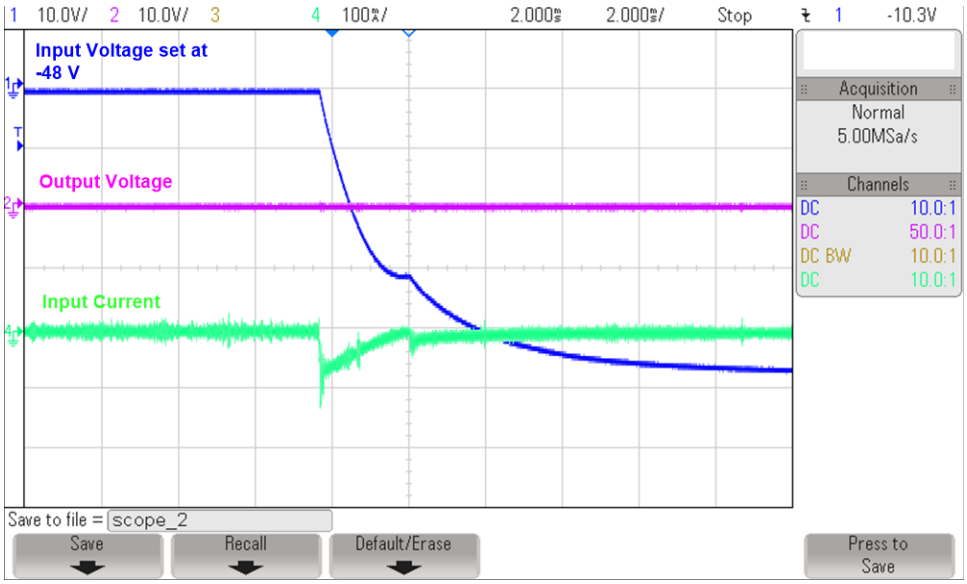
図 22. Undervoltage Protection at 38 V



3.2.1.1.3 Reverse Voltage Protection

The TIDA-010070 reference design is protected against reverse voltage at the input. 図 23 shows that when –48 V is applied at the input, the LM5050-1 device protects the subsequent stages by turning off the pass FET. A negligible amount of current (approximately 100 mA) is present to charge the input capacitor (C3) .

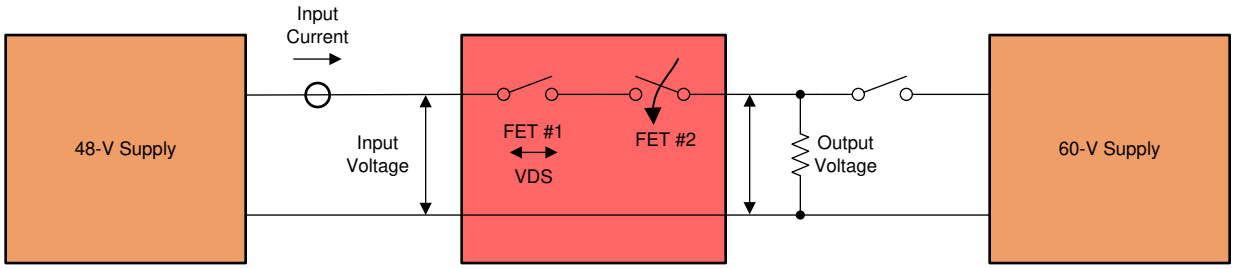
図 23. Reverse Voltage Protection at the Input



3.2.1.1.4 Reverse Current Protection

The reverse current protection is achieved by using the LM5050-1 controller. The test setup for carrying out the reverse current test is highlighted in 図 24. The input voltage is kept fixed at 48 V and a resistive load of 100 Ω is used at the output. The output terminal is also connected to a 60-V supply source. The ON/OFF key of the 60-V supply is represented in the test setup by a switch. When the 60-V supply is turned ON, the direction of input current reverses. The reverse current reaches 100 mA before the LM5050-1 device turns the pass FET off within 0.5 ms of current reversal. The LM5050-1 controller turns off the FET which can also be seen by looking at the drain-to-source voltage which changes from 0 V when the FET is closed to –12 V when the FET is turned off.

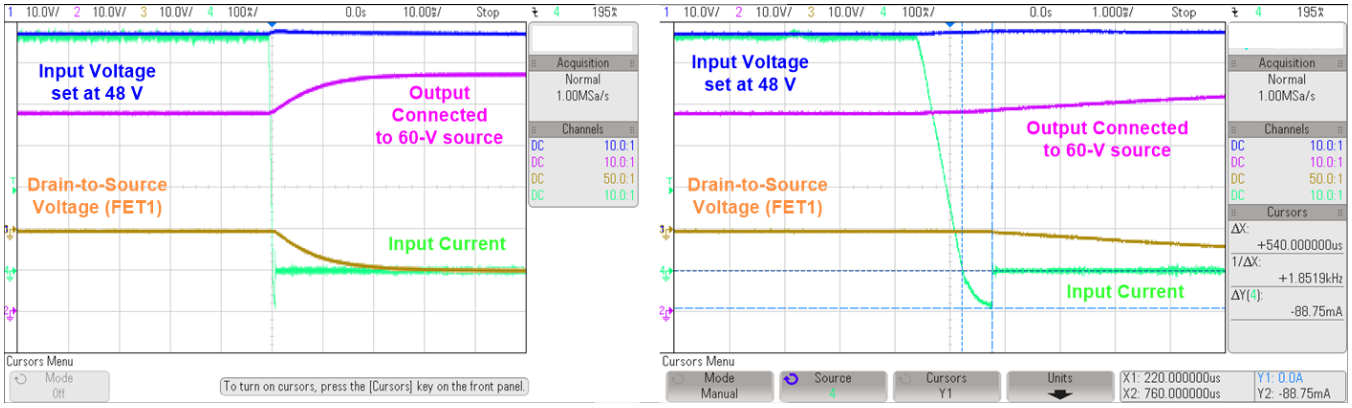
図 24. Reverse Current Test Setup



TIDA-010070

図 25 shows the test results of the reverse current protection tests.

図 25. Reverse Current Test Results

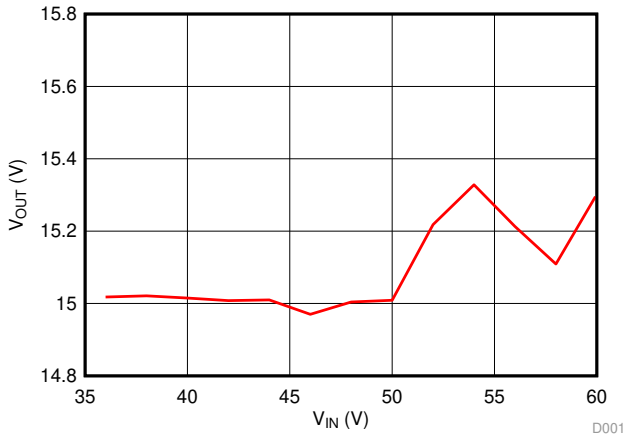


3.2.1.2 Voltage Rail for Gate Drive – 15 V

3.2.1.2.1 Line Regulation – 15 V

The line regulation of the 15-V rail is shown in 図 26 as the input voltage is varied from 36 V to 60 V. The variation of 15 V is limited from 15 V to 15.4 V.

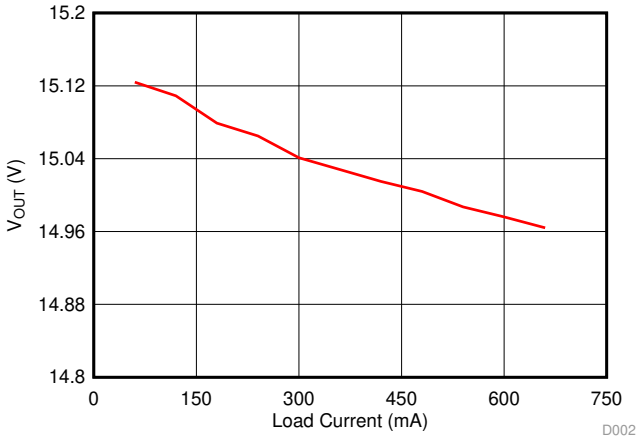
図 26. Line Regulation (15 V) From 36 V to 60 V



3.2.1.2.2 Load Regulation – 15 V

The 15-V rail varies between 15.2 V at no load to slightly less than 15 V at 600 mA as shown in 図 27.

図 27. Load Regulation at 15 V From No Load to Full Load (600 mA)

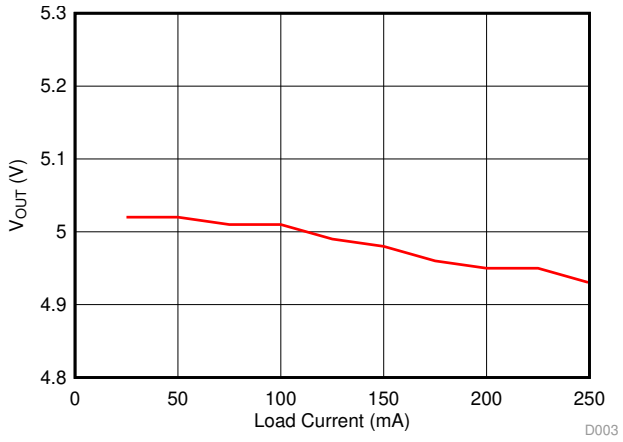


3.2.1.3 Voltage Rail for Encoder – 5 V

3.2.1.3.1 Load Regulation – 5 V

The TPS560430 device provides strict voltage regulation at varying load conditions. The 5-V rail varies between 5.2 V at no load to slightly less than 5 V at 250 mA (designated full load) as 図 28 shows.

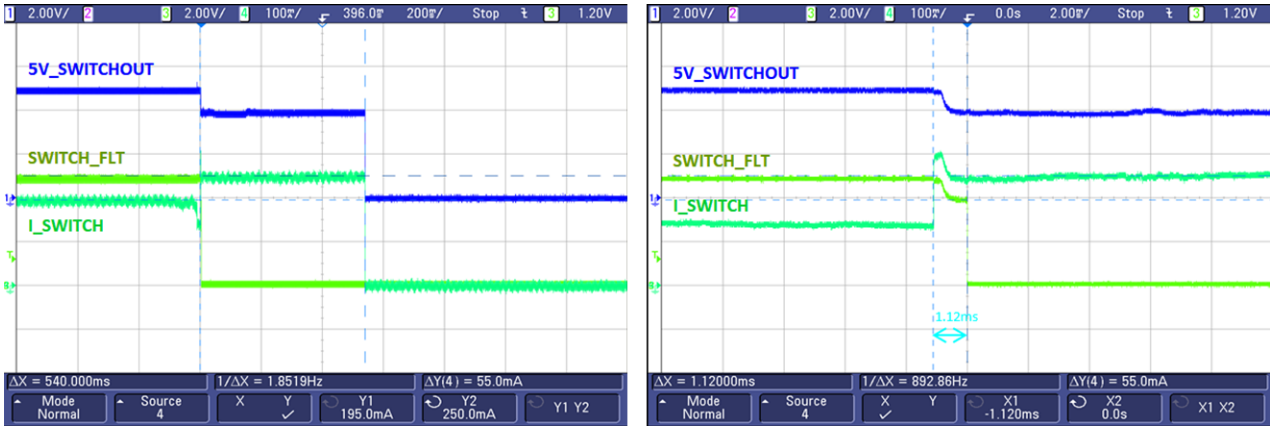
図 28. Load Regulation (5 V) From No Load to Full Load (250 mA)



3.2.1.3.2 Encoder Current Limit at 250 mA

The encoder power supply is designed to provide a current limit of 250 mA at the output. As the output current reaches 250 mA, the fault pin goes low indicating an overload condition as 図 29 shows. The output voltage stops regulating and decreases to 4 V and finally the output current decreases to 0 A after 550 ms.

図 29. Encoder Current Limit at 250 mA

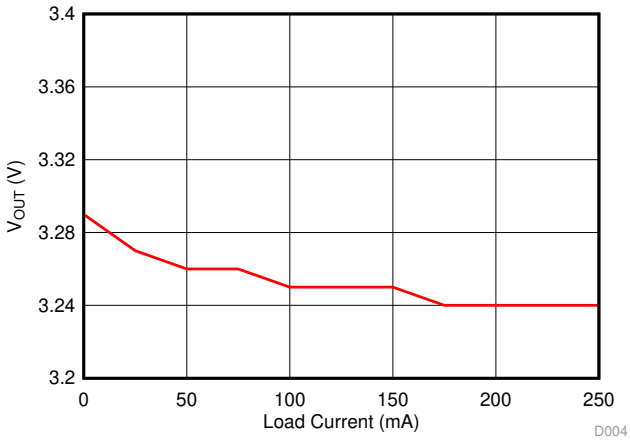


3.2.1.4 Voltage Rail for Controller – 3.3 V

3.2.1.4.1 Load Regulation – 3.3 V

The LP38691 device provides strict voltage regulation at varying load conditions as 図 30 shows.

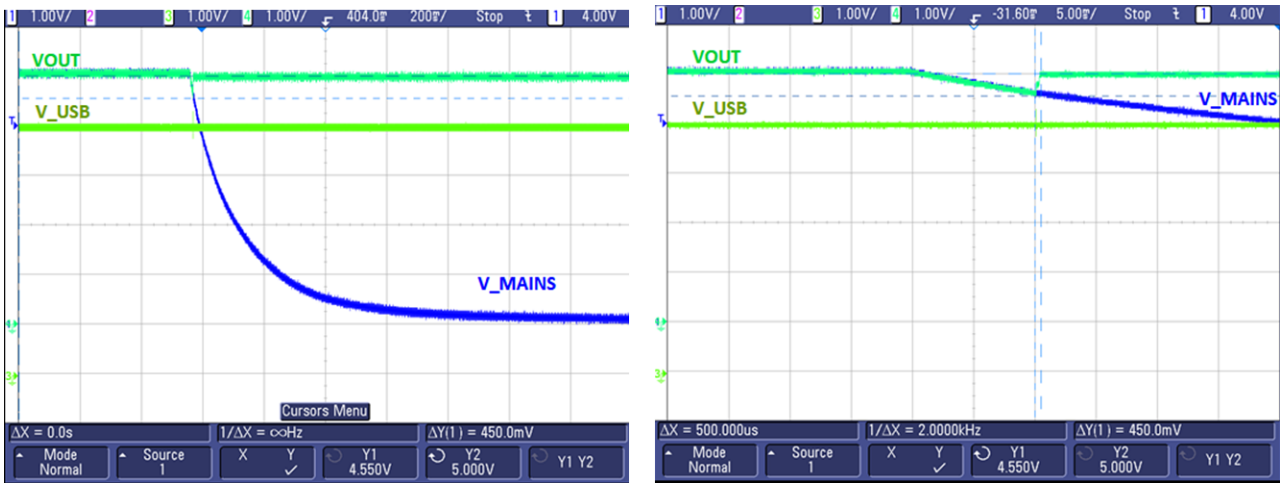
図 30. Load Regulation (3.3 V) From No Load to Full Load (250 mA)



3.2.1.4.2 Switchover From DC Bus to USB – 3.3 V

The TPS2121 is operated in automatic switchover mode to provide seamless supply to the MCU. Priority is set to channel 1 (mains supply). When the voltage at channel 1 drops to 4.5 V, the MUX switches to channel 2 (USB) as 図 31 shows.

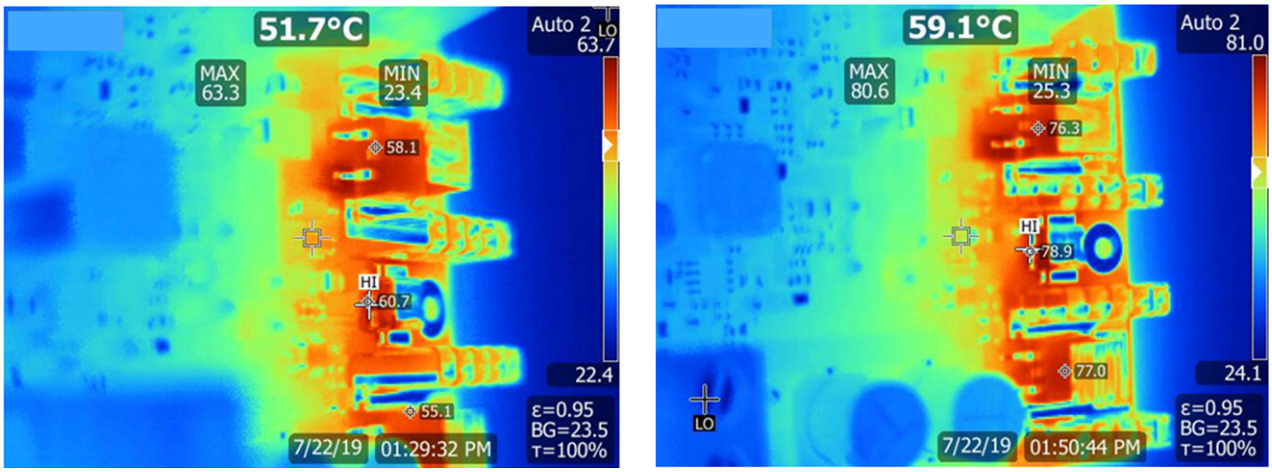
図 31. Automatic Switchover from DC Bus to USB for Controller Supply



3.2.1.5 TIDA-010070 Thermal Performance

図 32 shows the thermal image of the PCB. The temperature rise is 33°C for the output current of 18 A and 50°C for the current of 23 A. The FET rises 33°C above the ambient temperature at the output current of 18 A. Interpolating these temperatures, at an ambient temperature of 85°C, the case temperature of the FET would reach 125°C.

図 32. TIDA-010070 Thermal Image



4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010070.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010070.

4.3 PCB Layout Recommendations

Observe the following layout recommendations when implementing this design:

1. The trace width of the power signal should be wide enough to handle up to 20 A.
2. Care should be taken while designing the DC/DC switching power supply. Minimize the loop area formed by the input capacitor connections to the VIN and GND pins. Place the inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010070.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010070.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010070.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010070.

5 Related Documentation

1. Texas Instruments, *TPS2663x 60-V, 6-A Power Limiting, Surge Protection Industrial eFuse Data Sheet*
2. Texas Instruments, *LM5050-1/-Q1 High-Side OR-ing FET Controller Data Sheet*
3. Texas Instruments, *LM5069 Positive High-Voltage Hot Swap and In-rush Current Controller With Power Limiting Data Sheet*
4. Texas Instruments, *LM5164 100-V Input, 1-A Synchronous Buck DC/DC Converter With Ultra-low I_Q Data Sheet*
5. Texas Instruments, *TPS560430 SIMPLE SWITCHER® 4-V to 36-V, 600-mA Synchronous Step-Down Converter Data Sheet*
6. Texas Instruments, *TPS212x 2.8-V to 22-V Priority Power MUX with Seamless Switchover Data Sheet*
7. Texas Instruments, *TPS2662x 60-V, 800-mA Industrial eFuse with Integrated Input and Output Reverse Polarity Protection Data Sheet*
8. Texas Instruments, *TPS22919 5.5 V, 1.5 A, 90-mΩ Self-Protected Load Switch with Controlled Rise Time Data Sheet*
9. Texas Instruments, *LP3869x/-Q1 500-mA Low-Dropout CMOS Linear Regulators Stable With Ceramic Output Capacitors Data Sheet*

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