参考資料

デザイン・ガイド：TIDA-020030
サーマル・ダイオードとセンシング FET を搭載した SiC/IGBT 絶縁型ゲート・ドライバのリファレンス・デザイン

概要

このリファレンス・デザインは、IGBT モジュールを駆動する絶縁型ゲート・バイポーラ・トランジスタ (IGBT) またはシリコン・カーバイド (SiC) 絶縁型ゲート・ドライバ電力段であり、高度な保護機能を備えています。このデザインは、高レベルの安全性機能をサポートする単一のトラクション・インバータを使用して、単相電力段を形成しています。この IGBT モジュールは、温度監視用のサーマル・ダイオードと、過電流保護用のセンシング FET (電界効果トランジスタ) を内蔵しており、迅速で高精度の保護を実現します。このデザインは、バイアス電源および出力電圧監視、冗長回路による絶縁型 DC バス・センシング、ハイサイドおよびローサイド・ドライバの温度センシング、パルス幅変調 (PWM) ゲート信号監視、フォルト信号注入診断といった機能を備えています。この電源は、4.5V～65V DC の広い入力範囲に対応し、最大 180mA の出力電流を供給します。絶縁型ゲート・ドライバは最大 ±10A の駆動能力を達成しているほか、温度および電圧センシング用のアナログ / PWM コンバータも搭載しています。

リソース

TIDA-020030	デザイン・フォルダ
UCC21732-Q1、AMC1311-Q1	プロダクト・フォルダ
LM5180-Q1、TPS3700-Q1	プロダクト・フォルダ
ISO7762-Q1、ADS7049-Q1	プロダクト・フォルダ

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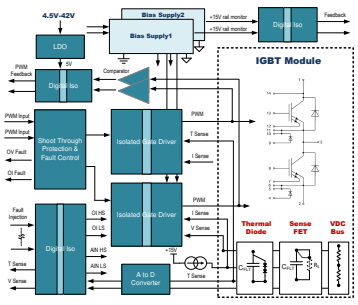
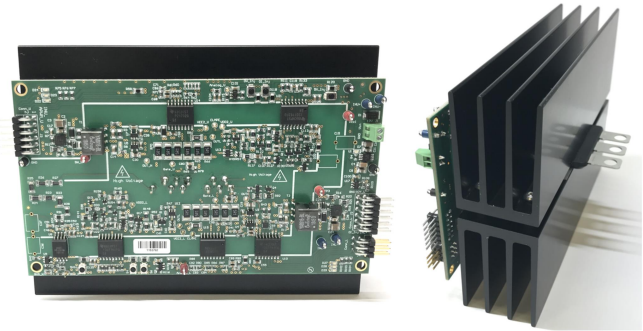
特長

- HEV/EV (ハイブリッド車と電気自動車) のトラクション・インバータ・アプリケーション向け単相電力段のデザイン
- 温度監視向けの内蔵サーマル・ダイオードと、過電流保護向けのセンシング FET を搭載した、700V、450A の両面冷却 IGBT モジュールを実装
- システムの安全性レベルを向上させる複数の冗長回路、電源電圧監視機能、および PWM 出力監視機能
- ±10A の駆動能力、過電流と短絡の高速保護機能、アナログ / PWM センサを搭載した統合型ゲート・ドライバをオンボードに実装
- 機能検証を目的とする障害信号注入機能
- シリアル・ペリフェラル・インターフェイス (SPI) と 12 ビット ADC により高精度の温度監視を実現

アプリケーション

- インバータおよびモータ制御
- オンボード・チャージャ (OBC) とワイヤレス・チャージャ
- ガソリン / ディーゼル・エンジン・プラットフォーム
- DC/DC コンバータ



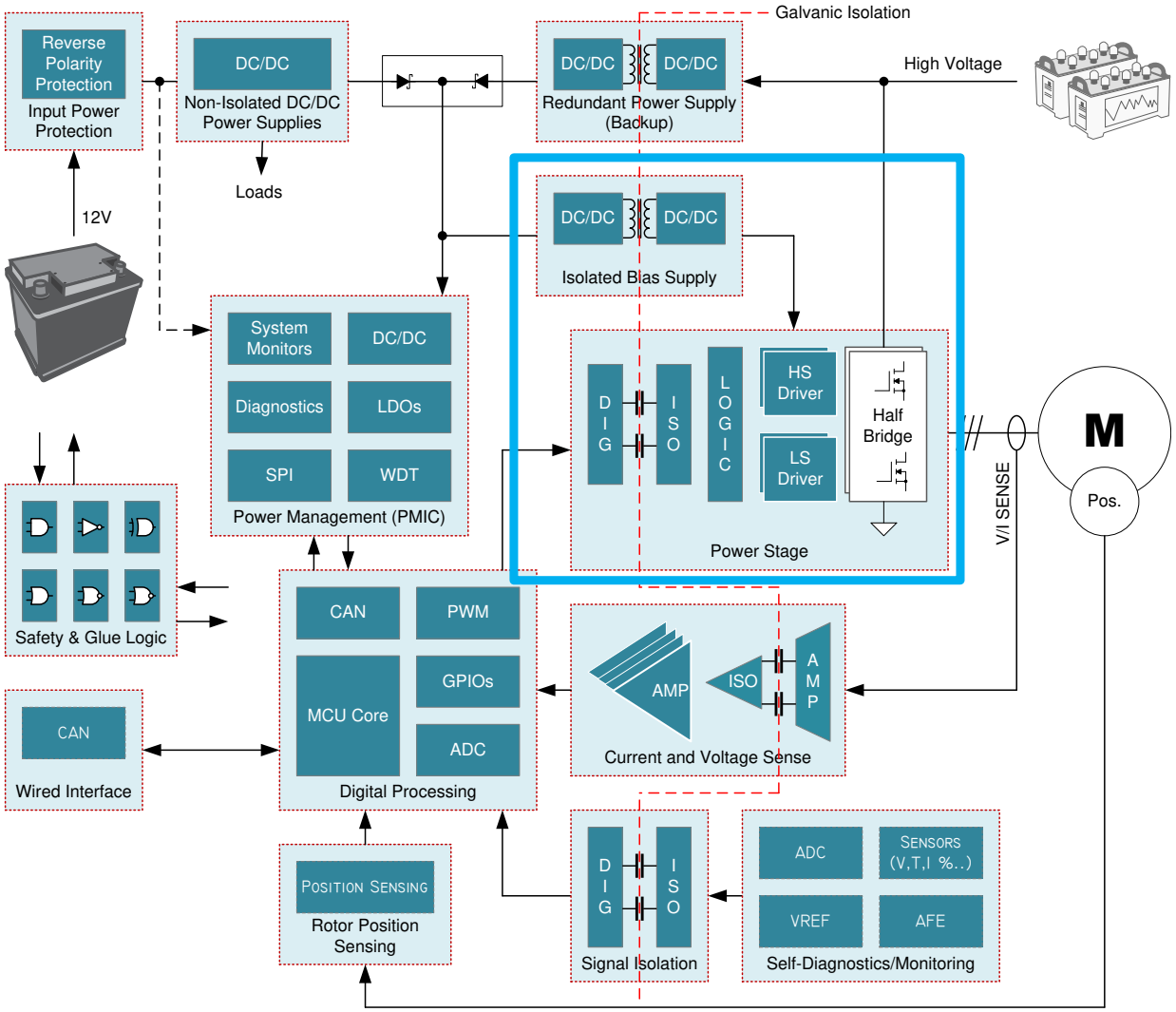


1 System Description

This reference design is a compact, high-voltage power stage solution implemented in hybrid electric vehicle and electric vehicle (HEV/EV) systems. It includes bias supplies, protections, redundancies, signal checks, and enhanced diagnostics needed to safely and efficiently drive the SiC MOSFET and Si IGBT power modules. The power stage in a half-bridge configuration is able to provide a ±10-A drive strength with reinforced isolation supporting up to 1.5-kVRMS working voltage and 12.8-kVPK surge immunity to the SiC or IGBT power switches. The bias supplies generate 4.2 W to each channel which is sufficient for driving high-power modules.

図 1 shows a traction inverter reference diagram where the position of the TIDA-020030 is highlighted. The isolated bias supply and the isolated gate drivers galvanically isolate the high-voltage power switches from the low-voltage control signals. Each isolated gate driver requires a pair of positive-supply and negative-supply rails to fully turn on and off the IGBT or SIC power modules.

図 1. HEV/EV Traction Inverter Reference Block Diagram and the Position of the TIDA-020030



2 System Overview

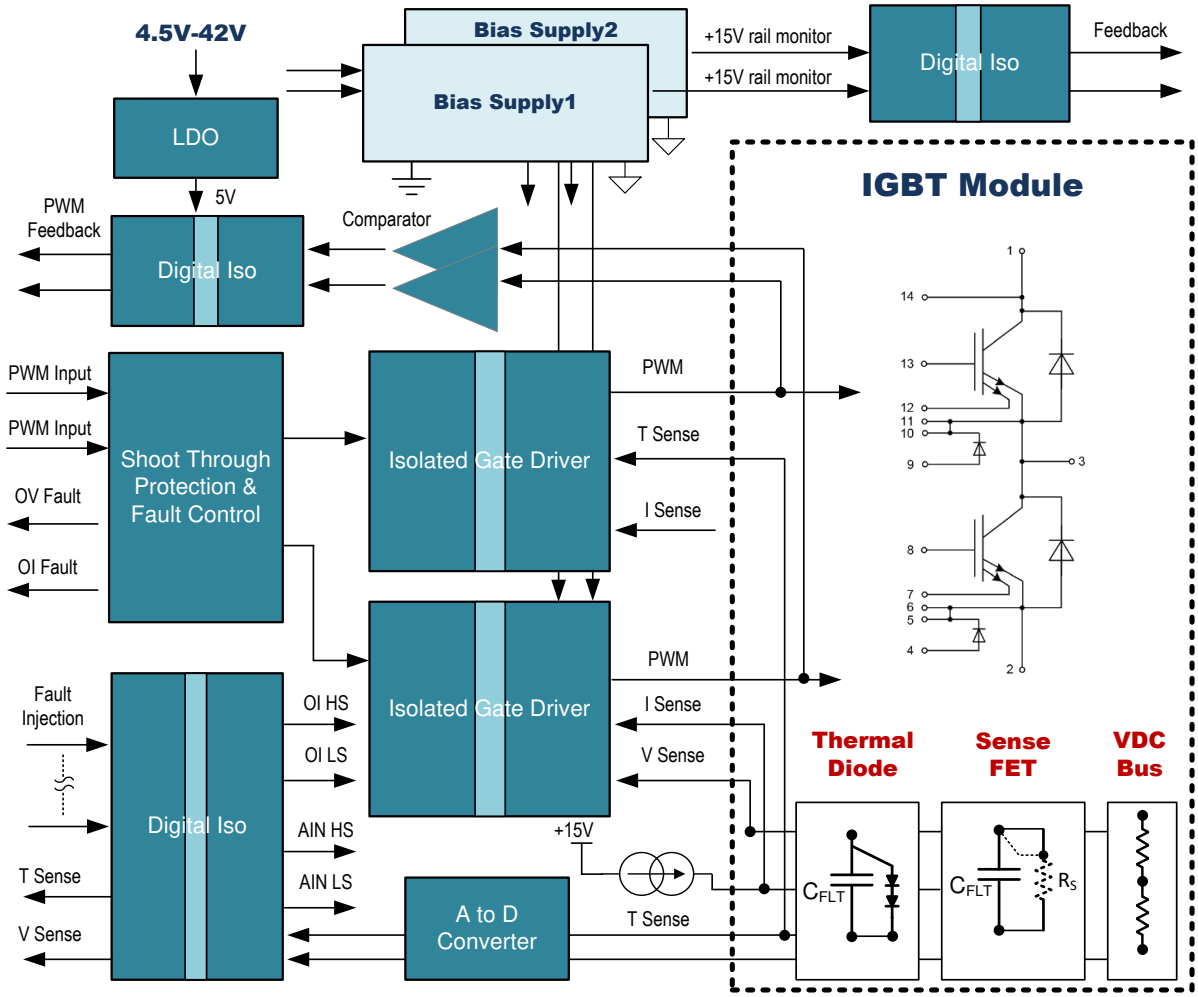
2.1 Block Diagram

The TIDA-020030 design drives a double-side-cooled IGBT power module with integrated thermal diode for temperature sensing and current sensing FET for overcurrent protection. The power stage provides up-to-date protection and diagnostic features enabling a high level of safety to the traction inverter system.

The boards consist of the high-side and low-side isolated gate drivers, DC bus voltage sensing, shoot-through protection and fault control, gate drive PWM monitoring, thermal diode sensing circuit, overcurrent and short-circuit protection, error signal injection channels, and various redundant channels for protections. The system block diagram is shown in 図 2. The design includes the following advanced features for an increased level of safety:

- Undervoltage and overvoltage monitoring on the bias supply rails
- Integrated analog-to-digital converter channel for temperature sensing
- Isolated DC bus voltage sensing path using an isolated amplifier
- Gate PWM comparator for control-signal monitoring
- Fast overcurrent detection through the isolated gate driver analog-to-digital converter
- Thermal diode temperature sensing through a high-side driver and DC bus voltage sensing through a low-side driver
- Logic shoot-through protection at PWM input
- Redundant sensing paths for increased level of safety:
  - DC bus voltage sensing
  - Thermal diode sensing
- Fault signal injection for:
  - Overcurrent detection on the high side
  - Overcurrent detection on the low side
  - Isolated analog-to-digital PWM sensor on the high side
  - Isolated analog-to-digital PWM sensor on the low side
- Fault signal report to the MCU side:
  - PWM gate fault
  - Overcurrent from the IGBT module
  - Overtemperature from the IGBT module
  - DC bus overvoltage
- 4.5-V-42-V input, 15-V - -8-V output, 4.2-W each isolated bias supplies on board

図 2. TIDA-020030 System Block Diagram



2.2 Design Considerations

The TIDA-020030 reference design features the following Texas Instruments devices.

2.3 Highlighted Products

2.3.1 UCC21732-Q1

The UCC21732-Q1 is a galvanic isolated single-channel gate driver designed for up to 1700-V SiC MOSFETs and IGBTs with advanced protection features. The UCC21732-Q1 has up to a ±10-A drive strength and supports up to 1.5-kVRMS working voltage and 12.8-kVPK surge immunity with longer than 40 years of isolation barrier life. The UCC21732-Q1 includes the following state-of-art protection features:

- High (±10-A) drive strength: Eliminates discrete high-current buffers, which are ideal for power modules, higher system reliability, and lower system cost.
- Fast (650-ns) isolated fault reporting: Faster system protection and shutdown and higher system reliability.
- Isolated analog-to-digital PWM sensing: Switch temperature sensing, DC bus sensing, auxiliary supply monitoring, alarm, and so forth.
- Fast (200-ns) overcurrent detection:
  - Important for fast-switch protection, especially SiC MOSFETs
  - Allows for flexible desaturation (DESAT) threshold setting for SiC MOSFET or IGBT
  - Applicable to IGBT modules with SenseFET
- External Miller clamp: Ideal for high-power IGBT/SiC modules (reduces clamp-to-gate parasitics).
- 2-level turnoff: Preferred for high-power modules for higher-power applications.

2.3.2 LM5180-Q1

The LM5180-Q1 device is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 70 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an opto-coupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results is a simple, reliable, and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1% load regulation and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

2.3.3 AMC1311-Q1

The AMC1311-Q1 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV peak according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The high-impedance input of the AMC1311-Q1 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

2.3.4 ADS7049-Q1

The ADS7049-Q1 device is a Q100-qualified, 12-bit, 2-MSPS, analog-to-digital converter (ADC). The device supports a wide analog input voltage range (2.35 V to 3.6 V) and includes a capacitor-based, successive-approximation register (SAR) ADC with an inherent sample-and-hold circuit. The SPI-compatible serial interface is controlled by the CS and SCLK signals. The input signal is sampled with the CS falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interface to a variety of host controllers. The ADS7049-Q1 complies with the JESD8-7A standard for a normal DVDD range (1.65 V to 1.95 V).

2.3.5 ISO776x-Q1

The ISO776x-Q1 devices are high-performance, six-channel digital isolators with 5000-VRMS (DW package) and 3000-VRMS (DBQ package) isolation ratings per UL 1577. The ISO776x-Q1 family of devices provides high-electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. The ISO776x-Q1 family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F.

2.3.6 TPS3700-Q1

The TPS3700-Q1 is a wide-supply voltage window comparator which operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The TPS3700-Q1 device can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors.

2.3.7 TPS7B82-Q1

The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 40 V (45-V load dump protection). Operation down to 3 V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7-µA typical quiescent current at light load, this device is an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in standby systems. The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to 125°C and with junction temperatures from –40°C to 150°C.

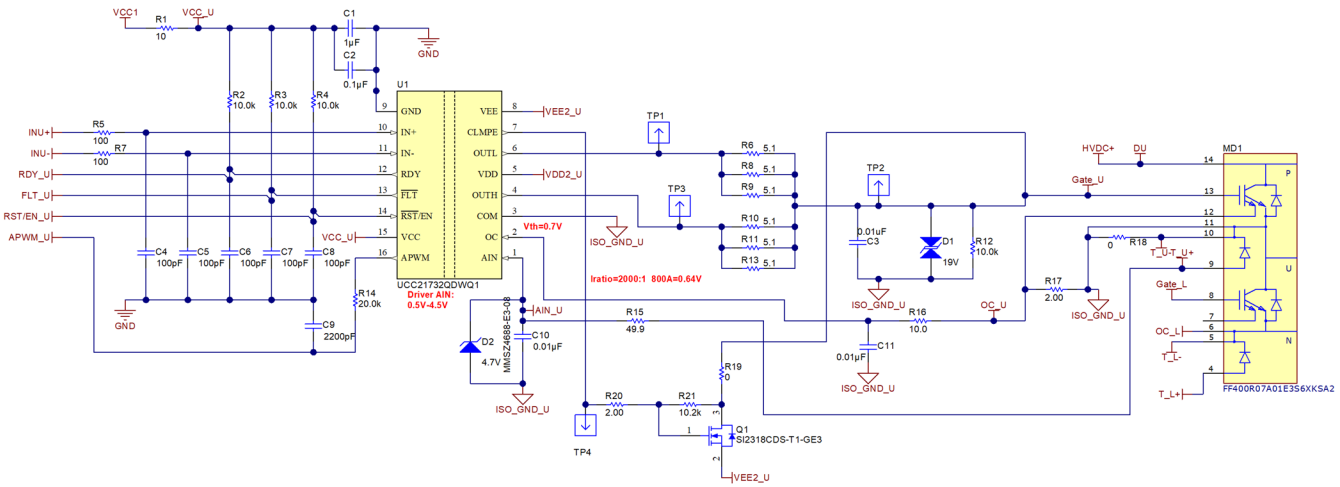
2.4 System Design Theory

2.4.1 Isolated Gate Driver

The schematic of one single-channel, isolated gate driver circuit is shown in 図 3. The IGBT half bridge module (FF400R07A01E3_S6) has the integrated thermal diode for temperature sensing and SenseFET for current sensing and protection. The isolated gate driver circuit is designed with following considerations:

- Three 5.1-Ohm gate resistors are connected in parallel to ensure high peak current drive and sink to the IGBT module. The 2010 package with a 0.75-W power rating is used to ensure sufficient heat dissipation.
- The overcurrent and short-circuit protection function is carried through the OC pin of the UCC21732-Q1. The current sense FET is connected with a 2-Ohm pulldown resistor. The scale down ratio of the main loop current and the sensed current through the sensing FET is set as 1:2000.
- A 19-V bidirectional Zener diode is placed close to the IGBT gate for protection.
- A thermal diode output is connected to the analog-to-digital channel input (AIN pin) of the isolated gate driver. The AD converter encodes the voltage signal VAIN to a PWM signal.
- An external Miller clamp is connected to the IGBT gate through the N-channel MOSFET.

図 3. Isolated Gate Driver Circuit With IGBT Module



2.4.2 DC Bus Voltage Sensing

It is important to continuously control the DC bus voltage to avoid catastrophic failure. Under certain operating conditions, the traction motor can act as a generator and deliver high voltage back into the DC link through the inverter's power device and the recovery diodes. This high voltage adds to the DC bus voltage, and the IGBTs could be damaged by the overvoltage stress. The DC bus voltage sensing circuit is designed in redundant paths for an increased level of safety. One sensing circuit is connected to the isolated gate driver, and the other circuit is connected to the isolated amplifier AMC1311-Q1.

The UCC21732-Q1 features an isolated analog-to-PWM signal function from the AIN to APWM pin. The UCC21732-Q1 encodes the voltage signal VAIN to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.5 V to 4.5 V, and the corresponding duty cycle of the APWM output ranges from 90% to 10%.The duty cycle increases linearly from 10% to 90% while the AIN voltage decreases from 4.5 V to 0.5 V.

While designing the circuit, influence from the internal current source IAIN must be considered. The internal current source is to bias an external thermal diode or temperature sensing resistor. The resistance at input is divided into two 2.49-kOhm to suit the input range of isolated gate driver and isolated amplifier AMC1311-Q1 respectively.

図 4. DC Bus Sensing Path Through the Isolated Gate Driver

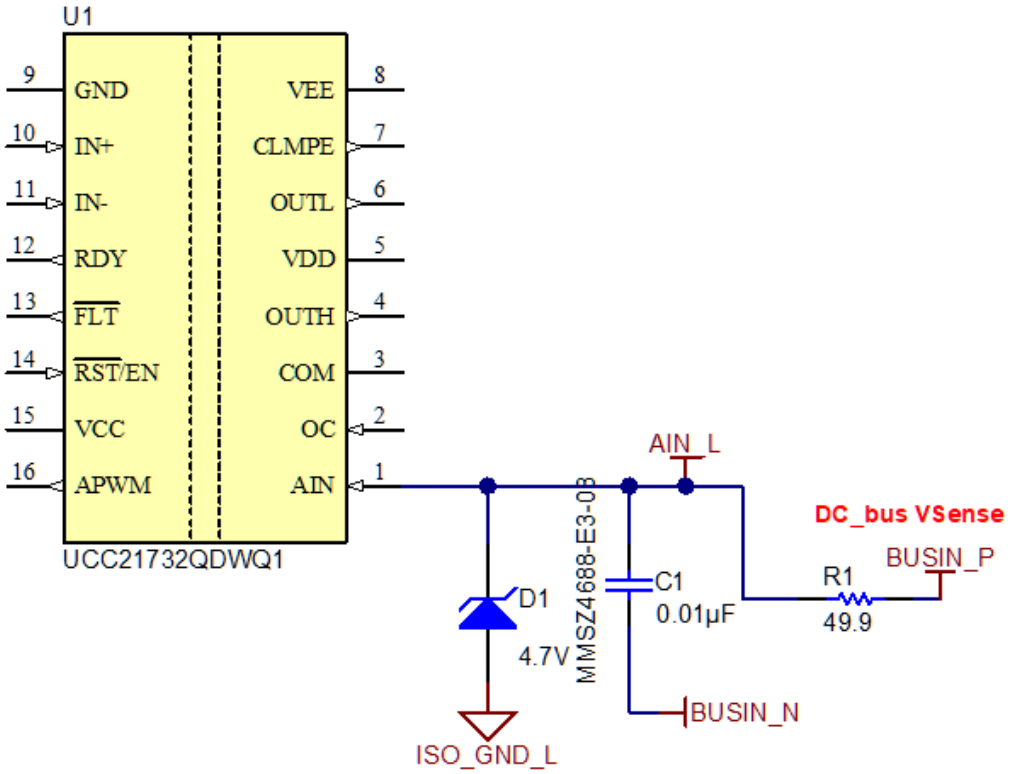
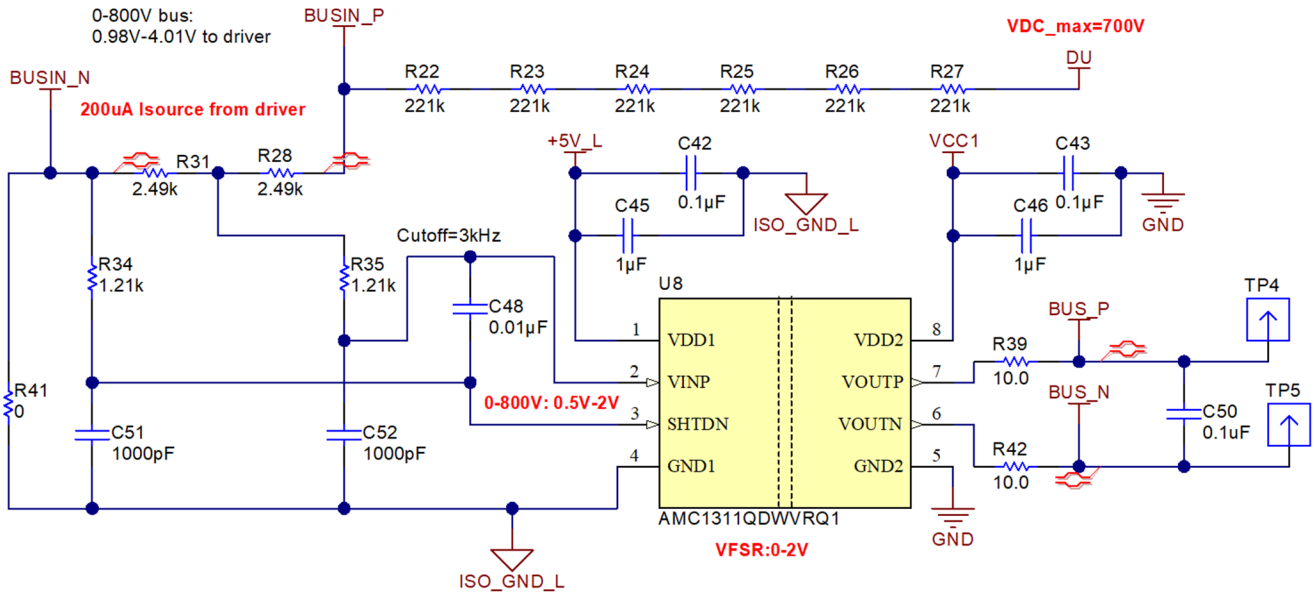


図 5. DC Bus Sensing Path Through the Isolated Amplifier



2.4.3 Gate Driver Bias Supply

The gate driver bias supply uses the flyback converter based on the LM5180-Q1 which has integrated MOSFET and internal compensation. The converter provides isolated output voltages with a tight regulation crossing load. The design specifications are shown in 表 1. The converter includes the following features:

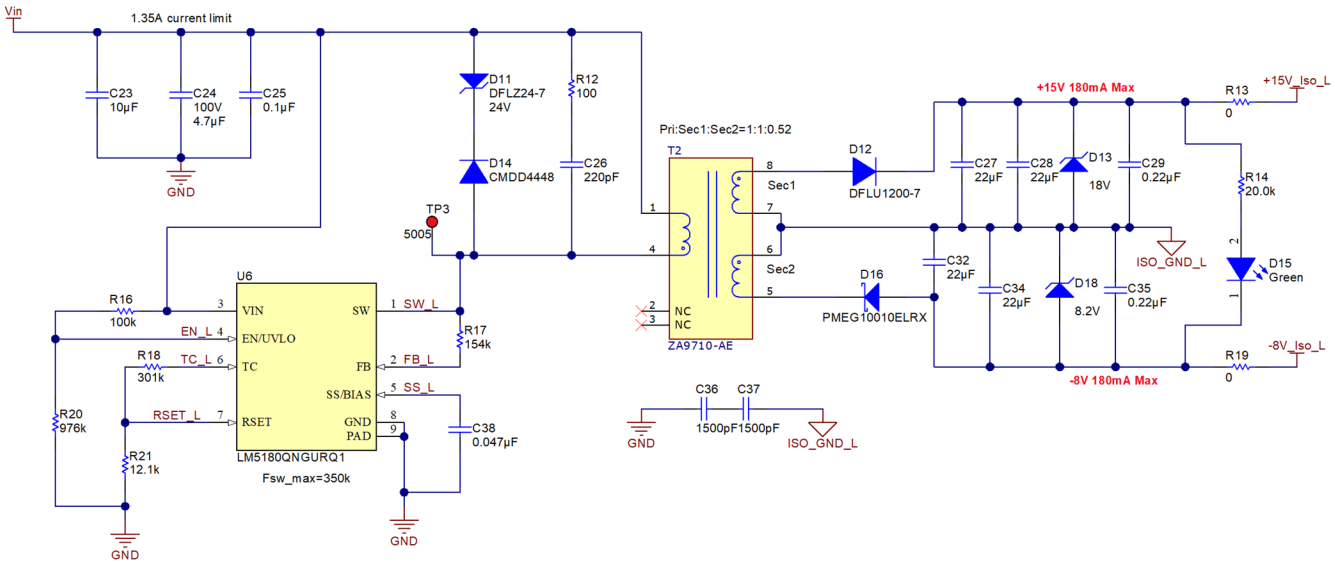
- Boundary conduction mode (BCM) control architecture provides fast line and load transient response
  - Peak current-mode control
  - Quasi-resonant switching for reduced power loss
  - Internal loop compensation
- Integrated 100-V flyback power MOSFET
  - Provides large headroom for input voltage transients
- Cycle-by-cycle overcurrent protection (OCP)
- Low transformer primary-to-secondary (inter-winding) capacitance to accommodate high dv/dt secondary-side common-mode swings

The schematic of the converter is shown in 図 6.

表 1. Design Specifications

PARAMETER	SPECIFICATION
Input voltage (Vin)	4.5-V – 70-V DC (100-V transient)
Output voltage (Vout)	+15 V -8 V
Output ripple	± 3%
Maximum output current (Iout_max)	180 mA
Switching frequency	<350 kHz
Output power (Pout_max)	4 W
Efficiency	>90% peak, 88% at full load

図 6. Isolated Gate Driver Bias Supply



2.4.3.1 Transformer Design

Key parameters to design the transformer include turns ratio, primary-side inductance, switching frequency, saturation current, and so forth.

If ignoring the drop voltage across the switching MOSFET, the winding turns ratio is calculated as:

$$V_{IN\_Min} \times T_{on} = (V_{OUT} + V_D) \times T_{off} \times N_{PS} \quad (1)$$

Where:

- V_{IN_Min} is the minimum input voltage
- T_{on} is the switch-on time of the switching MOSFET
- T_{off} is the off time of the switching MOSFET
- N_{PS} is the turns ratio of the transformer
- V_D is the output rectification diode

D is the duty cycle, and choosing the maximum duty cycle 75% at minimum input voltage, the turns ratio of the transformer primary winding to the secondary winding is calculated as:

$$N_{PS} = \frac{V_{IN\_Min}}{V_{OUT} + V_D} \cdot \frac{D}{1 - D} = 0.65 \quad (2)$$

Select a magnetizing inductance based on the minimum off-time constraint according to:

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \cdot N_{PS} \cdot t_{OFF\_MIN}}{I_{PRI\_PK}} = 26.5 \mu H \quad (3)$$

Where

- V_D is the forward drop voltage of the output rectification diode
- I_{PRI_PK} is the primary winding current when converter operates in frequency foldback mode (1.5 A according to the data sheet)

The built-in MOSFET of the LM5180-Q1 is rated at 100 V. In the off cycle, when the secondary (flyback) diode is on, the voltage on the drain (V_{DS}) is calculated as:

$$V_{DS} = V_{IN(MAX)} + V_{REF} + V_{RING} = 82V \quad (4)$$

Where:

- $V_{IN(MAX)}$ is the maximum input voltage
- I_{REF} is the voltage reflected from the secondary side
- V_{RING} is the excited spike due to resonance

The voltage across the secondary side diode is calculated as:

$$V_{Diode} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}} + V_{SPIKE} = 112V \quad (5)$$

Where:

- V_{OUT} is the maximum output voltage
- V_{SPIKE} is the excited spike due to resonance

The inductance of the transformer primarily determines the modes of operation in the LM5180 device as the load is varied from the minimum load to full load. An increase in the magnetic inductance generally leads to an increase in the leakage inductance of the transformer. The LM5180 device has a minimum off-time ($T_{OFF(MIN)}$) of 500 ns. The magnetizing current should not decrease to zero in less than 500 ns. Therefore the minimum primary-side inductance is calculated as:

$$L_{PRI} \geq \frac{\left(V_{out} + V_{FWD}\right) \cdot T_{OFF(MIN)} \cdot N_{PS}^2}{I_{PRI\_MIN} \cdot N_{PS}} = 30\mu H$$

Where:

- V_{OUT} is the nominal output voltage, which is 24 V
- $T_{OFF(MIN)}$ is the minimum off time of LM5180-Q1
- I_{PRI_MIN} is the minimum peak current flowing at primary side for the LM5180-Q1 which is 0.27 A
- N_{PS} is the primary to secondary turns ratio (6)

Thus, the designed transformer should have the minimum primary inductance of 30 µH.

Specifications of the designed flyback transformer are summarized in 表 2.

表 2. Flyback Transformer Specifications

PARAMETER		SPECIFICATION
Power rating		4.2 W
Input voltage		4.5 V - 42 V
Frequency		300 kHz
Maximum duty cycle		75%
Primary-side inductance		30 µH ± 10% at 300 KHz
Leakage inductance		<1% of primary inductance
Parasitic capacitance primary to secondary		<20 pF
Output voltage		+15 V and -9 V at 180-mA average current
Turns ratio		1:1:0.52
Peak current	Primary	1.45 A
	Secondary	1 A
RMS current	Primary	1.1 A
	Secondary	380 mA

TI recommends the flyback transformer ZA9710-AE from Coilcraft® for this reference design. The transformer features parasitic capacitance of 17 pF from the primary to secondary side.

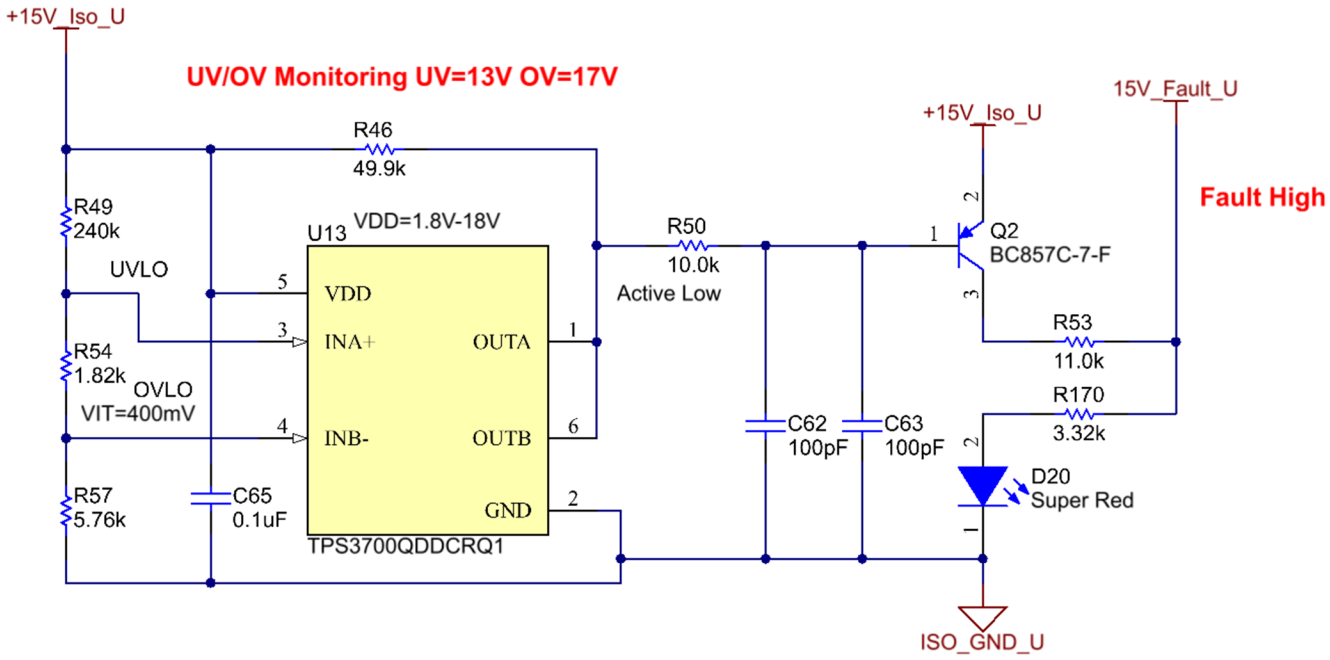
For more detailed design considerations for this bias supply, see the *4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers* (TIDA-020015).

2.4.3.2 Overvoltage and Undervoltage Detection

The IGBT gate is driven from the 15-V rail to turn on the IGBT. The 15-V rail should not drop below the minimum gate voltage to properly turn on the IGBT. Driving the IGBT with a lower gate voltage causes excessive power dissipation. Alternatively, excessive, higher-gate voltage will destroy the IGBT.

The overvoltage and undervoltage detection is designed with the window comparator TPS3700-Q1. It has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs. 図 7 shows the schematic of the detection circuit. The INA+ / INB- implements open-drain output. OUTA is driven low when the voltage at INA+ is below (VITP – VHYS). The output goes high when the sense voltage returns above the respective threshold. OUTB is driven low when the voltage at this comparator exceeds VITP. The output goes high when the sense voltage returns below the respective threshold. The undervoltage threshold is set as 13 V, and the overvoltage threshold is set as 17 V for this design. The OR logic is implemented by connecting the two open-drain outputs of the TPS3700-Q1. OUTA and OUTB can merge into one logic signal that goes low if either output is asserted. A 49.9-kΩ pullup resistor is used to hold these lines high when the output goes to high impedance.

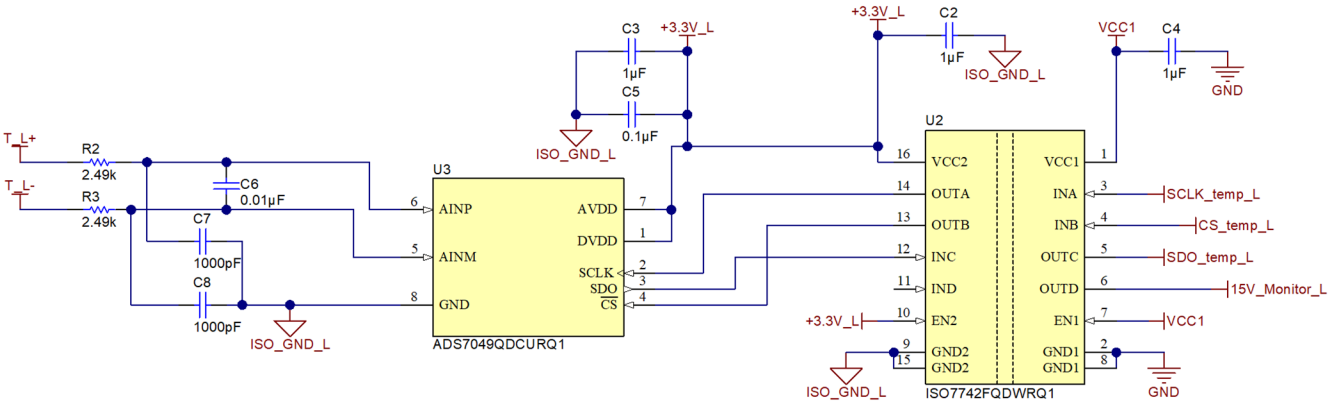
図 7. Overvoltage and Undervoltage Detection for Bias Supply



2.4.4 Thermal Diode Sensing Through External ADC

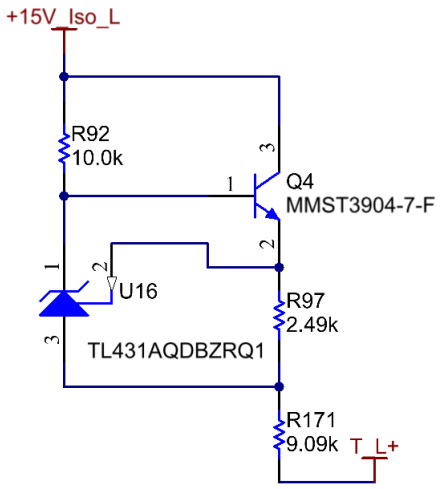
The thermal diode sensing for the low-side IGBT is achieved through the external analog-to-digital converter ADS7049-Q1, as shown in 図 8. The 12-bit resolution provides high accuracy while maintaining a high-speed data transfer rate. The SPI–compatible interface is controlled by the CS and SCLK signals. Output of the ADC is transferred to the low voltage side through a digital isolator.

図 8. ADC Interface for Thermal Diode Sensing



A key requirement for signal conditioning a diode-based temperature sensor is to generate a constant current source. When the current flowing through diode is constant, the diode voltage decreases as the temperature is increased. 図 9 shows the designed circuit with precision reference TL431A-Q1 to generate the 1-mA constant current source.

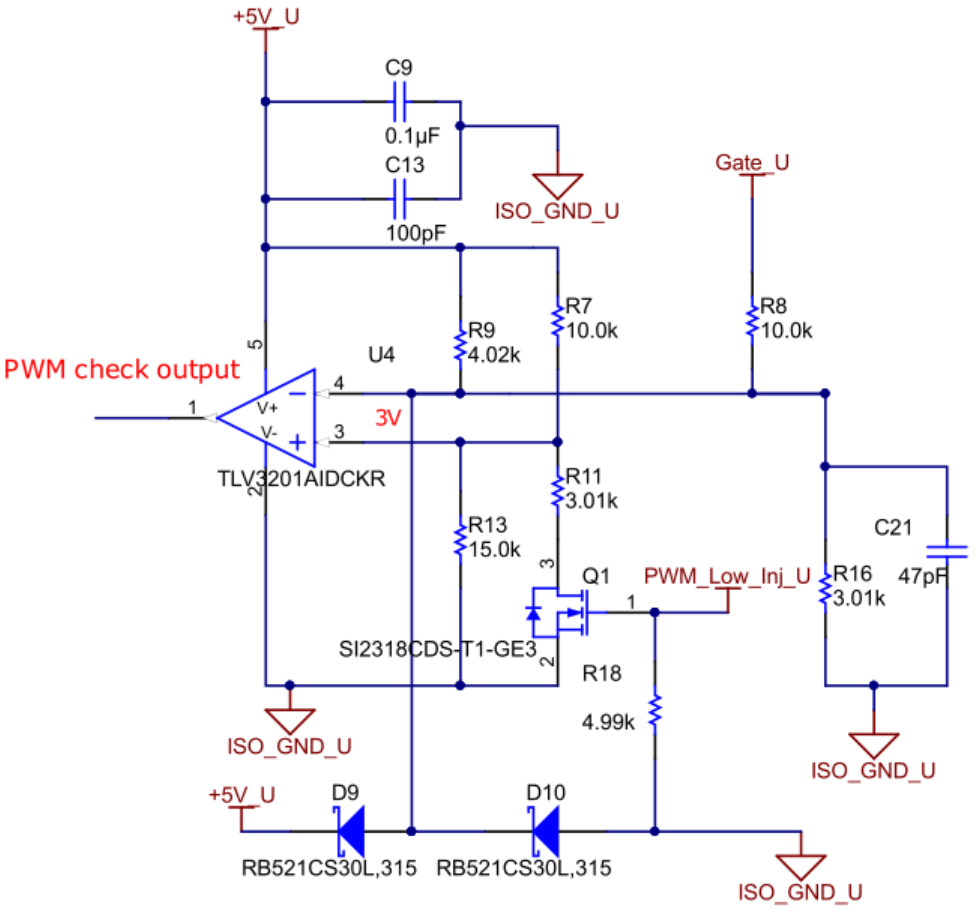
図 9. Constant Current Source for Biasing Thermal Diode



2.4.5 Gate PWM Signals Detection

Both high-side and low-side PWM signals at the gate of IGBT are monitored through a level-shifted comparator circuitry as shown in 図 10. The comparator voltage reference is set at two levels. The first level is set as 9 V through R7 and R13 for checking PWM high voltage levels. The second level is set by R7 and the paralleled value of R11 and R13 for checking the PWM low-voltage level. R9 functions as a pullup resistor enabling the comparator to generate positive pulse trains.

図 10. Level Shifted Comparator for Gate PWM Monitor

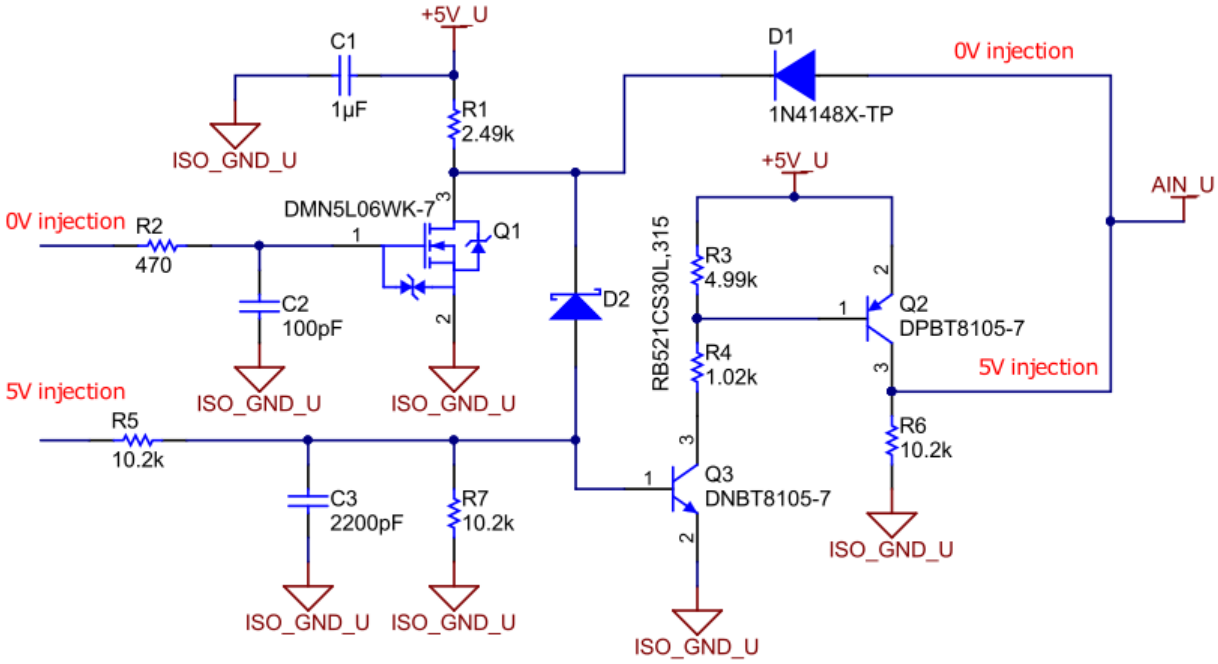


2.4.6 Fault Injection Circuit

In the case of custom hardware or software safety mechanisms, fault injection is a technique that can be used for a verification of the targeted function. This design includes fault signal to the UCC21732-Q1 analog-to-digital converter input pin and an overcurrent detection pin of the isolated gate driver and to the AMC1311-Q1 isolated amplifier.

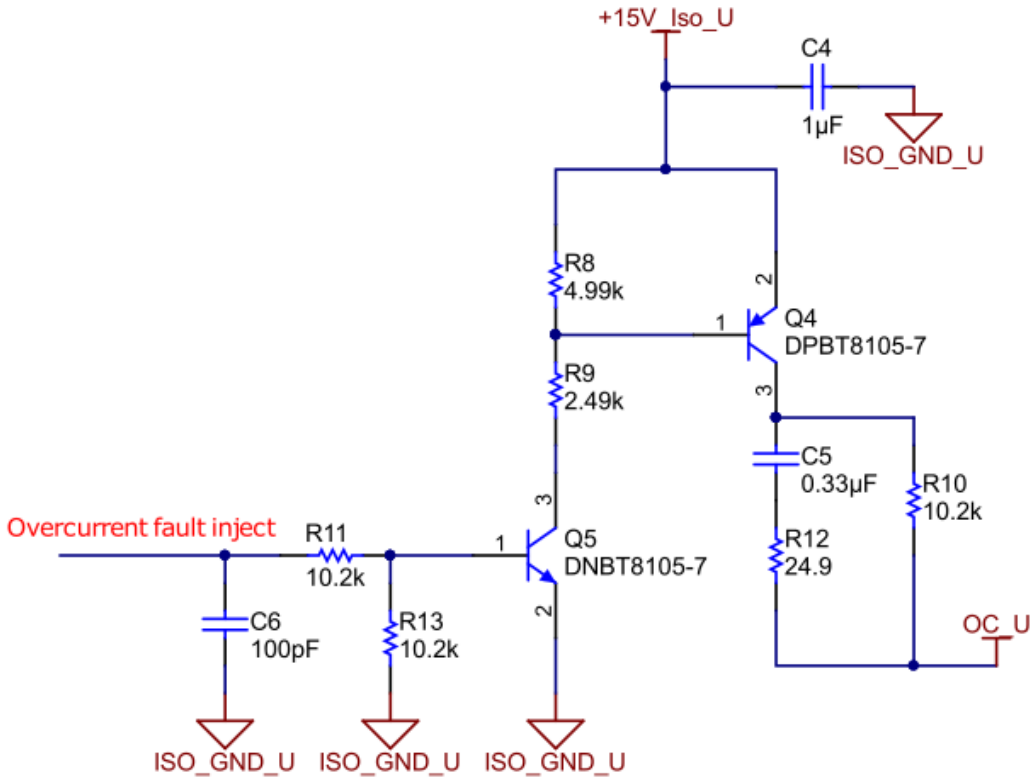
The fault injection circuit to the AIN pin of the isolated gate driver is shown in 図 11. When the 0-V injection line is triggered high, the UCC21732-Q1 AIN pin sees 0 V. When the 5-V injection line is triggered high, the UCC21732-Q1 AIN pin sees 5 V. The triggered signal is sent through the digital isolator ISO7762-Q1.

図 11. Fault Injection Circuit to AIN Pin of the UCC21732-Q1



The fault injection circuit to the OC pin of the isolated gate driver is shown in 図 12. When the overcurrent fault inject line is triggered high, the OC pin of the UCC21732-Q1 sees a 0.8-V peak pulse to emulate the overcurrent scenario.

図 12. Fault Injection Circuit to OC Pin of the UCC21732-Q1

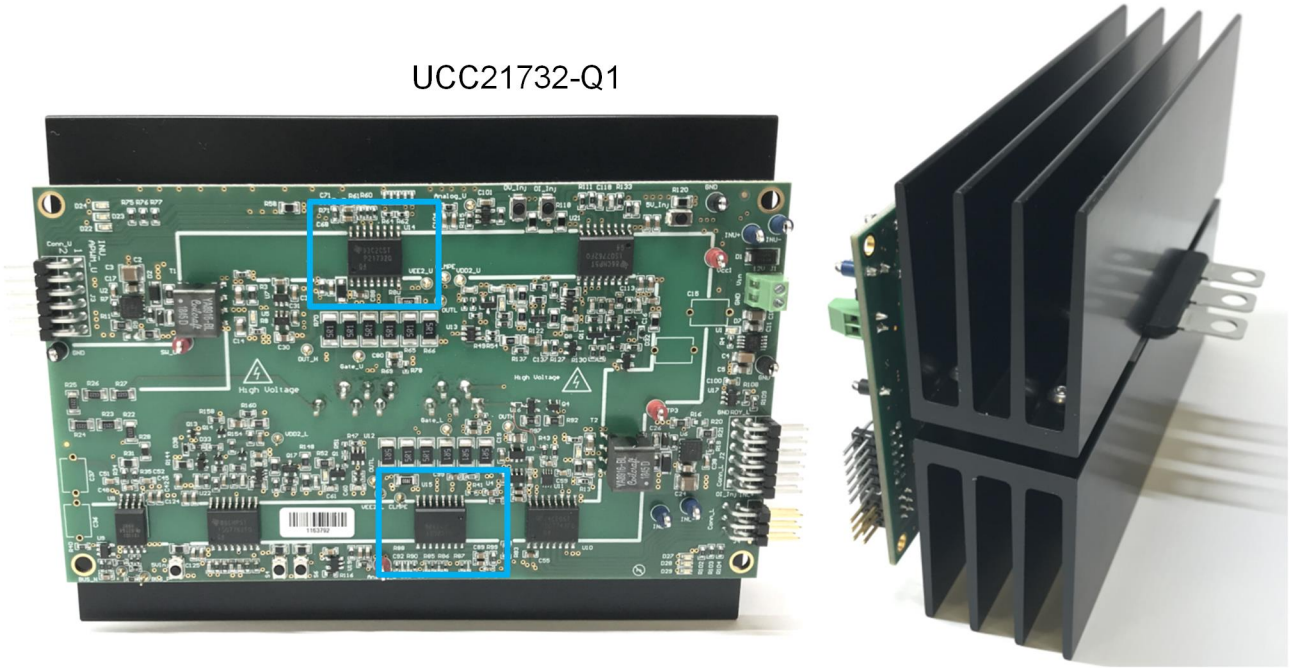


3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

図 13 shows the TIDA-020030 hardware and the IGBT module with double-sided cooling. The position of the isolated gate driver UCC21732-Q1 is shown. The heat sinks are symmetrically attached to the top and bottom side of the IGBT module respectively for maximum cooling. The isolated barrier on the driver board is outlined by the PCB silkscreen.

図 13. TIDA-020030 Hardware



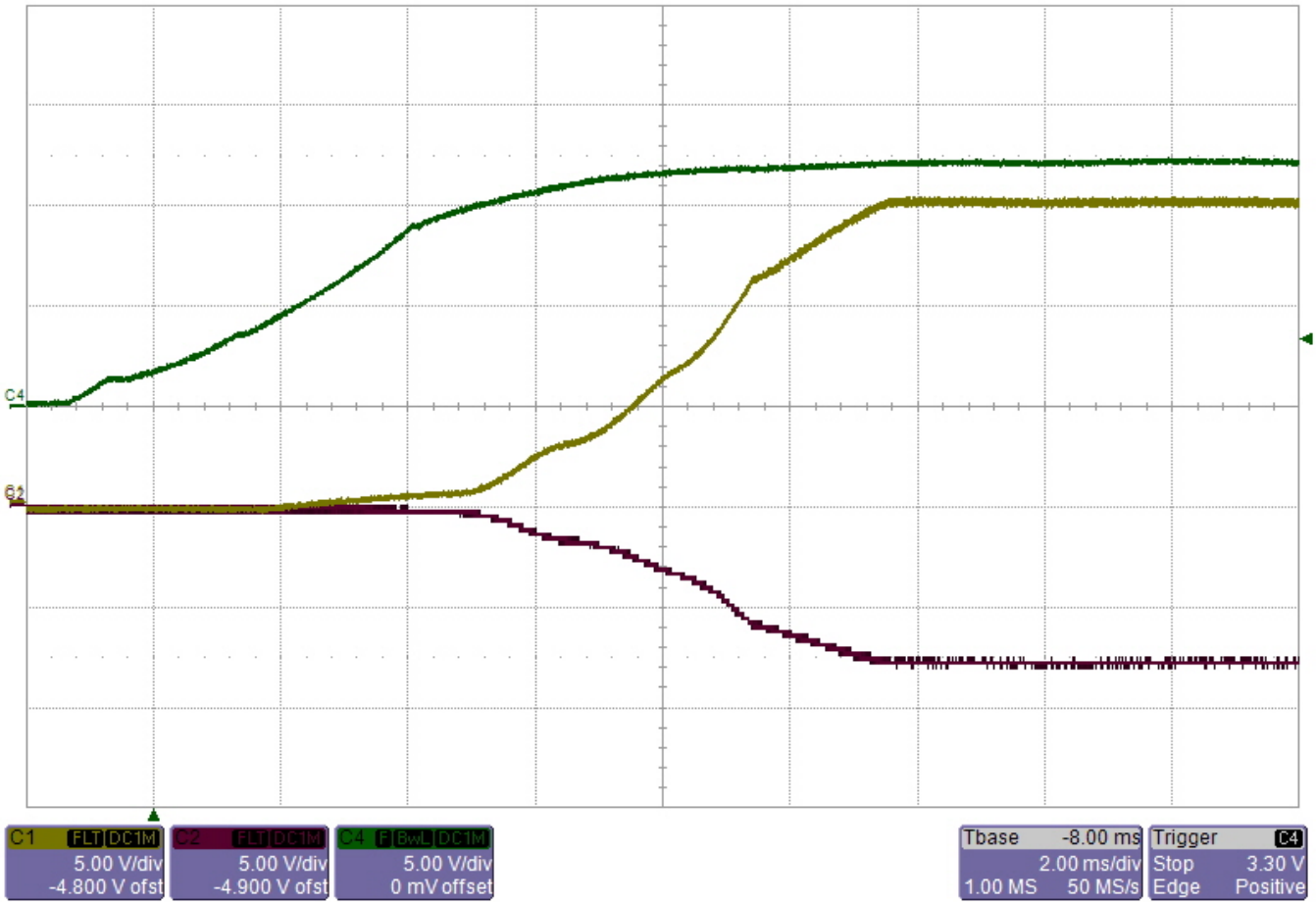
3.2 Testing and Results

3.2.1 Power Stage Startup

3.2.1.1 Bias Supply

The startup waveforms of the bias supply converter are measured at a 12-V input and with the isolated gate driver PWM switching frequency at 30 kHz.

図 14. Startup Waveforms of the +15-V and -8-V Rails

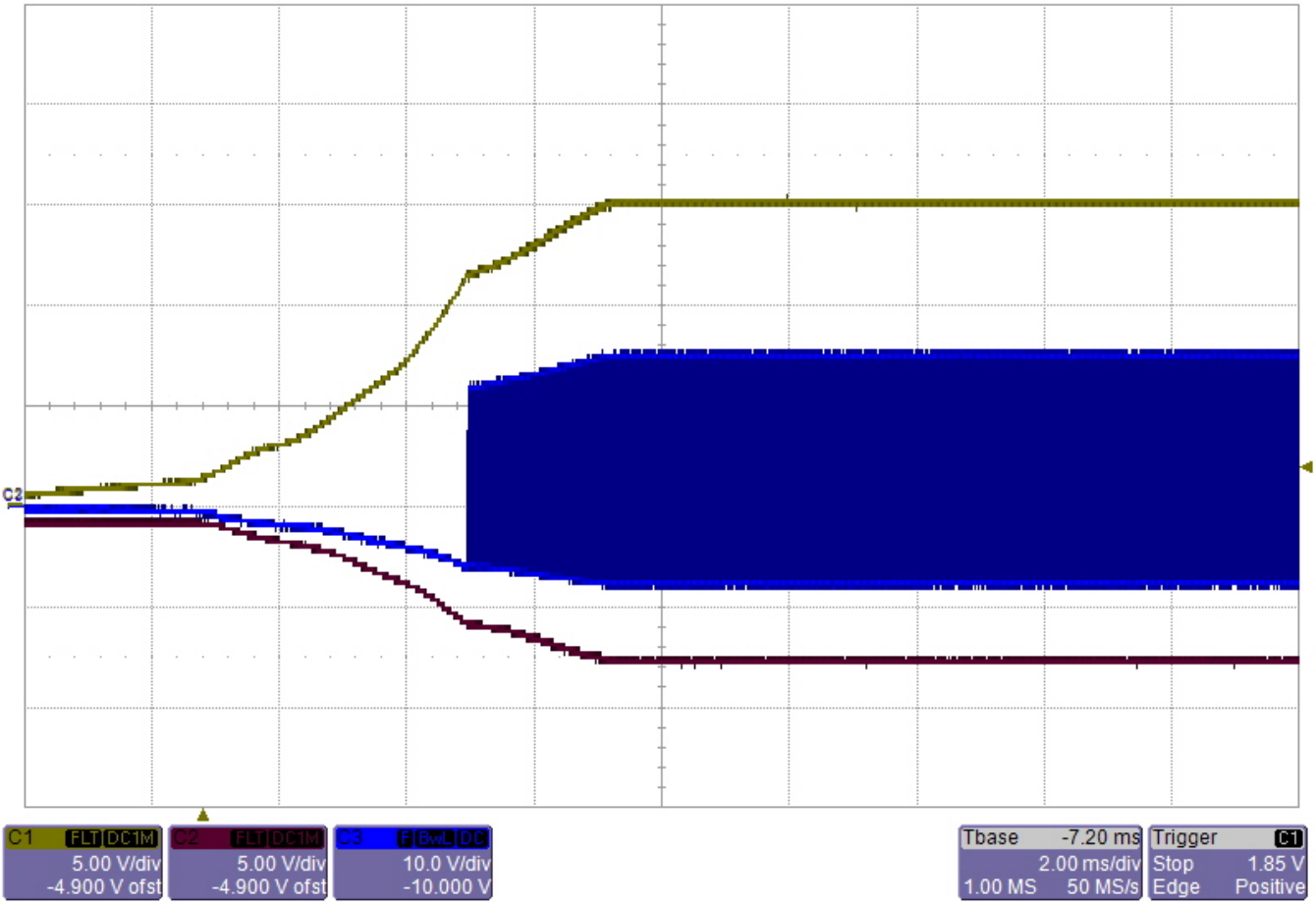


From top to bottom: CH4: input voltage 5 V/div, CH1: 15-V rail 5 V/div, CH2: -8-V rail 5 V/div, time scale: 2 ms/div

3.2.1.2 Isolated Gate Driver Output

図 15 shows the startup of the isolated gate driver PWM output signal measured together with the bias supply rails. PWM output is switched at 30 kHz.

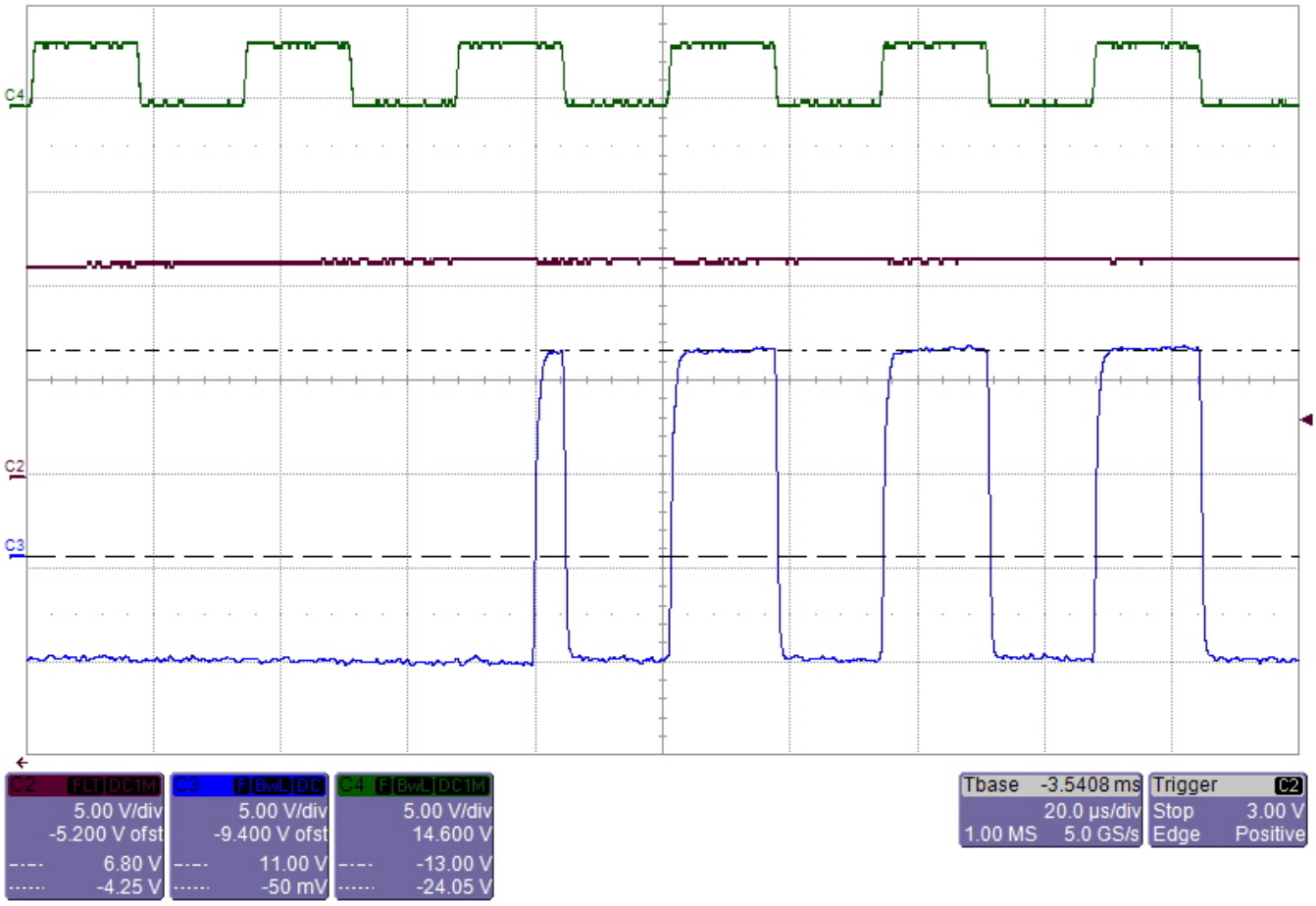
図 15. Startup of Isolated Gate Driver PWM Output Together With the Bias Supply Rails



From top to bottom: CH1: 15-V rail 5 V/div, CH3: isolated gate driver PWM output 10 V/div, CH2: -8-V rail 5 V/div, time scale: 2 ms/div

図 16 shows the startup of the isolated gate driver output with the 15-V bias supply rail. It shows that the isolated gate driver PWM output starts at 11 V.

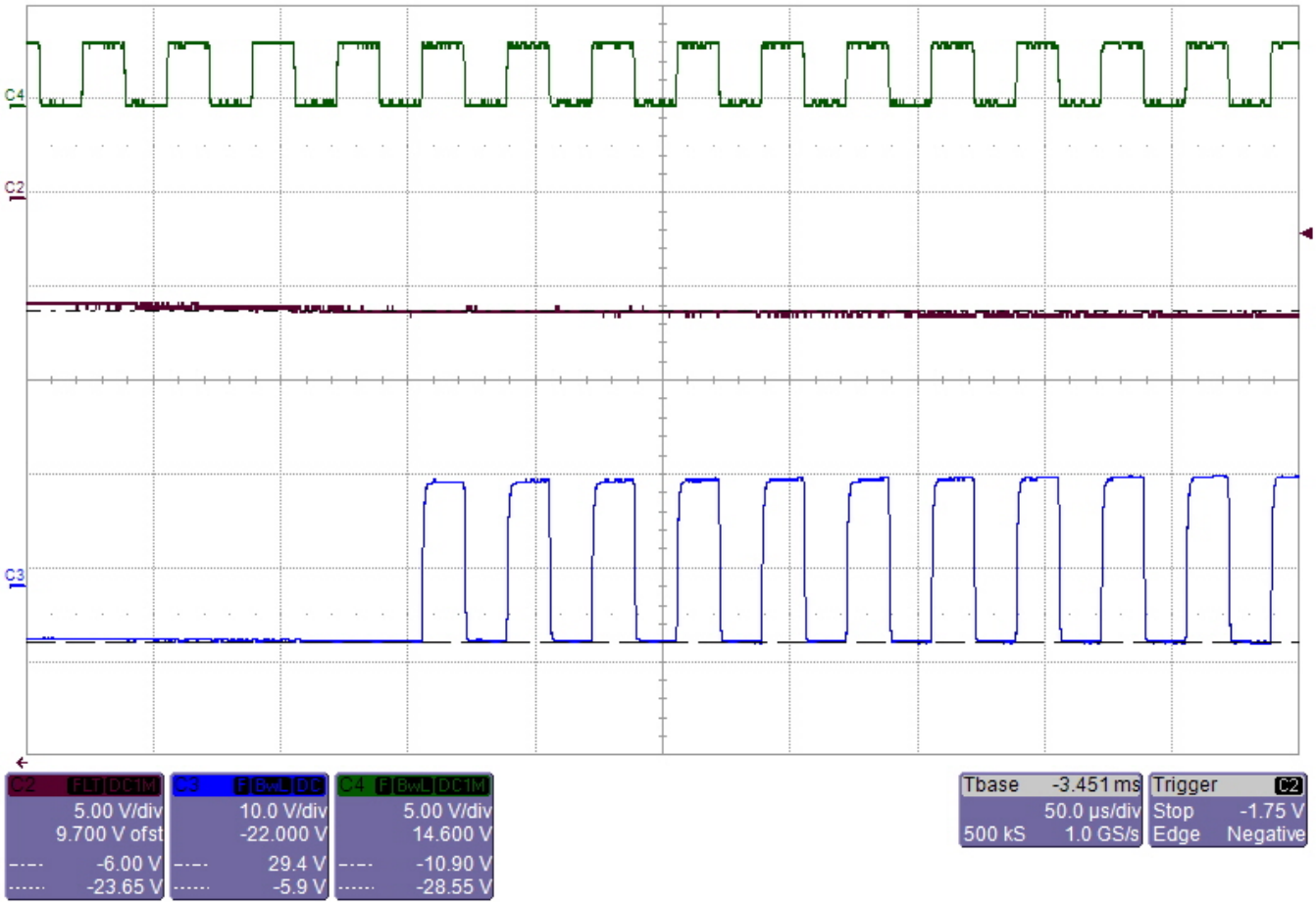
図 16. Startup of Isolated Gate Driver PWM Output Together With the 15-V Rail



From top to bottom: CH4: PWM input signal 5 V/div, CH2: 15-V rail 5 V/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 20 µs/div

図 17 shows the startup of the isolated gate driver output with the -8-V bias supply rail. It shows that the isolated gate driver PWM output starts at -5.9 V.

図 17. Startup of Isolated Gate Driver PWM Output Together With the -8-V Rail



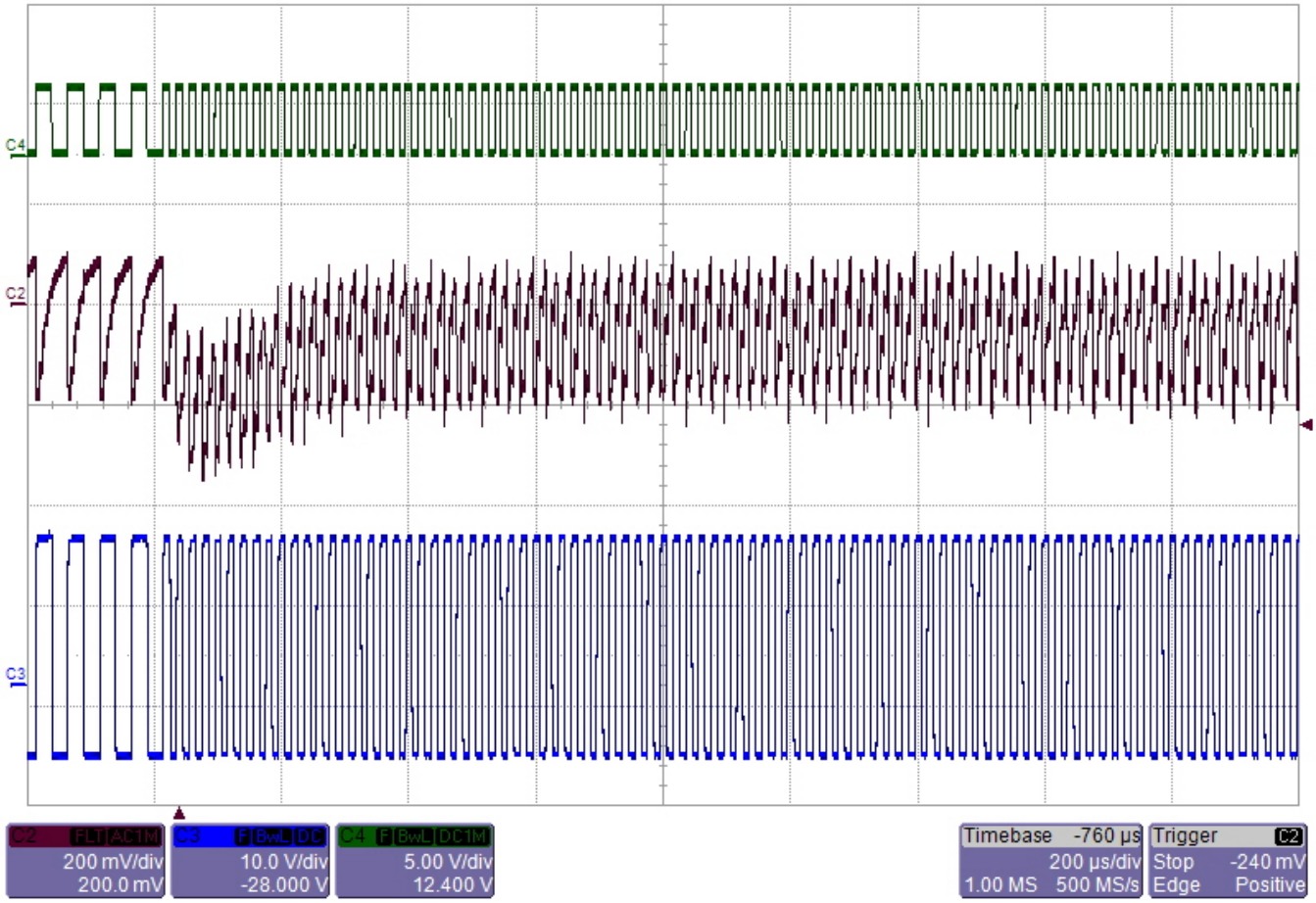
From top to bottom: CH4: PWM input signal 5 V/div, CH2: -8-V rail 5 V/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 20 µs/div

3.2.2 Bias Supply Load Transients

The bias supplies are measured under different load transient conditions. The 15-V and -8-V rails are measured separately.

図 18 shows the load transient of the 15-V bias supply rail when PWM switching frequency increases from 20 kHz to 50 kHz.

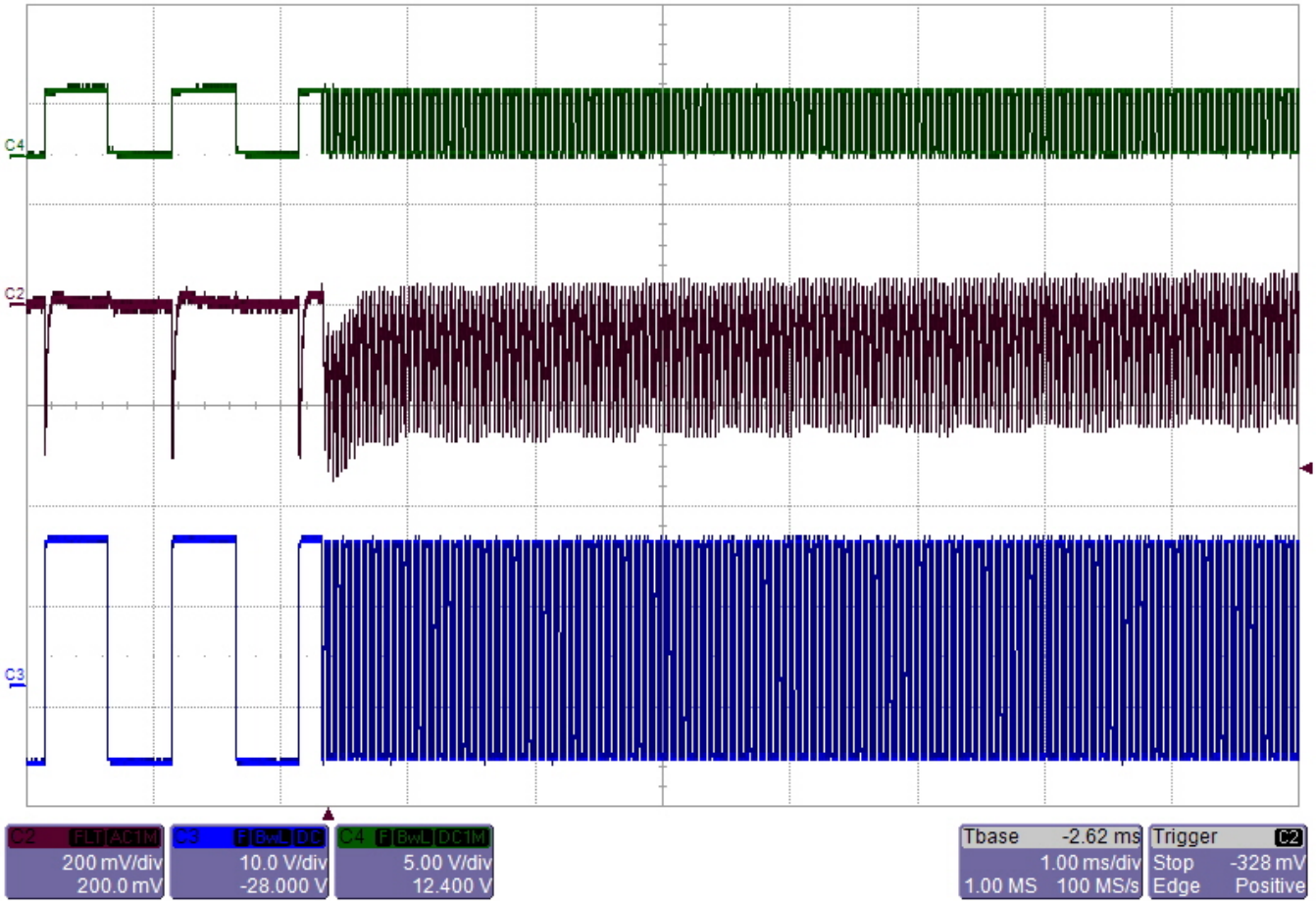
図 18. Load Transient of the 15-V Bias Supply Rail With PWM Switching Frequency Increasing From 20 kHz to 50 kHz



From top to bottom: CH4: PWM input signal 5 V/div, CH2: 15-V rail 20 0mV/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 200 µs/div

図 19 shows the load transient of the 15-V bias supply rail when PWM switching frequency increases from 1 kHz to 30 kHz.

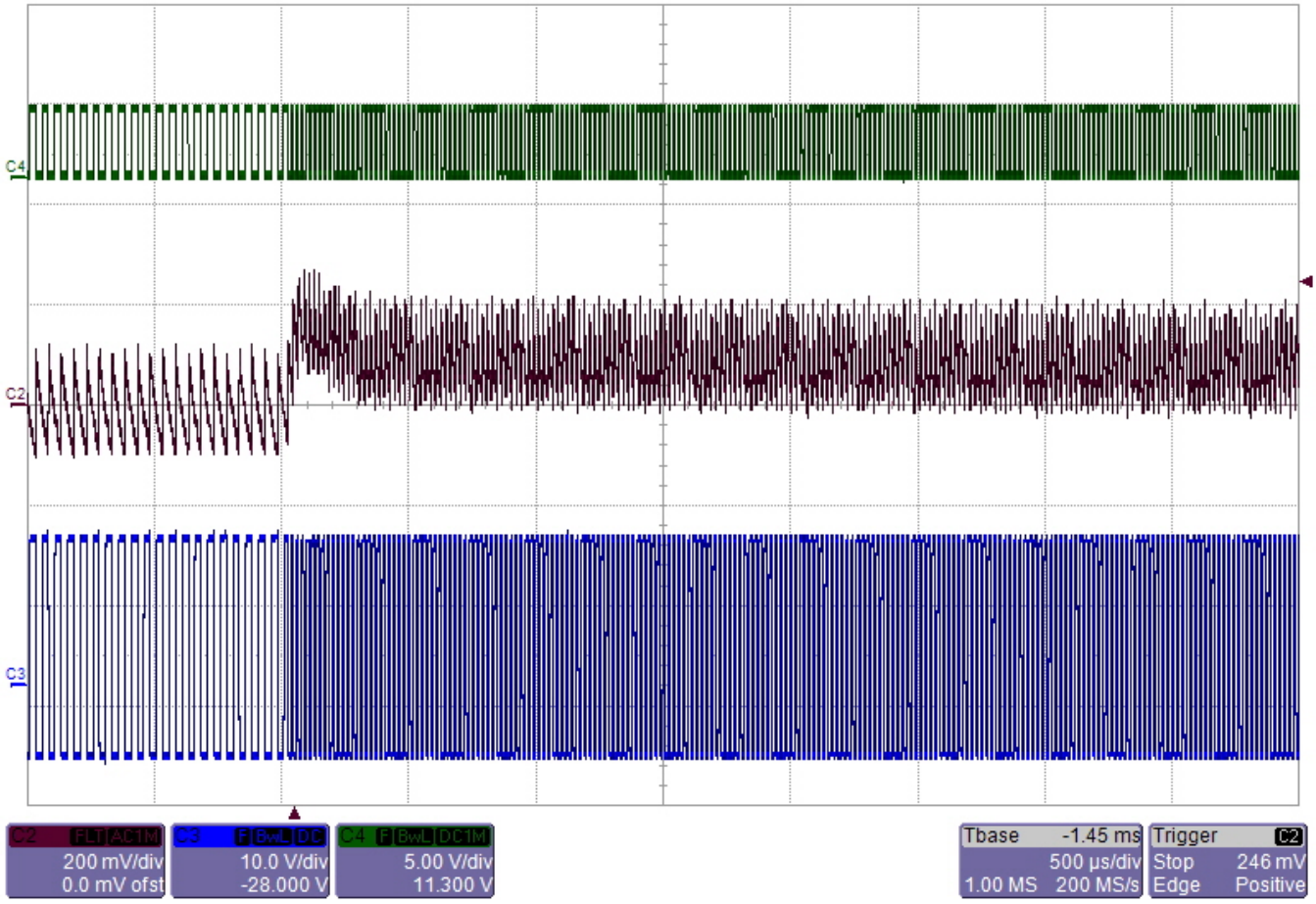
図 19. Load Transient of the 15-V Bias Supply Rail With PWM Switching Frequency Increasing From 1 kHz to 30 kHz



From top to bottom: CH4: PWM input signal 5 V/div, CH2: 15-V rail 200 mV/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 1 ms/div

図 20 shows the load transient of the -8-V bias supply rail when PWM switching frequency increases from 20 kHz to 50 kHz.

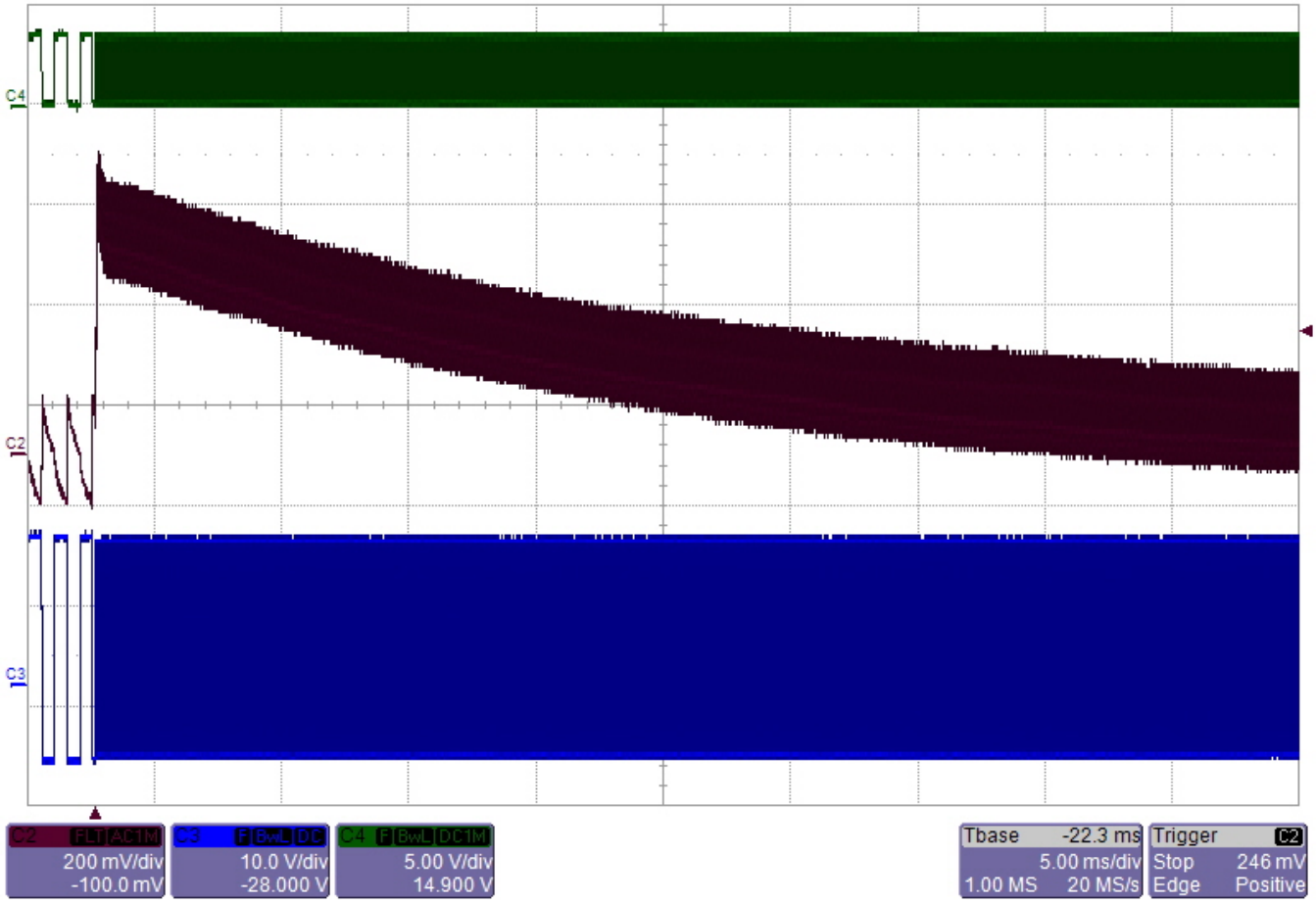
図 20. Load Transient of the -8-V Bias Supply Rail With PWM Switching Frequency Increasing From 20 kHz to 50 kHz



From top to bottom: CH4: PWM input signal 5 V/div, CH2: -8-V rail 200 mV/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 500 µs/div

図 21 shows the load transient of the -8-V bias supply rail when PWM switching frequency increases from 1 kHz to 30 kHz.

図 21. Load Transient of the -8-V Bias Supply Rail With PWM Switching Frequency Increasing From 1 kHz to 30 kHz

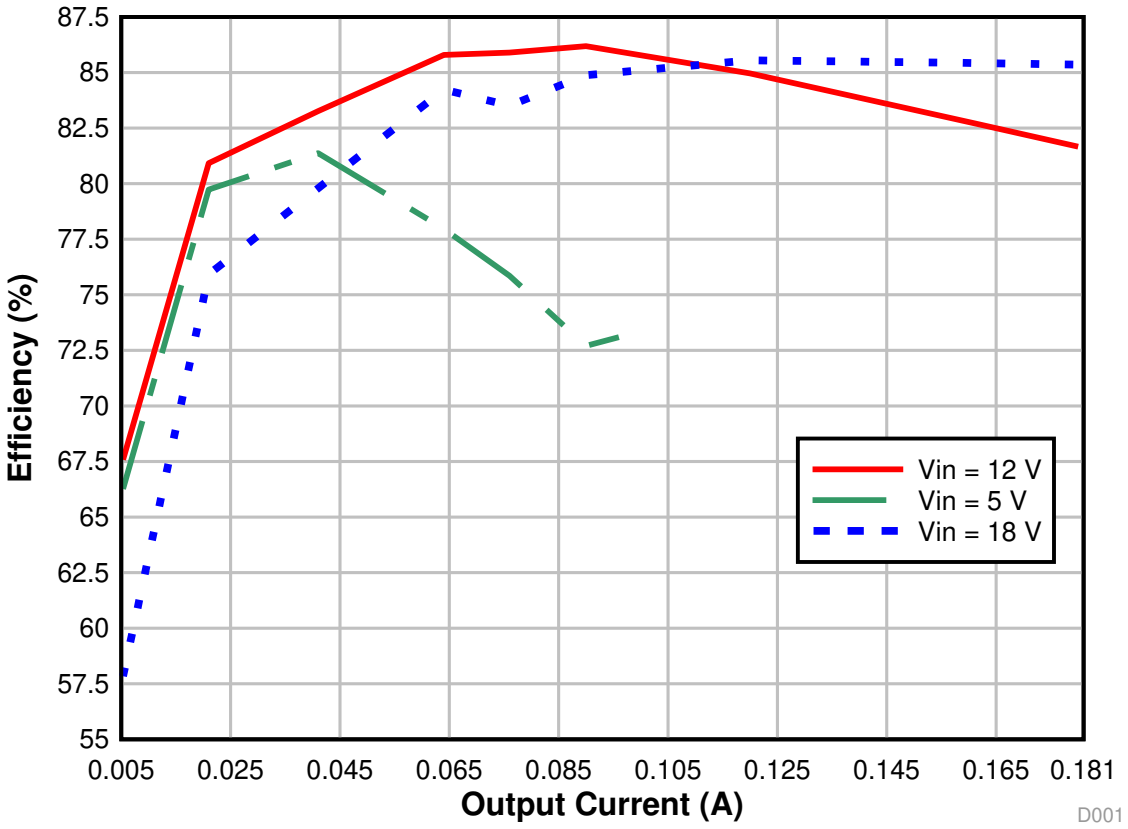


From top to bottom: CH4: PWM input signal 5 V/div, CH2: 15-V rail 200 mV/div, CH3: isolated gate driver PWM output 10 V/div, time scale: 5 ms/div

3.2.3 Bias Supply Efficiency

図 22 shows the measured efficiency of the bias supply rails over the full load range. As can be seen around 86%, peak efficiency is achieved with the input voltages of 5 V, 12 V and 18 V respectively.

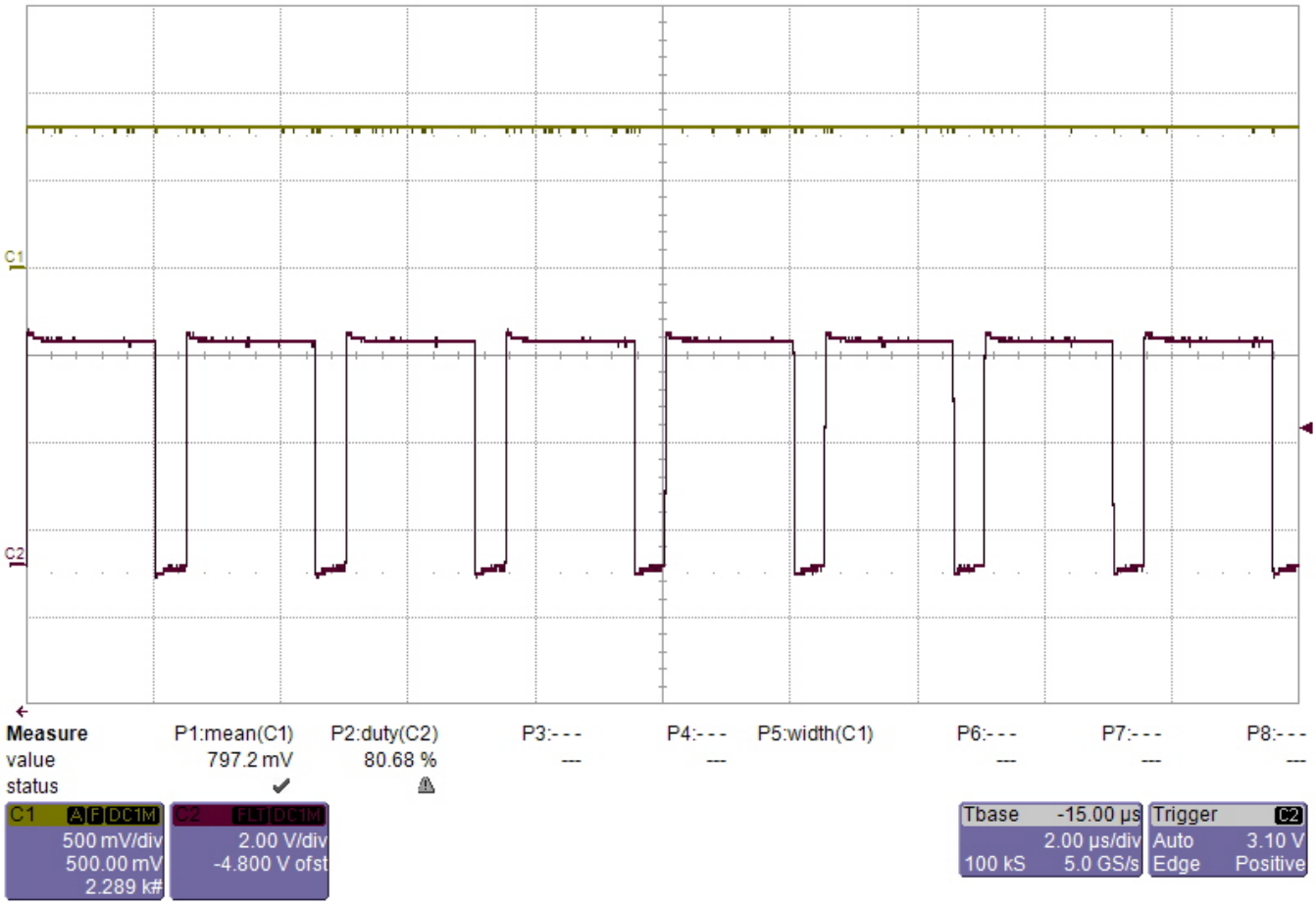
図 22. Measured Bias Supply Efficiency Under Input Voltages of 5 V, 12 V, and 18 V



3.2.4 DC Bus Sensing

The DC bus voltage is measured using the analog-to-PWM converter from the isolated driver and also from the isolated amplifier AMC1311-Q1. The waveforms are shown in 図 23.

図 23. Waveform of the Isolated Amplifier AMC1311-Q1 Output and the APWM Pin of the UCC21732-Q1 (120-V Bus Voltage)



From top to bottom: CH1: AMC1311-Q1 output 500 mV/div, CH2: APWM pin of UCC21732-Q1 duty cycle = 80.68%, time scale: 2 µs/div

DC bus voltage measurements using different sensing circuits are shown in 表 3.

表 3. Measured Data of DC Bus Voltages

DC BUS VOLTAGES (V)	0	50	100	125
APWM analog value (V)	4.317	4.192	4.071	4.01
AMC output (V)	0.544	0.645	0.744	0.794
APWM duty cycle (%)	86.80%	84.40%	81.96%	80.60%

3.2.5 Thermal Diode Sensing

The thermal diode output is sensed through the analog-to-PWM converter from the isolated gate driver and also from an external A-to-D converter (ADS7049-Q1) respectively. The schematic is shown in 図 8. The measurement data is shown in 表 4 and 表 5 respectively.

表 4. Thermal Diode Sensing Data Measured From APWM Pin of the Isolated Gate Driver

IGBT CASE TEMPERATURE (℃)	APWM PIN OUTPUT (%)	APWM CHANNEL (V)	POWER LOSSES ON THE IGBT (W)
25	59.95%	2.8859	0
43.2	60.59%	3.013	1.17832
48.7	60.90%	3.027	2.27362
55.8	61.42%	3.052	3.36532
63.6	61.89%	3.076	4.42389
65.7	62.16%	3.091	6.8154
72	62.62%	3.113	8.76435
80.7	63.45%	3.153	11.67854

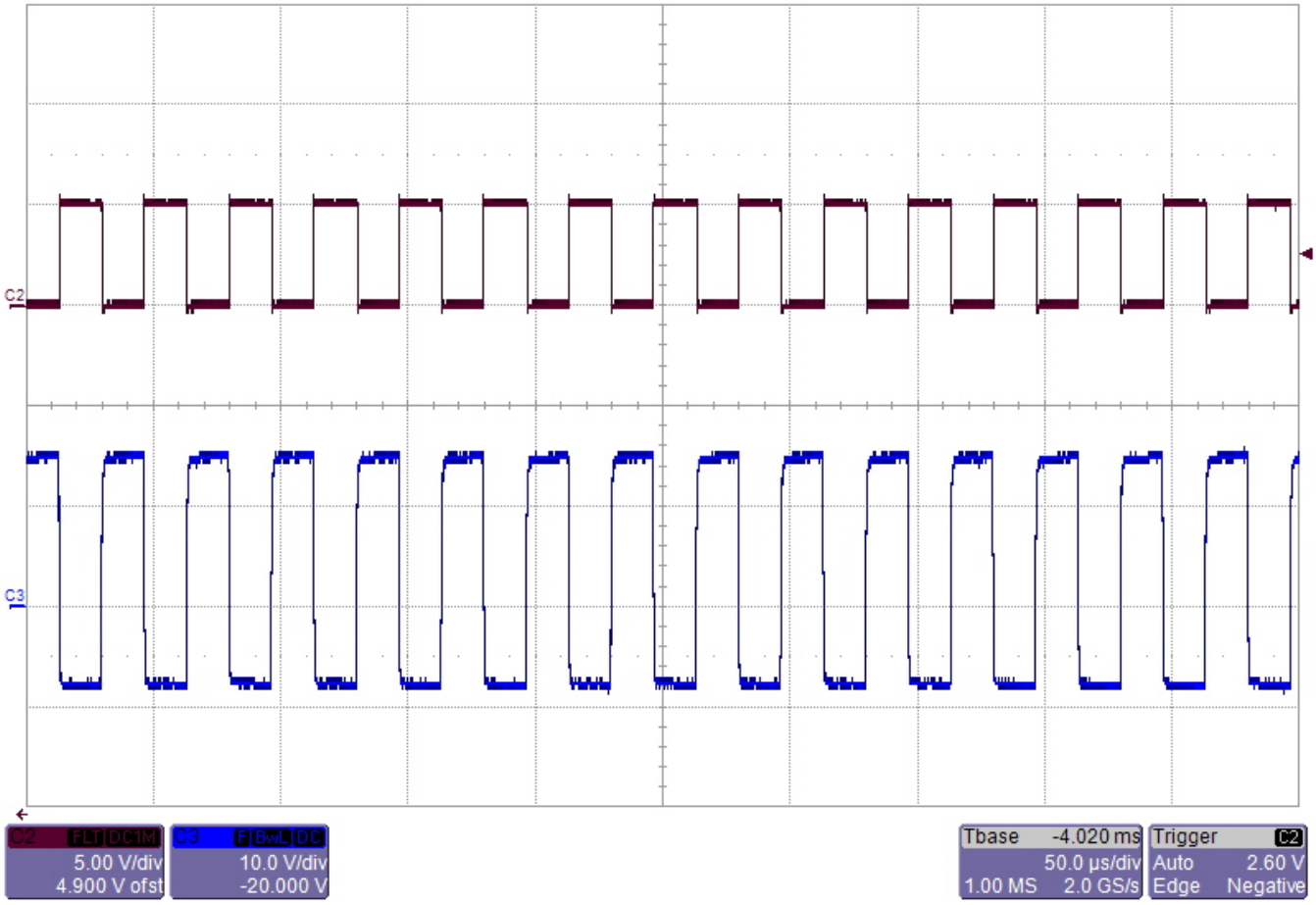
表 5. Thermal Diode Sensing Data Measured From the ADS7049-Q1

IGBT CASE TEMPERATURE (℃)	VOLTAGE MEASURED FROM MULTIMETER (V)	ADC OUTPUT (V)	POWER LOSSES ON THE IGBT (W)
25	2.8282	2.8359	0
48.7	2.70	2.707	2.64576
56.8	2.659	2.6651	4.07838
63.2	2.599	2.6039	5.93712
66.2	2.5633	2.5717	7.22202
71.8	2.522	2.5257	8.42072
74.8	2.4969	2.5056	9.3972
80.1	2.4604	2.4613	10.58616

3.2.6 Gate PWM Detection

The PWM detection circuit output is compared with gate PWM waveform, which is shown in 図 24.

図 24. Output Waveform of the PWM Detection Circuit

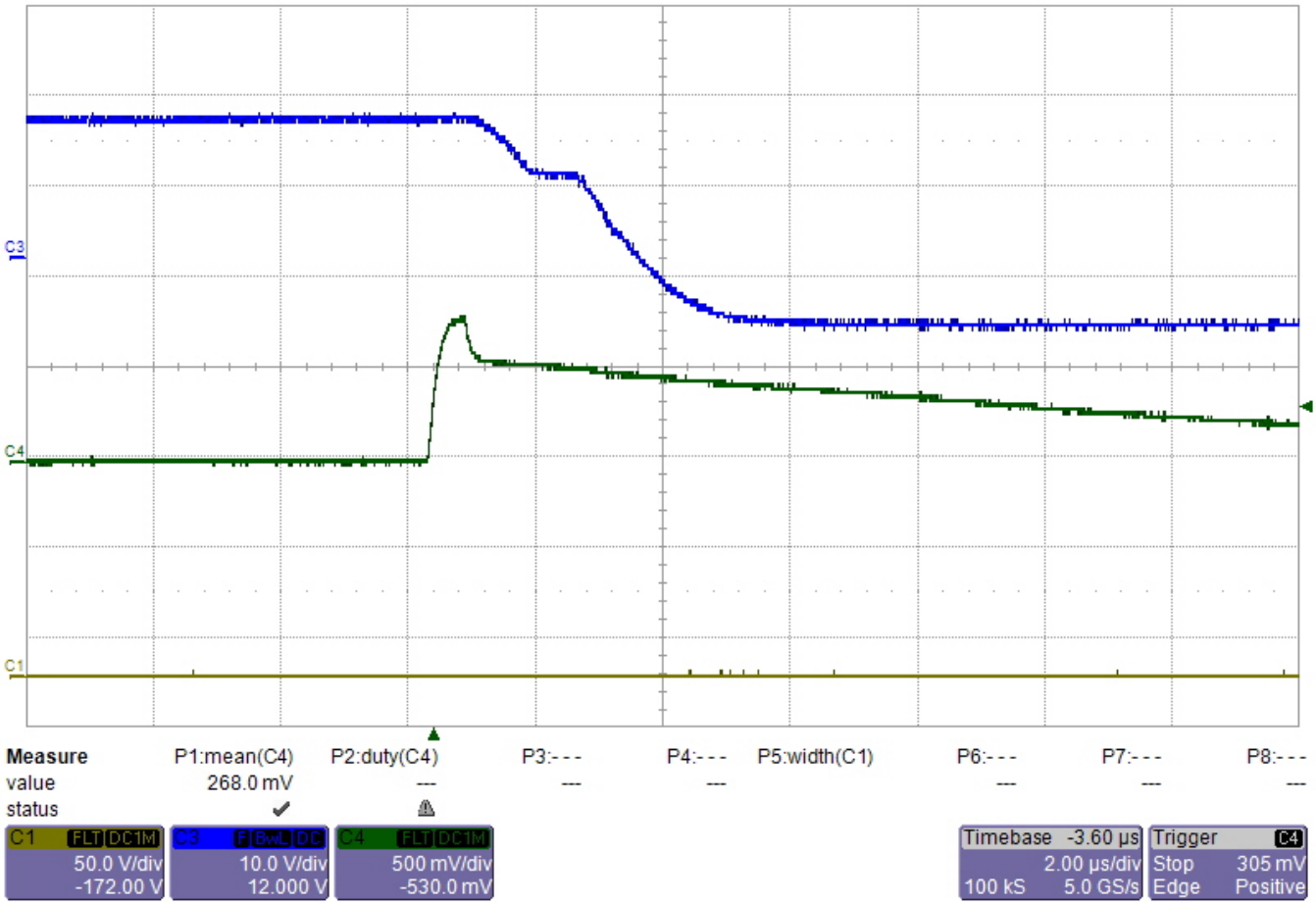


From top to bottom: CH2: PWM detection circuit output 5 V/div, CH2: Gate driver PWM output 10 V/div, time scale: 50 µs/div

3.2.7 Fault Injection Circuit

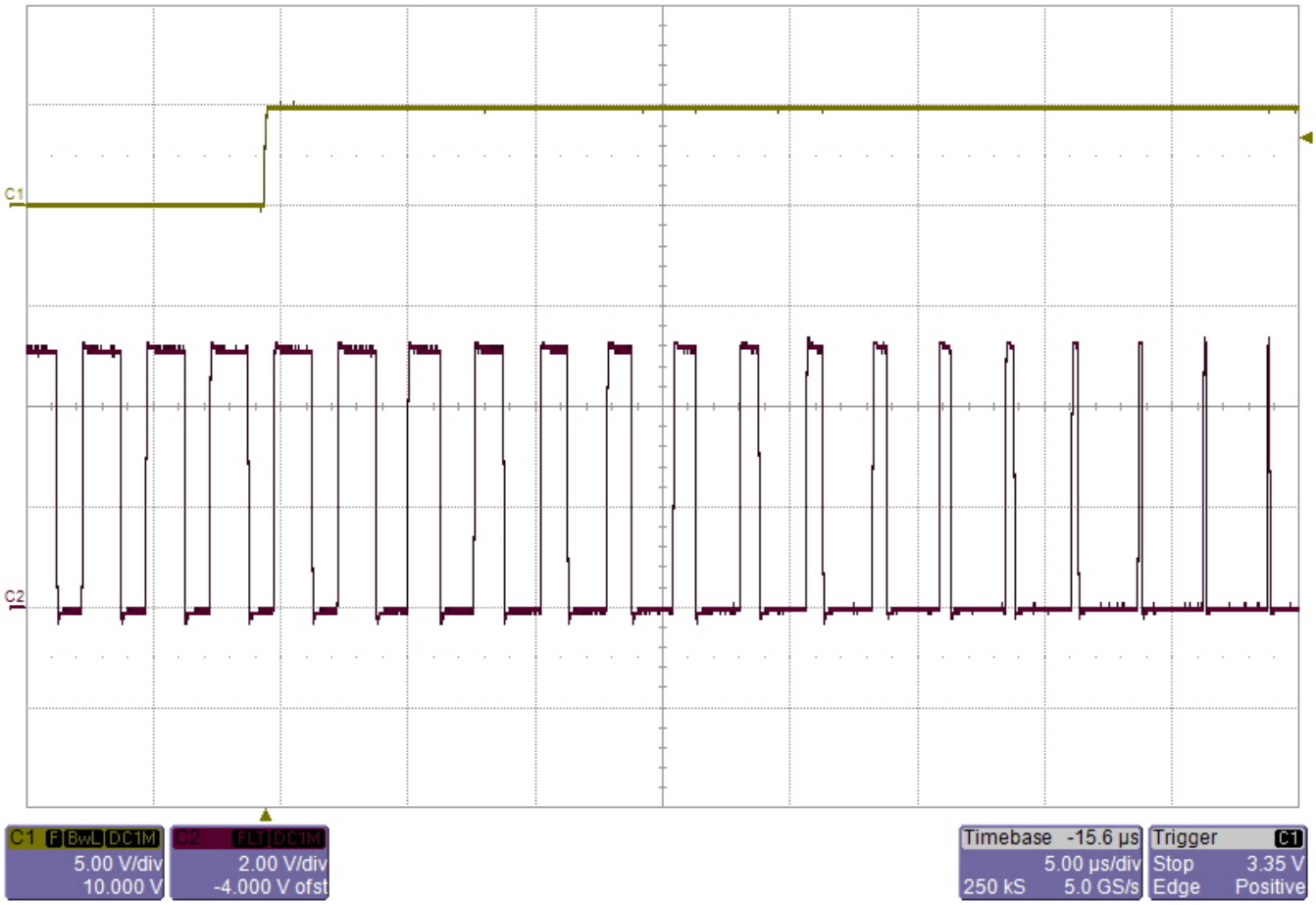
The waveforms of the isolated gate driver output with the corresponding fault injection are measured and shown in this section. 図 25 shows the driver PWM output with overcurrent injection. 図 26 shows the gate driver APWM pin output with a 5-V injection to the AIN pin. 図 27 shows the gate driver APWM pin output with a 0-V injection to the AIN pin.

図 25. Driver PWM Output With Over-current (OC) Injection



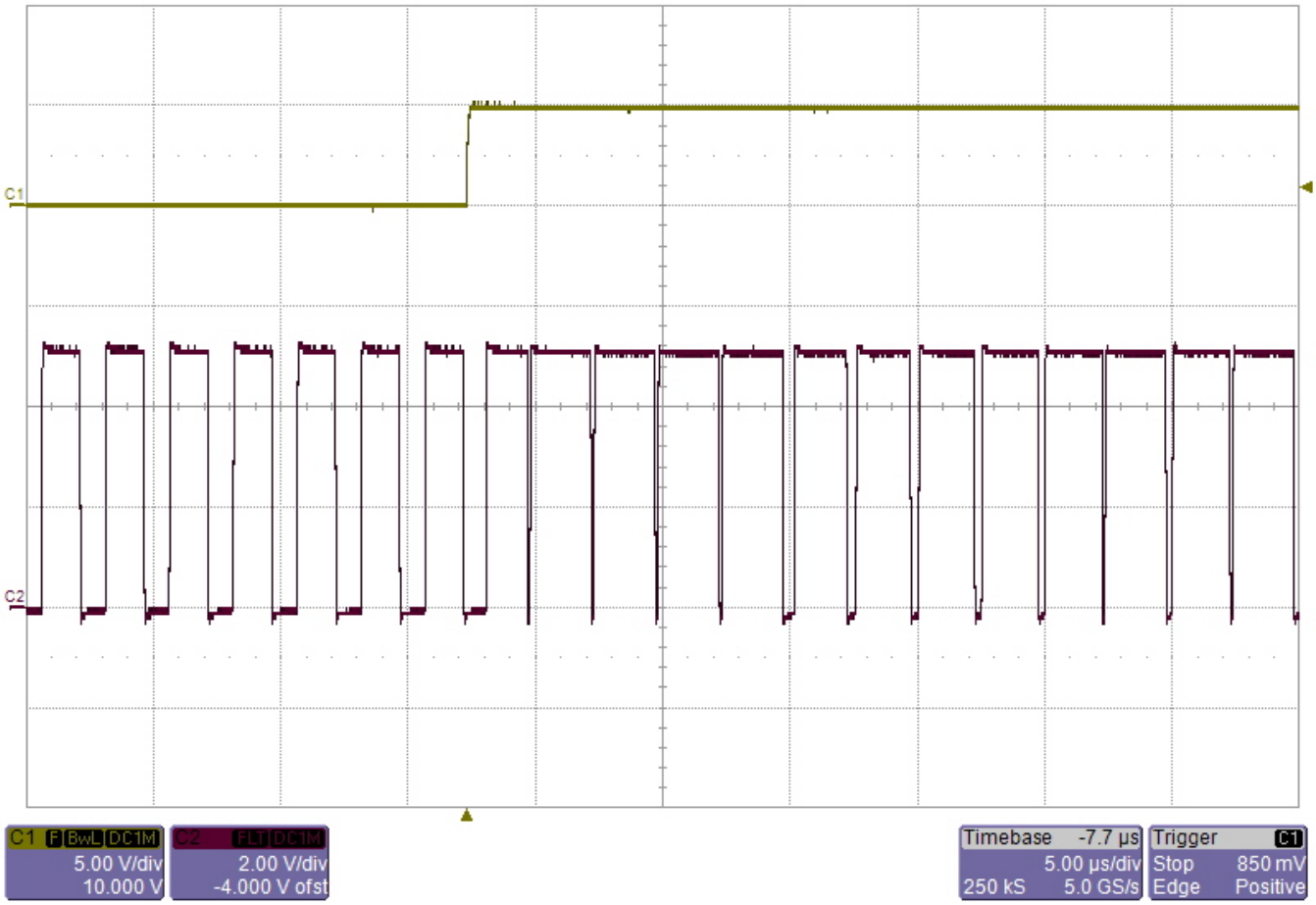
From top to bottom: CH3: Gate driver PWM output 10 V/div, CH4: OC injection signal to the OC pin 10 V/div, time scale: 2 µs/div

図 26. Gate Driver APWM Pin Output With 5-V Injection to the AIN Pin



From top to bottom: CH1: 5-V injection signal 5 V/div, CH2: Gate driver APMW pin output 2 V/div, time scale: 5 µs/div

図 27. Gate Driver APWM Pin Output With 0-V Injection to the AIN Pin



From top to bottom: CH1: 0-V injection signal 5 V/div, CH2: Gate driver APMW pin output 2 V/div, time scale: 5 µs/div

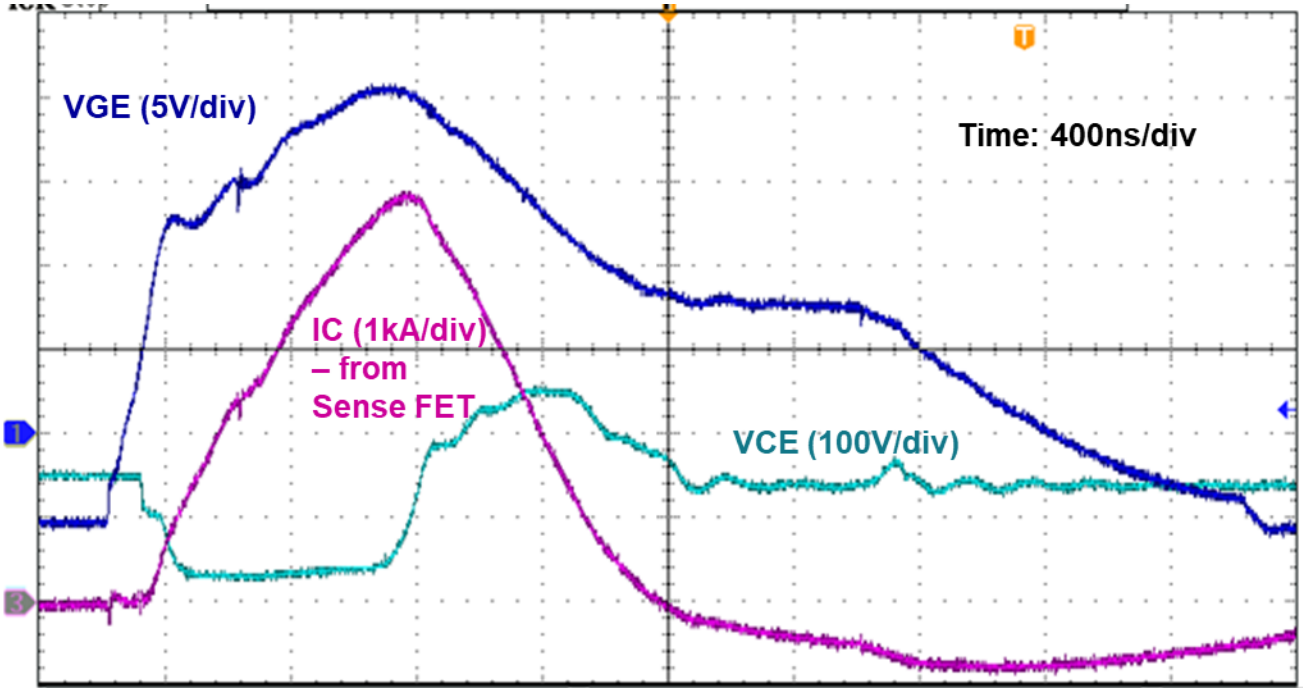
3.2.8 Double Pulse Test

The double pulse test is performed under high voltage to evaluate the switching parameters of the IGBT and the performance of the isolated gate driver. The test is considered as one periodical snapshot of the system, and it is done with a purely inductive load. The driver parameters of switching speed, thermal, oscillation or not can be observed.

3.2.9 IGBT Safe Shutdown

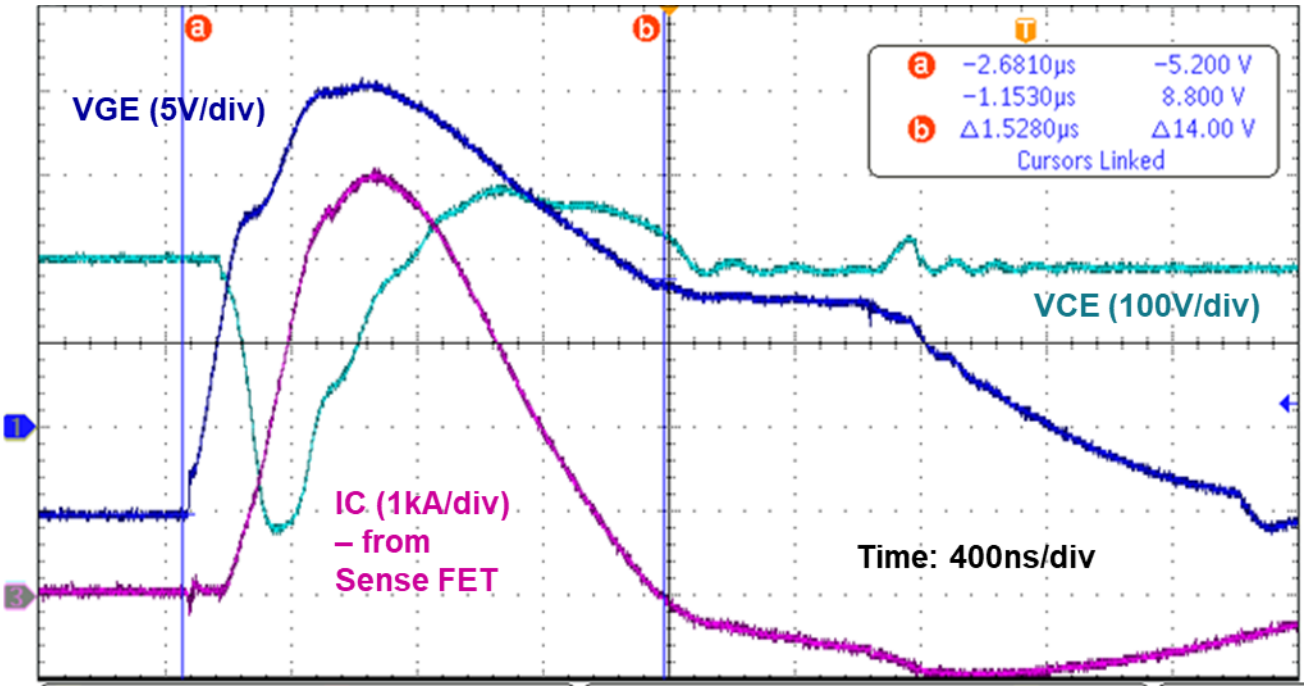
The IGBT module is turned on into short to measure the protection performance from the isolated gate driver. The high-side IGBT is constantly turned on with a battery voltage imposed on the gate. The low-side IGBT is pulsed once and turned on into short. The IGBT is switched with a 150-V DC bus and 400-V DC bus voltage respectively. The gate driver enters a two-level turnoff protection once the OC threshold is triggered.

図 28. IGBT Safe Shutdown Under 150-V DC Bus Voltage



From top to bottom: CH1: IGBT gate-to-source voltage 5 V/div, CH2: IGBT drain-to-source voltage 100 V/div, CH3: Current sense FET output 1 kA/div, time scale: 400 ns/div

図 29. IGBT Safe Shutdown Under 400-V DC Bus Voltage



From top to bottom: CH1: IGBT gate-to-source voltage 5 V/div, CH2: IGBT drain-to-source voltage 100 V/div, CH3: Current sense FET output 1 kA/div, time scale: 400 ns/div

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020030.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-020030.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

The TIDA-020030 implements a 4-layer PCB. To download the layer plots, see the design files at TIDA-020030.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-020030.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020030.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-020030.

5 Related Documentation

1. Texas Instruments, *HEV/EV Traction Inverter Power Stage With 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design* (TIDA-020014)
2. Texas Instruments, *98.6% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger* (TIDA-01604)
3. Texas Instruments, *Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection* (TIDA-01605)

5.1 商標

5.2 Third-Party Products Disclaimer

6 Terminology

AFE – Analog Front End

AEC – Automotive Electronics Council

ESR – Equivalent Series Resistance

EMI – Electromagnetic Interference

EMC – Electromagnetic Compatibility

DM – Differential Mode

CM – Common Mode

UVLO – Under Voltage Lockout

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

CISPR – International Special Committee on Radio Interference

PE – Protective Earth

RMS – Root Mean Square

ISO – International Organization for Standardization

BOM – Bill of Material

OEM – Original Equipment Manufacturer

AN – Artificial Network

LISN – line impedance stabilization network

EUT – Equipment Under Test

PCB – Printed Circuit Board

HEV – Hybrid Electric Vehicle

EV – Electric Vehicle

7 About the Author

XUN GONG is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for HEV/EV Powertrain applications. Xun brings to this role expertise in the field of Onboard Charger, DC/DC Converter, and Traction Inverter with IGBT and SiC (Silicon Carbide) power transistors. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the 1st prize paper of the Academic Journal IEEE Transactions on Power Electronics in 2014.

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