参考資料

Design Guide: TIDA-010085

*デジタル・アイソレータを使用した **24VAC** マルチチャネル・ソリッド ステート・リレーのリファレンス・デザイン*

概要

本リファレンス・デザインは、単一の絶縁を使用するマルチチャネル半導体リレー (solid state relay、SSR) を提示します。本リファレンス・デザインでは、複数の SSR を独立して制御するため、単一絶縁型電源と共通グランド・ゲート駆動回路を備えたマルチチャネル・デジタル・アイソレータを使っています。本リファレンス・デザインでは、24VAC 駆動リレーの電流定格は最大 2A です。しかし、最大 240VAC かつより大きい電流定格に拡張することもできます。各 SSR チャネルの専有面積は 75mm^2 未満であり、各部品の最大の高さは約 3mm なので、電磁リレーに比べるとかなりのサイズ縮小を実現できます。単一の絶縁型電源採用で、ボード面積の縮小と BOM (部品表) コストの削減に貢献します。

リソース

TIDA-010085	デザイン・フォルダ
ISO7760、ISO7740	プロダクト・フォルダ
CSD19538Q2、CSD17382F4	プロダクト・フォルダ
TPL7407LA	プロダクト・フォルダ
TLV760、TLC555	プロダクト・フォルダ

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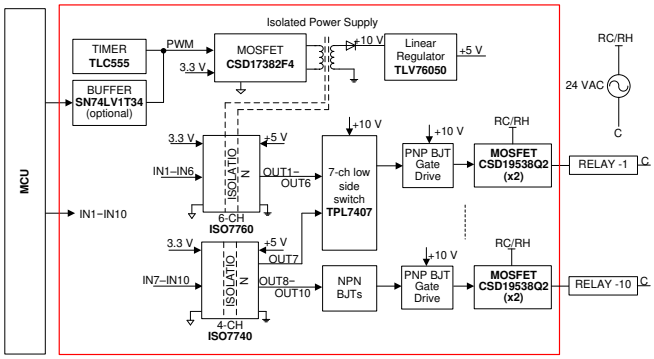
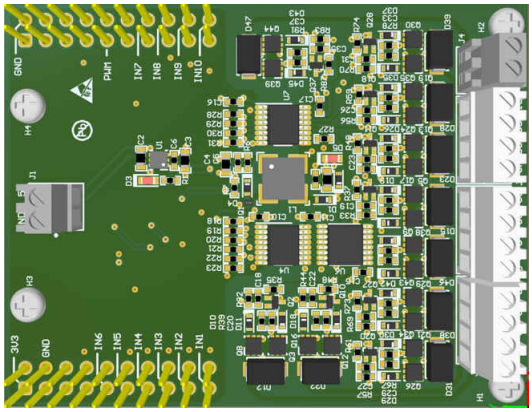
特長

- マルチチャネル・デジタル・アイソレータによる単一絶縁を使った複数の半導体リレーを、最小限の追加コストで任意の数の SSR チャネルに容易に拡張可能
- SSR ドライブの電圧は 24VAC ±20%、ドライブ電流は 2A RMS (電圧と電流の定格は、適切な定格の部品を使用する方法でスケール化可能)
- SSR のターンオン時間とターンオフ時間：15～300µs (調整可能)、SSR ドライブあたりの平均消費電流は (1 次側を基準として) 4mA 未満 (チャネルあたり最小 20µA まで調整可能)
- SSR のチャネルあたり面積は 75mm^2 未満。高さは約 3mm
- 機能的に絶縁された低コストの開ループ・フライバックに基づく電源。マイコン不要
- サージとスイッチング過電圧の保護機能を搭載

アプリケーション

- サーモスタット
- HVAC コントローラ





1 System Description

1.1 Key System Specifications

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
AC load voltage (RMS)	24 V	**Scalable with component selection**
Load current (RMS)	1 A	**Scalable with component selection**
MCU side voltage	3.3 V	**Works with 5-V MCU voltage, as well**
Quiescent current per SSR channel (MCU side)	0.02–4 mA	**Based on the turn on and turn off speed**
SSR turn on time	15–300 µs	**Adjustable**
SSR turn off time	15–300 µs	**Adjustable**
Board size per SSR	60–80 mm^2	**Based on the turn on and turn off speed**
Surge specification	1.2 kV	**Using a 40-V MOV onboard**
Operating temperature	–10°C to 70°C	

2 System Overview

A solid-state relay (SSR) is an electronic switching device that switches on or off when a small external voltage is applied across its control terminals. SSRs consist of an input logic to respond to an appropriate input (control signal), a solid-state electronic switching device to switch power to the load circuitry, and a coupling mechanism to enable the control signal to activate this switch without mechanical parts. The SSR may be designed to switch either AC or DC to the load. The SSR serves the similar function as an electromechanical relay (EMR), but has no moving parts. SSRs use power semiconductor devices such as thyristors or transistors as power switches. SSRs have fast switching speeds compared with electromechanical relays and have no physical contacts to wear out. The life of an SSR is much longer compared to an EMR, as the life of EMR is limited by the switching cycle. The control signal must be coupled to the controlled circuit (SSR power switches) in a way that provides galvanic isolation between the two circuits.

Thermostats are used as a user interface and controller in heating ventilation and air –conditioning (HVAC) systems. Thermostats use multiple relays to switch different loads like a heater, fan, compressor, valves, and so forth, as 図 2-1 shows. The electromechanical relays used in thermostats are getting replaced by solid state relays (SSR) due to silent operation, increased life time, faster switching and so on. The number of relays used in a typical thermostat can vary from 3–12 depending upon HVAC system.

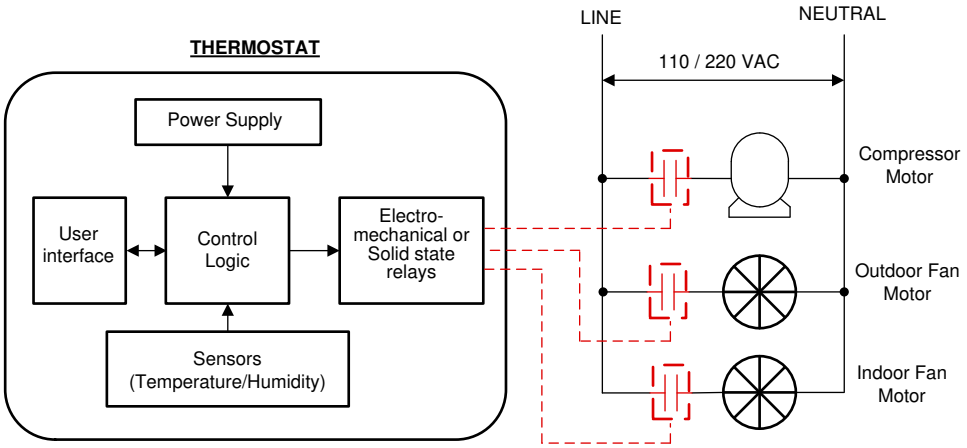


図 2-1. Multiple Relays Controlling Different Loads in Thermostats

Conventional SSRs use functional isolation between each SSR channel to ensure reliable independent control between relays, which causes the solution to take more PCB space at a higher cost. This reference design uses single isolating elements for multiple SSRs, but still enables reliable and independent operation. The single isolation is provided between the microcontroller and the SSR power switches connected to 24 VAC power. The design uses a multichannel digital isolator with a single isolated power supply to control individual SSR channels.

The design is rated for 24 VAC powered relays with current rating up to 2 A; however, this is easily scalable up to 240 VAC and a higher current rating. Each SSR channel consumes less than 75-mm^2 space with the maximum height of the component within around 3 mm, enabling considerable size-savings compared to electromechanical relays. The low-cost open loop flyback to generate the single isolated power supply enables low board space and height. The design is tested for functional operation with 24 VAC power supply, illustrating independent control of each SSR channel without cross-coupling.

2.1 Block Diagram

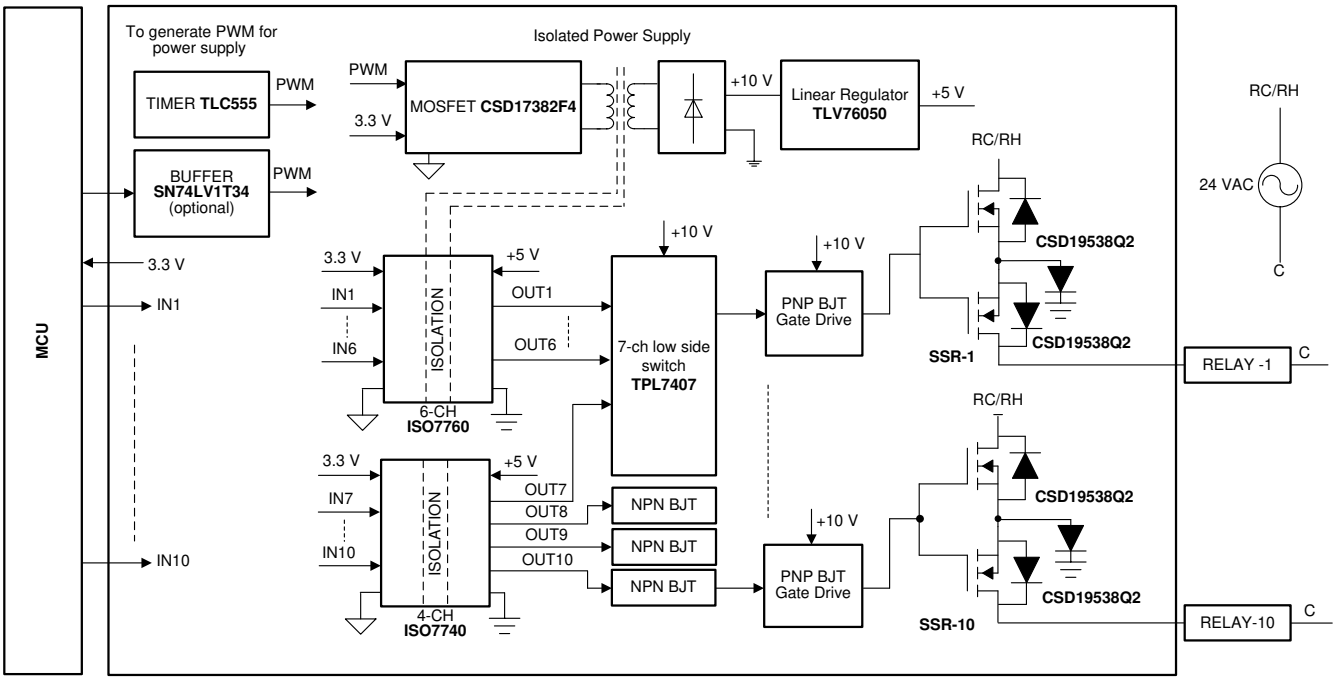


図 2-2. TIDA-010085 Reference Design Block Diagram

2.2 Design Considerations

2.2.1 Multichannel SSR with Independent Isolation Between SSR Channels

Conventional SSR solutions use isolated gate drive power supply for the MOSFETs of each SSR in a multichannel SSR circuit sharing the same AC supply. For example, with a six-channel SSR circuit, the conventional solutions use six isolation elements as shown in 図 2-3, to eliminate potential turn on of relays, when other relays connected in the same AC supply is turned on. The isolation can be realized using independent transformers or optocouplers or capacitive isolators or any other isolation methods. Use of individual isolated gate-drive circuits leads to increased system cost and more board space.

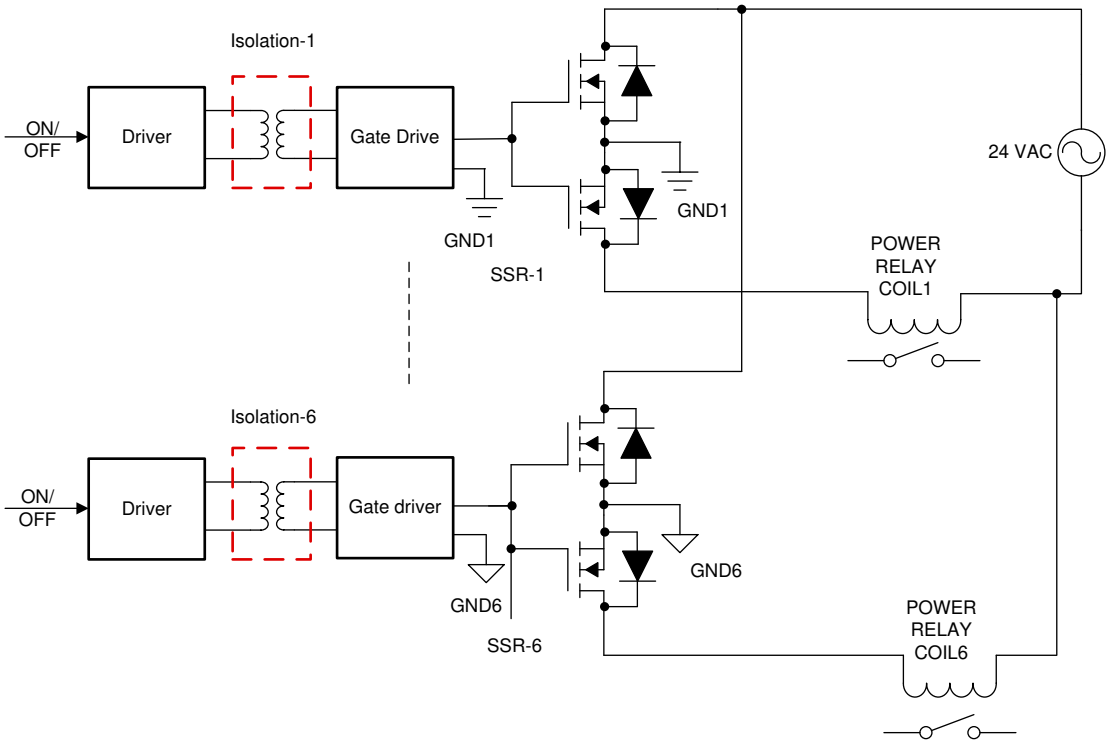


図 2-3. Multichannel SSR Topology With Independent Isolation Between SSR Channels

2.2.2 Design Challenge With Single Isolation

図 2-4 shows the configuration having SSR-1 and SSR-2 MOSFETs using a common ground for the gate drive at secondary of the isolator. Assume that SS-1 is turned on and SSR-2 is kept off. When the SSR-1 is turned on, the common ground at the gate drive causes circulating current through the common ground and the anti-parallel diode of the low-side MOSFET of SSR-2 during the negative half cycle of 24-V AC power supply. The unintentional half wave current flows through load (ILOAD2) connected through SSR-2 (despite being turned OFF), will turn on the SSR-2 load relay in the negative half cycle of input 24-V AC supply. 図 2-4 shows the unintentional half wave rectified current waveform.

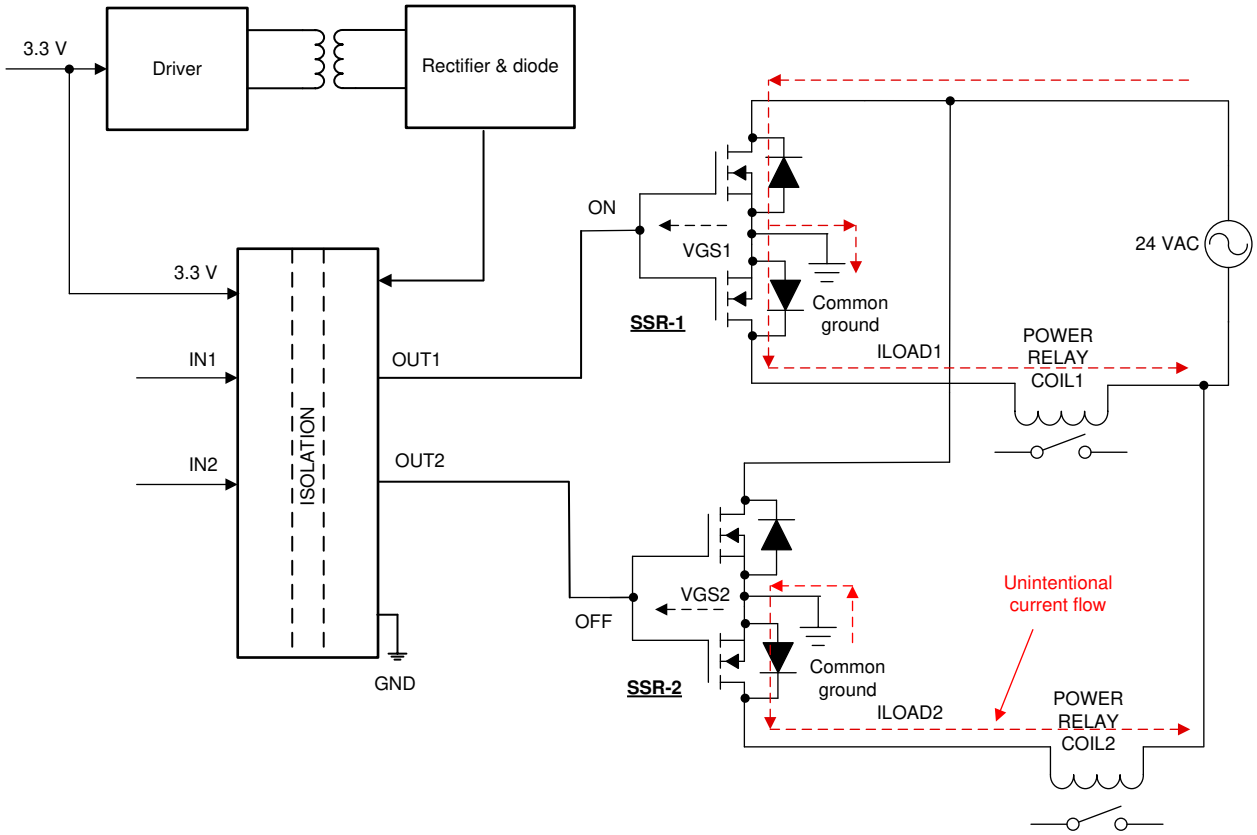


図 2-4. Unintentional Current Flow in Driving Multiple SSR With Common Ground Gate-Drive Supply

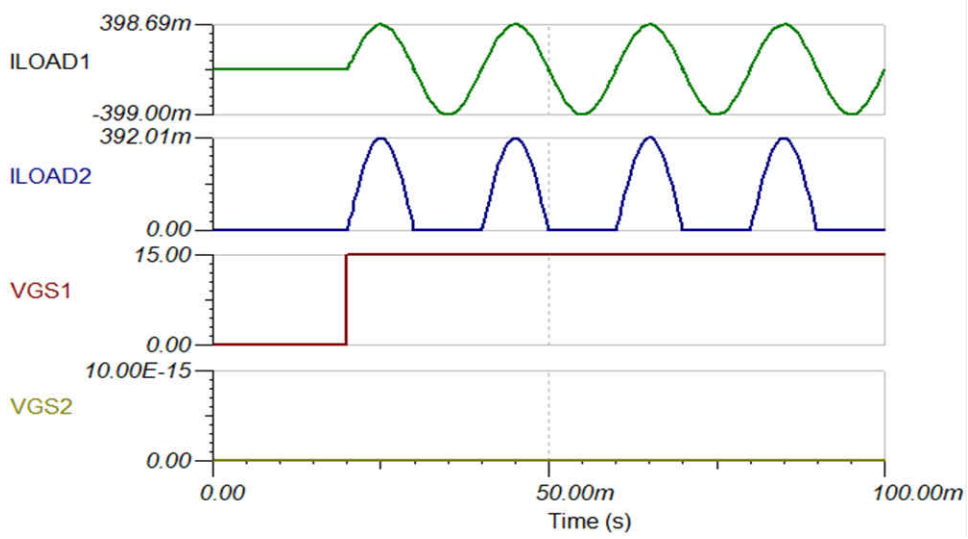


図 2-5. Half-Wave Rectified Current in Driving Multiple SSR With Common Ground Gate-Drive Supply

2.2.3 Multichannel SSR Drive With Single Isolation Multichannel Digital Isolator

図 2-6 shows the topology to drive multiple SSR with single isolating element. In this topology, a 6-channel digital isolator is used to drive six SSR circuits. A single transformer based isolated power supply is used to power the secondary of digital isolator and gate drive. The solution to the problem of unwanted current circulation when one SSR is activated, is to add diodes between common-source of the SSRs to the ground (Blocking diode). Added diodes will prevent load current flow through common ground across multiple SSRs. The diode will block gate discharge of the MOSFET and is solved by adding a PNP transistor circuit and resistor at gate-source of MOSFET. High-impedance voltage translators ensure high-impedance in the MOSFET gate path when digital

isolator output is zero, eliminating an otherwise possible small leakage current, that could lead to a false turn on of MOSFET of other SSRs. The functionality of one SSR does not impact the functionality of another SSR.

The turn off of the SSR MOSFET is done through the resistor connected between the gate and source terminals of the MOSFET pair of each SSR. The MOSFET gate will discharge through the turn off resistor when the gate-drive PNP transistor (Q1, Q2) is turned off. The turn off can be made faster by using a PNP transistor across the gate and source of SSR MOSFET pair. The circuit for faster SSR turn off is marked in 図 2-6 and is optional.

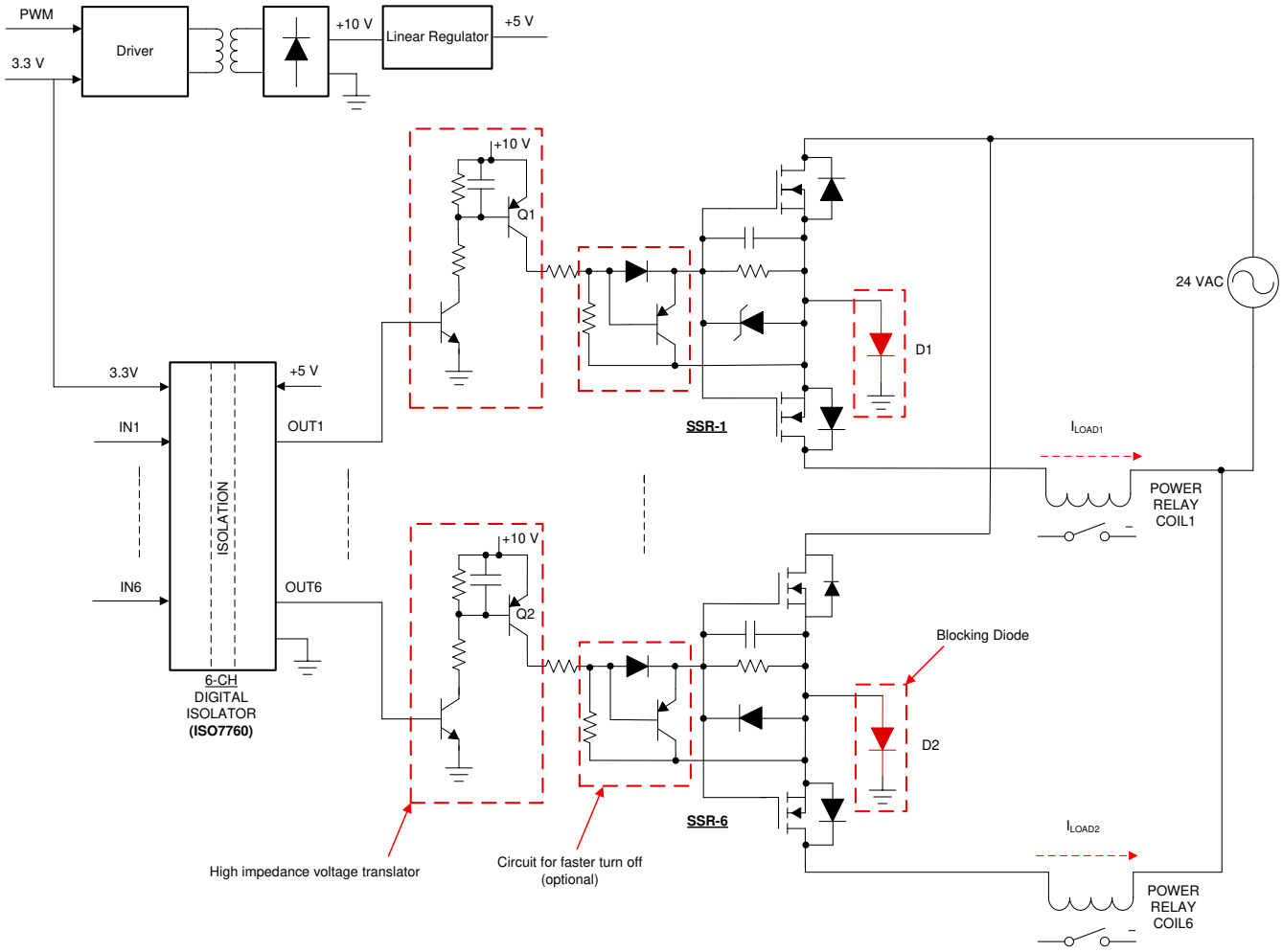


図 2-6. Circuit Topology to Drive Multiple SSR With Single Isolating Element

2.2.4 Need of High-Impedance Voltage Translator

The reference design SSR topology uses the high impedance voltage translator connected between the digital isolator and the SSR MOSFET gate. 図 2-7 illustrates the high-impedance voltage translator consists of a PNP transistor (Q_P) and an NPN transistor (Q_N).

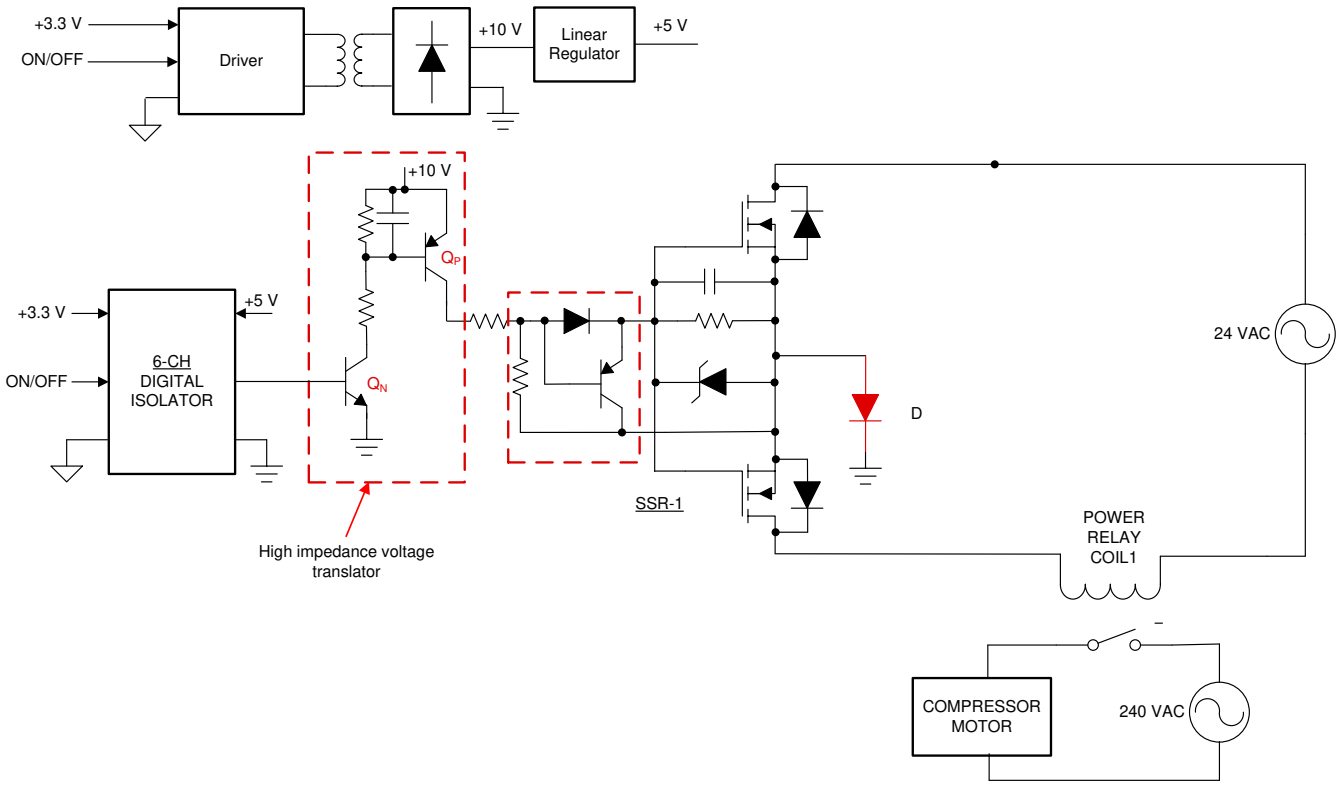


図 2-7. High Impedance Voltage Translator for Driving Multiple SSR With Single Isolating Element

When SSR is switching, the voltage across the blocking diode (D) changes. For a 24-VAC supply, the peak voltage across the blocking diode could be as high as 41 V (considering 20% tolerance on the AC voltage supply). The same voltage level appears across the PNP transistor (Q_P), and hence the PNP transistor has to be rated more than 41 V with sufficient voltage margin. If the digital isolator is used directly to turn on the SSR, the higher voltage will damage the output structure of isolator.

The NPN and the PNP transistor circuit forms the voltage translator circuit, translating the 5 V at the digital isolator output to a higher voltage for the MOSFET gate drive. It is also required that the off-state leakage of the PNP transistor has to be very low so that the resulting voltage drop across the resistor between the gate and source of the SSR MOSFET, is sufficiently less than the worst-case gate threshold voltage of MOSFETs.

2.2.5 Design to Minimize Cross-Coupling and MOSFET Gate Pick up Due to Other SSR Switching

Referring to 図 2-6, consider the scenario where SSR-6 is kept off and SSR-1 is turned on and off. When SSR-1 is switching, the voltage across the blocking diode D2 changes (the voltage change depends on the instantaneous AC voltage). The voltage change dv/dt across the SSR MOSFETs couples to the blocking diode of SSR6 (which is off) and then through the gate-driver power supply (10 V) low impedance path, couples to the gate-drive transistor circuit (Q2). This can cause momentary base current and resulting collector current in Q2, resulting a gate pick up at the MOSFET gate of SSR6 causing the SSR-6 to conduct. One way to reduce cross coupling is by controlling dv/dt during FET switching, by reducing switching turn on and turn off time by adjusting the gate resistor. The reference design uses decoupling capacitor at the base-emitter of transistor (Q2) to alleviate the unintentional turn on of the gate path transistor Q2, allowing faster MOSFET switching slew rate. The capacitor can be used at the gate to source the of MOSFET to further enhance the noise immunity. shows the simulation results confirming that the gate voltage pick up is negligibly small. The transistor remains off ensuring that there is negligible cross-coupling.

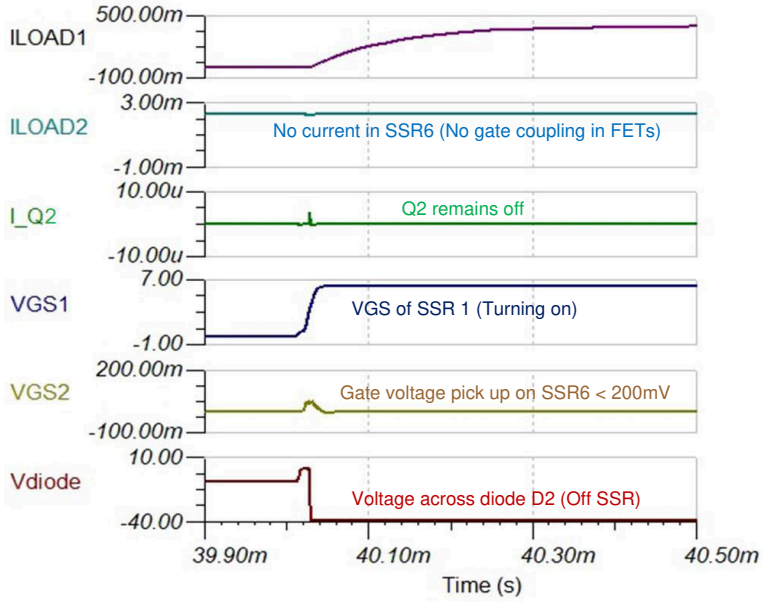


図 2-8. Simulation Results Illustrating Negligible Cross-Coupling

The performance comparison of the single isolation multichannel SSR topology against other independent isolation SSR topologies and electromechanical relays are listed in 表 2-1.

表 2-1. Comparison of Single Isolation Topology Against Other SSR Topologies and EMR

Parameter	Electromechanical Relay	SSR: Optical Isolated Drive	SSR: Independent Transformer Isolation	SSR: Single Isolation With Multichannel SSR
Cost per relay	Low	High	Medium	Low
PCB size per relay	Medium	Low	Medium	Low
Life	Low	Medium	High	High
Quiescent current per channel	High	Low - Medium	High	Low - Medium
Turn on, Turn off time	High	Medium	Medium	Low

2.2.6 Schematic: Design of Gate-Drive Circuit

図 2-9 shows the gate-drive circuit of one channel of SSR and the SSR turn on gate current path. OUT10 is the relay on and off signal at the secondary side of the digital isolator. When OUT10 goes from logic low (0 V) to logic high (5 V), the NPN transistor Q40 turns on. For multichannel implementation, the NPN transistor can be replaced by a low-side switch array device, the TPL7407LA. The TPL7407LA integrates seven low-side NMOS switches and can be used to replace the NPN transistors of seven SSR channels. Turning on the NPN transistor Q40 will bias the PNP transistor Q37 through the resistors R83 and R87 and enable sufficient base current to turn on Q37. Once Q37 turns on, the SSR MOSFET gate-to-source will be charged to VGD_ISO through Q37, R85 (gate resistor), D41, and D43. The components in the dotted box including D41, Q42, R89, and R93 are not required in most of the use cases, if a slow turn off is enough for the application (a few tens of micro seconds to hundreds of micro-seconds).

The peak gate current is to be designed by adjusting the biasing of the PNP transistor. In the reference design, the bias resistors used are R83 = 10 kΩ and R87 = 100 kΩ. The value is designed in such a way that Q37 gets sufficient bias voltage when VGD is greater than 6.5 V. With R83 = 10 kΩ, and R87 = 100 kΩ, the base current of Q37 is approximately 10 µA as per simulation results.

With VGD_ISO = 8.5 V and R87 = 100 kΩ, I_B = 10 µA. The saturation collector current of Q2 (same as the peak gate current) can be calculated as, $I_C = I_{gate\_peak}$ = DC current gain of Q37 × I_B.

Assuming DC current gain = 200 (from the PNP transistor data sheet), I_C = 2 mA.

The Zener diode D45 acts as a clamp for overvoltage protection at the gate-to-source of the MOSFET.

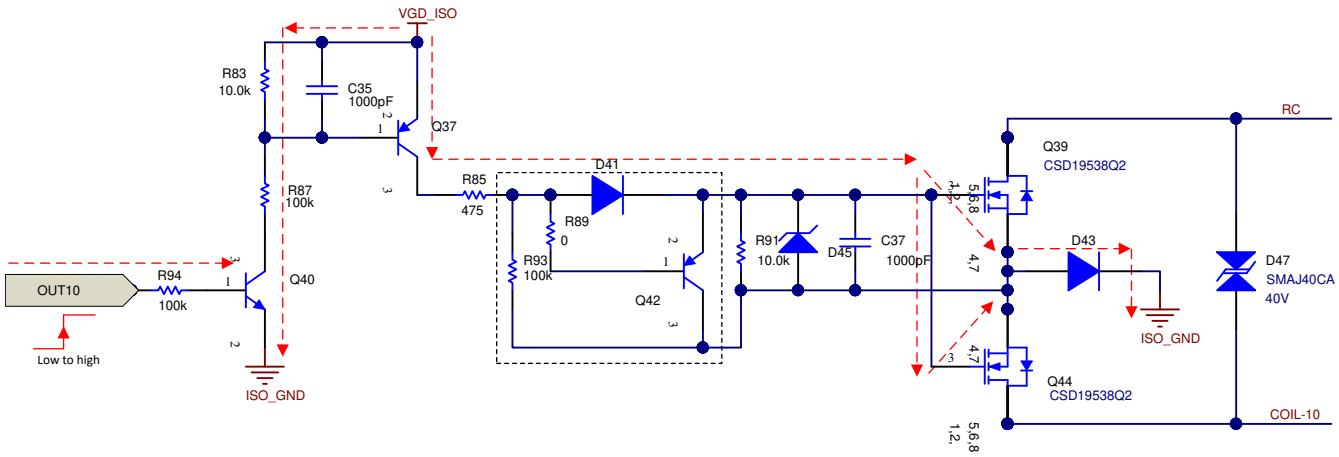


図 2-9. Gate Driver Circuit for the SSR MOSFETs and the Turn on Gate Current Path

The gate-drive circuit can experience overvoltage in the case of mis-wiring at the side of the power relay coil and 24 VAC transformer. Considering a mis-wiring, where the 24 VAC is connected to the RC terminal of SSR-1, and the RC terminal of SSR-2 is left unconnected. The relay coils are connected from both SSR MOSFET lower terminals (COIL-1 and COIL-2) to the common wire (C-wire). In this use case, if both SSR are kept ON, then the full AC voltage will appear across the blocking diode (diode connected between common source of MOSFET to ISO_GND) and the peak value of that voltage can be 41 V (corresponding to 24 VAC +20%). In this case, the possible overvoltage at the gate-source of MOSFET in any SSR channel needs to be avoided in design by adding Zener diode across the gate and source terminal of SSR MOSFET.

Approximate peak voltage across PNP transistor = 41 V, assuming VGD_ISO = 8.5 V, and VAC (peak) = 41 V.

The peak power loss in Q37 = 41 V × 2 mA = 82 mW, the average power loss across Q2 will be lower.

The peak current through gate-source resistance R91 (when the Zener diode clamps to Vz = 12 V) can be calculated as, I_{R91} = 12 V / R91 = 1.2 mA.

The peak current in the Zener diode = I_{gate_peak} – current through R91 = 0.8 mA.

The peak power loss in the gate clamp Zener diode = 12 × 0.8 mA = 9.6 mW.

A 250 mW–500 mW Zener is a good option in design.

The previously-mentioned power loss happens only during mis-wiring and during normal working condition the Zener diode will not be carrying any current and the PNP transistor power loss also will be much lower. The user has the option to reduce the peak gate current further by increasing the base bias resistors of PNP transistor Q37, at the expense of slow turn on and turn off of the SSR MOSFETs. While reducing the peak gate current, make sure that the gate-to-source resistance R91 value is increased accordingly to ensure enough gate voltage at the MOSFET gate.

図 2-10 shows the turn off gate drive path. When OUT10 goes low, Q40 turns off, Q37 turns off and the MOSFET gate discharges through R91 and Q42.

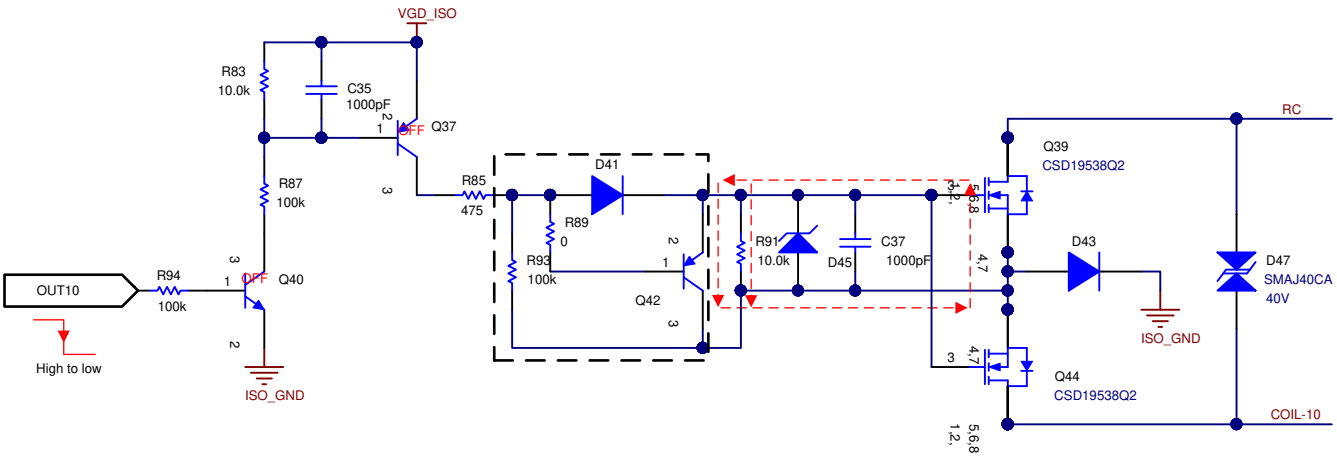


図 2-10. Gate Driver Circuit for the SSR MOSFETs and the Turn off Gate Current Path

2.2.6.1 Calculation of Gate-Driver Power Consumption

The gate-driver current consumption is calculated based on the following assumptions:

- Digital isolator primary side voltage = 3.3 V
- Digital Isolator secondary side voltage = 5 V
- Gate drive PNP transistor power supply voltage = 8.5 V
- The SSR MOSFET gate current consumption during switching is neglected.
- The AC current of digital isolators are neglected, as the SSRs are expected to be switching at a very low rate and the digital isolator AC current is negligible.
- The on-state voltage drop across PNP transistor Q2 is neglected

ISO7760 secondary current (Vi = Vcc), $I_{CC2\_ISO7760}$ = 3.3 mA.

ISO7740 secondary current (Vi = Vcc), $I_{CC2\_ISO7740}$ = 2.2 mA.

Gate current of single SSR, with 10-kΩ resistor across MOSFET gate and source, I_G = (8.5 – 0.7) V / 10 kΩ = 780 µA.

PNP transistor biasing current, I_{BIAS} = 8.5 V / (10 kΩ + 100 kΩ) = 77.3 µA.

Secondary side total gate drive current (approximate) with all SSR on, I_{GD_ON} = 3.3 mA + 2.2 mA + (10 × (780 + 77.3) µA) = 14.07 mA.

Secondary side total gate drive current (approximate) with all SSR off, I_{GD_OFF} = 3.3 mA + 2.2 mA = 5.5 mA.

The current consumption can be reduced by increasing the resistance across the gate-to-source terminals of the MOSFET, at the expense of increased SSR turn off time.

2.2.7 Schematic: Digital Isolator Circuit

図 2-11 shows the digital isolator circuit for the 10-channel SSR. To get ten SSR channels, a 6-channel (ISO7760) and a 4-channel (ISO7740) digital isolator is used. For any other number of SSR channels different combinations of digital isolators can be used. For example an 8-channel SSR circuit can be created using two 4-channel digital isolators (ISO7740). A 9-channel SSR can be realized using one 6-channel digital isolator (ISO7760) and one 3-channel digital isolator (ISO7730). The IN1-IN10 are the relay turn on and turn off control signal from the microcontroller. For example, to turn on the relay connected to SSR channel 1 (COIL-1), keep IN1 in the logic high state. To turn the relay off, keep IN1 in logic low state.

In the case where there is a requirement to route a diagnosis signal from the relay side to the MCU side, a digital isolator with one reverse channel can be used. For example, an ISO7761 device provides five forward-direction channels and one reverse-direction channel.

If the input power or signal is lost, the default output is *high* for ISO7760 devices without suffix F and *low* for devices with suffix F. This reference design uses the device with suffix F (ISO7760F and ISO7740F) to make sure that in the absence of input-side powers supply, all the SSR are turned off. The 100-kΩ pulldown resistors

at the input of the digital isolator is optional and may not be needed in a system-level board design. The resistor at the EN pin of ISO7740 is not populated, so as to enable the outputs of ISO7740. The 0-Ω resistors at the VCC terminals of digital isolator is a placeholder for current consumption measurement, if needed.

The reference design uses the TPL7407LA device as the low-side switch for 7 channels, connected at the output of the digital isolator. The remaining 3 channels of SSR use a separate NPN transistor.

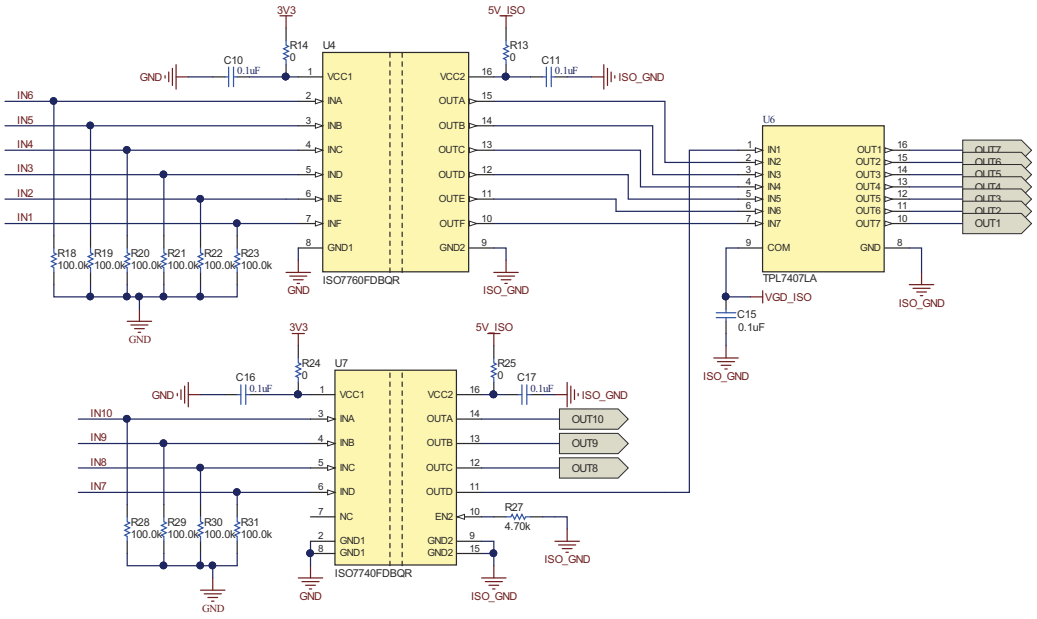


図 2-11. Digital Isolator Interface for Ten Channel SSR

2.2.8 Schematic: 3.3 V to 10V_ISO, 5V_ISO Power Supply

図 2-12 shows the open-loop flyback power supply. 図 2-13 shows the TIMER circuit to generate the pulse-width modulation (PWM) signal. The power supply does not have a closed loop to control the output voltage. The output voltage will be decided based on the output load. The output load will be minimum when all the SSRs are off and maximum when all the SSRs are OFF. The flyback is designed to ensure that the output voltage variation is within 7–10 V during the load change. 表 2-2 shows the design specification of the flyback power supply.

表 2-2. Design Specification of the Flyback Power Supply

Parameter	Minimum	Typical	Maximum	Comments
Flyback Input Voltage	3.2 V	3.3 V	3.4 V	Assuming 2% tolerance
Output Voltage	6.5 V	8.5 V	10 V	
Output Current	5.5 mA	10.2 mA	15 mA	Typ value when half of the SSR are ON

The flyback transformer used in the reference design board is the coupled inductor 744889030330 (Wurth). The coupled inductor has a turns ratio of 1:3 and primary inductance of 33 µH. The PWM frequency used is 250 kHz with a 34% duty cycle. An alternate part for the flyback transformer could be LPR4012-223DMR (Coil Craft) having 1:3 turns ratio and 22-µH primary inductance. With the couple inductor LPR4012-223DMR, the frequency used should be around 400 kHz. MOSFET Q1 is a logic FET to enable switching with a 3.3-V supply. The selected coupled inductor should provide sufficient function isolation voltage for the 24-VAC supply operation.

The TLC555 timer is configured to create a PWM frequency of 250 kHz at a 34% duty cycle. The designer can also generate a PWM from the MCU and connect to pin 9 of connector J3. If the PWM from the timer is used, then populate R15 and do not populate R26. If PWM from the MCU is used, then populate R26 and do not populate R15. The diodes D7 and D6 in the TIMER circuit are used to generate PWM frequency less than 50%. The resistors R16, R17, and capacitor C14 are tuned to get the desired frequency and duty cycle. See the *TLC555 LinCMOS™ Timer Data Sheet* for detailed design. The PWM from the timer or MCU is connected to the input of the buffer U6 (SN74LV1T34DCKR) and the gate resistor used is 100 Ω. Make sure that the resistor R12 is not populated. The MOSFET Q1 can be driven directly from the MCU as well (with a minimum 4- to 6-mA

drive capacity from the MCU), and in that case remove U6 and populate R12 with a 0-Ω resistor. The gate resistance R7 should be increased to limit the MCU pin current.

The linear regulator TLV76050 generates 5V_ISO from the 10V_ISO. The 5V_ISO is used as secondary side supply for ISO7760 and ISO7740 digital isolators. The 10V_ISO (In schematic 図 2-12, the 10V_ISO node is marked as 12V_ISO) is used as the power supply for the gate-driver circuit of SSR MOSFET (by connecting R8 and removing R9). The secondary side of the digital isolator can be powered with 3.3 V as well and in that case a 3.3-V output regulator can be used. The TLV70433 is a recommended 3.3-V regulator option in case an ultra-low quiescent current is required.

The resistor R5 is used at the output of the flyback to ensure the minimum load to ensure no load voltage regulation within control. The Zener diode D2 is used as a voltage clamp for overvoltage protection. IN1 – IN10 are the relay on and relay off control signal from the MCU for the SSR channels 1 to 10, in order. The VGD_ISO is the supply to the gate-drive PNP transistor. The VGD_ISO is connected to the 10-V supply by populating R8. The resistor R9 is not populated. The reference design uses 3.3-V voltage at the input of the isolated power supply by keeping R2 populated and R4 not populated.

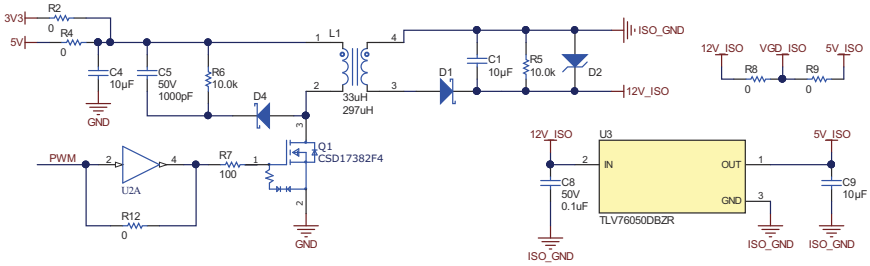


図 2-12. Open-Loop Flyback Power Supply

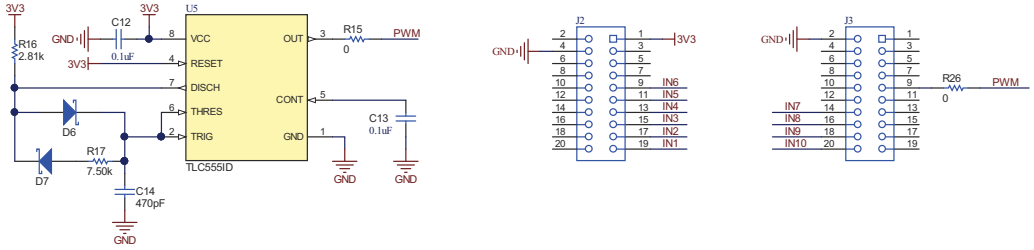


図 2-13. TIMER to Generate PWM Signal and Interface Connector

2.3 Highlighted Products

2.3.1 ISO7760

The ten channel SSR solution need a digital isolator circuit with a total of 10 channels. This is realized by using ISO7760 (6-channel digital isolator) and ISO7740 (4 channel digital isolator).

The ISO7760 devices are high-performance, six-channel digital isolators with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices is also certified according to VDE, CSA, TUV, and CQC. The device has a robust isolation barrier with more than 100-Year projected lifetime, up to 12.8-kV surge capability and ±100 kV/µs Typical CMTI. The ISO776x family of devices provides high-electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. The ISO776x family of devices is available in 16-pin SOIC and SSOP packages.

The ISO776x family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. If the input power or signal is lost, the default output is *high* for devices without suffix F and *low* for devices with suffix F. These options allow the designer to select the variant providing safe off state when the input side power supply is lost. This reference design uses the device with suffix F to make sure that in the absence of input side powers supply all the SSR are turned off.

2.3.2 ISO7740

The ISO7740 devices are high-performance, four-channel digital isolators with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices is also certified according to VDE, CSA, TUV, and CQC. The ISO774x devices are available in 16-pin SOIC and QSOP packages. The other features of the ISO7740 device are similar to the ISO7760 device. This reference design uses the device with suffix F to make sure that in the absence of input-side power supply, all the SSRs are turned off.

2.3.3 ISO7041

The ISO7041 device is the option when the SSR circuit needs to be designed for ultra-low power. The ISO7041 is an ultra-low power, multichannel digital isolator that can be used to isolate CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. Innovative edge-based architecture combined with an ON-OFF keying modulation scheme allows these isolators to consume very-low power while meeting 3000-V_{RMS} isolation rating per UL1577. The per channel static current consumption is 3.5 µA at 3.3 V, allowing for use of the ISO7041 in battery-powered thermostats and power-stealing thermostats.

The device can operate as low as 1.71 V, as high as 5.5 V , and is fully functional with different supply voltages on each side of isolation barrier. The four-channel isolator comes in a 16-QSOP package with three forward-direction channels and one reverse-direction channel. The device has default output high and low options. If the input power or signal is lost, default output is *high* for the ISO7041 device without the suffix F and *low* for the ISO7041F device with the F suffix.

2.3.4 CSD19538Q2

The CSD19538Q2 device is a 100-V, 49-mΩ, SON 2-mm × 2-mm NexFET™ power MOSFET. The device could be the right fit for realizing the back-to-back connected power MOSFETs in the SSR. The device ensures enough voltage margin for a 24-VAC powered SSR with continuous current within 2 A. The MOV, or, TVS diode, or both are used at the 24-VAC line to protect against surge, or EFT, or inductive switch spikes can have a clamp voltage as high as 65 V and a 100-V MOSFET ensure proper design margins here.

2.3.5 CSD17382F4

The reference design uses an open-loop flyback power supply to generate the 10-V isolated supply from the 3.3-V primary side supply. The steady-state peak primary current is less than 200 mA. Considering the reflected voltage and leakage voltage spikes, a MOSFET with voltage rating more than 20 V provides enough design margin. The MOSFET must support logic level gate voltage to enable gate drive from a 3.3-V line. The CSD17382F4 is used as the power switch for the open-loop flyback power supply to get a compact power supply. The CSD17382F4 device is a 30-V, 54-mΩ, N-Channel FemtoFET™ MOSFET technology and is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small-signal MOSFETs while providing at least a 60% reduction in footprint size.

2.3.6 TPL7407LA

The TPL7407LA device is a 30-V, high-current NMOS transistor array. This device consists of seven NMOS transistors with common-cathode clamp diodes for switching inductive loads. The maximum drain-current rating of a single NMOS channel is 600 mA. New regulation and drive circuitry is added to give maximum drive strength across all GPIO ranges (1.8 V–5 V). The key benefit of the TPL7407LA is its improved power efficiency and lower leakage than a bipolar Darlington implementation.

The design needs a low-side switch at the output of the digital isolator to interface to the PNP transistor of the gate-drive circuit. The gate-drive power supply is around 10 V; therefore, the TPL7407LA provides adequate design margins and a compact size with good integration.

2.3.7 TLV760

The TLV76050 device is used in the reference design to realize a low-cost linear regulator to generate the 5-V power supply at the secondary side of the power supply. The 5 V is used to power up the digital isolator.

The TLV760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the full 100-mA load across operating temperature. Standard packaging for the TLV760 is the 3-pin SOT-23 package. The TLV760 is available in 3.3 V, 5 V, 12 V, and 15 V.

The device has robust internal thermal protection, which protects itself from potential damage caused by conditions like short to ground, increases in ambient temperature, high load, or high dropout events.

If the design needs ultra-low current operation along with the ISO7041 device, then the linear regulator TLV704 can be used to generate the secondary-side power supply for the digital isolator. The TLV704 operates over a wide operating input voltage of 2.5 V to 24 V and provides 3.2-µA ultra-low quiescent current.

2.3.8 TLC555

The TLC555 device is used to generate the PWM for the open-loop flyback power supply. The TLC555 is a monolithic timing circuit fabricated using the TI LinCMOS™ technology. The timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Because of its high-input impedance, this device supports smaller timing capacitors than those supported by the NE555 or LM555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.1.1 Test Equipment Needed to Validate Board

The following list details the equipment required for board validation:

- 240 VAC to 24VAC or 120 VAC to 24 VAC, 20VA isolation transformer (20 VA is selected to supply less than 100 mA per SSR with a maximum of six SSRs on at a time). If the power relay coil current is more than 100 mA and if it is required to run the entire relays ON at a time, a transformer with increased VA rating must be used.
- Separately isolated 40-V, 1.5-A DC supply and 5-V, 0.2-A DC supply
- 24-V AC power relay (with coil current less than 1 A) – multiple quantity
- MSP430FR2355 LaunchPad™ or similar controller or function generator to generate relay control signals
- Oscilloscope (100 MHz) with two or more isolated voltage probes
- 4½ digit multimeter

3.1.2 Test Conditions

The following list details the required test conditions:

- Start testing the reference design with a 40-VDC source with 2-A current limit, before testing with a 24-V AC transformer.
- Connect a suitably-rated external fuse while testing with 24-VAC supply from the transformer. For example, use a 2-A fast blow fuse.
- The open-loop flyback power supply uses the coupled inductor 744889030330 (Wurth) as the flyback transformer for all the testing.
- The following components are not populated in the board while testing: C3, C7, R4, R9, R10, R11, R26, R27, and U2

3.1.3 Test Procedure

The following list details the procedure for board bring-up and testing:

1. Remove all the connections from the board. Apply a minimum 3.6-V DC to the 5-V DC terminal of the connector J1. Set the current limit to around 200 mA for the DC power supply.
2. Check the 3.3 V at any 3V3 node in the board (for example: at capacitor C4).
3. Check the PWM frequency at the output of the TIMER (at R15) or from the MCU. The board is tuned to work at 250 kHz and 34% duty cycle. The board uses the onboard PWM from the TIMER, and so external PWM

signal is **not** needed. However if an external PWM signal (for example from an external microcontroller) is to be used, then the PWM signal can be connected to J3 with R26 populated and remove R15.

4. Check the voltage at the output of flyback at 10V_ISO node (in the schematic, the 12V_ISO node). The expected readings are listed in 表 3-1. The LED D5 will light up on the availability of 10V_ISO. The voltage at the node 10V_ISO is expected to be more than 6.5 V at full load (all channels ON).
5. Check the availability of 5-V isolated power at the node 5V_ISO.
6. For testing the relay coils, switch off the supply at J1. Connect 24–41 VDC supply at J4 (between RC and C with any polarity) and set a current limit based on the expected relay current (for ex: 1 A)
7. Connect the relay coils between the Sx (S1 to S10) pin to the pin marked “C”, as shown in 図 3-1.
8. The ON/OFF signals can be given to the board at J2 and J3 at the pins marked IN1 to IN10, from an external controller or function generator. The logic voltage applied at IN1–IN10 pins must be less than 3.3 V.
9. Turn on the low-voltage supply at J1 and the 24V - 41 VDC supply at J4. Observe the relay switching according to the signal at INx.
10. Repeat the test (steps 7–9) with 24 - 41 VDC supply polarity reversed.
11. Repeat the test (steps 7–9) with 24-V AC supply connected at J4. Make sure that a properly-rated external fuse is used in series with the 24-VAC supply to avoid transformer saturation and further heating, if any unexpected short circuit occurs.

3.2 Test Setup

図 3-1 shows the details of input and output connectors in the reference design board and the SSR circuits. 図 3-2 shows the way to connect different relay coils and transformer to the reference design board.

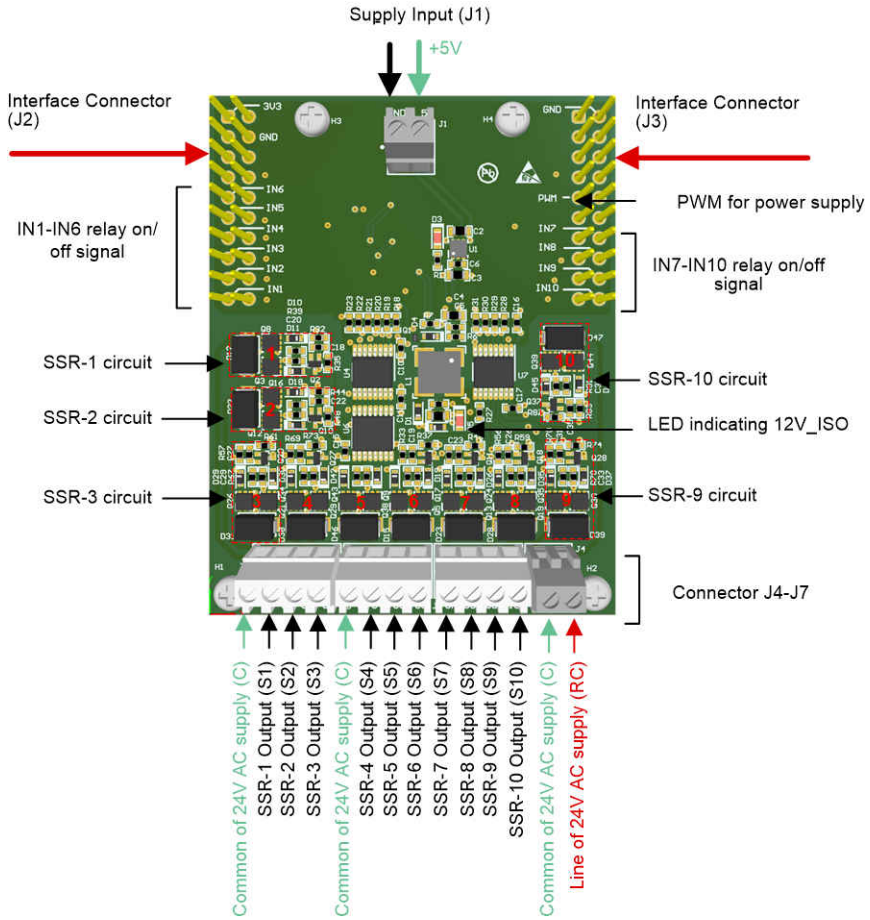


図 3-1. Input and Output Connectors in the Reference Design Board

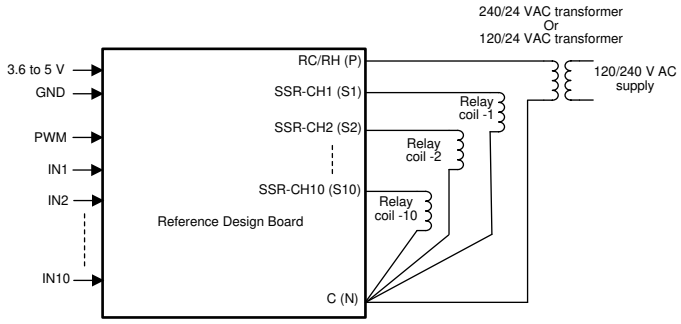


図 3-2. Interfacing External Control Signals, Relay coils and Transformer to the Board

3.3 Test Results

3.3.1 Functional Tests

図 3-3 shows the PWM signal from the TIMER and the gate-to-source voltage (VGS) of the SSR MOSFETs. The PWM frequency is 250 kHz and the duty cycle is 34%. The testing is done with the flyback inductor 744889030330 (Wurth). An alternate part is the LPR4012-223DMR (Coil Craft) and in that case the PWM frequency used was around 400 kHz at 34% duty cycle.

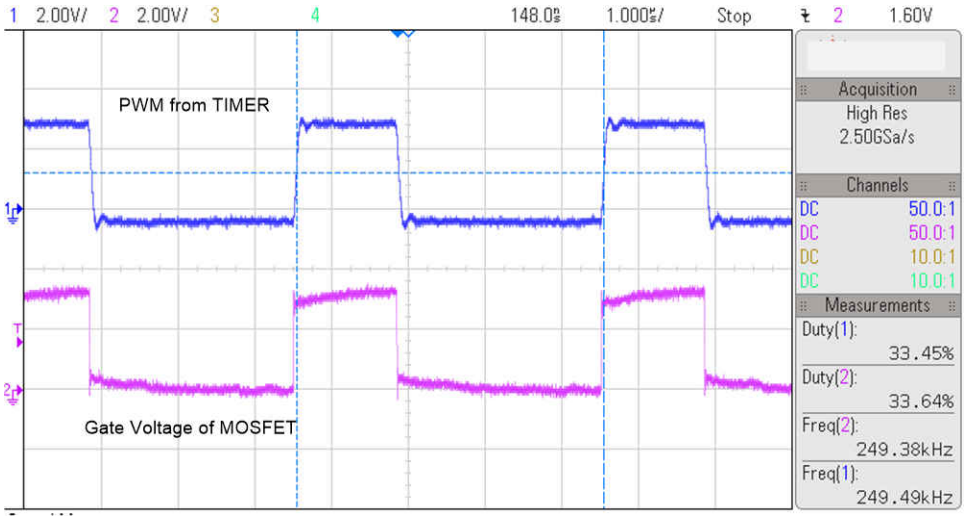


図 3-3. PWM Signal from the MCU or TIMER and MOSFET Gate-Source Voltage

図 3-4 shows the primary current of the transformer and the voltage across the flyback MOSFET when all the SSRs are ON. The steady-state peak current at the transformer primary is around 135 mA. The peak voltage across the flyback MOSFET is less than 10 V.

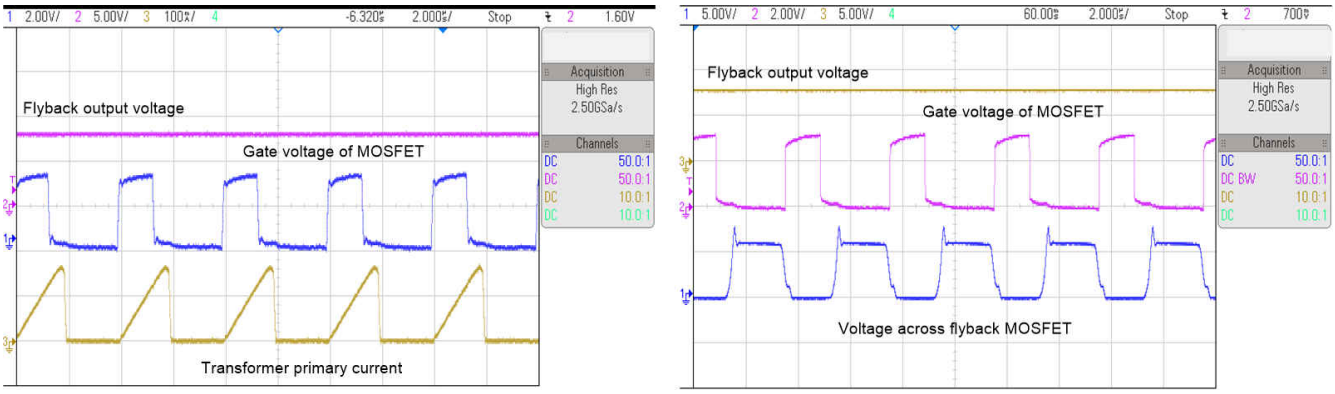


図 3-4. Flyback Circuit Voltage and Current Waveforms - All SSR On

図 3-5 shows the primary current of the transformer and the voltage across the flyback MOSFET when all the SSRs are OFF. The steady-state peak current at the transformer primary is around 135 mA. The peak voltage across the flyback MOSFET is less than 10 V.

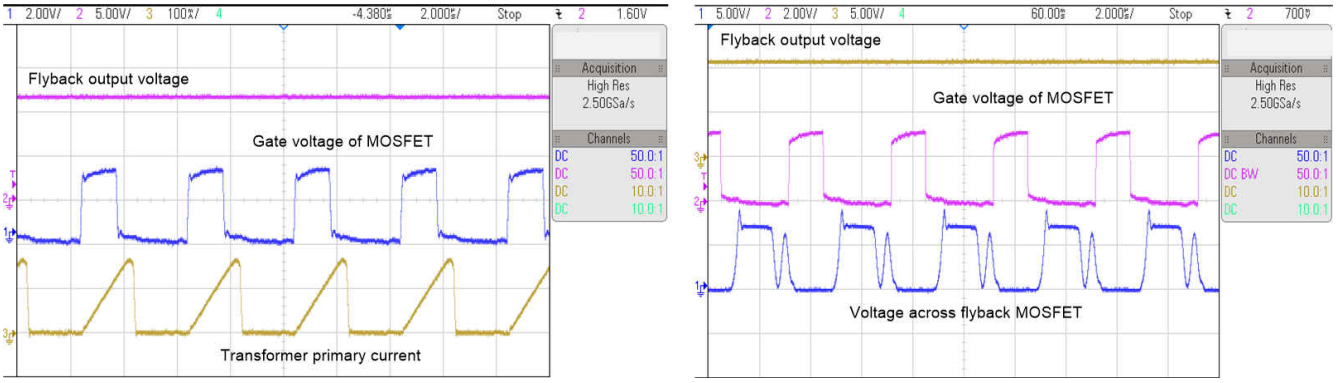


図 3-5. Flyback Circuit Voltage and Current Waveforms - All SSR Off

表 3-1 illustrates the output voltage of the flyback power supply when all the SSR channels are on and all channels are off.

表 3-1. Output Voltage of the Flyback Power Supply

Operating Condition	Input Voltage	Output Voltage	Input Current on 3.3-V Rail
All SSR channels On	3.3 V	7 V	47 mA
All SSR channels Off	3.3 V	9.5 V	56 mA

図 3-6 to 図 3-9 show the SSR switching with a DC power supply of +40 V and –40 V. During the SSR turn off, the voltage across the SSR MOSFET pair shows spikes due to the inductive kickback from the relay coil and the voltage got clamped to approximately ±46 V, by the bidirectional TVS chip, SMAJ40CA.

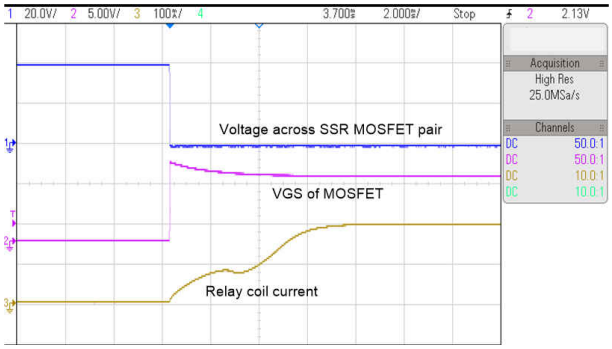


図 3-6. SSR Turn on Waveform at 40 V

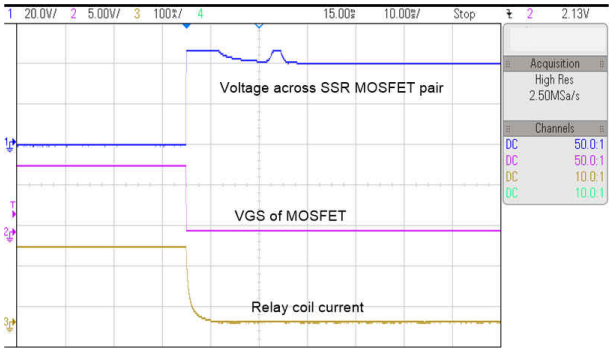


図 3-7. SSR Turn off Waveform at 40 V

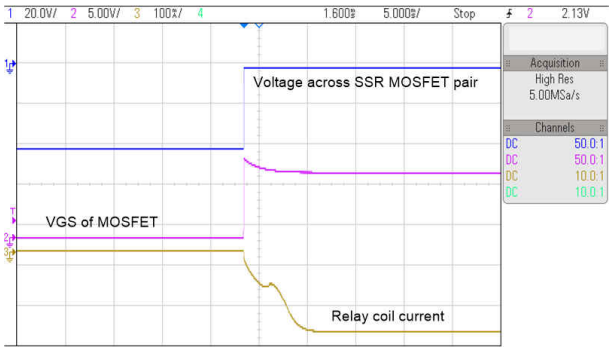


図 3-8. SSR Turn on Waveform at –40 V

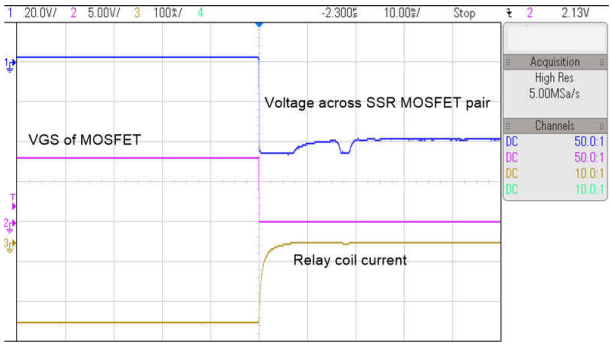


図 3-9. SSR Turn off Waveform at –40 V

図 3-10 and 図 3-11 show the VGS and VDS slew rate waveforms during MOSFET turn on and turn off. The VDS slew depends on the gate-circuit parameters, the gate resistance, gate-drive voltage, gate-drive PNP

transistor saturation current, and so forth. The VDS slew also depends on the load current and load inductance. The FET switching turn on and turn off times are adjustable in hardware and need to be tuned in the application. The VDS slew time is approximately 1–2 µs during turn on and turn off. The turn on slew time can be decreased by increasing the base current of the gate-drive PNP transistor and by reducing the gate resistor. The turn off time can be decreased by decreasing the resistor connected across the gate and source of SSR MOSFETs.

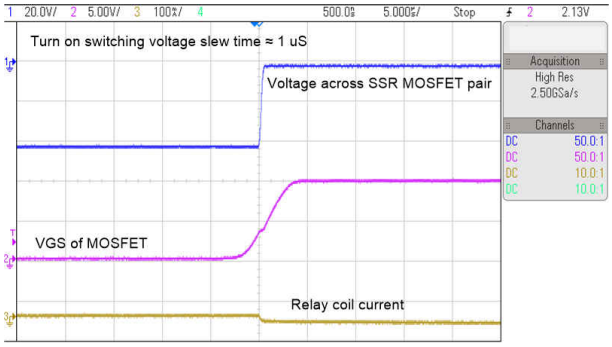


図 3-10. MOSFET Turn on Switching Waveform

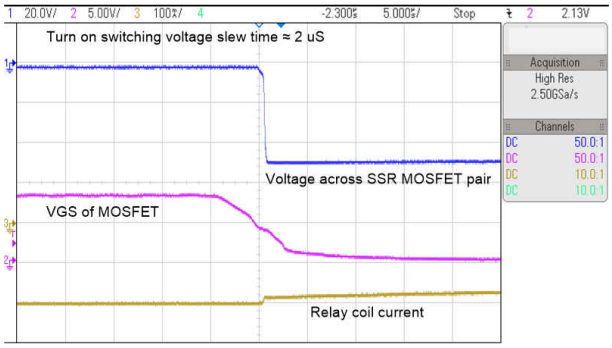


図 3-11. MOSFET Turn off Switching Waveform

図 3-12 and 図 3-13 show the total turn on and turn off time of the SSR from the control signal toggling to the complete turn on or turn off of the SSR MOSFETs. The turn on and turn off time of the SSR after the turn on and turn off command from control signal (INx signals of digital isolator) is less than 15 µs. The time can be adjusted by changing the MOSFET gate biasing.

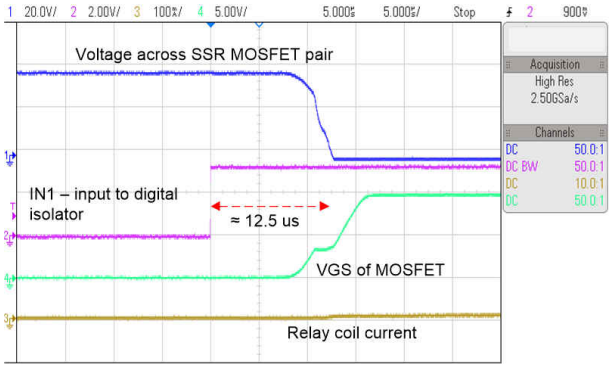


図 3-12. Waveforms Showing SSR Turn on Time

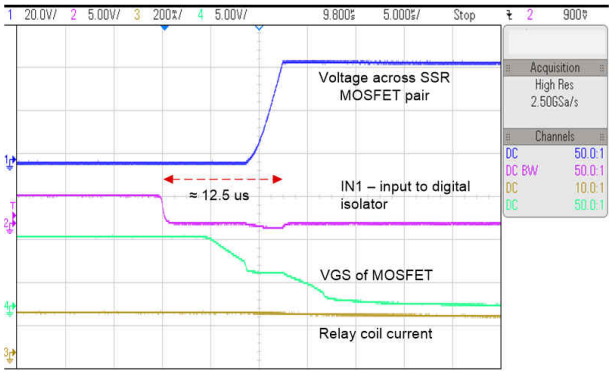


図 3-13. Waveforms Showing SSR Turn off Time

図 3-14 and 図 3-15 show the gate voltage pick up of an SSR channel that is in off state, while another SSR channel is turned on or off. In 図 3-14, The SSR-2 is in off state. The already on SSR-1 is turned off with negative DC supply voltage, while doing so, the voltage across SSR-1 MOSFET pair changes from 0 V to –40 V in around 2 µs. During this event the gate-to-source pick up voltage (VGS) of SSR-2 MOSFETs is monitored. The VGS pick up of SSR-2 is approximately 100 mV. In 図 3-15, the SSR-2 is in off state. The already off SSR-1 is turned on with negative DC supply voltage, while doing so, the voltage across SSR-1 MOSFET pair changes from –40 V to 0 V in around 2 µs. During this event the VGS pick up of SSR-2 is approximately 150 mV.

In both the cases, the gate pick-up voltage observed at V_{GS} of the OFF state SSR is less than 200 mV. This ensures that the V_{GS} is well below the threshold voltage of the MOSFET (V_{GS_th} = 2.4 V at 150°C for CSD19538Q2) ensure very good design margin. In other way, the design has least cross-coupling between channels ensuring a reliable independent control of SSR.

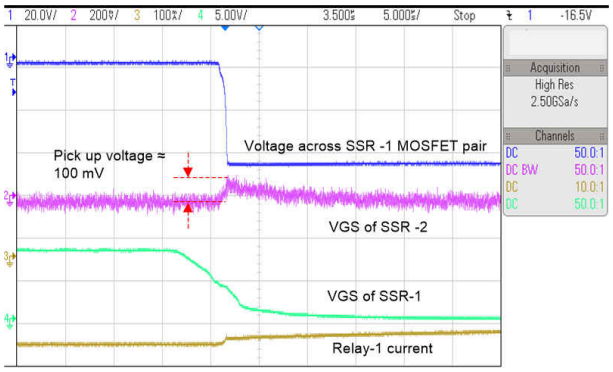


図 3-14. Test Waveforms Showing Least Cross-Coupling During SSR Turn Off

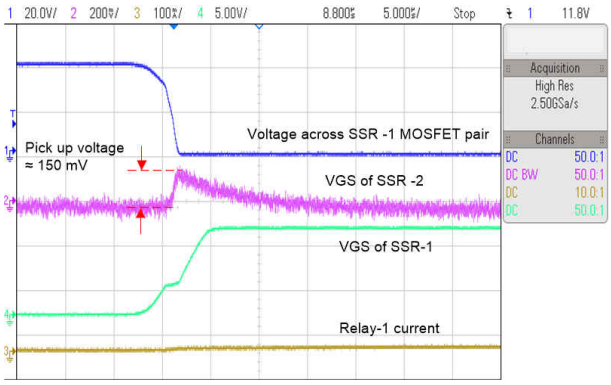


図 3-15. Test Waveforms Showing Least Cross-Coupling During SSR Turn On

図 3-16 shows the independent control of two SSR channels with a 24-V AC supply. A 120 VAC to 24 VAC, 20VA transformer is used to provide the 24-VAC power supply to the SSR.

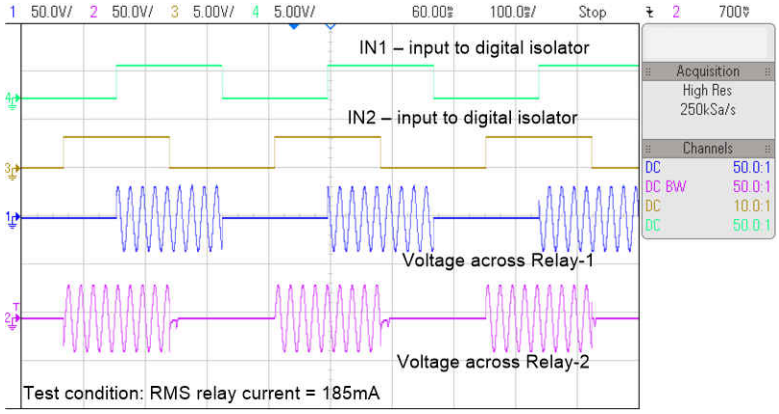


図 3-16. Test Waveforms at 24-VAC Supply - Independent Operation of SSR

3.3.2 Overcurrent Testing With External Fuse

The reference design is tested for short-circuit conditions with an external fuse. 図 3-17 shows the wiring diagram during testing. The short circuit is created by shorting the relay coil (COIL-1).

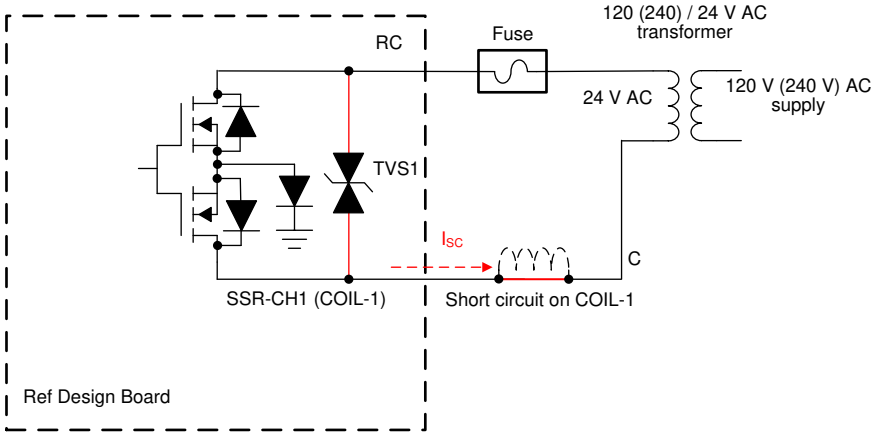


図 3-17. Overcurrent Protection Circuit With External Fuse

Test Condition:

- The COIL-1 is short-circuited
- The short-circuit current at the secondary of the transformer is limited by the secondary short-circuit impedance of transformer
- Specification of the transformer used for testing:
  - Manufacturer part number: 4000-09C02K999 (TE connectivity - laminated 20VA transformer)
  - Secondary winding resistance = 2 Ω
- Specification of the fuse used in series with the transformer secondary line RC:
  - Manufacturer part number: 046601.5NR (Littelfuse Inc.)
  - Rating: 1.5 A, 63-V AC/DC board mount fuse, 1206
  - Response time: Fast blow. Melting I²t: 0.1103

Observations during testing:

- During the short-circuit test, the fuse was blown within one electrical cycle (< 20 ms) with peak short-circuit current of approximately 7 A. The SSRs were functional after testing.
- 図 3-18 shows the test result waveforms.

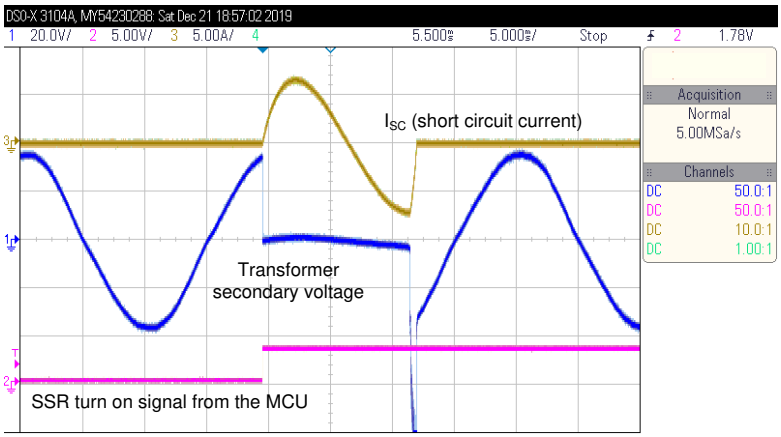


図 3-18. Short-Circuit Test Waveforms With External Fuse

3.3.3 Surge Testing

The board is tested for surge voltage up to 1.2 kV with a 12-Ω line impedance. The testing is done with the MOV - ZV40K2220102NIR1HT, connected across the SSR terminal (between the drain of top FET and drain of bottom FET). During the testing the TVS was not mounted. No failure was observed during testing and the SSR worked as usual after surge testing up to 1.2 kV

3.3.4 Multichannel SSR Driven From Two 24-VAC Transformers

図 3-19 shows a 6-channel SSR topology powered from two transformers, for example from the cooling transformer (RC) and heating transformer (RH) in an HVAC thermostat. The common wires (C – wire) of both the transformers are connected together. The single-isolation gate-drive circuit in the reference design can be used to drive all the six SSR channels. However, in this case the turn on PNP transistor (Q1, Q2 in 図 2-6) in the gate-drive circuit and the blocking diodes (D1, D2 in 図 2-6) has to be rated for two times the peak AC voltage plus the gate-drive voltage (this is by considering a use case where the transformers are mis-wired to create opposite polarity). For example, with a 24-VAC ±20% AC supply, having a peak instantaneous value of 41 V, the gate-drive PNP transistors and the blocking diodes has to be rated for more than 100 V.

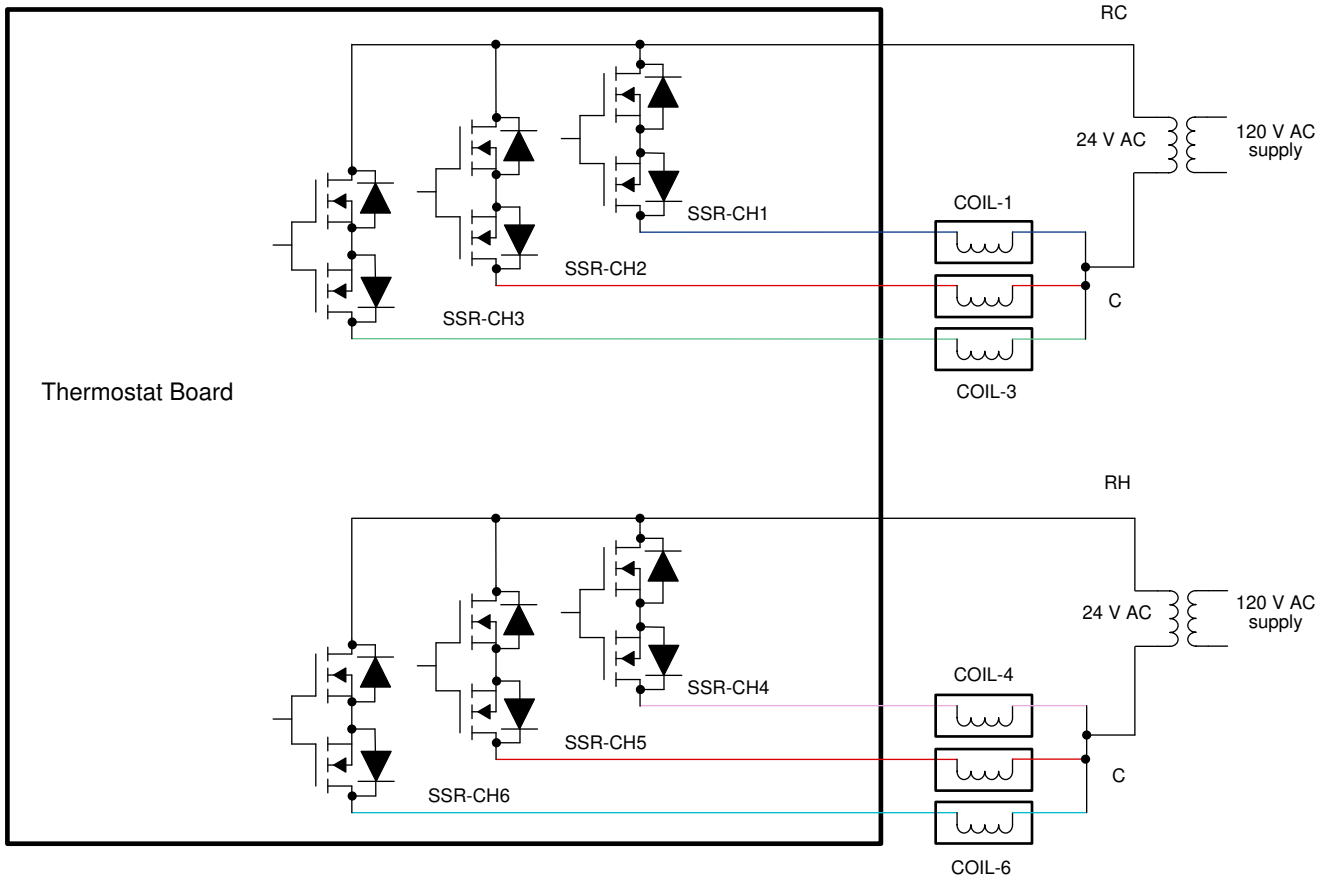


図 3-19. Circuit Topology in Driving Multiple SSRs With two AC Transformers

3.3.5 Alternate SSR Topology for High Voltage

図 3-20 shows a cost-effective way of implementing SSRs at higher voltages like 120 VAC or 240 VAC. The SSR circuit normally consists of two back-to-back connected MOSFETs. The high-voltage (240 VAC) SSR needs 600-V MOSFETs and that can be costly. The topology shows a cost-effective SSR where one MOSFET is replaced by four high-voltage slow diodes. The gate drive can be similar to the rest of the part of reference design. Here the PNP transistor T1–T6 needs to be rated for 500 V. The diode D1–D6 has be rated for more than 600 V. The isolation rating of the flyback power supply transformer needs to be appropriately selected.

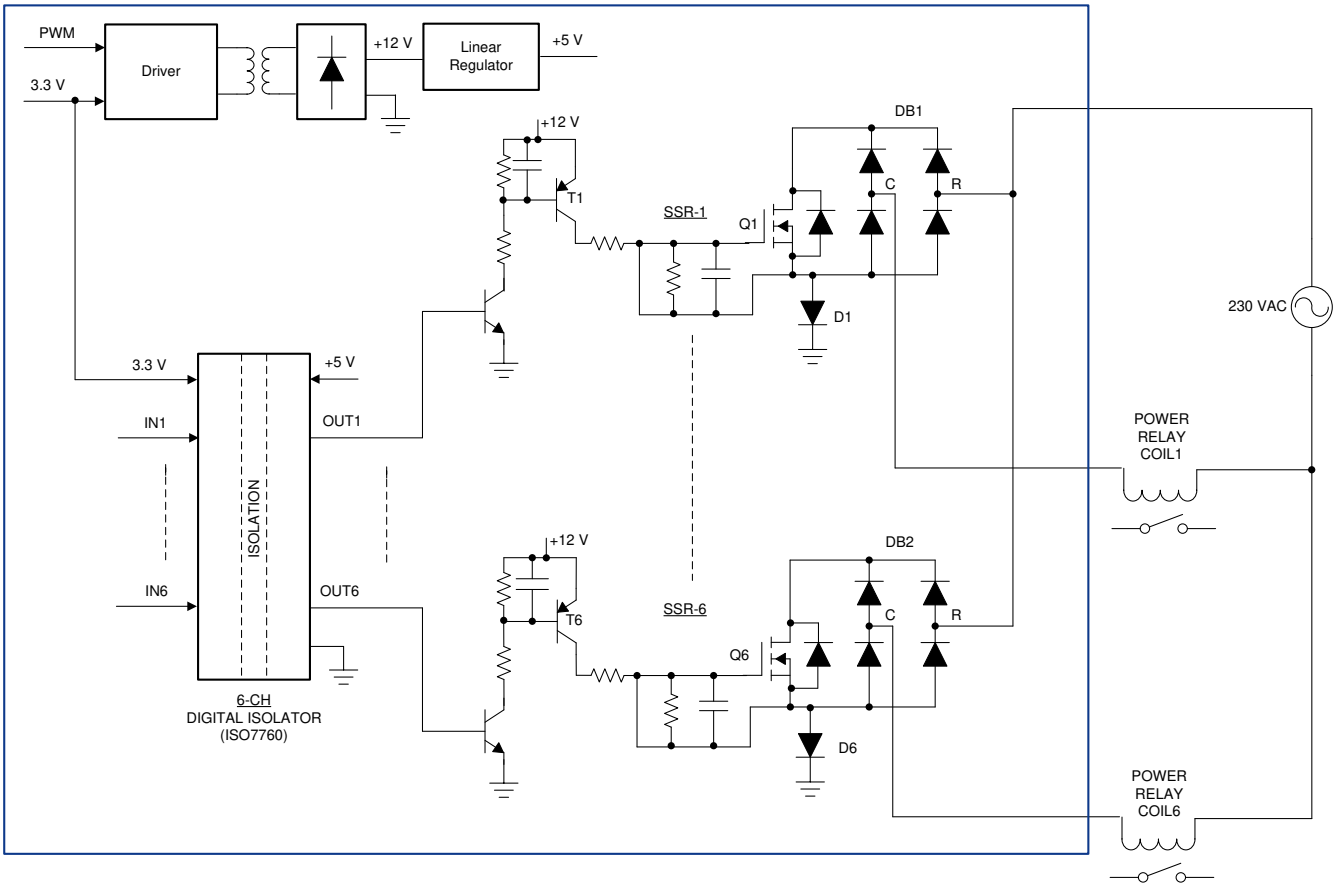


図 3-20. Circuit Topology for Cost Reduction at High Voltage

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010085.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010085.

4.2 Documentation Support

1. Texas Instruments, *ISO776x High-Speed, Robust EMC, Reinforced Six-Channel Digital Isolators Data Sheet*
2. Texas Instruments, *ISO774x High-Speed, Robust-EMC Reinforced and Basic Quad-Channel Digital Isolators Data Sheet*
3. Texas Instruments, *ISO7041 Ultra-Low Power Four-Channel Digital Isolator Data Sheet*
4. Texas Instruments, *TIDA-00751 - Solid State Relay 24V AC Switch with Galvanic Isolation Reference Design*

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5 About the Author

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