参考資料

Design Guide: TIDA-010242

MIL-STD-1275E サージ保護のリファレンス・デザイン

概要

MIL-STD-1275E 規格は、ミリタリー向け車両で各種機器を使用するための 28V DC 入力電力に関する最新の特性を規定しています。この規格は、ミリタリー向け車両の動作中に発生する 3 つの主な事象の特性を規定しており、28V の主電源に接続されている各種機器をこれら 3 つの事象から保護する必要があります。これらの事象とは、逆極性、電圧スパイク、電圧サージです。これらの事象に対応するために、逆極性事象が発生している間は保護回路を動作させないでください。また、スパイクおよびサージ事象が発生している間は、保護回路の出力を公称 28V、最大 34V にする必要があります。このリファレンス・デザインは、最大 120W の出力を処理できる 2 段クランプ回路を採用しています。2 段クランプ回路を実装した結果、部品表 (BOM) の総コストを削減し、全体のサイズを最小限に抑えることができます。

特長

- 2 段の 100V サージ抑制
  - 1 段目のサージ 100V→50V (LM7480-Q1 で処理)
  - 2 段目のサージ 50V→34V (LM5069 で処理)
- ±250V のスパイク・サージ抑制
- 最低 –65V までの逆入力保護

アプリケーション

- ソフトウェア無線
- GPS レシーバ

リソース

TIDA-010242	デザイン・フォルダ
LM7480-Q1	プロダクト・フォルダ
LM5069	プロダクト・フォルダ

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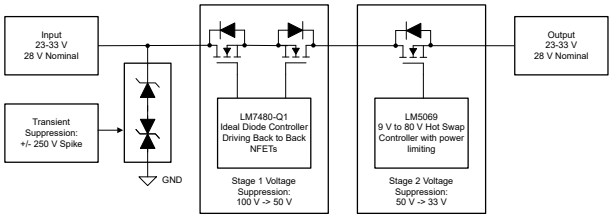

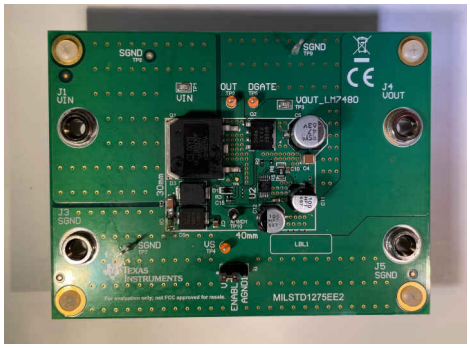

English Document: TIDUDG1

1 System Description

The MIL-STD-1275E reference design is a two-stage clamping system capable of handling the reverse input, spiking, and surging event while protecting systems up to 120 W (28 V at 4.3 A). The two-stage clamping approach allows for better thermal distribution, meaning that the selected MOSFETs can be smaller and reduce the overall solution size compared to a single-stage clamping solution.

2 System Overview

2.1 Block Diagram

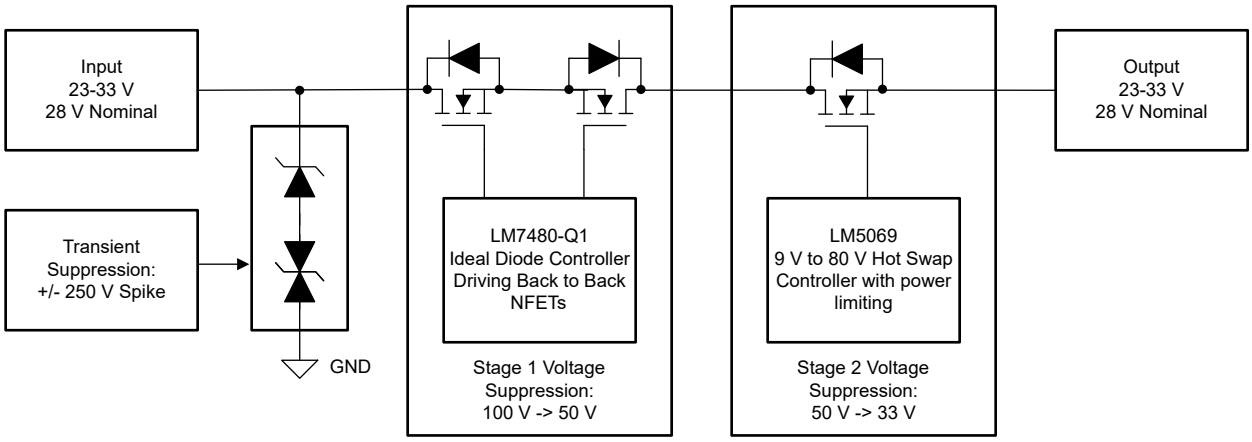

図 2-1. MIL-STD-1275E Protection Block Diagram

2.2 Design Considerations

In the MIL-STD-1275E, there are three events that the protection circuit needs to handle: reverse polarity, voltage spike, and voltage surge event. To handle these events, a two-stage clamping circuit utilizes the LM7480-Q1 and LM5069 to provide protection to the three events. For more information on each of these events, refer to the MIL-STD-1275E standard documentation.

2.2.1 MIL-STD-1275E versus MIL-STD-1275D

The TIDA-010242 is design to meet the specifications that are outlined by MIL-STD-1275E. However, there are several differences between the MIL-STD-1275E standard and the MIL-STD-1275D standard. 表 2-1 shows the difference between the two standards.

表 2-1. MIL-STD-1275E vs MIL-STD-1275D

	MIL-STD-1275E	MIL-STD-1275E
Operating mode	Single Operating Mode	Generator-Only Mode (G) and Normal Operating Mode (N)
Starting disturbance limits	12-V to 33-V cranking start-up	No start-up limits
Spike Event	+250 V for 70 µs ≥ +100 V at 1 ms and –250 V for 70 µs ≥ +18 V at 1 ms. Injected spike energy = 2 J and Emitted Voltage Spike = 125 mJ	(G) ±250 V for 70 µs ≥ ±100 V at 1 ms. Total energy 15 mJ
		(N) ±250 V for 70 µs ≥ ±40 V at 1 ms. Total energy 15 mJ
Surge Event	100 V for 50 ms ≥ 33 V for 500 ms. Injected energy surge = 60 J	(G) 100 V for 50 ms ≥ 40 V at 500 ms. Source impedance 500 mΩ
		(G) 40 V for 50 ms ≥ 32 V at 500 ms. Source impedance 20 mΩ

2.2.2 Reverse Polarity Event

The reverse polarity event occurs when the power terminals are inverted. For example, the positive terminal is connected to the negative terminal and the negative terminal is connected to the positive terminal. During this event it is important that the system does not see any power.

To protect against this event, the LM7480-Q1 has built-in reverse protection up –65 V. This means that during a reverse polarity event, there is no output voltage and no current drawn by the system. Protecting the system until the revers polarity event is rectified.

2.2.3 Voltage Spike Event

In the MIL-STD-1275E documentation, the *injected voltage spikes* section describes two different voltage spike events that can occur during vehicle operation: injected spikes and emitted spikes.

Injected voltage spikes are the higher energy spikes that can occur on the 28-V bus. The voltage spike is ±250 V while having a energy content of 2 Joules. The injected voltage spike event occurs when high-power systems in the vehicle, turn on in the system.

Emitted voltage spikes, conversely, are much lower energy spikes that occur on the 28-V bus. The maximum total energy in a single spike is 125 mJ. These events occur when other low-power accessories are toggled on an off on the bus line.

2.2.4 Voltage Spike Event: Component Selection

To protect against the ±250-V voltage spike event outlined by MIL-STD-1275E, there are three main components of the circuits that help suppress the voltage spike. The first component is the main MOSFET or Q1 in the schematic. Select a MOSFET with a voltage rating greater than 250 V to help with the spike voltage suppression and ensure that the MOSFET is not damaged due to the voltage spike event. The other two components to help suppress the two TVS diodes are D3 and D5. The TVS diode, D3, suppresses the main +250-V voltage spike event. Set the breakdown voltage of D3 greater than the maximum voltage of the surge event (100 V) but less than the maximum voltage spike event to ensure that the TVS diode does not get damaged during the surge event. In this circuit, the 5.0SMDJ120A was used which has a breakdown voltage of 120 V.

D5 is used to suppress the main –250-V voltage spike event. To select the proper diode, there are a couple of parameters that must be considered. The first is that during the –250-V body diode of Q1 makes it so that the spike event is seen completely by Q2. This means that D5 should have a breakdown voltage that is less than the voltage rating of Q2. For this design, the 5.0SMDJ33CA is a bidirectional TVS diode that has a reverse breakdown voltage of –33 V which is lower than the voltage rating of Q2 (60 V).

2.2.5 Voltage Surge Event

Voltage surges are described in the MIL-STD-1275E documentation. In the section on *voltage surges*, two different voltage surge events are described that can occur during vehicle operation: injected and emitted voltage surges. However, for this reference design only the injected voltage surges pertain to the protection circuit.

The injected voltage surge is a 100-V surge that has a total energy content of 60 J. These injected voltage surge events typically occur during motor events, such as the main turret turning, which is then seen by any accessory that is connected to the 28-V bus.

2.2.6 Voltage Surge Event: Component Selection

To protect against the voltage surge event defined in MIL-STD-1275E, a two-stage clamping solution is used to deal with the large amount of energy, while helping to reduce overall solution size, and to allow for power to be provided throughout the entire surge event.

The advantage of using a two-stage clamping topology is that it reduces the amount of thermal and electrical stress on the MOSFET. For example, in the reference design, the first stage clamps the voltage from 100 V to 50 V, and the second stage goes from 50 V to 33 V. This means that Q1 must be able to handle a maximum of 4.28 A with a drain-to-source voltage of 50 V during the surge event.

To determine the MOSFET, the safe operating stress of the MOSFET must be calculated. There is a MIL-STD-1275E SOA calculator that can be downloaded to help determine if a MOSFET is capable of handling the

surge event. The first step is to approximate the surge envelope as a square pulse. To do that, find the total area under the curve (which equates to the energy) and then translate that to a square pulse for easier calculations.

1. The first portion of the surge event is the maximum 100 V for 50 ms. This means Q1 detects a 50-V drop across it, and the system pulls about 4.28 A at its maximum load. This results in a power dissipation on the MOSFET at 50 V × 4.28 A = 214 W for 50 ms, or 10.7 J of energy dissipation.
2. The second portion of the surge event is the linear decrease from 100 V at 50 ms to 33 V at 500 ms, which means the FET detects a voltage drop of 50 V to 0 V over that span. This results in about 107 W for 336 ms assuming a linear line between 100 V and 33 V or 36 J of energy dissipation
3. After calculating each segment of the surge event, the total power dissipation is 10.7 J + 36 J resulting in a total of 46.7 J.
4. Next, to approximate the equivalent time of the square wave, take the maximum power (214 W) and the total energy that was just calculated (46.7 J) and solve for the time which is 46.7 J / 214 W = 218 ms. Now, approximate that the MOSFET must withstand 214 W for 218 ms.

Calculate the amount of power the MOSFET can withstand for 218 ms at 25°C. The following equations are used to determine the safe operating area (SOA) of the MOSFET.

$$SOA(t) = a \times t^m \tag{1}$$

$$m = \frac{\ln(SOA(t_1)/SOA(t_2))}{\ln(t_1/t_2)}, \; a = \frac{SOA(t_1)}{t_1^m} \tag{2}$$

To solve for m and a, the information comes from the SOA graph found in the MOSFET data sheet. From the SOA graph, the important information is the time and the current capabilities at 50 V. So in this design, the IXTT88N30P was used, and using it as an example, the SOA(t_1) = 23 A for t_1 = 0.01 s. While SOA(t_2) = 13 A for t_2 = 1 s. Plugging in the numbers for the IXTT88N30P results in an SOA of 15.7 A, meaning that the IXTT88N30P can handle 439.6 W for 252 ms. Which indicates this is more than enough for a 120-W system at 25°C.

The second part of the SOA calculation is to calculate for thermal derating. To determine the thermal derating, the following equations are used:

$$SOA(T_C) = SOA(25ºC) \times \frac{T_{J,ABSMAX} - T_C}{T_{J,ABSMAX} - 25ºC} \tag{3}$$

$$T_C = T_A + R_{\theta CA} \times I_{LOAD,MAX}^2 \times R_{DSON}\left(T_J\right) \tag{4}$$

T_A is the ambient temperature of the system. For example, calculating the SOA of the IXTT88N30P at a T_A = 100°C results in an adjusted SOA of 6.15 A. Which means that the MOSFET can handle 172.2 W for 252 ms at 100°C.

2.3 Highlighted Products

2.3.1 LM7480-Q1

The LM7480x-Q1 ideal diode controller drives and controls external back-to-back N-channel MOSFETs to emulate an ideal diode rectifier with power path ON and OFF control and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 28-V military vehicle electrical systems. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path, the device allows load disconnect (ON and OFF control) and overvoltage protection using HGATE control. The LM7480x-Q1 independent gate drive topology, enables it to be configured in a common-source topology to provide load dump protection with reverse input protection.

2.3.2 LM5069

The LM5069 positive hot-swap controller provides intelligent control of the power supply connections during insertion and removal of circuit cards from a live system backplane or other hot power sources. The LM5069 provides in-rush current control to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-channel MOSFET are programmable, ensuring operation within the SOA. The POWER GOOD output indicates when the output voltage is within 1.25 V of the input voltage. The input undervoltage and overvoltage lockout levels and hysteresis are programmable, as well as the initial insertion delay time and fault detection time. The LM5069-1 latches off after a fault detection, while the LM5069-2 automatically restarts at a fixed duty cycle. LM5069 is available in a 10-pin VSSOP package.

To configure the LM5069 in a clamping configuration see the *AN-2040 Output Voltage Clamping Using the LM5069 Hot Swap Controller* application report.

3 Hardware, Testing Requirements and Test Results

3.1 Hardware Requirements

図 3-1 shows the TIDA-010242 board.

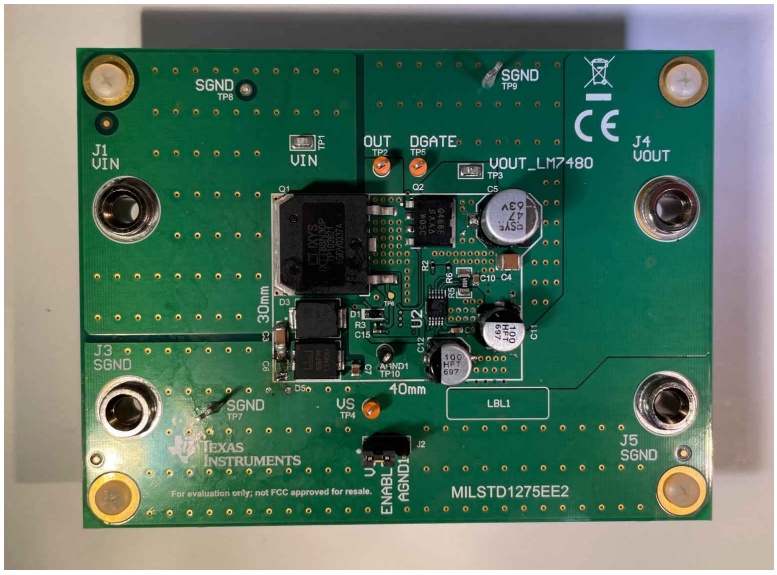

図 3-1. MIL-STD-1275E board

This sections shows how to setup the TIDA-010242 for testing.

1. **Power Supply Input** - Connect the input power to J1 and J3 (SGND). The nominal power supply is 28 V and put the current limit for the power supply at 5 A.
2. **Enable Jumper** - Place a shunt across pin 1 and 2 of J2 to enable the device. A shunt across 2 and 3 or the shunt is DNP disables the LM7480-Q1.
3. **Power Output** - The output power can be measured or connected to via J4 and J5 (SGND). These jumpers can also be used to connect to a electronic load for load testing.

3.2 Test Setup

To test the TIDA-010242, TI partnered with NTS to do the MIL-STD-1275E electrical testing. All test setups for reverse polarity, voltage spike, and voltage surge testing were in accordance to the MIL-STD-1275E as outlined in the section about *voltage compatibility verification*. Please refer to the standard for more information.

The following images show the test setup diagrams.

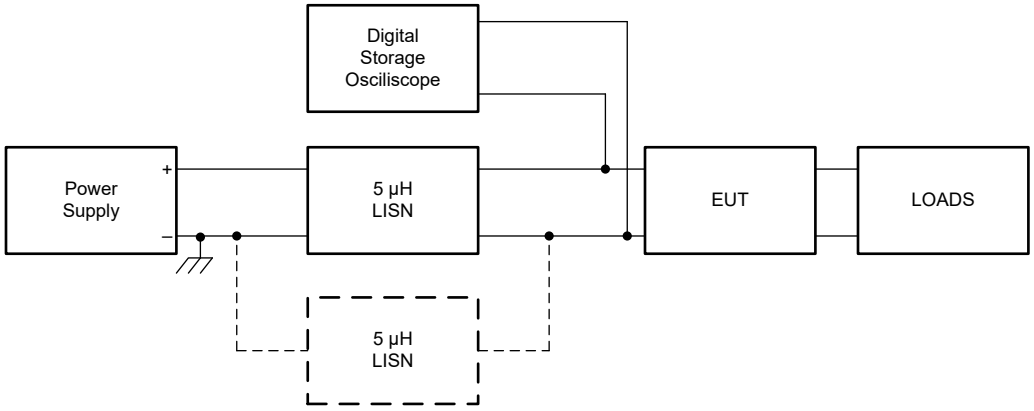

図 3-2. Emitted Spike Test Setup

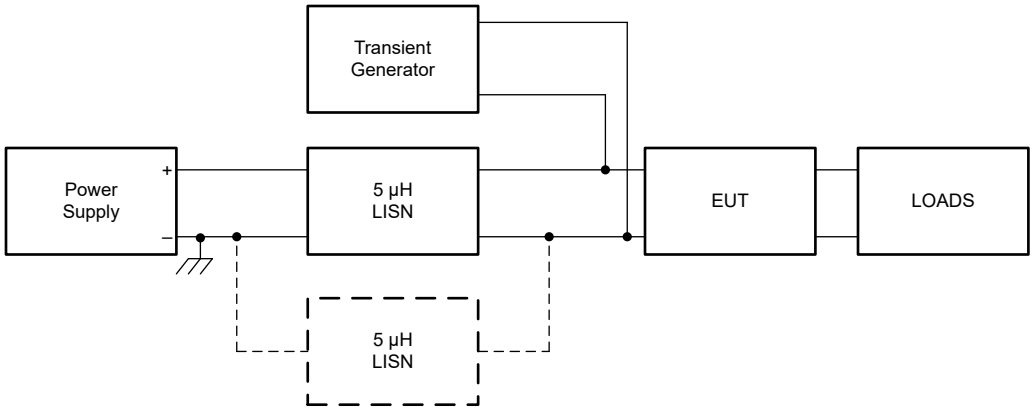

図 3-3. Injected Spike Test Setup

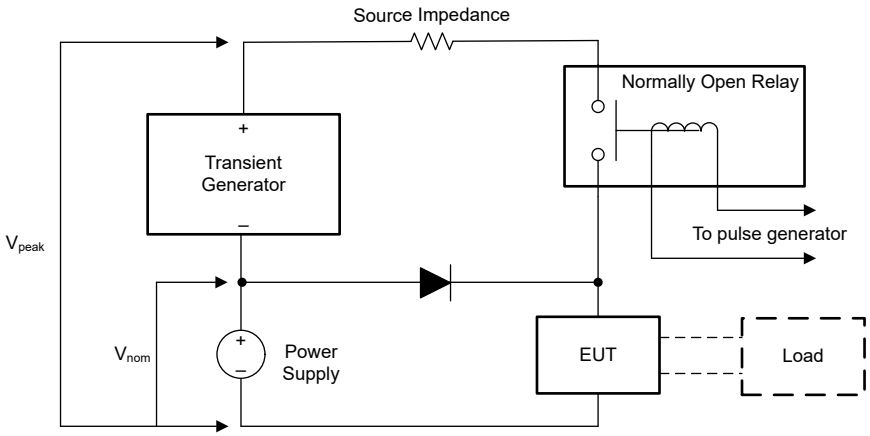

図 3-4. Surge Test Setup

3.3 Test Results

The following testing was done by NTS, and probed and captured by Texas Instruments.

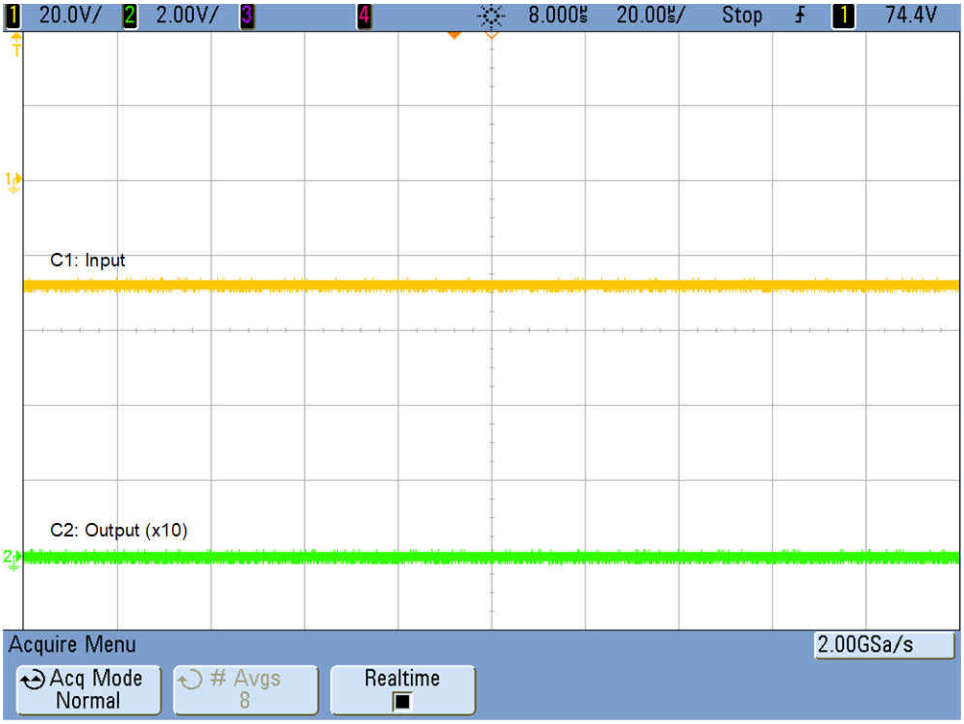

図 3-5. Reverse Polarity Event

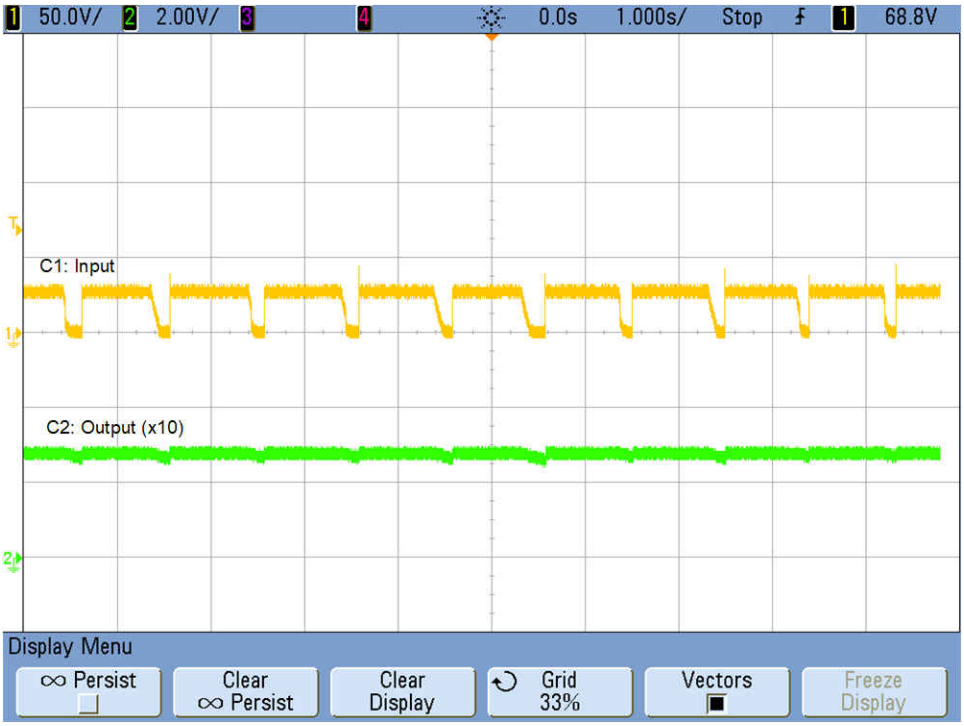

図 3-6. Emitted Voltage Spike Event

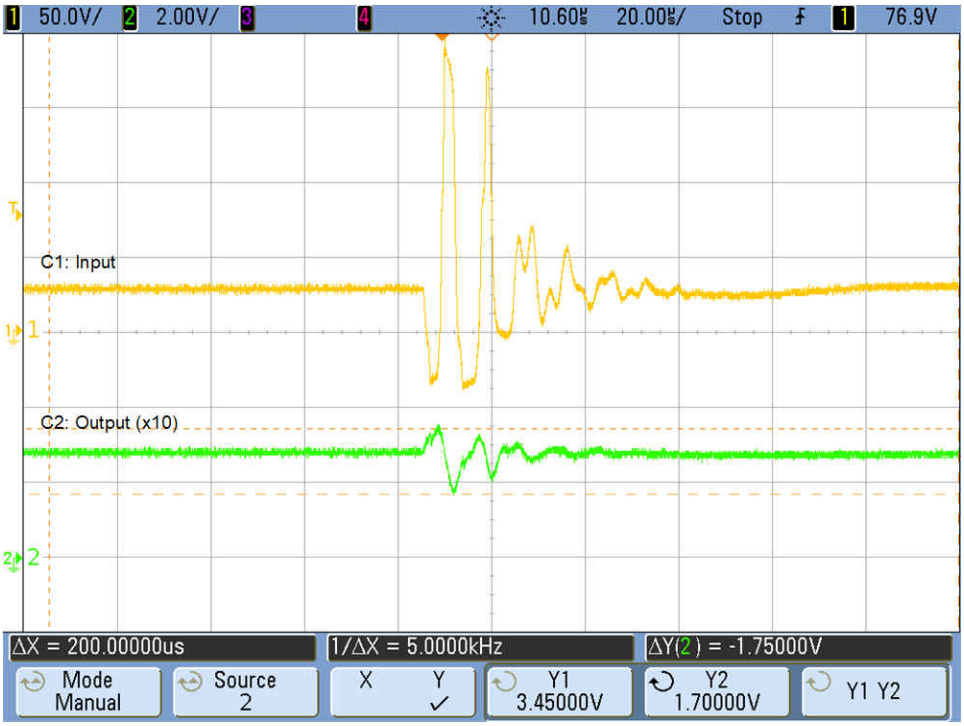

図 3-7. +250-V Injected Voltage Spike

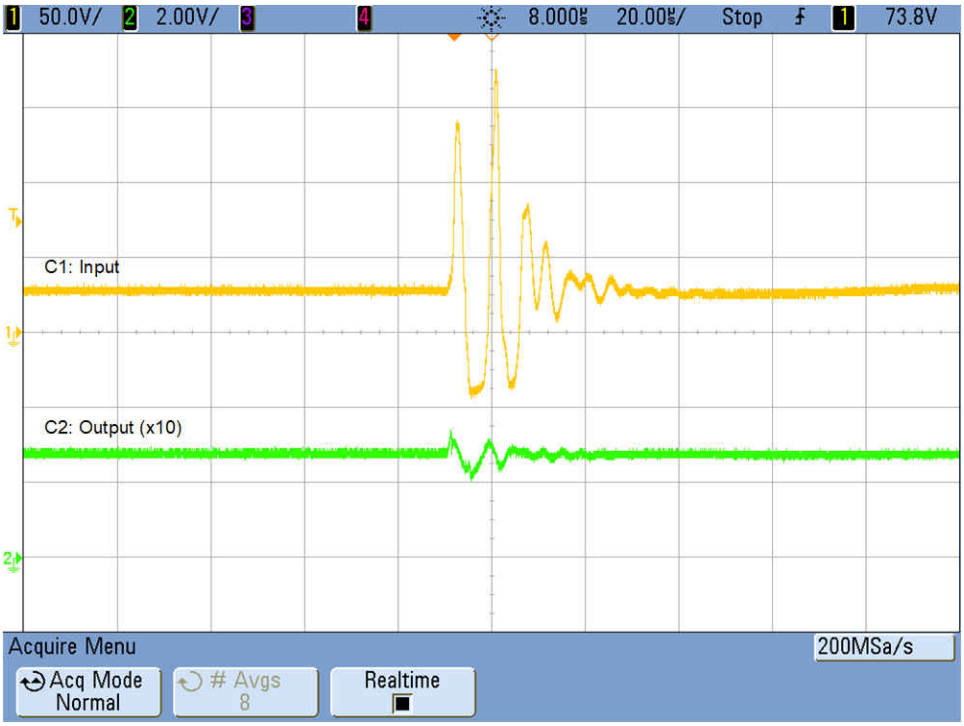

図 3-8. –250-V Injected Voltage Spike Event

図 3-9. 100-V Surge Event: Low Current

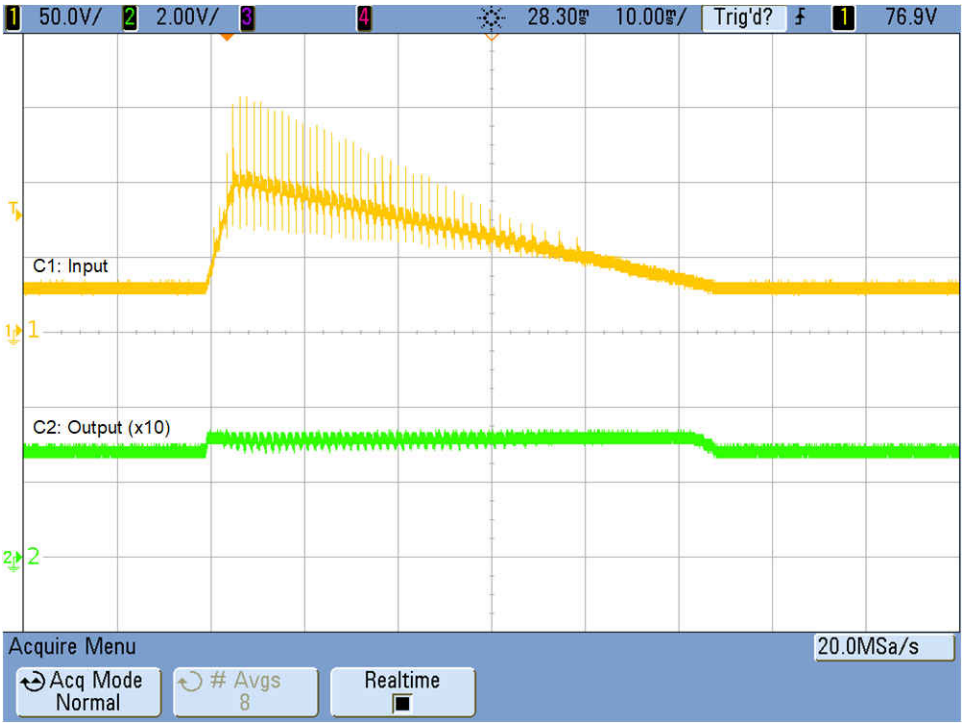

図 3-10. 100-V Surge Event: 2-A Load

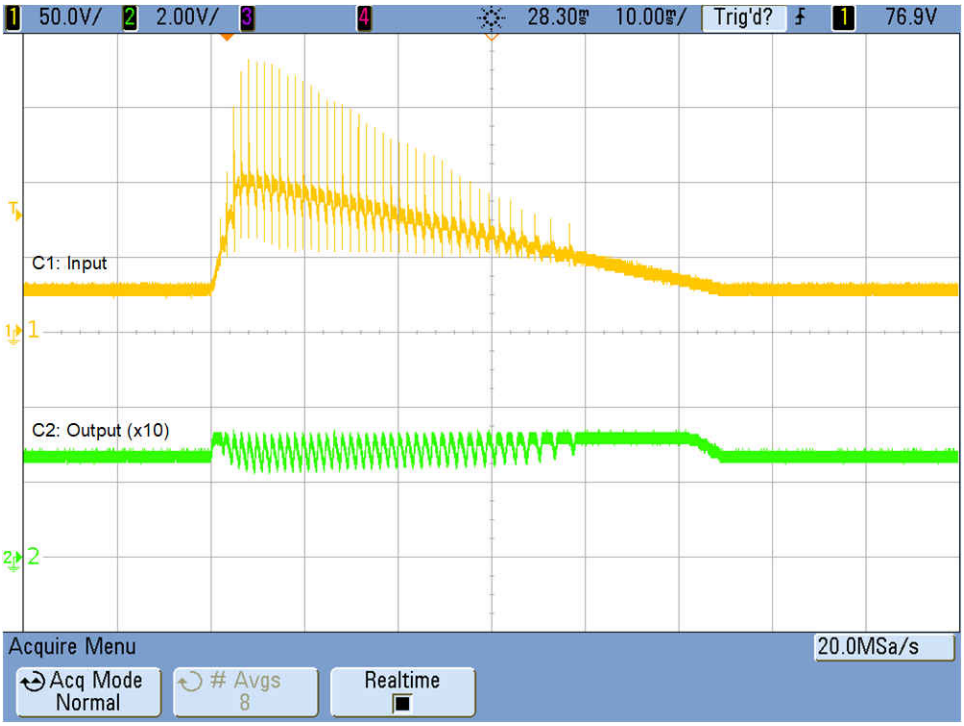

図 3-11. 100-V Surge Event: 4-A Load

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010242.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010242.

4.2 Documentation Support

1. Texas Instruments, *LM7480-Q1 Ideal Diode Controller with Load Dump Protection* data sheet
2. Texas Instruments, *LM5069 Positive High-Voltage Hot Swap and In-Rush Current Controller with Power Limiting* data sheet

4.3 サポート・リソース

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