参考資料

Design Guide: TIDA-010072

呼吸アプリケーション用の空気ブロワおよびバルブ制御のリファレンス・デザイン

概要

このリファレンス・デザインでは、最大 ±200kRPM/s のレートでモーターの加速と減速をサポートする、コンパクトなシステムの設計を示します。この加減速レートは、多くの呼吸器アプリケーションにとって重要な要件です。この設計は、TMS320F28027F など多数のオフボード C2000 コントローラをサポートしており、低コストのセンサレス FOC (フィールド・オリエンテッド制御) を実現できます。加えて、この設計は広い入力電圧範囲 (6～28V) もサポートしており、レギュレートされたライン電源とバッテリ電源の両方に対応できます。この設計では、空気ブロワやバルブを駆動するため、DRV8323R スマート・ゲート・ドライバと DRV8847 モーター・ドライバをそれぞれ使用しています。

リソース

TIDA-010072	デザイン・フォルダ
DRV8323R、DRV8847	プロダクト・フォルダ
LM5122、LMR33630	プロダクト・フォルダ
MSP430FR2155、TMP1075	プロダクト・フォルダ
TPS62840、TPS7A02	プロダクト・フォルダ

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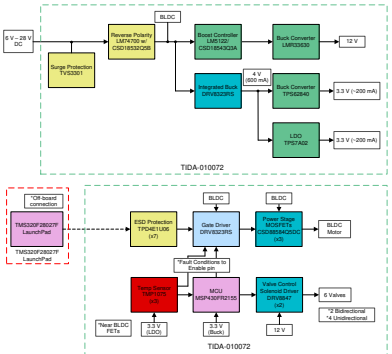
特長

- 最大 ±200kRPM/s の迅速な加速と減速
- 250ms の期間で 10kRPM から 40kRPM への速度変更が可能 (C65MS1-L5)
- 200ms の期間で 40kRPM から 10kRPM への速度変更が可能 (C65MS1-L5)
- 広い入力電圧範囲 (6～28V) をサポートしており、レギュレートされた DC 入力とバッテリ入力に対応できるほか、電源保護機能の搭載によりサージ、過電流、逆極性から保護
- DRV8323R モーター・ドライバと、オフボードの FOC 制御機能とを組み合わせることにより、静かで効率的に圧縮空気を生成
- UVLO、過電流、過熱などのドライバ保護機能を内蔵
- デュアル DRV8847 H ブリッジ・ステッパ・ドライバにより 6 個のソレノイド・バルブを制御

アプリケーション

- 呼吸補助装置
- 麻酔供給システム
- CPAP マシン
- 酸素濃縮器



1 System Description

1.1 Medical Respiratory Systems

There are several instances where it may become medically necessary for machines to assist with patient respiration, and these machines may require motors and valves depending on the specific application. For example, ventilators use motors to generate pressurized air and a system of valves to either deliver pressurized air or release air in the lungs back to the atmosphere to mechanically assist respiration. Ventilators can also be coupled with anesthesia delivery systems to keep the patient in a safe and anesthetized state. Anesthesia delivery systems incorporate numerous valves for drug mixing and patient protection. Ventilators are typically used in hospital, institutional, transport, and home environments.

There are three basic drive mechanisms in a ventilator system: bellows, piston, and turbine. For a bellows system, typically the air compression of a bellows is from a pneumatic force controlled by servo valves. For a piston system, typically the air compression is achieved from a BLDC or DC servo motor to move a piston. For a turbine system, typically a BLDC motor is used to drive a turbine (blower).

図 1-1. Ventilator system showing patient vital parameters

The key system requirements for a ventilator system are shown in 表 1-1.

表 1-1. Ventilator System Requirements

KEY REQUIREMENTS	TYPICAL
System reliability and functional safety	IEC 60601-1, ISO 80601-2
Accurate sensing of key parameters	flow, pressure, respiration rate, FiO2, temperature, and humidity
Power source	AC or DC
Efficient system design for portable systems	8-10 hours of continuous use on battery
DC power input voltage	6-28 V
Input power	150-200 W
Operation temperature range	5-40 °C
Operating pressure range	0 – 90 cmH_2O
Operating flow range	0-200 L/m
Flow accuracy	± 5 L/min or 20% of reading
Pressure accuracy	± 0.5 cmH_2O or 10% of reading

表 1-1. Ventilator System Requirements (continued)

KEY REQUIREMENTS	TYPICAL
Minimum inspiratory/expiratory time	200 ms
Valve response time	< 5ms
Motor operating voltage	24 V
Motor operating current	3-5 A continuous
High speed operation	40-60 kRPM
Wide operating speed range	1-60 kRPM
High accelerations and braking	150-200 kRPM/s

Note, many medical ventilators will also support continuous positive airway pressure (CPAP) operating mode and include an oxygen concentrator (for example, Ventec VOCSN, Medtronic Puritan Bennett™ 980). However, there are many standalone CPAP machines (for example, Philips DreamStation, ResMed AirMini™) and oxygen concentrators used for home healthcare. For CPAP machines, the pressurized air is delivered to sleeping patients through a mask to treat sleep apnea by helping to prevent the throat from closing.

Similar to ventilators, many CPAP machines and oxygen concentrators rely on a BLDC motor in their application to pressurize the air due their reliability, efficiency, and audible noise characteristics. In general, these standalone machines are designed to be portable and many weights less than 10 lbs. Standalone CPAP machines have less stringent motor requirements compared to ventilators. In addition, CPAP machines typically specify a lower sound level (~29 dBA) compared to ventilators (~50 dBA) and they have a narrower operating pressure range compared to ventilators.

The key system requirements for a CPAP system are shown in 表 1-2.

表 1-2. CPAP System Requirements

KEY REQUIREMENTS	TYPICAL
System reliability and functional safety	IEC 60601-1, ISO 80601-2
Accurate sensing of key parameters	Flow, pressure, temperature, and humidity
Power source	AC or DC
Efficient system design for portable systems	8-12 hours of continuous use on battery
DC power input voltage	6-28 V
Input power	30-80 W
Operation temperature range	5 to 35 °C
Operating pressure range	4-20 cmH_2O, sensor range 0-40 cmH_2O
Operating flow range	0-150 L/min
Flow accuracy	± 1.5 L/min or ± 2.7 % of reading (ISO 80601-2-70)
Static and dynamic pressure accuracy	± 0.15 , ± 0.27 cmH_2O (ISO 80601-2)
Sound level / noise emissions	<29 dBA (ISO 4871)
Service life	5 years
Physical weight	1-4 lbs
Motor operating voltage	12 or 24 V
Motor operating current	2-3 A continuous
High speed operation	30-40 kRPM
Wide operating speed range	1-40 kRPM

Standalone oxygen concentrators will similarly use a motor to pressurize air and will use multiple valves to mix air with pure oxygen to increase the oxygen concentration in the mixture delivered to the patient. One of the key differences in requirements compared to the previous applications is the lower motor speed (2-4 kRPM) due to a lower flow rate requirement (typically less than 2 L/min).

The key system requirements for an oxygen concentrator are shown in 表 1-3.

表 1-3. Oxygen Concentrator System Requirements

KEY REQUIREMENTS	TYPICAL
System reliability and functional safety	IEC 60601-1, ISO 8359, ISO 80601-2-67
Accurate sensing of key parameters	Flow, pressure, FiO2, temperature, and humidity
Power source	AC or DC
Efficient system design for portable systems	4-10 hours of continuous use on battery
DC power input voltage	10-28V
Input power	100-150W
Operation temperature range	5 to 35 °C
Maximum outlet pressure	30 to 90 psi
FiO2 Range	21-100 %
O2 sensor accuracy	3-6 %
Operating flow range	0-10 L/min
Flow accuracy	+/- 15 %
Sound level / noise emissions	40 dBA
Service life	5 years
Physical weight	5-10 lbs
Motor operating voltage	12 or 24 V
Motor operating current	2-5 A continuous
Motor speed	2-4 kRPM

1.2 Respirator System Components

Different respiratory applications will require various aspects of this reference design. CPAP machines will mainly need the BLDC motor driver portion of the design while Anesthesia delivery systems will require the valve driver portion. Oxygen concentrators and ventilators will use a combination of both. 図 1-2 shows a high-level block diagram of the system and delineates the separation between the valve drivers and motor driver. The system connects to a C2000 Launchpad to drive the BLDC motor.

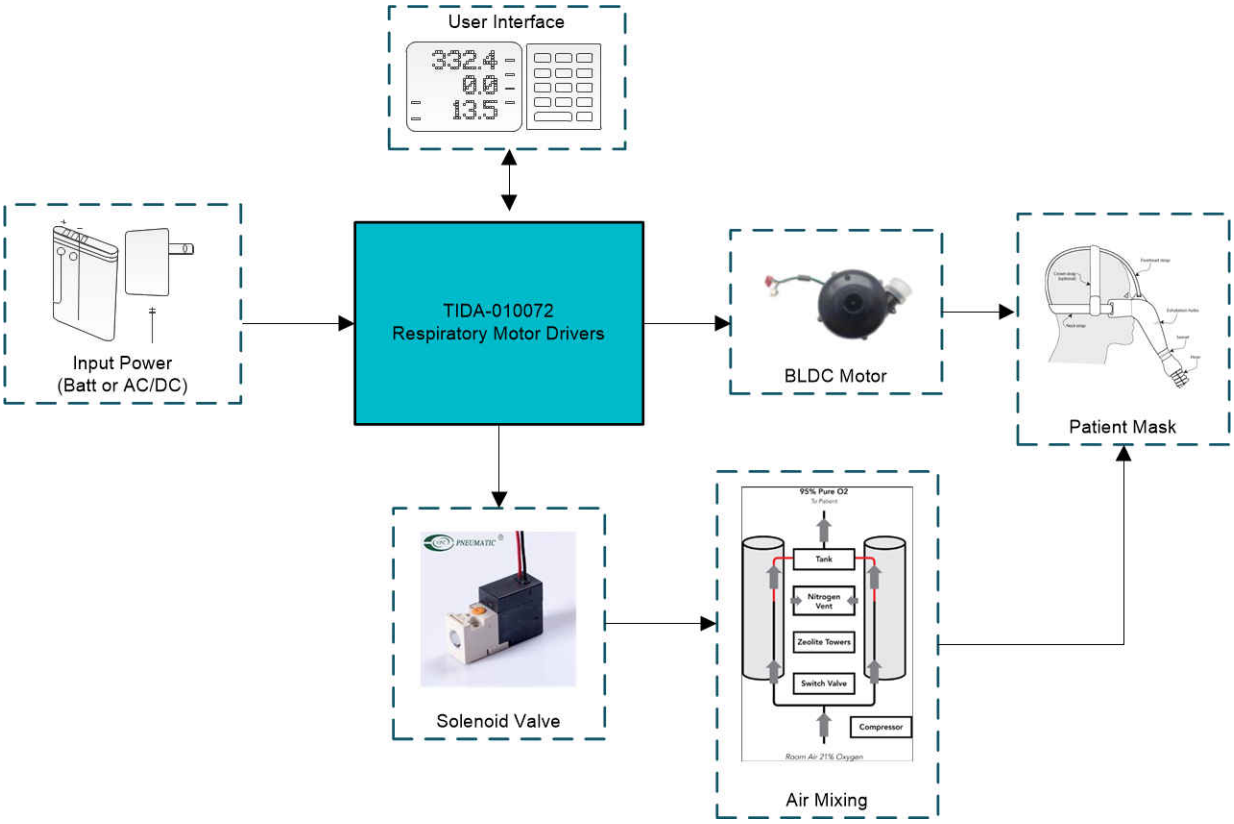


図 1-2. Respirator system block diagram

1.3 Key System Specifications

This reference design showcases a compact driver system design used to drive a single brushless DC (BLDC) motor and up to six solenoid valves. The BLDC motor is used to quietly and efficiently generate pressurized airflow. The solenoid valves are used to both create different gas mixtures and to provide safety mechanisms in the event of failures. The design supports up to 10 A of continuous motor drive, which can cover the motor operating requirements in most respirator applications. Additionally, this design includes a power tree capable of handling typical regulated DC voltage rails and battery voltage levels (6-28 V) for applications that are moving to portable designs.

表 1-4 lists the different characteristics and specifications of the TIDA-010072 board.

表 1-4. TIDA-010072 Key System Specifications

KEY REQUIREMENTS	TYPICAL
Input Voltage	6-28 V
BLDC Motor Current	10 A Continuous, 20 A peak
Max electrical frequency	1.2 kHz
Max Pulse Width Modulation (PWM) Frequency	45 kHz
Key Protection Features	Surge, OCP, UVLO, OTW/OTSD, and RVP
BLDC Motor Max Acceleration	200 kRPM/s
Solenoid Operating Voltage	12 V

表 1-4. TIDA-010072 Key System Specifications (continued)

KEY REQUIREMENTS	TYPICAL
Unidirectional Solenoid Drive	4 Channels
Bidirectional Solenoid Drive	2 Channels
Solenoid Drive Current	4x 0.5 A (unidirectional), 2x 0.5 A (bidirectional)
Max valve response time	1 ms
Operation Temperature Range	5 to 40 °C

DRV8323RS Integrated Protection Features:

- VM Undervoltage Lockout (UVLO)
- Charge Pump Undervoltage (CPUV)
- MOSFET Overcurrent Protection (OCP)
- Gate Driver Fault (GDF)
- Thermal Warning and Shutdown (OTW/OTSD)
- Fault Condition Indicator (nFAULT)

DRV8847 Integrated Protection Features:

- VM undervoltage lockout
- Overcurrent protection
- Open load detection
- Thermal shutdown
- Fault condition indication pin (nFAULT)

2 System Overview

2.1 Block Diagram

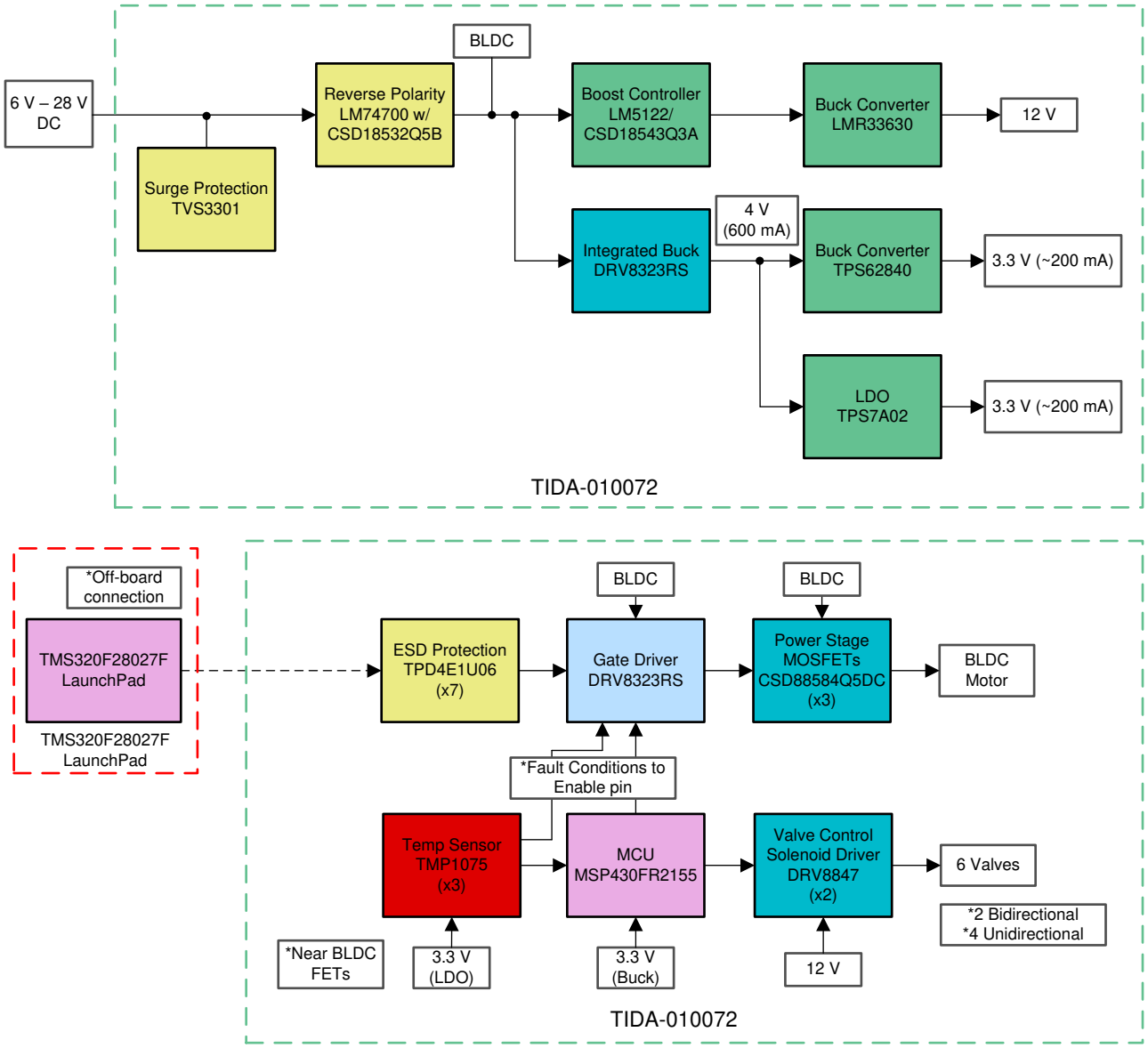


図 2-1. TIDA-010072 Block Diagram

This reference design is capable of driving a BLDC motor, four unidirectional valves, and two bidirectional valves in a compact and efficient platform. The DRV8323RS is selected as the BLDC motor driver with FOC control provided from an off-board Piccolo MCU. Three TMP1075 Integrted Circuits (ICs) are selected to monitor the temperature of the BLDC half-bridges to prevent over-temperature conditions. Two DRV8847 ICs are selected to drive the solenoid valves with control provided by the MSP430FR2155.

The system is capable of running off of a wide input voltage range of 6-28 V. This range covers typical battery input voltages as well as typical regulated DC voltages that are seen in many respiratory systems. The LM5122 boost controller is used to convert lower input voltages to 14 V, with a pass-through mode for higher voltages. The LMR33630 buck converter is used to step the output of the LM5122 down to a regulated 12 V, which is used by the DRV8847 ICs. The DRV8323RS uses the full input voltage range, and also integrates a buck converter, which is used to step the full input voltage range down to 4 V. The TPS7A02 low-dropout linear regulator (LDO) is selected to step 4 V down to a clean 3.3 V to power the temperature sensors. The TPS62840 buck converter

is selected to step 4 V down to 3.3 V to provide power for the remaining digital devices including the MCU, and system pull-up resistors.

2.2 Design Considerations

This reference design targets two key challenges for respiratory applications including CPAP machines, oxygen concentrators, ventilators, and anesthesia delivery systems. The first challenge is to achieve an efficient and quiet design for operating a three-phase BLDC air blower with multiple solenoid valve configuration options. The second challenge is to power the system from a wide input voltage range to account for typical regulated DC rails and newer portable 3s/4s battery applications.

2.2.1 Brushless DC Motor (BLDC)

Pressurized air for these applications can be generated using several motor types including brushed-DC (BDC), BLDC, and even AC motors. Of the three types mentioned, AC motors are the easiest to control. However, AC motors use additional energy to create the electromagnet, which decreases their efficiency, and they tend to be physically larger than both BDC and BLDC motors. AC motors also do not have capability to change speed quickly. BDC motors tend to have a lower cost and simpler control schemes than BLDC motors. However, BLDC motors offer several advantages that make them especially desirable for respiratory medical applications. The largest benefit of these motors is that they lack the brushes and are contactless, which means that they are inherently much quieter than BDC motors and will have a longer lifetime. Brushed-DC motors will wear out more quickly due to the brushes degrading over time. Additionally, while the control can be far more complex for BLDC motors, BLDC motors are the most efficient motor type and smallest in size for a given motor power. Brushless-DC motors are also capable of the highest speed and best dynamic speed performance (acceleration and deceleration) compared to other motor types.

To achieve the quietest and most efficient operation, field-oriented control (FOC) is often used as a control algorithm. FOC is a technology that applies all torque on the motor perpendicular to the rotor; this allows for maximum drive effectiveness. Additionally, many systems implement a sensorless control scheme, meaning that there are no Hall-Effect sensors embedded on the motor itself. Sensorless drive schemes allow a wider range of motors to be used, however sensored drive systems may also be implemented if the motor used has sensors built in. TI features a technology called InstaSpin-FOC, which runs on select Piccolo series MCU and can be a quicker way to bring up sensorless FOC compared to designing the control scheme from the ground up.

The DRV8323RS was selected as the motor gate driver for this design based on several features. For example, the DRV8323RS has three integrated half-bridge drivers capable of sourcing 2 A and sinking 1 A to the MOSFET gates. It also integrates the charge pump for the high side MOSFETs for 100% duty cycle, an asynchronous buck converter capable of supporting up to 600 mA for external use, and three low-side current sense amplifiers to sense the motor current. Another important aspect in the selection of this device is that it is capable of handling the entire voltage range desired for this reference design, 6-28 V.

To achieve the desired FOC algorithm, the latest Piccolo MCU, TMS320F28027F, has been selected to run TI's InstaSpin-FOC control software. The reference design includes connectors to attach to the Piccolo's Launchpad. In this way, FOC is integrated into the design through a plug-and-play peripheral to allow users to easily test this control algorithm.

2.2.1.1 DRV8323RS BLDC Motor Driver Design Calculations

External MOSFET Support

The DRV832x MOSFET support is based on the capacity of the charge pump and PWM switching frequency of the output. For a quick calculation of MOSFET driving capacity, use the following equations for three phase BLDC motor applications.

Trapezoidal 120° Commutation:

$$I_{VCP} > Q_g \times f_{pwm} \quad (1)$$

Sinusoidal 180° Commutation and FOC:

$$I_{VCP} > 3 \times Q_g \times f_{pwm} \quad (2)$$

where

- f_{pwm} is the maximum desired PWM switching frequency
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage
- The multiplier based on the commutation control method, may vary based on implementation
- Q_g is the total gate charge

The DRV8323RS device is capable of supporting PWM frequencies up to 200 kHz and the selected CSD88584Q5DC power block is capable of 50 kHz. However, the actual PWM frequency will be limited by the charge pump specification. For a VM supply voltage ≥ 13 V, the charge pump is rated for 25 mA and the V_{cp} operating voltage is 11 V relative to VM. From the CSD88584Q5DC data sheet, the typical Q_g is rated at 137 nC (178 nC max).

The maximum 24-V application PWM frequency operating FOC is:

$$f_{pwm} < \frac{I_{VCP}}{3 \times Q_g} = \frac{25\ mA}{3 \times 178\ nC} = 46.8\ kHz \quad (3)$$

In this design, the PWM frequency was set to 45 kHz.

Power Dissipation Calculations

The maximum input supply of 28 V and I_{load} of 10 A were used for the following calculations. These calculations are applicable for sinusoidal PWM (SPWM) and FOC motor controls. Note, for sinusoidal and FOC, each FET has 180º of conduction. The CSD88584q5dc and DRV8323RS data sheets were referenced for the electrical specifications. Each loss type is split evenly between the high and low FETs.

Half-bridge FET Losses

The max conduction loss for the half-bridge is:

$$P_{COND} = {I_{RMS}}^2 \times R_{DS\_ON} \times 1.5 = {I_{load}}^2 \times R_{DS\_ON} \times 1.5$$
$$P_{COND} = {I_{load}}^2 \times R_{DS\_ON} \times 1.5 = 10A^2 \times 0.95m\Omega \times 1.5 = 143\ mW \quad (4)$$

The 1.5 correction factor accounts for junction temperature effect on the FET resistance. That is, a 50% increase in resistance due to temperature. This is a rule-of-thumb for moderate junction temperature (50-100 ºC). If the FET junction operates at 125 ºC, this factor must be adjusted accordingly (e.g. 1.8 instead).

The DRV8323 can source and sink up to 1A and 2A, respectively. The rise and fall switching times are:

$$t_R = \frac{Q_{gs(afterVth)} + Q_{gd}}{I_{source}} = \frac{Q_{gs} - Q_{g,Vth} + Q_{gd}}{I_{source}} = \frac{24\ nC - 16\ nC + 26\ nC}{1A} = 34\ ns$$
$$t_F = \frac{Q_{gs(afterVth)} + Q_{gd}}{I_{sink}} = \frac{Q_{gs} - Q_{g,Vth} + Q_{gd}}{I_{sink}} = \frac{24\ nC - 16\ nC + 26\ nC}{2\ A} = 17\ ns \quad (5)$$

where t_R and t_F are the switching times (including the rise and fall times) corresponding to the rise and fall transitions.

The max switching loss for the half-bridge is (assume negligible soft switching losses):

$$P_{SW} = 0.5 \times VM \times I_{load} \times (t_R + t_F) \times f_{sw}$$
$$P_{SW} = 0.5 \times 28V \times 10A \times (34\ ns + 17\ ns) \times 45\ kHz = 321\ mW \quad (6)$$

注

The recommended rise and fall times for most applications is around 100 ns.

The dead time loss is:

$$P_{DT} = V_D \times I_{load} \times t_{dead} \times f_{sw} \quad (7)$$

$$P_{DT} = 1\ V \times 10\ A \times 200\ ns \times 45\ kHz = \ 90\ mW \quad (8)$$

The DRV8323RS's dead time is programmable with 50-ns, 100-ns, 200-ns, and 400-ns options. The default setting is 100 ns. There are two instances of dead time per a switching cycle.

The reverse recovery charge loss is:

$$P_{RR} = Q_{rr} \times VM \times f_{sw}$$
$$P_{RR} = 34\ nC \times 28\ V \times 45\ kHz = 43\ mW \quad (9)$$

The gate drive voltage is 11 V (typical) for VM >13 V and the Q_g (V_{gs} =10 V) is 178 nC from the data sheet.

Assume half of the gate charge loss is on the FET side and half on the driver IC side. The half-bridge gate charge loss is:

$$P_G = 0.5 \times V_{gs} \times (Q_{G(LS)} + Q_{G(HS)}) \times f_{sw}$$
$$P_G = 0.5 \times 11V \times 356nC \times 45kHz = 88mW \quad (10)$$

The total half-bridge loss is:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{DT} + P_{RR} + P_G$$
$$P_{LOSS} = 143\ mW + 321\ mW + 90\ mW + 43\ mW + 88\ mW = 685\ mW \quad (11)$$

DRV8323RS Driver Losses

The operating supply current loss is:

$$P_{VM} = VM \times I_{VM}$$
$$P_{VM} = 28\ V \times 14\ mA = 392\ mW \quad (12)$$

$$P_{DVDD} = (VM - VDD) \times I_{VDD}$$
$$P_{DVDD} = 0 \quad (13)$$

For high-side (HS) driver supply loss, assume a 50% charge pump efficiency:

$$P_{CP\_GH} = P_{out} \times \frac{1-\eta}{\eta} = 3 \times (V_{gs} \times Q_g \times f_{sw}) \times \frac{1-\eta}{\eta}$$
$$P_{CP\_GH} = 3 \times 11\ V \times 178\ nC \times 45\ kHz \times \frac{1-0.5}{0.5} = 264\ mW \quad (14)$$

For low-side (LS) driver supply loss:

$$P_{LDO\_GL} = 3 \times (VM - V_{gs}) \times Q_g \times f_{sw}$$
$$P_{LDO\_GL} = 3 \times (28\ V - 11\ V) \times 178\ nC \times 45\ kHz = 408\ mW \quad (15)$$

For gate drive loss inside driver IC, again assume half is on the driver side. Note, the driver drives three half-bridges:

$$P_{G\_IC} = 0.5 \times V_{gs} \times 3 \times (Q_{g(LS)} + Q_{g(HS)}) \times f_{sw}$$
$$P_{G\_IC} = 0.5 \times 11V \times 3 \times 356\ nC \times 45\ kHz = 264\ mW \quad (16)$$

For the DRV8323RS integrated buck (LMR16006X), assume a maximum load of 200 mA and an 85% efficiency:

$$P_{BUCK} = P_{out} \times \frac{1-\eta}{\eta}$$
$$P_{BUCK} = (4\ V \times 200\ mA) \times \frac{1-0.85}{0.85} = 141\ mW \quad (17)$$

The total driver IC loss is:

$$P_{LOSS\_DRV\_IC} = P_{VM} + P_{CP\_GH} + P_{LDO\_GL} + P_{G\_IC} + P_{BUCK}$$
$$P_{LOSS\_DRV\_IC} = 392\ mW + 264\ mW + 408\ mW + 264\ mW + 141\ mW = 1.5\ W \quad (18)$$

Junction Temperature Estimation

For CSD88584q5dc power block, assume a $R_{\theta JA}$ = 50 °C/W (1 in^2 of 2-oz Cu) based on the data sheet:

$$T_J = T_{ambient} + R_{\theta JA} \times P_d \quad (19)$$

$$T_J = 40\ C + \frac{50\ C}{W} \times (685\ mW) = 74\ C \quad (20)$$

For DRV8323RS (RGZ package) driver, assume a $R_{\theta JA}$ = 26.6 °C/W based on the data sheet:

$$T_J = 40\ C + \frac{26.6\ C}{W} \times (1.5\ W) = 80\ C \quad (21)$$

These temperature estimates are well below the max ratings, which allows for an adequate operating margin.

IDRIVE Configuration

The strength of the gate drive current, IDRIVE, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If IDRIVE is selected to be too low for a given MOSFET, then the MOSFET may not turn on completely within the tDRIVE time and a gate drive fault may be asserted. In this design, the default IDRIVE was set to 1A/2A (default). However, for most applications, a lower drive current is recommended to reduce EMI.

VDS Overcurrent Monitor Configuration

The VDS monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs. Using a 1.8 temperature factor for 0.95 mΩ, the max $R_{DS(on)}$ is 1.7 mΩ. The target OCP threshold is 30 A so V_{DS_OCP} must be:

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max}$$
$$V_{DS\_OCP} > 30\ A \times 1.7\ m\Omega = 51\ mV \quad (22)$$

The V_{DS_OCP} threshold was set to 60 mV (closest available) and the OCP deglitch time was set to 4 µs (default).

Unidirectional Current Sense Operation

The sense amplifier gain and sense resistor values are selected based on the target current range, V_{REF}, power rating of the sense resistor, and operating temperature range. In unidirectional operation of the sense amplifier, use the following equation to calculate the approximate value of the dynamic range at the output:

$$V_{O\_DR} = (V_{ref} - 0.25\ V) - 0.25\ V$$
$$V_{O\_DR} = 3.3\ V - 0.5\ V = 2.8\ V \quad (23)$$

Using the default gain of 20 V/V and the maximum input current of 12 A (10 A plus a 20% margin):

$$R_{sense} < \frac{V_{O\_DR}}{Gain \times I_{max}}$$
$$Rsense < \frac{2.8\ V}{20\ V/V \times 12\ A} = 11.7\ m\Omega \quad (24)$$

10 mΩ was selected for Rsense. The minimum power rating for Rsense must be:

$$P_{R\_SENSE} > I^2 \times R = 12\ A^2 \times 10\ m\Omega = 1.44\ W \quad (25)$$

In this design, a 10-mΩ, 3-W Rsense was used for each of the three channels. In addition, 1.3-kHz RC low pass filters were used for these sensing channels to limit noise.

The full scale ADC current is (ignore the headroom limitation):

$$I = \frac{V_{ref}}{Gain \times R_{sense}} \quad (26)$$

$$I_{FS\,(ADC)} = \frac{3.3\ V}{20V/V \times 10\ m\Omega} = 16.5\ A \quad (27)$$

注

This value is defined as USER_ADC_FULL_SCALE_CURRENT_A in the user.h file.

Buck Regulator Configuration

The LMR16006 buck is capable of supplying up to 600 mA. The switching frequency is fixed at 700 kHz (typical). In this design, the buck was configured for a 4-V output. The expected application load is 200 mA. This 4-V rail is the primary supply for the digital loads. The basic inductor calculations are shown below. For more information, please reference the LMR16006 data sheet design example.

The first step to calculate the peak inductor/switch current is to determine the duty cycle, D, for the maximum input voltage. The maximum input voltage is used because this leads to the maximum switch current:

$$D_{min} = \frac{V_{out}}{V_{in}} = \frac{4\ V}{28\ V} = 0.143 \quad (28)$$

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20 to 40 % of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load (0.2 A) than the maximum available from the device (0.6 A), the maximum device current should be used:

$$L = \frac{V_{out}}{I_{out} \times RR \times f_{sw}} \times (1 - D)$$
$$L = \frac{4\ V}{0.6\ A \times 0.4 \times 700\ kHz} \times (1 - 0.143) = 20.4\ \mu H \quad (29)$$

RR of 0.4 was selected.

For this design, 22 µH was selected.

The actual worst-case ripple current is:

$$\Delta I_L = \frac{V_{out}}{f_{sw} \times L} \times (1 - D)$$
$$\Delta I_L = \frac{4\ V}{700\ kHz \times 22\ \mu H} \times (1 - 0.143) = 0.22\ A \quad (30)$$

The actual ripple ratio is:

$$RR = \frac{\Delta I_L}{I_{out}} = \frac{0.22A}{0.6A} = 0.37 \quad (31)$$

The peak inductor/switch/diode current and the minimum saturation current rating of the inductor plus a 25% margin are calculated as follows:

$$I_{peak} = I_{out} \times \left(1 + \frac{RR}{2}\right)$$
$$I_{peak} = 0.6\ A \times \left(1 + \frac{0.37}{2}\right) \times 1.25 = 0.89\ A \quad (32)$$

The LMR16006 has a current limit at 1.7 A (max). Using a saturation rating near 1.7 A will enable the LMR16006 to current limit without saturating the inductor. This is preferable to the LMR16006 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

In this design, the selected inductor (74438356220) has saturation ratings of 1.85 A (ΔL=-20%). Based on the data sheet, this inductor RMS rating is well suited to handle 1.7 A with a 40 ºC rise.

For the RMS current calculations, the 0.2 A max application current is used instead of the device maximum:

$$I_{RMS} = I_{out} \sqrt{1 + \frac{RR^2}{12}}$$
$$I_{RMS} = 0.2A \sqrt{1 + \frac{0.37^2}{12}} = 0.2\ A \quad (33)$$

Note, I_{RMS} is approximately I_{out} given a small RR value.

Inductor wire loss is calculated as follows:

$$P_{IND\_DC} = {I_{RMS}}^2 \times R \cong {I_{out}}^2 \times R = 0.2A^2 \times 250\ m\Omega = 10\ mW \quad (34)$$

Temperature monitor and over temperature protection

The design is equipped with three TMP1075 digital temperature sensors designed to monitor and protect the power blocks. Three TMP1075 ALERT outputs (active low) and the DRV8323RS Enable control signal are connected to a quad-input AND gate. The DRV8323RS will be disabled if one of the inputs is logic LOW.

2.2.1.2 BLDC Motor Driver Circuit

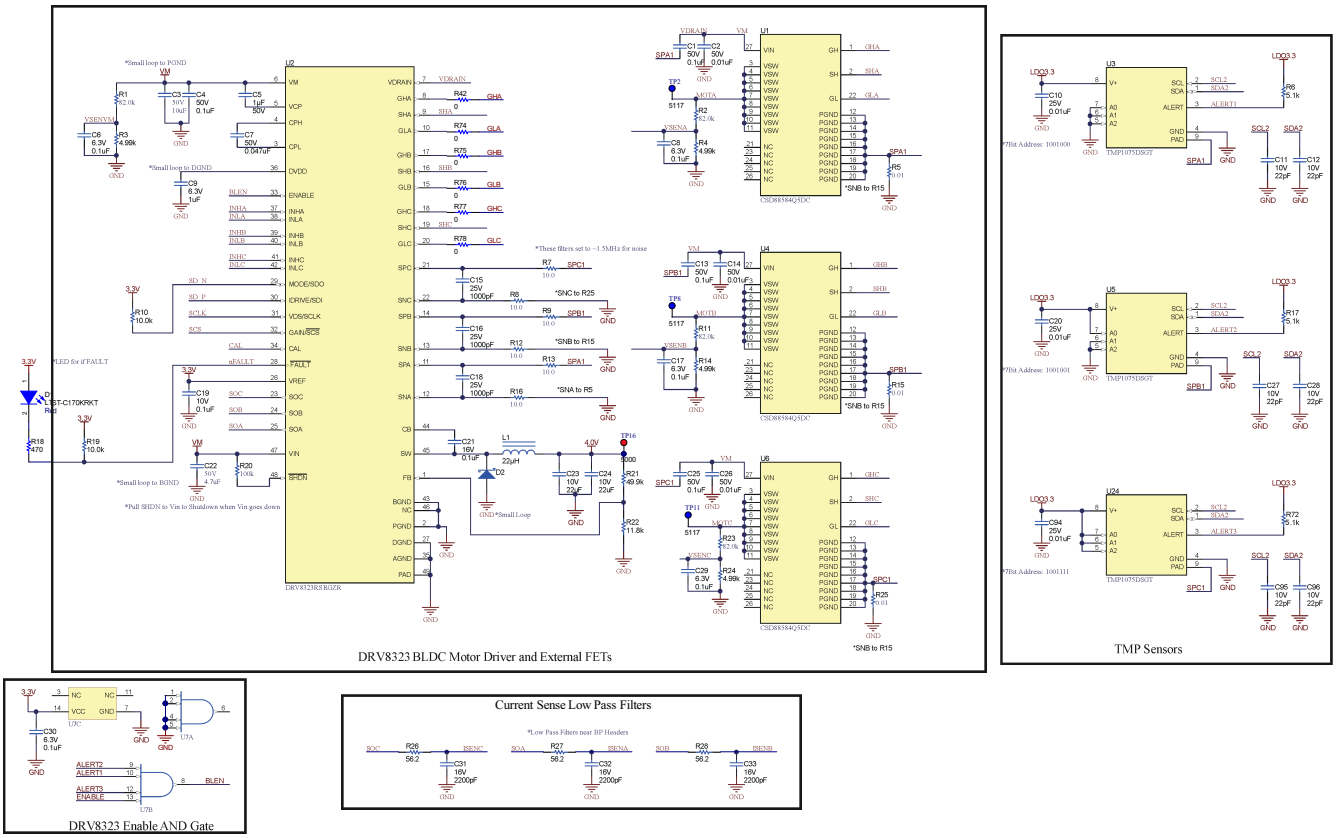


図 2-2. BLDC Motor Driver Circuit

2.2.2 Solenoid Valve Drivers

Solenoid valves are a key component of many respiratory applications, such as oxygen concentrators, and are used to accomplish multiple functions. Oxygen concentrators use a compressor to separate air and oxygen into separate canisters. Solenoid valves are then activated to release specified amounts of each gas into a chamber, which then uses a separate valve to supply the mixture to the patient through a mask. Solenoid valves can also be used to stop the flow of gas to the mask if a fault is detected. These valves are similarly useful in anesthesia delivery systems where multiple gases are typically mixed together before delivery to the patient. Oxygen concentrators tend to have 4 – 6 such valves while anesthesia delivery systems tend to have more than 15.

Solenoid valves have different configurations for how they can control the flow of fluid or gas. The simplest configuration is a 2-way valve that connects two pipes or tubes together, but there are also options for 3-way and 4-way junctions that can simple on/off, binary/latching or dithering valves. Each different valve type requires a different control method, but this reference design focused only on controlling the simplest, the on/off valves. On/off valves have a natural, un-energized position and are operated by applying current to energize the solenoid, which changes the position of the valve. In a naturally closed 2-way valve, the valve will be closed and prevent the flow of fluid or gas until the solenoid is energized, which will open the valve to flow. As an alternative example, in a 3-way junction valve, the natural position will connect two of the three pipes together and will connect two different pipes when the valve is energized.

The control for on/off valves can be straight forward implementation in which current needs to be applied to the solenoid to energize the valve. Some on/off valves are unidirectional, in that they can only accept current in a single direction to be energized, while others are bidirectional. The amount of current required depends on the specific valve, but the current waveform for solenoid valves is consistent. A peak current is required to energize the valve initially while a lower amount of current is required to maintain the energized state. Regardless of directionality, these valves can be minimally controlled by a low-side or high-side MOSFET and valve driver that can receive input from an MCU to energize the valve. While simple, this control scheme can be inefficient because it will maintain current flow at the peak current rather than reducing to maintain the energized state. By

adding a current feedback path it is possible to implement peak-and-hold control which backs off the current but maintains the energized state to increase system efficiency. Some valve drivers integrate the peak-and-hold control while others will require the MCU to read the current and implement that control.

For this reference design, the DRV8847, an 18-V, 2-A dual H-bridge motor driver, was selected to drive the solenoid valves. Each of the half bridges in the device can be independently controlled, which means that the DRV8847 is capable of driving up to four unidirectional valves or two bidirectional valves. This design has two DRV8847 ICs, one for unidirectional control and one for bidirectional control. The DRV8847 is capable of driving 1 A through each half bridge and the integrated MOSFETs have a 1-Ω $R_{DS(on)}$. The device also integrates a current sense amplifier to do overcurrent protection; however, the driver does not incorporate options for peak-and-hold control, so this would have to be implemented by the MCU. Each half-bridge of the DRV8847 is driven by PWM from a local MCU, which was selected as the MSP430FR2155. This MCU was selected because it has all of the required peripherals, is physically small, and is cost-effective.

Pumps are also an integral part of ventilation system that helps with pumping air and medicine to the lungs. These pumps often need precise and fine motorized control that can operate electrically. Stepper motor and dual H Bridge drivers are favored with high microstepping like DRV8825 and DRV8886AT.

As system requirements can vary, solenoids/valves and pumps may be connected to a 12-V, 24-V, 36-V or even 48-V rail with varying current requirement. Some other key devices to be considered based on system requirements are as follows:

表 2-1. Alternative Devices to be Considered Based on System Requirements

DEVICE	SYSTEM CONDITION	FUNCTION
DRV8876, DRV8874	37 V, 3.5 A peak for bidirectional control or independent control for 2 solenoid	Operate solenoid/valve
DRV8844	Up to 60 V, 2.5 A drive quad independent half bridge for 4 solenoid control	Operate solenoid/valve
DRV8886AT	40 V, 1 A to 2 A FS dual H-bridge motor driver	Operate pump
DRV8825	47 V, 1.6 A FS dual H-Bridge motor driver	Operate pump

2.2.2.1 DRV8847 Solenoid Driver Design Calculations

The DRV8847 device is configured for independent half-bridge operation. Mode selection is done using the I^2C registers in the DRV8847S device variant. Refer to the data sheet for more details. The solenoid driver design is summarized below:

表 2-2. Solenoid Driver Design Summary

PARAMETER	SPECIFICATION
Solenoid operating voltage	12 V
Unidirectional solenoid drive	4 Channels
Bidirectional solenoid drive	2 Channels
Solenoid drive current	4x 0.5 A (unidirectional), 2x 0.5 A (bidirectional)
Max valve response time	1 ms
Operation temperature range	5-40 °C

Based on the data sheet, the DRV8847 integrated FET max $R_{DS(on)}$ is 700 mΩ (VM = 12 V; I_{OUT} = 0.5 A; T_A = 85 °C). For unidirectional drive, each channel conduction loss is:

$$P_{COND} = {I_{load}}^2 \times R_{DS\_ON} = 0.25A^2 \times 700\ m\Omega = 175\ mW \quad (35)$$

For four active channels, the total conduction loss is 700 mW. The junction temperature is calculated as follows:

$$T_J = T_{ambient} + R_{\theta JA} \times P_d = 40\ C + \frac{108\ C}{W} \times (4 \times 175\ mW) = 116\ C \quad (36)$$

For bidirectional drive, each channel conduction loss is

$$P_{COND} = I_{load}{}^2 \times (R_{DS\_ON\_HS} + R_{DS\_ON\_LS}) = 0.5\ A^2 \times 1.4\ \Omega = 350\ mW \quad (37)$$

For two active channels, the total conduction loss is 700 mW. The junction temperature is calculated as follows:

$$T_J = T_{ambient} + R_{\theta JA} \times P_d = 40\ C + \frac{108\ C}{W} \times (2 \times 350\ mW) = 116\ C \quad (38)$$

This junction temperature allows some margin for other sources of power dissipation and design tolerances.

The switching frequency for solenoid is expected to be relatively low (e.g. 200 Hz), thus the switching loss is negligible:

$$P_{SW} = 0.5 \times VM \times I_{load} \times (t_R + t_F) \times f_{sw}$$
$$P_{SW} = 0.5 \times 12\ V \times 0.5\ A \times (300ns) \times 200\ Hz = 0.18\ mW \quad (39)$$

2.2.2.2 Solenoid Driver Circuit

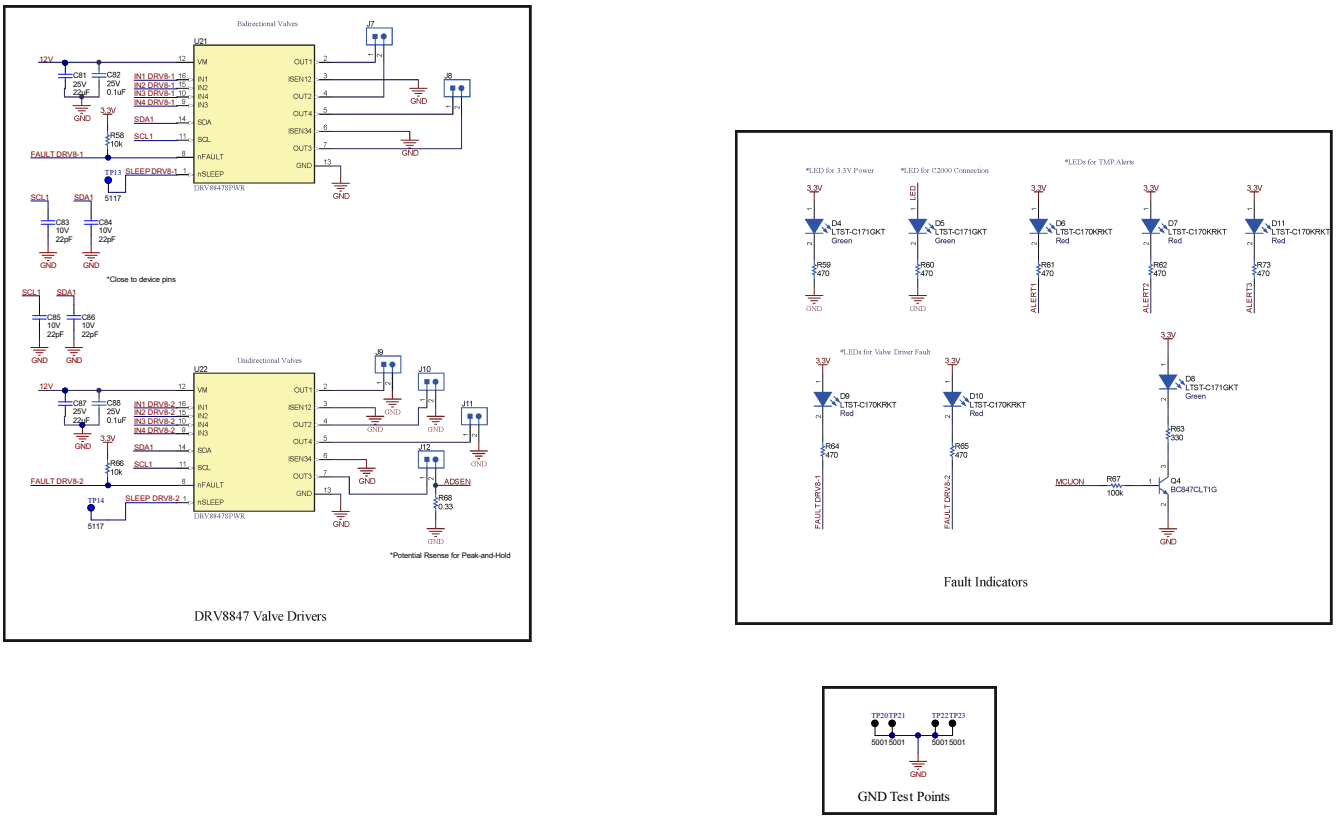


図 2-3. Solenoid Driver Circuit

2.2.3 Power Tree Architecture

Historically, these respiratory applications have used isolated AC/DC power bricks to provide 12 V, 19 V, or 24 V DC bus voltages to the system. The system then either uses the higher DC bus voltage to drive the motors and valves directly, or they step down the voltage through a buck converter. However, as the market for many of these systems move towards portability, they will have to be operated off of battery voltages which are estimated to range from 6-14 V. Given this shift, the reference design has a defined input voltage range of 6-28 V. Additionally, the transition to portability means that the key system requirements include high efficiency to allow longer battery lifetimes. Generally, solution size also has a higher priority for these systems, which was considered in this reference design.

The DRV8323RS is capable of operating under the full voltage range, so the DRV8323RS and BLDC motor has been tied directly to the input voltage source. However, solenoid valves need to operate at a single DC voltage,

so a stable 12 V DC voltage was selected as a required rail. Given that 12 V falls in the middle of the input voltage range a buck-boost or SEPIC topology converter would be the optimal choice to generate the 12 V DC rail. However, with the understanding that some manufacturers will only need a buck converter (for regulated DC inputs) or a boost converter (for battery inputs), separate buck and boost converters were selected to work in sequence to generate the 12 V rail.

The LM5122 wide input synchronous boost controller was selected as the first stage of the power tree after the input. The device was configured to boost to 14 V to cover the battery voltage range and was also selected to get the highest efficiency as a synchronous controller offers the opportunity to select both switching MOSFETs. Additionally, this device has the unique feature of an external charge-pump that can drive the high-side MOSFET when the input voltage goes higher than the set output voltage. This mode is called pass-through and allows power to be efficiently delivered through the high-side MOSFET without changing the input voltage. It is also useful to note that the device operates in peak current-mode control for fast transient response. The LMR33630 is a 3 A synchronous buck converter that was selected due to its small size and high efficiency. The device has been configured to step down to 12 V from the possible input range of 14-28 V, covering the rest of the input voltage range. Placement was optimized in the design for these two devices to showcase their individual solution sizes.

2.2.3.1 Input protection - overvoltage and reverse voltage

This system input voltage range is 6-28 V. A general rule-of-thumb for selecting a transient-voltage-suppression (TVS) device is by selecting the standoff voltage rating 25% above the maximum input voltage (i.e. 35 V). This will allow some margin for device process and temperature variations to minimize unnecessary TVS activation during normal operation. In this design, TVS3301 was selected to provide the input overvoltage protection (OVP). The device has a standoff rating of 33 V and IEC 61000-4-5 clamp rating of 40 V.

The target reverse voltage protection (RVP) should include the maximum input voltage 28 V plus at least a 25% margin to account for transient behaviors and device tolerances (i.e. 35 V). For this design, a 60 V reverse voltage protection target was chosen.

The RVP circuit included an ideal diode controller (LM74700) and an NMOS (CSD18532Q5B). The MOSFET selection for the reverse voltage protection circuit is guided by the typical application conduction current and the VDS voltage rating. There is a tradeoff between reverse voltage detection and conduction loss. As recommended by the LM74700 data sheet, the $R_{DS(ON)}$ should be (20 mV / $I_{Load(Nominal)}$) ≤ $R_{DS(ON)}$ ≤ (50 mV / $I_{Load(Nominal)}$). This guideline balances reverse current detection sensitivity and conduction loss. In this design, $I_{Load(Nominal)}$ is 5 A. Thus, 4 mΩ ≤ $R_{DS(ON)}$ ≤ 10 mΩ.

CSD18532Q5B was selected to provide a -60V RVP and it is rated at:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 3.3-mΩ typical and 4.3-mΩ maximum rated at 4.5-V V_{GS}
- MOSFET V_{th}: 2.2-V maximum

表 2-3. Input protection design summary

PARAMETER	SPECIFICATION	COMMENTS
Clamping voltage	40 V at 27-A (IEC 61000-4-5)	Limited by TVS3301
Maximum reverse voltage	-60 V	Limited by CSD18532Q5B
Reverse block time	<0.75 µs	Limited by LM74700

Input Inrush Protection

Although not implemented in this design, it is recommended to add inrush current protection (for example, soft-start) to the design. Due to the inherent path from input to output, a large inrush current can flow when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising should be controlled by a hot-swap controller or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side N-channel MOSFET switch. An alternative low-cost option is to use a NTC or PTC thermistor for soft-start.

2.2.3.2 LM5122 Boost Design Calculations

Based on the key system specification, the maximum solenoid load is 1.7 A. The boost-buck DC-DC power stage, consisting of LM5122 and LMR33630, is designed to support 2 A of continuous load. Note, WEBENCH® Power Designer was used to help design the power stage. The key design calculations for the LM5122 Boost Stage are shown below. For more details on design considerations, please refer to the device data sheet.

表 2-4. Boost Stage Summary

PARAMETER	SPECIFICATION	COMMENTS
Input Voltage	6-28 V	From input supply
Input Power	31.1 W	Max, η = 90%
UVLO	5.5 V & 5 V	Start and Shutdown
F_{sw}	250 kHz	Switching frequency
Output Voltage	14-28 V	If Vin >14 V, Vin passes through
Output Power	28 W	Max
Max Load Current	2 A	Vout = 14 V (28 W)

Timing Resistor RT (R53)

The boost switching frequency of 250 kHz was selected as a good compromised between size and efficiency. The RT resistor is calculated as follows:

$$RT = \frac{9 \times 10^9}{f_{sw}} = \frac{9 \times 10^9}{250\ kHz} = 36\ k\Omega \tag{40}$$

A standard value of 36.5 kΩ was selected for RT.

UVLO Divider RUV2 (R43), RUV1 (R47)

The desired startup voltage and the hysteresis are set by the voltage divider RUV2, RUV1. The UVLO shutdown voltage should be high enough to enhance the low-side N-channel MOSFET switch fully. For this design, the startup voltage was set to 5.5 V, which is 0.5 V below the minimum input voltage. VHYS was set to 0.5 V. This resulted in an input-voltage shutdown threshold of 5 V. The values of RUV2, RUV1 are calculated as follows:

$$RUV2 = \frac{VHYS}{IHYS} = \frac{0.5\ V}{10\ \mu A} = 50\ k\Omega \tag{41}$$

$$RUV1 = \frac{1.2\ V \times RUV2}{V_{in\_startup} - 1.2\ V} = \frac{1.2\ V \times 50\ k\Omega}{5.5\ V - 1.2\ V} = 14\ k\Omega \tag{42}$$

49.9 kΩ and 14 kΩ were selected for RUV2 and RUV1, respectively.

Input Inductor LIN (L2)

The first step is to calculate the maximum duty cycle and maximum input current. Assuming an efficiency of 0.9:

$$D_{max} = \left(1 - \frac{V_{in}}{V_{out}}\right) = \left(1 - \frac{6\ V}{14\ V}\right) = 0.57 \tag{43}$$

$$I_{in} = \frac{I_{out} \times V_{out}}{V_{in} \times \eta} = \frac{I_{out}}{(1 - D_{max}) \times \eta} = \frac{2\ A}{(1 - 0.57) \times 0.9} = 5.2\ A \tag{44}$$

The inductor ripple current is typically set between 20% and 40% of the full load current, known as a good compromise between core loss and copper loss of the inductor. Higher ripple current allows for a smaller inductor size, but places more of a burden on the output capacitor to smooth the ripple voltage on the output. In addition, a higher ripple may require a higher inductor saturation rating. For this example, a high ripple ratio (RR)

of 0.6, 60% of the input current was chosen to minimize inductor size. Knowing the switching frequency and the typical input voltage, the inductor value can be calculated as follows:

$$L_{in} = \frac{V_{in}}{I_{in} \times RR} \times \frac{1}{f_{sw}} \times D_{max} = \frac{6\ V}{5.2\ A \times 0.6} \times \frac{1}{250\ kHz} \times 0.57 = 4.4\ \mu H \quad (45)$$

The closest standard value of 4.7 µH (XAL6060-472ME) was chosen for L_{in} (i.e. L2) for this design. Alternatively, if a ripple ratio of 0.3 is desired, a 10 µF (XAL6060-103ME) could be chosen.

The saturation current rating of inductor should be greater than the peak inductor current, which is calculated at the minimum input voltage and full load:

$$\Delta I_L = \frac{V_{in}}{L_{in} \times f_{sw}} \times D_{max} = \frac{6\ V}{4.7\ \mu H \times 250\ kHz} \times 0.57 = 2.9\ A \quad (46)$$

$$I_{peak} = I_{in} + 0.5 \times \Delta I_L = 5.2\ A + 0.5 \times 2.9\ A = 6.7\ A \quad (47)$$

To account for tolerances (i.e. inductor, frequency, voltage) a 25% margin is added to the result. The Ipeak = 6.7A × 1.25 = 8.4 A (worst-case). The chosen inductor (XAL6060-472ME) saturation current rating is 10.5 A.

Note, I_{RMS} is approximately I_{IN} given a small RR value:

$$I_{RMS} = \frac{I_{out}}{1 - D}\sqrt{1 + \frac{RR^2}{12}} = I_{in}\sqrt{1 + \frac{RR^2}{12}} \quad (48)$$

Inductor wire loss is calculated as follows:

$$P_{IND\_DC} = {I_{RMS}}^2 \times R \cong {I_{in}}^2 \times R = 5.2A^2 \times 14.4\ m\Omega = 0.39\ W \quad (49)$$

Note: for higher power applications (i.e. higher flux density), inductor core losses may be significant.

Current Sense Resistor RS (R40)

The maximum peak input current capability should be 20% to 50% higher than the required peak current at low input voltage and full load, accounting for tolerances (that is, $V_{CS\text{-}TH1}$, peak current). For this design, a 40% margin was selected.

$$Rs = \frac{V_{CS-TH1}}{I_{peak}} = \frac{75\ mV}{6.7A \times 1.4} = 8\ m\Omega \quad (50)$$

8 mΩ was selected for Rs. The maximum power loss of Rs is calculated as follows:

$$P_{loss\_rs} = I^2 \times R = (6.7\ A \times 1.4)^2 \times 8\ m\Omega = 0.7\ W \quad (51)$$

To account for the sense resistor temperature derating and tolerance, a minimum power rating of 1 W is required. For this design, the chosen Rs (PMR100HZPFU8L00) is rated for 2 W.

Current Sense Filter RCSFP (R45), RCSFN (R46), CCS (C58)

The current sense filter is optional. Based on the data sheet recommendations, 100 pF for CCS and 100 Ω for RCSFP, RCSFN were chosen.

Slope Compensation Resistor RSLOPE

For duty cycles greater than 50%, peak current mode regulators are subject to sub-harmonic oscillation. In this design the maximum duty cycle is about 57% when V_{in} is 6 V. Subharmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles. This subharmonic oscillation can be eliminated by a technique, which adds an artificial ramp, known as slope compensation, to the sensed inductor current.

The K value was selected to be 0.6 at the minimum input voltage. R_{slope} should be carefully selected so that the sum of sensed inductor current and slope compensation is less than COMP output high voltage. In any case, K should be greater than at least 0.5. At higher switching frequency over 500 kHz, K factor is recommended to be greater than or equal to 1 because the minimum on-time affects the amount of slope compensation due to internal delays.

$$R_{slope} > \frac{8 \times 10\text{^}9}{f_{sw}} = \frac{8 \times 10\text{^}9}{250\ \text{kHz}} = 32\ \text{k}\Omega \tag{52}$$

$$R_{slope} = \frac{L_{in} \times 6 \times 10\text{^}9}{\left[K \times V_{out} - V_{in(min)}\right] \times Rs \times 10} = \frac{4.7\ \mu\text{H} \times 6 \times 10\text{^}9}{(0.6 \times 14\text{V} - 6\text{V}) \times 8\text{m}\Omega \times 10} = 146.9\ \text{k}\Omega \tag{53}$$

For this design, 140 kΩ was selected for R_{slope}.

Output Capacitor COUT

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors. In this design, one 180-µF bulk aluminum capacitor (EEE-FK1H181SP) and three 10-µF ceramic capacitors (UMK316BBJ106KL-T) were used to share the output ripple current and source the required charge. Assuming an effective 50 mΩ ESR for the hybrid output capacitor network, the output voltage peak-peak ripple at the minimum input voltage is calculated as follows:

$$V_{ripple\_max(C_{out})} = \frac{I_{out}}{V_{in(min)}/V_{out}} \times \left(R_{ESR} + \frac{1}{4 \times C_{out} \times f_{sw}}\right) = I_{in} \times \left(R_{ESR} + \frac{1}{4 \times C_{out} \times f_{sw}}\right)$$

$$V_{ripple\_max(C_{out})} = 5.2\ \text{A} \times \left(50\ \text{m}\Omega + \frac{1}{4\ \times\ 210\ \mu\text{F}\ \times 250\ \text{kHz}}\right) = 285\ \text{mV} \tag{54}$$

The calculated output ripple voltage is 2% of the output voltage, which is dominated by the effective output ESR. Adding a 25% margin to account for tolerances, the worst-case output voltage ripple is 2.5%.

The output cap RMS current is:

$$I_{RMS\_Cout} = I_{out}\sqrt{\frac{D + \frac{RR^2}{12}}{1 - D}}$$

$$I_{RMS\_Cout} = 2\ \text{A} \times \sqrt{\frac{0.57 + \frac{0.6^2}{12}}{1 - 0.57}} = 2.4\ \text{A} \tag{55}$$

Input Capacitor CIN

The input capacitors smooth the input voltage ripple. In this design, two 330 µF bulk aluminum capacitors (EMVA500ATR331MKE0S), five 10-µF ceramic capacitors (CL31B106KBHNNNE), and one 1-µF ceramic capacitor (UMK107AB7105KA-T) were used. The maximum input voltage peak-peak ripple which happens when the input voltage is half of the output voltage can be calculated as follows:

$$V_{ripple\_max(C_{in})} = \frac{V_{out}}{32 \times L_{in} \times C_{in} \times {f_{sw}}^2} = \frac{14\text{V}}{32 \times 4.7\ \mu\text{H} \times 711\ \mu\text{F} \times 250\ \text{kHz}^2} = 2\ \text{mV} \tag{56}$$

The input cap RMS current is:

$$I_{RMS\_Cin} = \frac{I_{out}}{1-D} \times \frac{RR}{\sqrt{12}}$$
$$I_{RMS\_Cin} = \frac{2A}{1-0.57} \times \frac{0.6}{\sqrt{12}} = 0.8\ A \quad (57)$$

Bootstrap Capacitor CBST (C64) and Boost Diode DBST (D3)

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side N-channel MOSFET device gate during each cycle's turn-on and also supplies recovery charge for the bootstrap diode. These current peaks can be several amperes. C_{BST} must be a good-quality, low-ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. The minimum value for the bootstrap capacitor is calculated as follows:

$$C_{BST\_min} = \frac{Q_g}{\Delta V_{BST}} \quad (58)$$

where

- Q_g is the high-side N-channel MOSFET gate charge
- ΔV_{BST} is the tolerable voltage droop on CBST, which is typically less than 5% of VCC or 0.15 V, conservatively

The chosen CSD18543Q3A MOSFET has 10 nC at 10 V, which means the C_{BST_min} is only 66.7 nF:

$$C_{BST\_min} = \frac{10\ nF}{0.15\ V} = 66.7\ nF \quad (59)$$

In this design, a 0.1-µF ceramic capacitor (C1005X5R1H104K050BB) was used based on the data sheet recommended value.

The voltage rating of DBST must be greater than the peak SW node voltage plus 16 V. The maximum switch node voltage is approximately the output voltage plus some ringing. Thus a minimum diode voltage rating including the 16 V margin is 30 V. A low leakage diode is mandatory for the bypass operation. The leakage current of DBST must be low enough for the BST charge pump to maintain a sufficient high-side driver supply voltage at high temperature. For this design, a 100-V, 1-A Schottky diode (MBR1H100SFT3G) was chosen.

VCC Capacitor CVCC

The primary purpose of the VCC capacitor is to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. These peak currents can be several amperes. The value of CVCC must be at least 10 times greater than the value of CBST (i.e. 1 µF) and should be a good-quality, low-ESR, ceramic capacitor. Also, to account for voltage derating, the voltage rating should be at least 2 times the VCC voltage. In this design, a 10-µF, 16-V ceramic capacitor (EMK107BBJ106MA-T) was used.

Output Voltage Divider RFB1 (R44), RFB2 (R48)

RFB1 and RFB2 set the output voltage level. The ratio of these resistors is calculated as follows:

$$\frac{RFB2}{RFB1} = \frac{V_{out}}{1.2\ V} - 1 \quad (60)$$

The ratio between R_{COMP} and RFB2 determines the mid-band gain, AFB_MID. A larger value for RFB2 may require a corresponding larger value for R_{COMP}. RFB2 should be large enough to keep the total divider power dissipation small. In this design, 39.9 kΩ and 3.65 kΩ were chosen for RFB2 and RFB1, respectively (i.e. Vout = 14.3 V).

Soft-Start Capacitor CSS (C65)

The soft-start time (t_{SS}) is the time for the output voltage to reach the target voltage from the input voltage. The soft-start time is not only proportional with the soft-start capacitor, but also depends on the input voltage. With 0.1 µF of CSS, the soft-start time is calculated as follows:

$$t_{ss\,(max)} = \frac{C_{ss} \times 1.2\ V}{I_{ss}} \times D_{max} = \frac{0.1\ \mu F \times 1.2\ V}{10\ \mu A} \times 0.57 = 6.8\ ms \quad (61)$$

Restart Capacitor CRES (C66)

The restart capacitor determines restart delay time t_{RD} and hiccup mode off time t_{RES}. t_{RD} must be greater than $t_{SS(MAX)}$. The minimum required value of C_{RES} can be calculated at the low input voltage as follows:

$$C_{RES\,(min)} = \frac{I_{RES} \times t_{ss\,(max)}}{V_{RES}} = \frac{30\ \mu A \times 6.8\ ms}{1.2\ V} = 0.17 \mu F \quad (62)$$

A standard value of 0.33 µF was selected for C_{RES} (i.e. t_{RD} = 13.2 ms).

Low-Side Power Switch Q

Selection of the power N-channel MOSFET devices by breaking down the losses is one way to compare the relative efficiencies of different devices. Losses in the low-side N-channel MOSFET device can be separated into conduction loss, switching loss, and gate charge loss. Low-side conduction loss of CSD18543Q3A is approximately calculated as follows:

$$P_{COND\,(LS)} = {I_{RMS}}^2 \times R_{DS\_ON\,(LS)} \times 1.5 = D_{max} \times {I_{in}}^2 \times R_{DS\_ON\,(LS)} \times 1.5$$
$$P_{COND\,(LS)} = 0.57 \times 5.2\ A^2 \times 12\ m\Omega \times 1.5 = 278\ mW \quad (63)$$

Where, D is the duty cycle and the factor of 1.5 accounts for the increase in the N-channel MOSFET device on-resistance due to heating. The $R_{DS(ON)}$ used here is based on a conservative estimate (V_{gs} = 4.5 V) since the actual V_{gs} drive is about 6 V.

Switching loss occurs during the brief transition period as the low-side N-channel MOSFET device turns on and off. During the transition period both current and voltage are present in the channel of the N-channel MOSFET device. The low-side switching loss is approximately calculated as follows:

$$P_{SW\,(LS)} = 0.5 \times V_{out} \times I_{in} \times (t_R + t_F) \times f_{sw}$$
$$P_{SW\,(LS)} = 0.5 \times 14\ V \times 5.2\ A \times (3.5\ ns + 1.6\ ns) \times 250\ kHz = 46\ mW \quad (64)$$

t_R and t_F are the switching times (including the rise and fall times) corresponding to the rise and fall transitions. During these times switching loss occurs for the low-side N-channel MOSFET device. They are calculated as follows:

$$t_R = \frac{Q_{gs\,(afterVth\ )} + Q_{gd}}{I_{source}} = \frac{Q_{gs} - Q_{g,Vth} + Q_{gd}}{I_{source}} = \frac{3.1\ nC - 2\ nC + 1.7\ nC}{0.8\ A} = 3.5\ ns$$
$$t_F = \frac{Q_{gs\,(afterVth\ )} + Q_{gd}}{I_{sink}} = \frac{Q_{gs} - Q_{g,Vth} + Q_{gd}}{I_{sink}} = \frac{3.1\ nC - 2\ nC + 1.7\ nC}{1.8A} = 1.6\ \ ns \quad (65)$$

MOSFET gate losses are caused by the energy required to charge the MOSFET gate. That is, the total Q_g at the gate voltage of the circuit. These are both turn-on and turn-off gate losses. The power dissipation is approximately split between the gate driver and the MOSFET:

$$P_{G(LS)} = Q_{G(LS)} \times V_{GS\,(LS)} \times f_{sw} = C_{G(LS)} \times {V_{GS\,(LS)}}^2 \times f_{sw}$$
$$P_{G(LS)} = Q_{G(LS)} \times V_{GS\,(LS)} \times f_{sw} = 7\ nC \times 6\ V \times 250\ kHz = \ 10.5\ mW \quad (66)$$

Note, the temperature factor assumption can be verified afterwards by determining the junction temperature from the total power dissipation calculations. The $R_{DS(ON)}$ of the MOSFET versus temperature is shown in the data sheet:

$$T_J = T_{ambient} + R_{\theta JA} \times P_d = 40\ C + \frac{45\ C}{W} \times (278 + 46 + 10.5)\ mW = 55\ C \quad (67)$$

From the data sheet, the normalized on-state resistance for CSD18543Q3A (V_{gs} = 4.5 V) is well under 1.2 at this junction temperature so our initial assumption of 1.5 is still valid. Note, the case temperature is very close to the junction temperature since $R_{\theta JC}$ = 1.9 ºC/W.

An alternative design approach is to start with the target FET junction temperature, working back to the maximum $R_{DS(ON)}$, and then cross check with the data sheet $R_{DS(ON)}$ at that temperature.

High-Side Power Switch QH and Additional Parallel Schottky Diode

Losses in the high-side N-channel MOSFET device can be separated into conduction loss, dead-time loss, reverse recovery loss, and gate charge loss. Switching loss is calculated for the low-side N-channel MOSFET device only. Switching loss in the high-side N-channel MOSFET device is negligible because the body diode of the high-side N-channel MOSFET device turns on before and after the high-side N-channel MOSFET device switches (i.e. zero voltage switching).

High-side conduction loss is approximately calculated as follows:

$$P_{COND\,(HS)} = {I_{RMS}}^2 \times R_{DS\_ON\,(LS)} \times 1.5 = (1 - D) \times {I_{in}}^2 \times R_{DS_{ON\,(HS)}} \times 1.5$$
$$P_{COND\,(HS)} = (1 - 0.57) \times 5.2\ A^2 \times 12\ m\Omega \times 1.5 = 209\ mW \quad (68)$$

Dead-time loss is approximately calculated as follows:

$$P_{DT\,(HS)} = V_D \times I_{in} \times (t_{DLH} + t_{DHL}) \times f_{sw}$$
$$P_{DT\,(HS)} = 0.8\ V \times 5.2\ A \times (80\ ns + 80\ ns) \times 250\ kHz = 166\ mW \quad (69)$$

where

- V_D is the forward voltage drop of the high-side NMOS body diode.
- t_{DLH} and t_{DHL} are the low to high and high to low dead time delays, respectively.

Reverse recovery characteristics of the high-side N-channel MOSFET switch strongly affect efficiency, especially when the output voltage is high. Small reverse recovery charge helps to increase the efficiency while also minimizes switching noise. Reverse recovery loss is calculated as follows:

$$P_{RR\,(HS)} = V_{out} \times Q_{RR} \times f_{sw} = 14\ V \times 37\ nC \times 250\ kHz = 130\ mW \quad (70)$$

Gate charge loss is calculated as follows:

$$P_{G\,(HS)} = Q_{G\,(HS)} \times V_{GS\,(HS)} \times f_{sw} = 7\ nC \times 6\ V \times 250\ kHz = 10.5\ mW \quad (71)$$

Note, an additional Schottky diode can be placed in parallel with the high-side switch to improve efficiency. Usually, the power rating of this parallel Schottky diode can be less than the high-side switch's because the diode conducts only during dead-times. The power rating of the parallel diode should be equivalent or higher than high-side switch's if bypass operation is required, hiccup mode operation is required or any load exists before switching.

Bias Losses

An additional source of power loss includes bias losses. The total bias current budget is about 10 mA. With a 6 V input, the loss is 60 mW from biasing.

Snubber Components

A resistor-capacitor snubber network across the high-side N-channel MOSFET device reduces ringing and spikes at the switching node. Selecting the values for the snubber is best accomplished through empirical methods. A 470-pF capacitor and 8.2-Ω resistor were chosen as placeholders in this design.

Loop Compensation Components CCOMP, RCOMP, CHF

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the following four steps:

1. Select:

Select the cross over frequency (f_{cross}) at one fourth of the RHP zero or one tenth of the switching frequency, whichever is lower. RHP zero at minimum input voltage should be considered if the input voltage range is wide.

$$f_{Z\_RHP} = \frac{R_{load} \times (1-D)^2}{2\pi \times L} = 44\ kHZ \tag{72}$$

$$f_{cross} \leq \frac{f_{sw}}{10} \text{ or } \frac{f_{Z\_RHP}}{4} \tag{73}$$

$$\frac{f_{sw}}{10} = 25\ kHz \tag{74}$$

$$\frac{f_{Z\_RHP}}{4} = \frac{R_{load} \times (1-D)^2}{4 \times 2\pi \times L} = \frac{\frac{V_{out}}{I_{out}} \times (1-D)^2}{4 \times 2\pi \times L} = \frac{\frac{14\ V}{2\ A} \times (1-0.57)^2}{4 \times 2\pi \times 4.7\ \mu H} = 11\ kHZ \tag{75}$$

In this design, a 5 kHz crossover frequency was used instead of 11 kHz for added margin.

Note, the size of the output capacitor plays a significant role in how wide the loop bandwidth is (Reference SLVA452). Once the minimum capacitance is met, meeting the output ripple specification, the following equation is used to estimate the output capacitance needed to meet the application's load transient requirement for the maximum voltage dip (V_{TRAN}) after a given load step (ΔI_{TRAN}). V_{TRAN} is 2.5% of output voltage and ΔI_{TRAN} is 2 A:

$$C_{out\_min} = \frac{\Delta I_{TRAN}}{2\pi \times f_{cross} \times V_{TRAN}} = \frac{2\ A}{2\pi \times 5\ kHZ \times 0.35\ V} = 182\ \mu F \tag{76}$$

2. Determine required R_{COMP} to set crossover.

Knowing f_{cross}, R_{COMP} is calculated as follows:

$$R_{COMP} = f_{cross} \times \pi \times Rs \times RFB2 \times 10 \times C_{out} \times \frac{V_{out}}{V_{in}}$$
$$R_{COMP} = 5\ kHz \times \pi \times 8\ m\Omega \times 39\ k\Omega \times 10 \times 210\ \mu F \times \frac{14\ V}{6\ V} = 24\ k\Omega \tag{77}$$

In this design, 23.2 kΩ was selected for R_{COMP}.

3. Determine C_{COMP} to cancel load pole.

Place error amplifier zero at the twice of load pole frequency. For boost converters with ceramic capacitor(s) in parallel with a much larger, high-ESR capacitor, use the total capacitance in parallel for C_{out} for this step (Reference SLVA452). Knowing R_{COMP}, C_{COMP} is calculated as follows:

$$\omega_{P\_LF} = \frac{2}{R_{load} \times C_{out}} = \frac{2}{7\ \Omega \times 210\ \mu F} = 1361 \frac{rad}{s} (i.e.\ f_{P_{LF}} = 217\ Hz) \tag{78}$$

$$C_{COMP} = \frac{R_{load} \times C_{out}}{4 \times R_{COMP}} = \frac{\frac{14\ V}{2\ A} \times 210\ \mu F}{4 \times 23.2\ k\Omega} = 15.8\ nF \quad (79)$$

A standard value of 15 nF is recommended.

4. Determine C_{HF} to cancel ESR zero.

$$f_{Z\_EA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} = \frac{1}{2\pi \times 23.2\ k\Omega \times 15\ nF} = 457\ Hz \quad (80)$$

For boost converters with ceramic capacitor(s) in parallel with a much larger, high-ESR capacitor, only use the high-ESR capacitor's capacitance and ESR for this step (Reference SLVA452). Knowing R_{COMP}, RESR and C_{COMP}, C_{HF} is calculated as follows:

$$C_{HF} = \frac{R_{ESR} \times C_{out} \times C_{COMP}}{R_{COMP} \times C_{COMP} - R_{ESR} \times C_{out}} = \frac{340\ m\Omega \times 180\ \mu F \times 33\ nF}{23.2\ k\Omega \times 33\ nF - 340\ m\Omega \times 180\ \mu F} = 2.87\ nF \quad (81)$$

A standard value of 2.7 nF is recommended.

$$f_{Z\_ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{out}} = \frac{1}{2\pi \times 340\ m\Omega \times 180\ \mu F} = 2.6\ kHz \quad (82)$$

$$f_{P\_EA} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} = \frac{1}{2\pi \times 23.2\ k\Omega \times 2.7\ nF} = 2.54\ kHz \quad (83)$$

Alternatively, if a lower ESR bulk capacitor were used the f_{Z_ESR} can be moved beyond the f_{cross}.

Bypass Operation (VOUT = VIN)

MODE pin is tied to 3.3 V to enable Forced-PWM (FPWM). Forced-PWM mode is the recommended PWM configuration when bypass operation is required.

2.2.3.3 LMR33630 Buck Design Calculations

Based on the key system specification, the maximum solenoid load is 1.7 A. The boost-buck DC-DC power stage, consisting of LM5211 and LMR33630, is designed to support 2 A of continuous load. Note, WEBENCH® Power Designer was used to help design the power stage. The key design calculations for the LMR3360 Buck Stage are shown below. For more details on design considerations, please refer to the device data sheet.

表 2-5. Buck stage summary

PARAMETER	SPECIFICATION	COMMENTS
Input Voltage	14-28 V	From boost stage
Input Power	26.7 W	Max, η = 90%
Output Voltage	12 V	For solenoid drive
Output Power	24 W	Max
Max Load Current	2 A	Vout = 12 V (24 W)

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. For this design, 400 kHz was chosen (i.e. LMR33630A variant) as a compromise between efficiency and overall solution size.

Setting the Output Voltage

The output voltage of the LMR33630 is externally adjustable using a resistor divider network. The target output is 12 V. Start with the recommended 100 kΩ value. The R_{FBB} is:

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{out}}{V_{ref}} - 1}$$
$$R_{FBB} = \frac{100\ k\Omega}{\frac{12V}{1V} - 1} = 9.1\ k\Omega \quad (84)$$

9.1 kΩ was selected.

Inductor Selection

The first step to calculate the peak inductor/switch current is to determine the duty cycle, D, for the maximum input voltage. The maximum input voltage is used because this leads to the maximum switch current:

$$D_{min} = \frac{V_{out}}{V_{in}} = \frac{12\ V}{28\ V} = 0.43 \quad (85)$$

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20-40 % of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load (2 A) than the maximum available from the device (3 A), the maximum device current should be used.

$$L = \frac{V_{out}}{I_{out} \times RR \times f_{sw}} \times (1 - D) \quad (86)$$

The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions:

$$L_{max} = \frac{12\ V}{3\ A \times 0.1 \times 400\ kHz} \times (1 - 0.43) = 57\ \mu H \quad (87)$$

From the data sheet, the minimum inductance is given by:

$$L_{min} = 0.28 \times \frac{V_{out}}{f_{sw}}$$
$$L_{min} = 0.28 \times \frac{12\ V}{400\ kHz} = 8.4\ \mu H \quad (88)$$

RR of 0.3 was selected for the following inductance calculation:

$$L = \frac{12\ V}{3A \times 0.3 \times 400\ kHz} \times (1 - 0.43) = 19\ \mu H \quad (89)$$

For this design 33 µH was selected. This value is inside the recommended inductance range. Alternatively, a smaller inductance 22 µH (SPM7054VT-220M-D) could be used since the saturation current rating would be higher.

The actual worst-case ripple current is:

$$\Delta I_L = \frac{V_{out}}{f_{sw} \times L} \times (1 - D)$$
$$\Delta I_L = \frac{12V}{400kHz \times 33\ \mu H} \times (1 - 0.43) = 0.52\ A \quad (90)$$

The actual ripple ratio is:

$$RR = \frac{\Delta I_L}{I_{out}} = \frac{0.52\ A}{3\ A} = 0.17 \tag{91}$$

The peak inductor/switch/diode current and the minimum saturation current rating of the inductor plus a 25% margin are calculated as follows:

$$I_{peak} = I_{out} \times \left(1 + \frac{RR}{2}\right)$$
$$I_{peak} = 3\ A \times \left(1 + \frac{0.17}{2}\right) \times 1.25 = 4.1\ A \tag{92}$$

However, the LM33630 has specific inductor saturation requirement for its normal operation due to internal current limits. Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, ISC. The ISC is 4.5 A typical and 5 A max.

In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT}. The I_{LIMIT} is 3.5 A typical and 4.1 A max.

In this design, the selected inductor (SPM7054VT-330M-D) has saturation ratings of 3.6 A (ΔL=-20%) and 4.9 A ΔL=-30%). Based on the data sheet, this inductor RMS rating is well suited to handle 3.4 A with a 40 ºC rise.

For the RMS current calculations, the 2 A max application current is used instead of the device maximum:

$$I_{RMS} = I_{out}\sqrt{1 + \frac{RR^2}{12}}$$
$$I_{RMS} = 2\ A\sqrt{1 + \frac{0.17^2}{12}} = 2.01\ A \tag{93}$$

Note, I_{RMS} is approximately I_{out} given a small RR value.

Inductor wire loss is calculated as follows:

$$P_{IND\_DC} = {I_{RMS}}^2 \times R \cong {I_{out}}^2 \times R = 2\ A^2 \times 97.7\ m\Omega = 0.39\ W \tag{94}$$

Output Capacitor Selection

The value of the output capacitor and the ESR of the capacitor determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. The following equations can be used to estimate a lower bound on the total output capacitance and an upper bound on the ESR, which is required to meet a specified load transient. Assume a 2 A transient step with 5% voltage drop (600 mV), using the worst-case input:

$$C_{out} \geq \frac{\Delta I_{out}}{f_{sw} \times \Delta V_{out} \times RR} \times \left[(1 - D) \times (1 + RR) + \frac{RR^2}{12} \times (2 - D)\right]$$
$$C_{out} \geq \frac{2A}{400\ kHz \times 600\ mV \times 0.3} \times \left[(1 - .43) \times (1 + 0.3) + \frac{0.3^2}{12} \times (2 - 0.43)\right] = 21\ \mu F \tag{95}$$

$$ESR \leq \frac{(2 + RR) \times \Delta V_{out}}{2 \times \Delta I_{out}\left[1 + RR + \frac{RR^2}{12} \times \left(1 + \frac{1}{1 - D}\right)\right]}$$
$$ESR \leq \frac{(2 + 0.3) \times 600\ mV}{2 \times 2\ A\left[1 + 0.3 + \frac{0.3^2}{12} \times \left(1 + \frac{1}{1 - .43}\right)\right]} = 261\ m\Omega \tag{96}$$

In this design, three 22-µF and one 1-µF were used, which accounts for tolerance and voltage derating. These ceramic caps are rated for 25 V, so the de-rated output capacitance is 32 µF. Ceramic capacitors can easily meet the minimum ESR requirements. Assume an effective ESR of 50 mΩ for the ripple voltage calculations.

The peak-to-peak output voltage ripple is:

$$Vr_{p-p} \cong \Delta I_L \sqrt{ESR^2 + \frac{1}{(8 \times f_{sw} \times C_{out})^2}}$$

$$Vr_{p-p} \cong 0.52\ A \sqrt{50\ m\Omega^2 + \frac{1}{(8 \times 400\ kHz \times 32\ \mu F)^2}} = 26\ mV \quad (97)$$

The output cap RMS current is:

$$I_{RMS\_Cout} = I_{out} \times \frac{RR}{\sqrt{12}}$$

$$I_{RMS\_Cout} = 2\ A \times \frac{0.3}{\sqrt{12}} = 0.173\ A \quad (98)$$

Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10 µF of ceramic capacitance is required on the input of the LMR33630. This must be rated for at least the maximum input voltage (28 V). For this design, 10-µF and 220-nF ceramic caps were selected. Both capacitors are rated at 50 V, which accounts for voltage-derating.

The input cap RMS current is:

$$I_{RMS\_Cin} = I_{out} \times \sqrt{D \times \left[1 - D + \frac{RR^2}{12}\right]} \cong \frac{I_{out}}{2}$$

$$I_{RMS\_Cin} \cong \frac{2\ A}{2} = 1\ A \quad (99)$$

CBOOT

The LMR33630 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. For this design, a 100-nF, 50-V ceramic cap was selected based on the data sheet guidelines.

VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation.

CFF Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin:

$$CFF < \frac{V_{out} \times C_{out}}{120 \times R_{FBT} \sqrt{\frac{V_{ref}}{V_{out}}}} \quad (100)$$

$$CFF < \frac{12\ V \times 32\ \mu F}{120 \times 100\ k\Omega \sqrt{\frac{1\ V}{12\ V}}} = 111\ pF \quad (101)$$

In this design, the CFF is DNP (Do Not Populate).

UVLO

This is not applicable for this stage of the power tree since it was implemented in the boost stage. If specific UVLO is required, refer to the LMR33630 data sheet for more information.

Maximum Ambient Temperature

The power dissipation is approximated with:

$$P_d = P_{out} \frac{1 - \eta}{\eta} \quad (102)$$

Assume a 90% efficiency (V_{in} = 28 V) at max load:

$$P_d = (12\ V \times 2\ A) \times \frac{1 - 0.9}{0.9} = 1.26\ W \quad (103)$$

Assume a $R_{\theta JA}$ of 40 ºC/W:

$$T_J = T_{ambient} + R_{\theta JA} \times P_d$$
$$T_J = 40\ C + \frac{40\ C}{W} \times 1.26\ W = 90\ C \quad (104)$$

2.2.3.4 Secondary Power Stage – TPS62840 3.3V Buck

表 2-6. Buck Stage Summary

PARAMETER	SPECIFICATION	COMMENTS
Input Voltage	4 V	From DRV8323RS
Input Power	0.78 W	Max, η = 85%
Output Voltage	3.3 V	System digital supply
Output Power	0.66 W	Max
Max Load Current	200 mA	Vout = 3.3V

This is the system digital power supply. Although this application requires only 200 mA or less, the passive components selected for the design are based on the data sheet recommendations, which can support up to 750 mA load. For more details on the design considerations, please refer to the device data sheet.

2.2.3.5 Secondary Power Stage – TPS7A02 3.3V LDO

The purpose of the LDO is to provide a low noise power rail (130 µVrms, BW = 10 Hz to 100 kHz) for the TMP1075 temperature sensors. Although the LDO is capable of sourcing up to 200 mA, the expected load is much less (<5 mA) since the temperature sensors are very low power devices.

The maximum TPS7A02 dropout for a 3.3 V output is 310 mV. The input voltage is 4 V from the DRV8323RS's integrated buck, which allows for up to 0.7 V of dropout.

A minimum output capacitance of 1 µF is required for stability. For this design, 1-µF, 10-V ceramic capacitors were selected for the input and output.

2.2.3.6 Power Tree Circuit

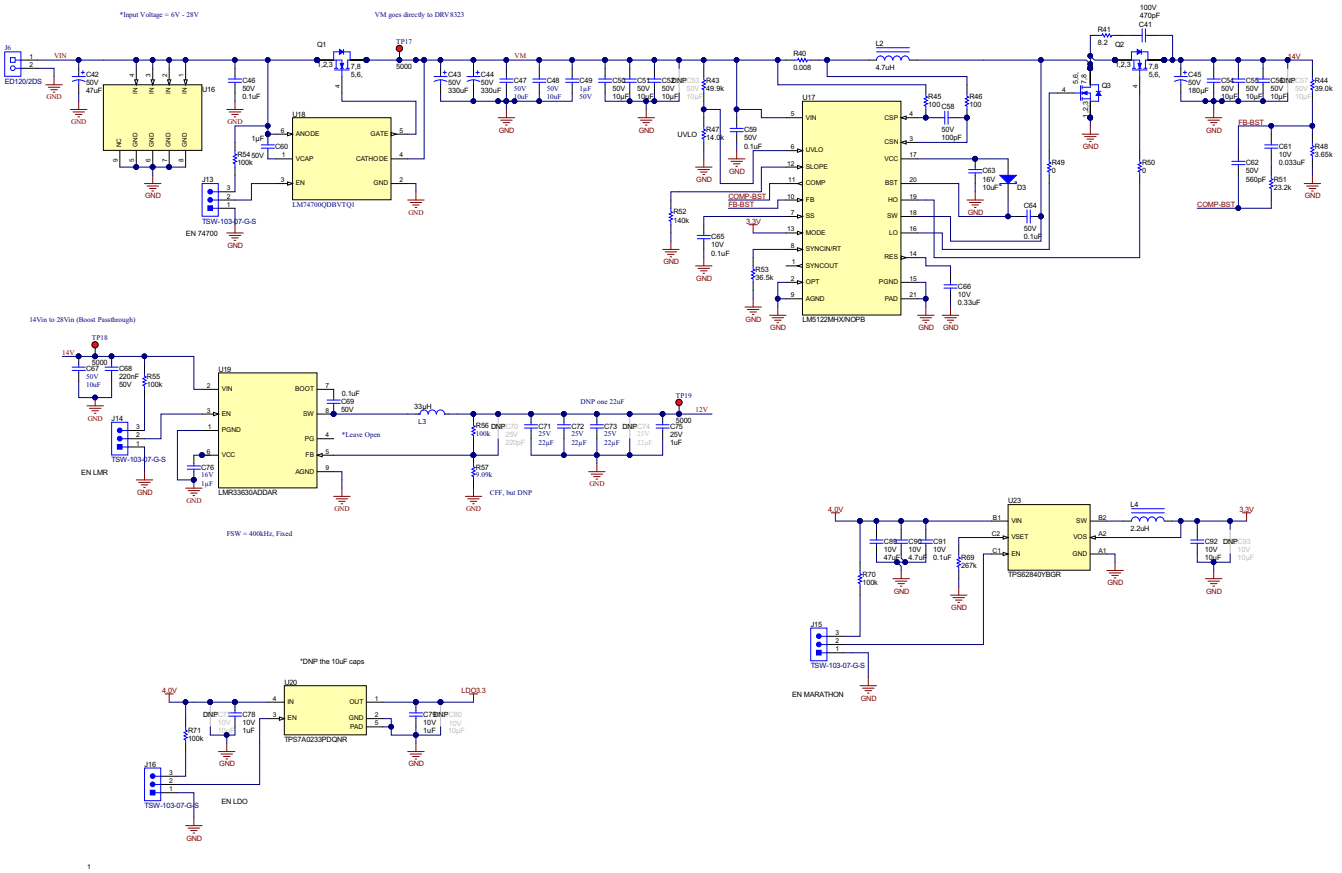


図 2-4. Power Tree Circuit

2.3 Highlighted Products

DRV8323RS

The DRV8323RS is a smart gate three-phase BLDC motor driver that integrates multiple features to provide accurate gate drive control, achieve safe operation, and a small solution size. The DRV8323RS integrates three half-bridge gate drivers, a charge pump to drive the high-side N-channel MOSFETs, and a linear regulator to drive the low-side N-Channel MOSFETs. These half bridges are controlled with a smart gate drive architecture that is capable of sourcing up to 1 A and sinking up to 2 A to the MOSFET gates for accurate control. The smart gate technology also allows the motor driver to dynamically adjust the strength of the gate drive output to optimize efficiency and reduce the external passive components required for the gate drive circuit. In addition to the gate drivers, the DRV8323RS integrates three current shunt amplifiers for each of the three phases for over-current protection (OCP). The DRV8323RS settings can be programmed through SPI while the gate drivers take PWM inputs from a MCU.

The DRV8323RS has a wide input voltage range of 6-60 V, which means that it is capable of operating over the full input voltage range of the reference design. This device incorporates a 600 mA, 60 V simple switcher buck converter typically used to power MCU's or other low power devices. The integrated buck regulator switches at 700 kHz and requires an external inductor, diode, and external capacitors. The buck converter also has a wide input voltage range, which allows it to operate over the full design input voltage range.

DRV8847

The DRV8847 is a dual H-bridge motor drive that is capable of driving single BDC motors, dual BDC motors, bipolar stepper motors, and solenoid valves depending on the configuration used and selected settings. The device is comprised of four individual half-bridges with integrated N-Ch MOSFETs that each have an $R_{DS(ON)}$ of 1000 mΩ. Depending on the configuration of the DRV8847, the half-bridges can be driven separately, as individual H-bridges, or as a combined dual H-bridge depending on the settings selected through I2C or through

external resistors depending on the variant. Each H-bridge is capable of driving up to 1 A individually or 2 A together under ambient conditions. Additionally, each H-bridge has pins to read the voltage across an external current shunt for over-current protection. A MCU or processors can be used to provide the required input PWM signals to the DRV8847. As for powering the device itself, the DRV8847 is capable of taking an input voltage range of 2.7-18 V and has a 1.7 µA sleep mode for high efficiency designs.

TPS62840

The TPS62840 is the latest low-voltage, low I_Q synchronous step-down DC-DC converter optimized for high-efficiency and a small solution size. The device integrates both the high- and low-side N-Ch MOSFETs with varying $R_{DS(ON)}$ values estimated between 200 mΩ and 650 mΩ. The integrated MOSFETs are capable of delivering up to 750mA in output current. This highly efficient device also has a reported operating quiescent current (I_Q) of 60 nA and is able to maintain 80% efficiency at a 1-µA output current, a light load condition.

The TPS62840 family is capable of taking a 1.8V – 6.5V input voltage and stepping down to 0.8V – 3.4V output voltage. Depending on the variant of the device selected, an external resistor is used to select the output voltage from 16 options. In order to ensure the efficiency of the design, the compensation network was integrated into the device. Therefore, it has specifically been designed to operate with an external 2.2 µH inductor and external 10 µF capacitor that allow for the reported ±2% output voltage accuracy specification. Certain device packages also include the additional run/stop feature, which allows the device to stop regulating output without turning off completely, meaning that it won't have to go through startup conditions again. This is specifically useful for taking noise-sensitive measurements because the switching noise can be temporarily eliminated while a measurement is taken. The output capacitor holds the voltage rail up for the short duration of the measurement and then the device goes back to switching.

TPS7A02

The TPS7A02 is the latest low-voltage, ultralow I_Q Low-Dropout Regulator (LDO) that is optimized for solution size and efficiency. The family of devices is capable of sourcing 200mA, and is specified to have a maximum 204 mV dropout for the 3.3 V output variant. Supporting an efficient design, the ultralow I_Q of the device is typically 35 nA and is partially achieved with the help of the smart enable pull-down. This low-I_Q allows the device to be targeted for battery-powered applications where efficiency, especially in the off-state, is the most important parameter for maintaining the life of the battery.

To minimize solution size and remove extra external components, the LDO comes in fixed output voltage variants that range from 0.8-5.0 V. The device does require external input and output capacitors. However, the device only requires a minimum capacitance of 0.1 µF for stability and is specified to have a maximum of 1.5% deviation from the set output voltage. The TPS7A02 comes in three potential package options including an X2SON, a DSBGA, and a SOT-23, with the DSBGA as the smallest at 0.65 mm x 0.65 mm for the most size critical applications.

LM5122

The LM5122 is a wide-input synchronous step-up (boost) controller that is capable of utilizing an input voltage range of 3-65 V and has a maximum output voltage of 100 V. In this design, this device is used to step-up battery level voltages to 14 V as a pre-boost for the DRV8847 ICs and solenoid valves. However, since the design includes an input voltage range as high as 28 V, the largest benefit of this boost controller is the highly efficient bypass mode. For input voltages equal to or higher than the set output voltage this device uses an internal charge pump, tied to the input voltage, to keep the gate of the series MOSFET high. This results in an efficient bypass of the LM5122 with the main losses from the $R_{DS(ON)}$ of the MOSFET.

In addition to the bypass mode, the device has many other features and specifications that make it an ideal choice. The use of external MOSFETs with this design allows for flexibility in finding a compromise between cost and efficiency that is driven by the needs of the specific design. To complement the use of selectable external MOSFETs, the integrated gate drivers are capable of sinking and sourcing up to 3 A. Additionally, the switching frequency of the boost is adjustable through an external resistor up to 1 MHz. The LM5122 is also a peak-current-mode control device that takes a differential current sense input from a series sense resistor.

LMR33630

The LMR33630 is a simple switcher 3 A synchronous DC/DC step-down converter that is optimized for solution size and efficiency. The device can take a wide input voltage range of 3.8-36 V and is capable of supply an

output voltage between 1-24 V. The integrated power MOSFETs have $R_{DS(ON)}$ values <100 mΩ, which help with achieving high efficiencies. The switching frequency of the converter is selectable between three options based on the variant of the device selected. A switching frequency of 400 kHz was selected for this design to get the highest possible efficiency while only incurring a small increase in solution size.

The LMR33630 also integrates most of the passive components required for most settings, which allows for a smaller solution size. However, it does require both a Vcc capacitor and bootstrap capacitor, in addition to the external inductor, input capacitors, output capacitors, and feedback network for output voltage regulation. The device comes in an HSOIC package that is 5 mm x 4 mm or a VQFN package that is 3 mm x 2 mm.

TMP1075

The TMP1075 temperature sensor is an updated replacement for the LM75 or TMP75, which are industry-standard digital temperature sensors. There is an SOIC and a VSSOP package that are pin-to-pin compatible with the TMP75 and LM75 for easy compatibility. The TMP1075 does also offer a new WSON package that is 2mm x 2mm that can save significantly on the solution size over the previous generation devices. Software from existing designs using the LM75 and TMP75 is also compatible with the new temperature sensor.

This digital temperature sensor can communicate over I2C or SMBus interfaces and can support up to 32 unique device addresses to accommodate a wide variety of designs. The device is capable of running on a wide voltage supply range of 1.7- 5.5 V and has a low average current consumption of 2.7 µA. Additionally, the temperature sensor has ±1 ºC accuracy over a wide range, with a maximum of ±2 ºC over the full temperature range. The integrated analog-to-digital converter (ADC) is a 12-bit ADC that provides a 0.0625 ºC temperature resolution. In addition to these specifications, the TMP1075 also includes an open-drain Alert pin, the threshold of which can be configured using I2C or SMBus communication. Apart from its size and accuracy, the device is also a cost-effective solution for many applications that are able to tolerate the accuracy range.

MSP430FR2155

The MSP430FR2155 is a part of the MSP430 MCU value line portfolio of ultra-low power, low-cost devices for sensing and measurement applications. The device has an integrated 12-channel, 12-bit ADC, two enhanced comparators, and a 32 KB nonvolatile FRAM. This MSP430 is able to operate off of a supply voltage between 1.8-3.6 V and has optimized low power modes to reduce the power consumption. When active, the device draws 142 µA/MHz, at an input voltage of 3 V, while the device will draw around 1.43 µA in standby mode and 42 nA in shutdown mode. In addition to low power consumption, internal voltage references allow for solution size savings and accurate ADC readings.

There are many resources available to support quick development on the MSP430FR2155 including example software, documentation, and trainings. The MSP430FR2355 LaunchPad development kit is a useful platform for developing code that can then be ported to a final design. The MSP430s also include several libraries of functions that streamline the software development.

LM74700-Q1

The LM74700-Q1 is a Low I_Q reverse battery protection ideal diode controller, which drives an external N-Ch MOSFET as an ideal diode rectifier to achieve low power loss and regulating the voltage drop at 20 mV from input to output. Specifically, the device is a reverse polarity protection IC that has integrated comparators to measure the voltage at the cathode (output) and anode (input) pins of the device. If the cathode voltage goes higher than the anode voltage, the device disables the gate of the MOSFET at a maximum rate of 2.3 A, which disconnects the downstream ICs and prevents reverse current flow. To enable the MOSFET, a charge pump is also integrated in the design and uses an external capacitor as part of the charge pump. While the device is operational, it sources 80 µA while it only sources 1 µA in shutdown mode.

Originally designed for automotive applications, the LM74700-Q1 is capable of operating with a wide input voltage range of 3.2-65 V, and is able to handle up to -65 V of reverse voltage. The device also has an enable pin that can be used to externally enable and disable the LM74700-Q1 for precise control beyond the internal output voltage and input voltage comparator. The LM74700-Q1 comes in a small SOT-23 package, which allows for small form factor designs, but does require the external MOSFET as previously mentioned.

CSD88584Q5DC

The CSD88584Q5DC is a 40-V Half-Bridge NexFET Power Block device that integrates two Power N-Ch MOSFETs into a single 5 mm x 6 mm package with pins for gate drive signals and a sense pin for the switch

node. These devices were specifically designed to be coupled with half-bridge gate drivers that are integrated with motor driver ICs. The MOSFETs have $R_{DS(ON)}$ values below 2 mΩ to minimize the power loss during motor operation and are well rated for the maximum input voltage expected in the design. To help mitigate any potential thermal issues, these devices also have an exposed metal pad on the top side that can be connected to a heat sink for optimal heat dissipation. These MOSFETs have also been optimized to operate at switching frequencies between 5 kHz and 50 kHz, which is the typical switching frequency range for BLDC motors.

CSD18543Q3A

The CSD18543Q3A is a single 60-V N-Ch NexFET Power MOSFET optimized for solution size and power density. The device comes in a 3.3 mm x 3.3 mm package and has an $R_{DS(ON)}$ below 12 mΩ to help limit power loss and mitigate potential thermal concerns. The device is rated to handle a maximum continuous current of 12 A, which is double the input current expected in the design. The total gate charge of 11.1 nC and typical gate drive voltage of 10 V are also beneficial specifications, especially given that this device is paired with the gate drive of the LM5122, which is capable of driving to those specifications. Other advantages of this device include a rated pulsed drain current of 156 A and a wide temperature operating range up to 150 ºC.

CSD18532Q5B

The CSD18532Q5B is a single 60-V N-Ch NexFET Power MOSFET optimized for low power loss with a low $R_{DS(ON)}$ of 2.5 mΩ. This device was selected to operate as the reverse polarity MOSFET paired with the LM74700-Q1, so power loss, current ratings, and thermal characteristics are among the key specifications when selecting the appropriate device. The continuous rated current for this MOSFET is 23 A, which is above the expected peak current in the design. The device is also in a 5 mm x 6 mm package that is optimized for thermal dissipation. In addition to these specifications, the total gate charge of 44 nC is important to consider because that helps to determine how quickly the MOSFET can be switched off in the event of a reverse polarity detected.

TVS3301

The TVS3301 is a bi-directional flat-clamp surge protection device that serves the same functionality as a bidirectional TVS diode. This device is capable of protecting against the IEC 61000-4-5 surge current and voltage waveforms as well as against the IEC61643-321 waveforms. The device has a ±33V operating range, clamps the voltage to a maximum of 40 V during surge events, and is capable of sinking up to 27 A, which is defined by the IEC 61000-4-5. The device also has a low capacitance of 54 pF, which is beneficial especially in signal chain applications.

The largest benefits of the TVS3301 are highlighted when compared to traditional TVS diodes. The TVS3301 is a smart gate driver with integrated MOSFETs that have significantly lower on-state resistances than TVS diodes. The TVS3301 also integrated a feedback circuit to monitor the current, which is how it is able to clamp the over-voltage precisely at 40 V during surge events. The lower resistance of the TVS3301 means that it will have significantly smaller power dissipation during surge events and also allows the package to be significantly smaller than traditional SMA and SMB diode packages.

TPD4E1U06

The TPD4E1U06 is a quad channel, high-speed unidirectional ESD protection device that is capable of withstanding the ESD events as well as surge events. The device is specified to be capable of withstanding the IEC61000-4-2 Level 4 ESD events, which include ±15 kV contact discharge and ±15 kV air gap discharge. The device is also rated to withstand a 3 A surge of the IEC 61000-4-5 and an 80-A EFT event according to the IEC 61000-4-4. The device is also specified to have only 0.8 pF of line capacitance, which makes it an ideal choice for multiple applications including HDMI and USB2.0 communications. Another useful benefit of the device is the ultra-low leakage specified at a maximum of 10 nA, which helps maintain signal integrity and limit efficiency losses from incorporating the device.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware and Software Requirements

The following hardware (HW) equipment and software (SW) are required to allow full evaluation of the TIDA-010072 reference design.

表 3-1. Hardware and Software Requirements

HW AND SW	COMMENTS
6-28 V, 10-A adjustable power supply	Required current capability depends on load under test
TIDA-010072	Design Folder
LAUNCHXL-F28027F & USB cable	Tool Folder
MSP-FET	Tool Folder
CCS 10.0.0 or newer	Download Link
Motorware 1.01.00.18	Download Link
DRV832x Firmware (InstaSpin)	Download Link

Alternatively, the user can use LAUNCHXL-F280049C or LAUNCHXL-F28069M. However, motorware may not have solutions available for DRV8323 specifically. The user may need to port some FW.

The MSP-FET is required only if the user intends to evaluate the DRV8847 solenoid drivers and the TMP1075 temperature sensors. CCS provides the user interface to control the valve drivers and readout the temperature. The BLDC motor control can be evaluated independent of the MSP430 functions.

3.2 Test Setup

3.2.1 Hardware Configuration

PCB Overview

図 3-1 and 図 3-2 show the top and bottom views of the TIDA-010072 with the LAUNCHXL-F28027F Launchpad (LP) connected. The top side of the LP is shown in 図 3-3.

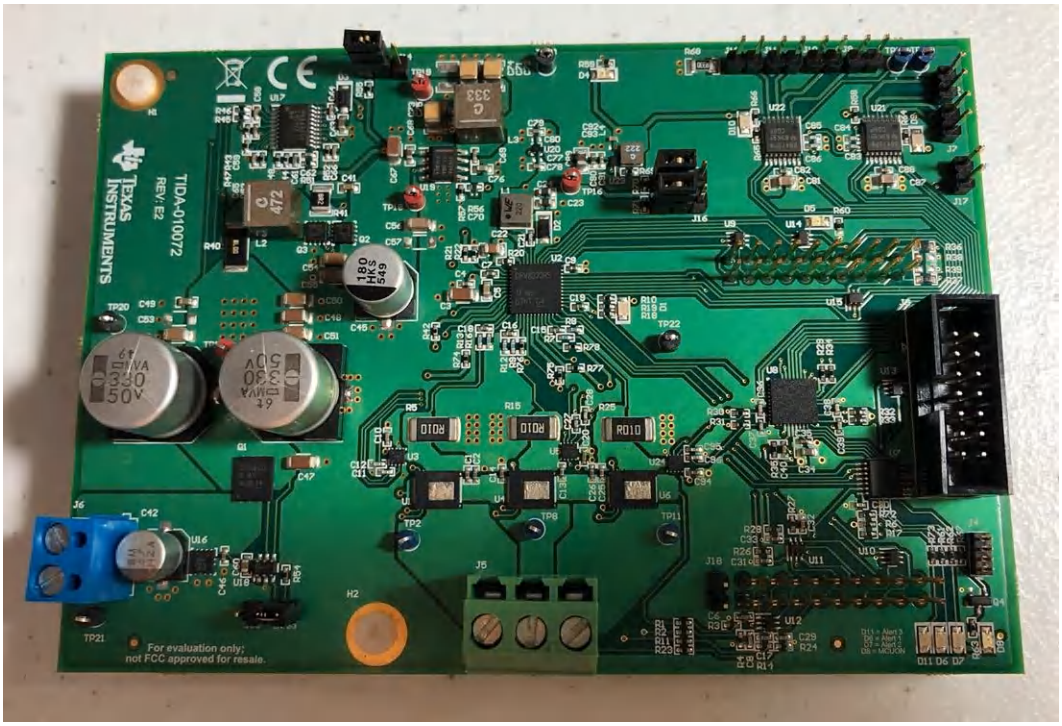


図 3-1. TIDA-010072 Top

図 3-2. TIDA-010072 Bottom

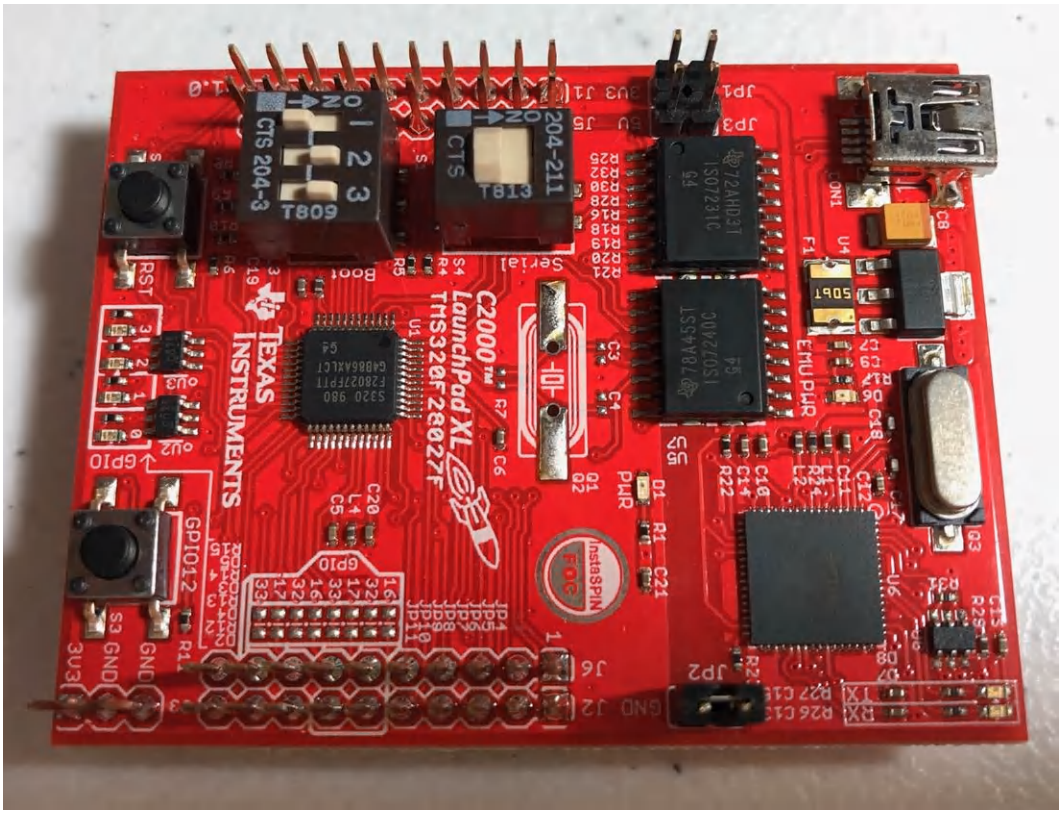


図 3-3. Launchpad Top

LaunchPad Configuration

The C2000 LaunchPad has two separate power domains for the purpose of allowing JTAG isolation. Jumpers JP1, JP2, and JP3 configure whether the USB power is passed to the target device.

When using the LAUNCHXL-F28027F, the following configuration of the LP board is necessary. The jumper and switch settings are outlined in 表 3-2. Jumpers JP1, JP2, and JP3 are disconnected because the target device will be powered from the TIDA-010072 power supply.

表 3-2. LaunchPad Configuration

CONNECTOR	CONNECTION	DESCRIPTION
JP1	Disconnected	Enable 3.3 V to target device
JP2	Disconnected	Enable GND to target device
JP3	Disconnected	Enable 5.0 V to target device
S3	OFF	Disconnect the Piccolo serial pins from the XDS100 UART
S1	OFF-ON-ON	bootROM configuration

For more details, please refer to the LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit User's Guide.

TIDA-010072 Configuration

表 3-3. TIDA-010072 Configuration

CONNECTOR	CONNECTION	DESCRIPTION
J1	LP	Launchpad connector
J2	LP	Launchpad connector
J3	MSP-FET JTAG	Required for valve control and TMP1075 readout

表 3-3. TIDA-010072 Configuration (continued)

CONNECTOR	CONNECTION	DESCRIPTION
J4	Optional	MSP430FR2155 serial connector
J5	Motor	3-P BLDC Motor connector
J6	Power Input	DC Power Supply Input connector
J7	Bidirectional Valve	U21 DRV8847 OUT1 & OUT2 connector
J8	Bidirectional Valve	U21 DRV8847 OUT3 & OUT4 connector
J9	Unidirectional Valve	U22 DRV8847 OUT1 connector
J10	Unidirectional Valve	U22 DRV8847 OUT2 connector
J11	Unidirectional Valve	U22 DRV8847 OUT3 connector
J12	Unidirectional Valve	U22 DRV8847 OUT4 connector
J13	Pin 2-3	Enable LM74700 Ideal Diode Controller
J14	Pin 2-3	Enable LMR33630 12V Boost
J15	Pin 2-3	Enable TPS62840 3.3V Buck
J16	Pin 2-3	Enable TPS7A0233 3.3V LDO
J17	Optional	I2C connector for debugging DRV8847
J18	Optional	I2C connector for debugging TMP1075

System Hardware Test Setup

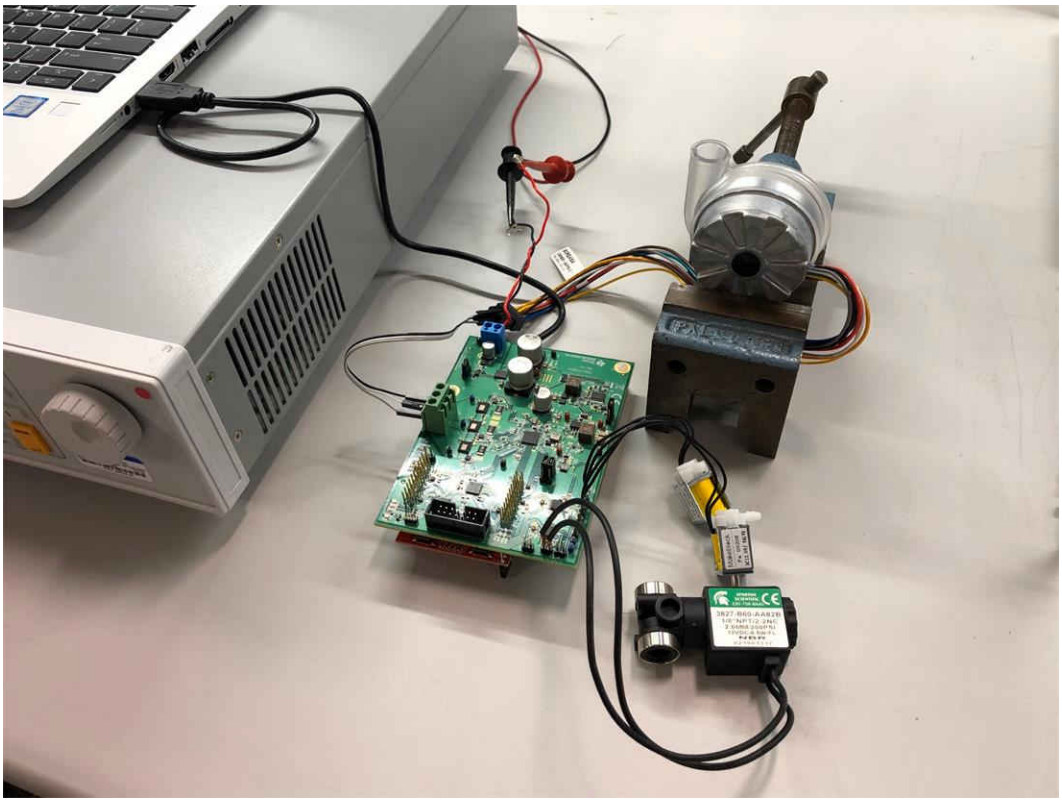


図 3-4. HW Setup for Blower Tests

The HW setup for blower tests is shown in 図 3-4. The test equipment used for the TIDA-010072 test session is shown in 表 3-4.

表 3-4. Test Equipment

EQUIPMENT	PART NUMBER
Adjustable power supply	Chroma 62006p-30-80
C2000 LaunchPad	LAUNCHXL-F28027F
Oscilloscope	Teledyne LeCroy WaveSurfer 24Xs
Laptop	HP Elitebook 830 G6
MSP MCU Programmer and Debugger	MSP-FET
24-V Single Pole Pair BLDC	Wonsmart WS7040-24-V200
24-V Single Pole Pair BLDC	Boreasa C65MS1-L5
12-V Solenoid Valve, Unidirectional Operation	Makeblock 59001
12-V Solenoid Valve, Bidirectional Operation	Spartan Scientific 3827-B60-AA82B

The jumpers on the TIDA-010072 and LP boards were set as described in 表 3-3 and 表 3-2, respectively.

The boards were connected using the TIDA-010072 female headers (J1 and J2) to the LP male headers (J1, J5, J2 and J6) as shown in 図 3-2. The LP was connected to the computer via a USB cable.

The power supply was connected to the TIDA-010072 J6 terminal connector and the BLDC motor was connected to the TIDA-010072 J5 terminal connector as shown in 図 3-4. The Chroma power supply was set to 24V with the current limit set to 10A.

For the valve functional test, two Makeblock and one Spartan Scientific valves were connected to the TIDA-010072 male headers (J7, J11, J12) for unidirectional and bidirectional operation, respectively. To control the valves, the MSP-FET was connected to TIDA-010072 JTAG connector (J3) and the USB port of the laptop as shown in 図 3-5. Note that this test is independent of the C2000 LP.

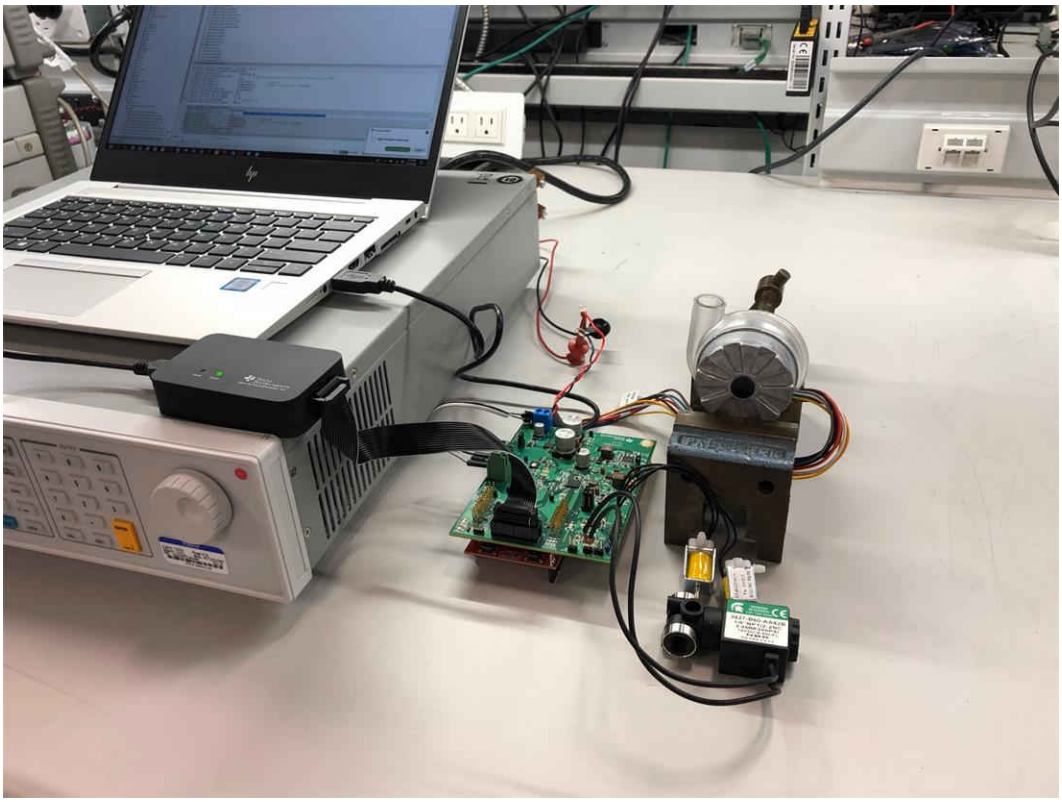


図 3-5. HW Setup for Valve Tests

3.2.2 Software Configuration

Initial setup

Step 1. Download Motorware 1.01.00.18 from ti.com and install in the default directory as shown in 図 3-6 and 図 3-7.

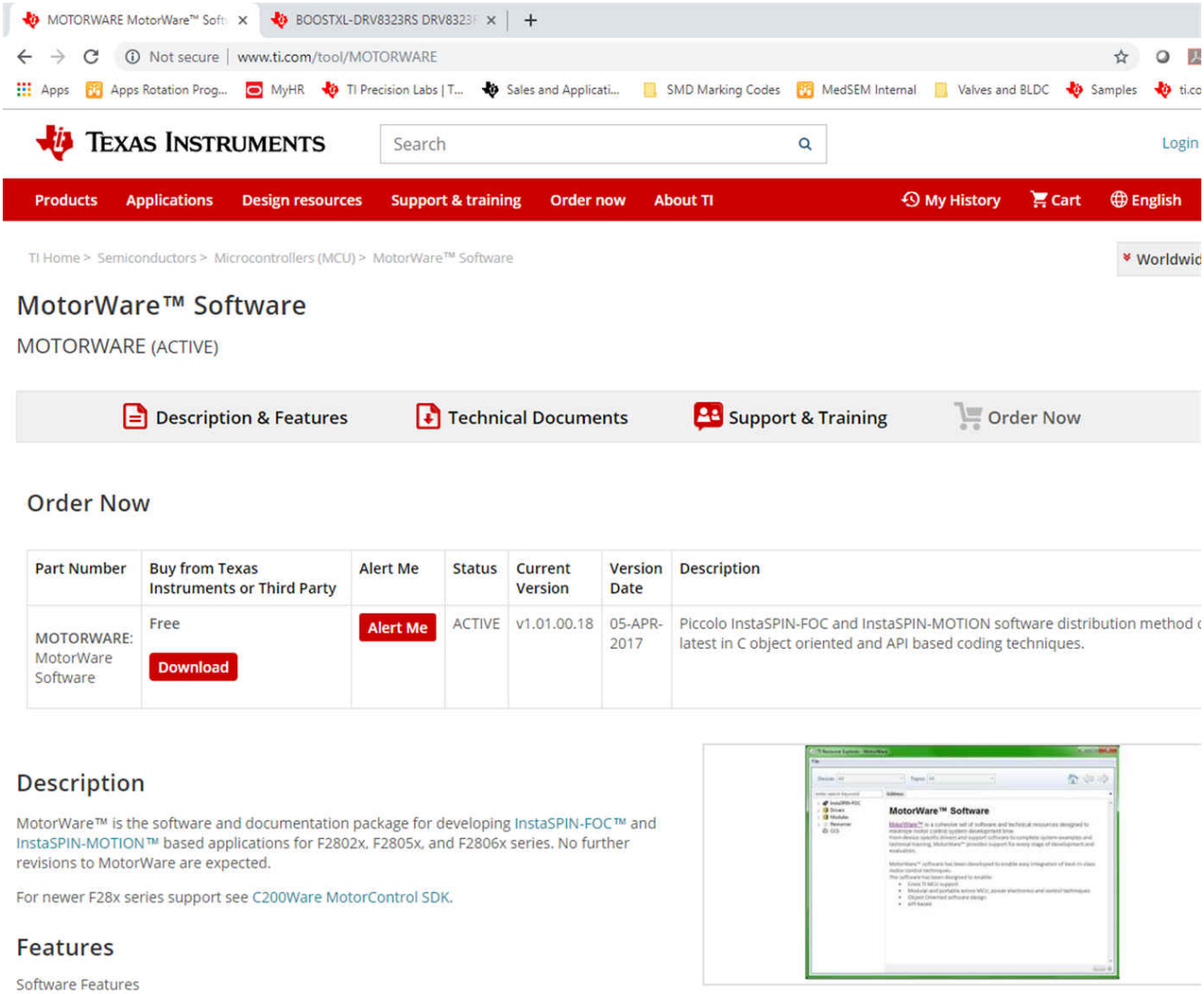


図 3-6. Download Motorware

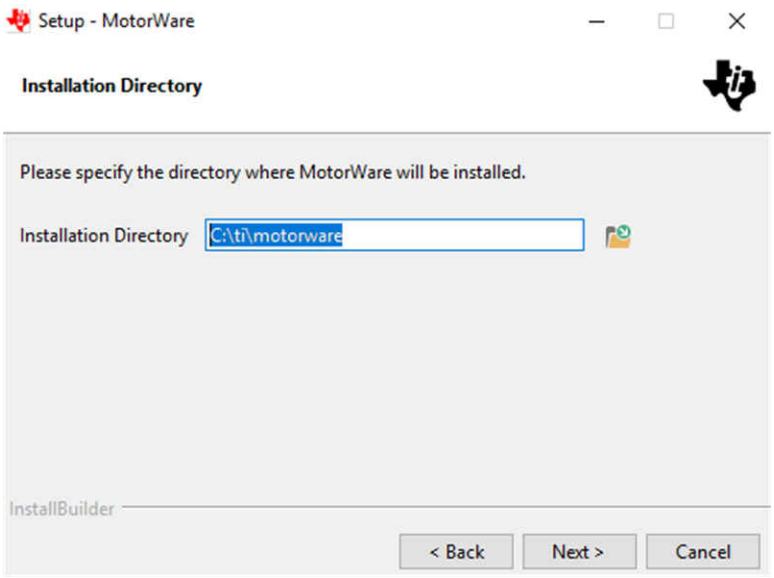


図 3-7. Install in the default directory

Step 2. Download DRV832x Firmware (InstaSpin) from ti.com.

Step 3. Copy the downloaded DRV832x FW folders (**drvic, hal and instaspin_foc**) to the corresponding motorware_1_01_00_18 directory (C:\ti\motorware\motorware_1_01_00_18) as shown in 図 3-8 and 図 3-9. The specific target locations are shown here:

- C:\ti\motorware\motorware_1_01_00_18\sw\drivers**drvic**
- C:\ti\motorware\motorware_1_01_00_18\sw\modules**hal**
- C:\ti\motorware\motorware_1_01_00_18\sw\solutions**instaspin_foc**

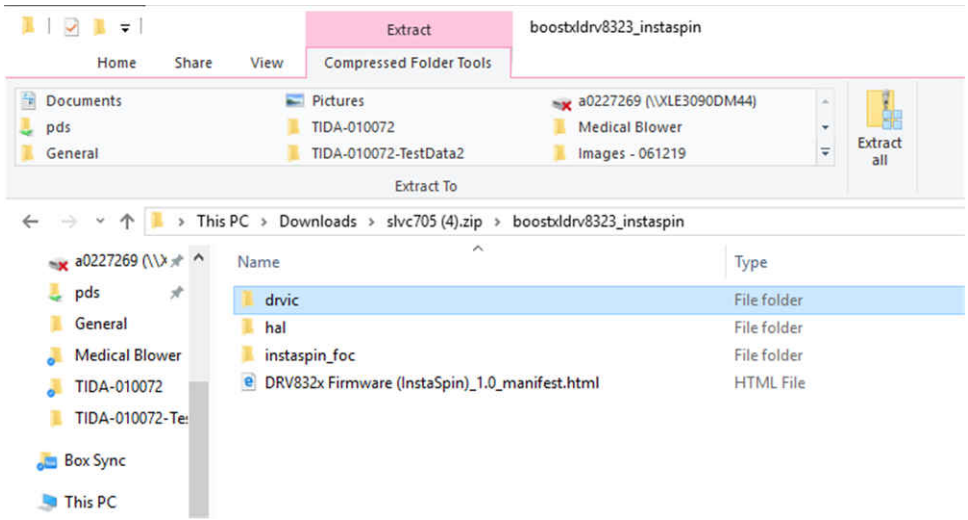


図 3-8. Copy the downloaded DRV832x FW folders

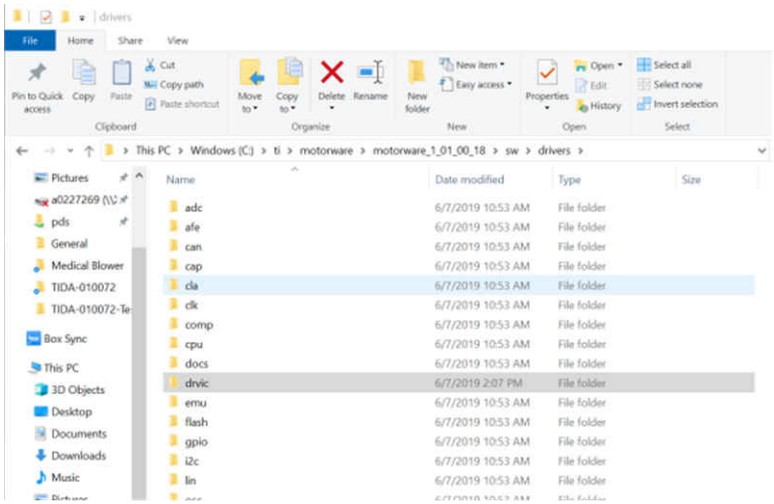


図 3-9. Target locations

Porting lab05h for DRV8323

Unfortunately, the default DRV8323 FW download doesn't include Proj_lab05h (at the writing of this design guide). In order to use the lab05h project with the DRV8323 device, a pre-existing DRV8353 lab05h from the motorware solution folder was ported. The template project under located in this directory:

- C:\ti\motorware\motorware_1_01_00_18\sw\solutions\instaspin_foc\boards\drv8353rx_evm_revA\f28x\f2802xF\projects\ccs

Note, when copying a CCS template project from one directory to another, do not copy the .launches and .settings folders. This will cause errors when debugging the newly ported project. CCS will auto generate the appropriate .launches and .settings folders.

Once the lab05h project is copied from the template DRV8353 to the target DRV8323 solutions directory, import the project to CCS to begin the porting process. The following items require minor modifications to support DRV8323 instead of DRV8353:

1. proj_lab05h.c (locate instances of DRV8353 and change to DRV8323 as necessary)
2. .project, .cproject, .ccsproject project files (locate instances of DRV8353 and change as necessary)
3. Project settings: Linked resources (locate instances of DRV8353 and change as necessary)
4. Project settings: Build->C2000 Compiler->Include Options (locate instances of DRV8353 and change as necessary)

After making the changes, be sure to delete the old DRV8353 links under CCS project explorer to ensure proper compilation.

Import the CCS Projects

Step 1: Project->Import CCS Projects

Step 2: Browse for:

- C:\ti\motorware\motorware_1_01_00_18\sw\solutions\instaspin_foc\boards\boostxldrv8323_revA\f28x\f2802xF\projects\ccs

Step 3: Import *Proj_lab02c* and *Proj_lab05h* to local working directory as shown in 図 3-10.

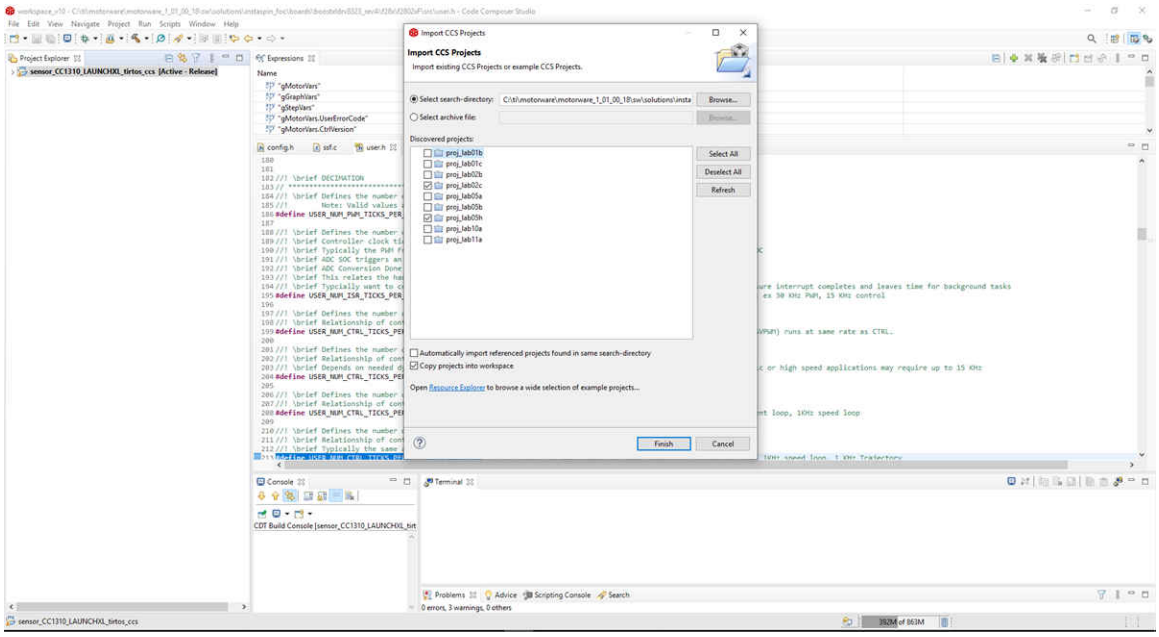


図 3-10. Import project

This design guide uses the following examples:

- Proj_lab02c (for identifying the motor parameters)
- Proj_lab05h (for motor step response)

> When running these examples, reference the document *InstaSPIN Projects and Labs User's Guide* located in the document folder of MotorWare (**motorware_1_01_00_xx\docs\labs**).

CCS User Interface

Each project has a specific .js scripting file located in the project. The first time running each lab, the user needs to copy the scripting file content to scripting console as shown in 図 3-11. This will populate the CCS *Expressions* tab, which will enable the user to have specific controls during debug session.

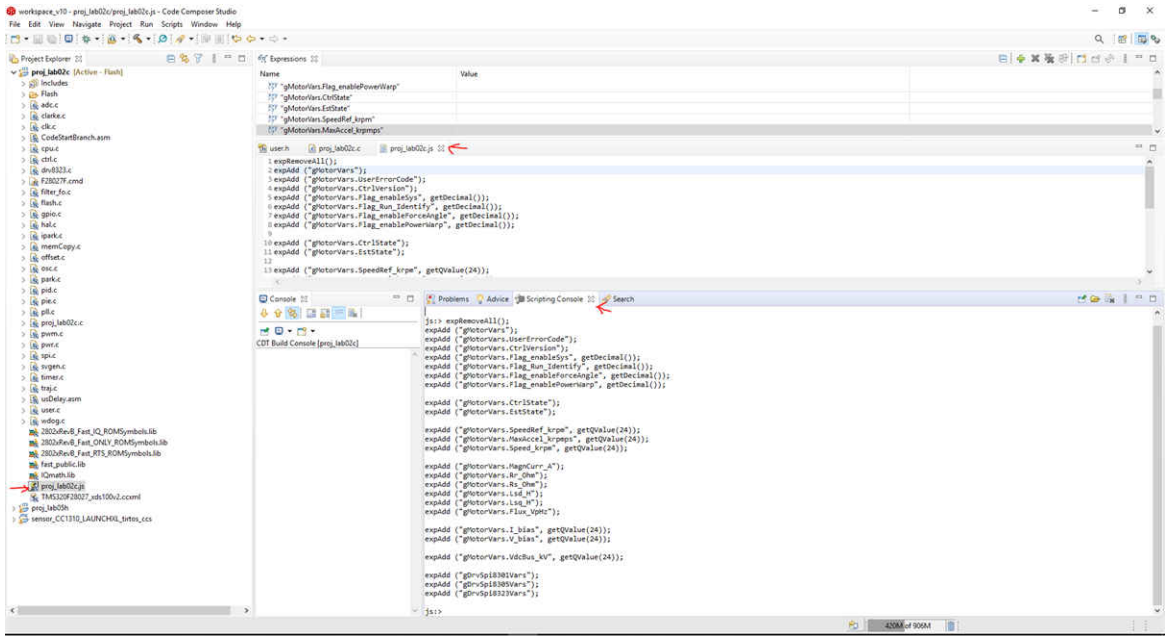


図 3-11. Copy the scripting file to scripting console

For more details on the user interface in CCS, see the *InstaSPIN Projects and Labs User's Guide* in the MotorWare installation folder.

Identifying the Motor

For source code of the software, download MotorWare and go through proj_lab02c. This lab is built to identify PMSM motors with low inductance. After this lab, the motor parameters are in the following configuration: Rs, Lq, Ld, and Rated Flux. For more details on the values, see the InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide.

The complete instructions to use proj_lab02c is in the *InstaSPIN Projects and Labs User's Guide* located in the document folder of MotorWare (**motorware_1_01_00_xx\docs\labs**).

The first time running each lab, the user needs to copy the scripting file content to scripting console.

To identify the motor (e.g. Wonsmart motor), the following initial settings were used in user.h:

```
#define Wonsmart_WS7040_24_V200     111
#define USER_MOTOR Wonsmart_WS7040_24_V200

#elif (USER_MOTOR == Wonsmart_WS7040_24_V200)
#define USER_MOTOR_TYPE                 MOTOR_Type_Pm
#define USER_MOTOR_NUM_POLE_PAIRS       (1)
#define USER_MOTOR_Rr                   (NULL)
#define USER_MOTOR_Rs                   (NULL)
#define USER_MOTOR_Ls_d                 (NULL)
#define USER_MOTOR_Ls_q                 (NULL)
#define USER_MOTOR_RATED_FLUX           (NULL)
#define USER_MOTOR_MAGNETIZING_CURRENT  (NULL)
#define USER_MOTOR_RES_EST_CURRENT      (1.0)
#define USER_MOTOR_IND_EST_CURRENT      (-1.0)
#define USER_MOTOR_MAX_CURRENT          (7.5)
#define USER_MOTOR_FLUX_EST_FREQ_Hz     (40.0)
```

Note that the USER_MOTOR_MAX_CURRENT parameter limits the peak current of the motor and thus determines the maximum motor acceleration/deceleration rate.

With this definition in the user.h file, the motor can be identified with running proj_lab02c. In CCS debug mode, use the *Expressions* tab to enable the system and run the motor identification routine as shown in 図 3-12.

Make sure to have *Continuous Refresh* checked.

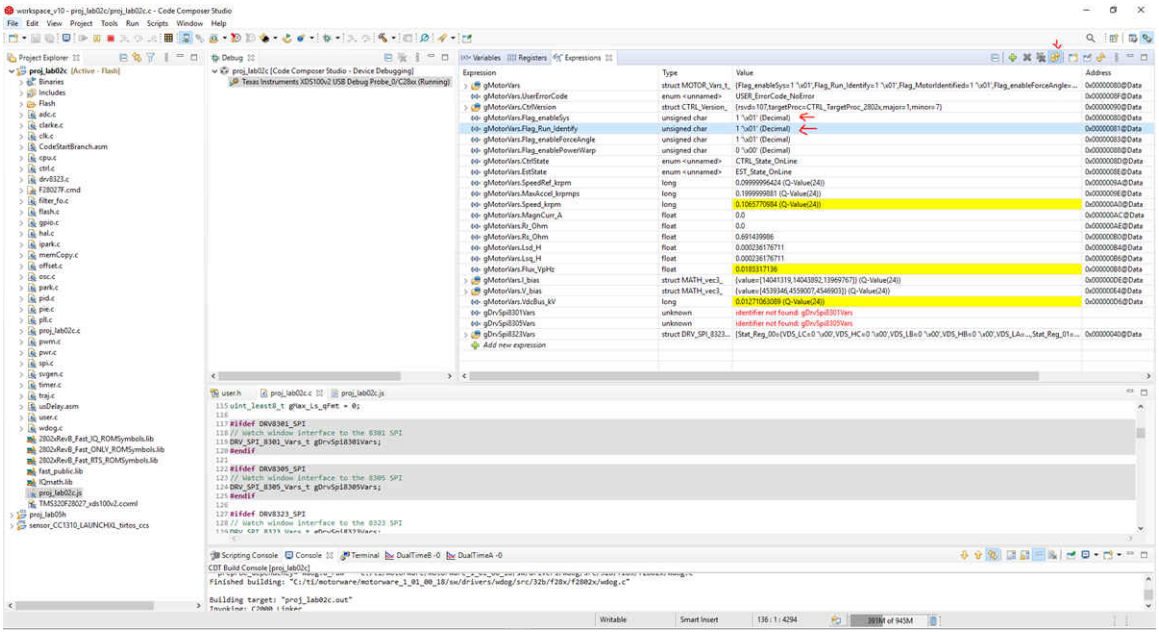


図 3-12. Identifying motor test

After the identification routine is done, save these newly identified motor parameters to the user.h for future tests:

```
#define USER_MOTOR_Rs (0.103635125)
#define USER_MOTOR_Ls_d (3.24286011e-05)
#define USER_MOTOR_Ls_q (3.24286011e-05)
#define USER_MOTOR_RATED_FLUX (0.00302618463)
```

Generating the Step Response

To generate the step responses, use the lab proj_lab05h. To use this lab, see the lab instructions located in the file *instaspin_labs.pdf*. This file can be found under the documentation folder when installing MotorWare.

Generating these step responses will give the user the option to test the PI controller of the system. When generating the step response, the actual load used for the system must be connected to the motor. This will generate the most accurate data when running the motor. Having this lab enables the user to adjust the control according to the system performance.

The first time running each lab, the user needs to copy the scripting file content to scripting console.

To import the graph during debug session, go to Tools->Graphs->Dual Time->Import as shown in 図 3-13. Find proj_lab05h.graphProp config file located here:

- C:\ti\motorware\motorware_1_01_00_18\sw\solutions\instaspin_foc\src

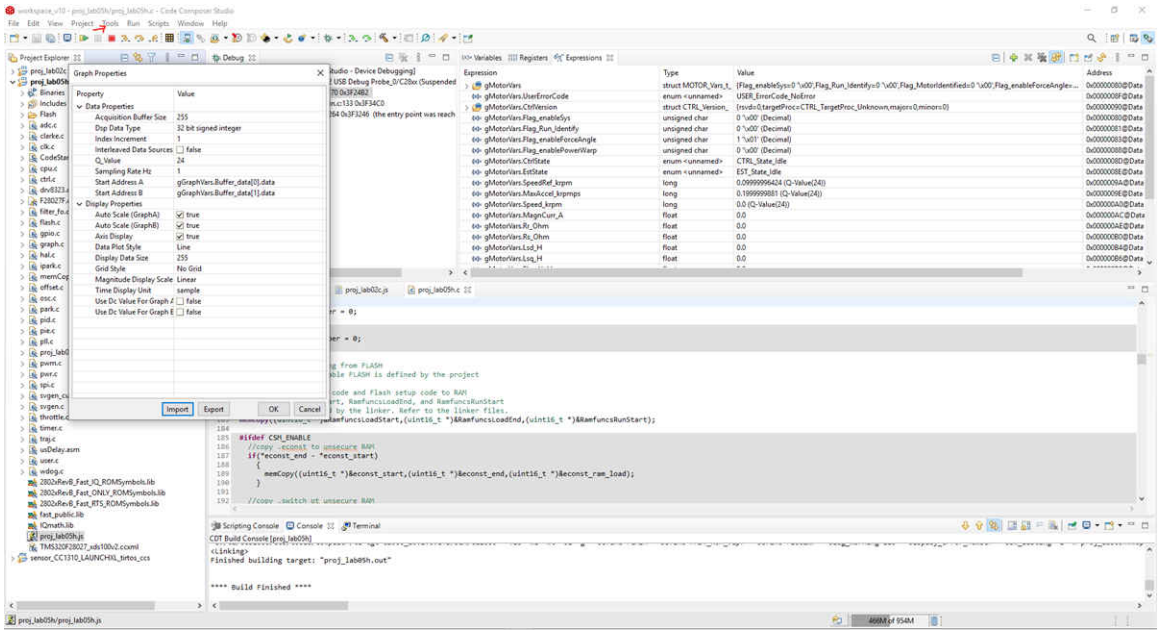


図 3-13. Importing the graph

Run debug session.

Check the *continuous refresh* setting for both the Expressions and Graph tabs as shown in 図 3-14.

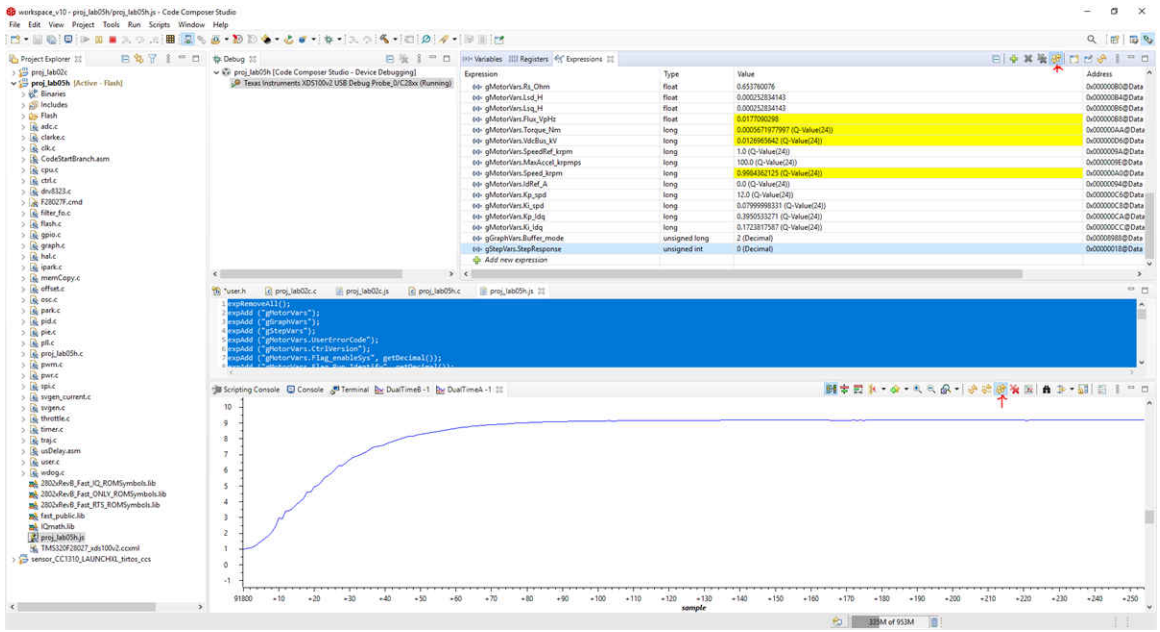


図 3-14. Measuring step response in CCS

Due to the high acceleration required for the step response test (150 kRPM/s), USER_MOTOR_NUM_POLE_PAIRS #define in user.h was changed from 1 to 2 as a workaround to the 127.0 (Q-Value(24)) max acceleration limit (gMotorVars.MaxAccel_krpmps parameter in the CCS Expressions tab).

The following settings were used for the 10 kRPM to 40 kRPM speed response test. Since the USER_MOTOR_NUM_POLE_PAIRS was redefined to 2. The real speed will be doubled of these reference *spdRef* settings in CCS.

These are the user control parameters used in the Expressions tab during the debug session.

- gGraphVars
  - Buffer_tick unsigned long 50 // this scales the time capture window
  - Buffer_mode unsigned long 2 // 1 is for current step and 2 is for speed step
- gStepVars
  - StepResponse 1 // enter 1 to start the step response test
  - spdRef_Default 5 (Q-Value(24)) //initial reference speed of 10kRPM
  - spdRef_StepSize 15 (Q-Value(24)) //step size is 30kRPM to achieve a target speed of 40kRPM
- gMotorVars.CtrlVersion
  - gMotorVars.Flag_enableSys 1
  - gMotorVars.Flag_Run_Identify 1
  - gMotorVars.MaxAccel_krpmps 100 (Q-Value(24)) //200kRPM/s max acceleration limit
  - gMotorVars.Kp_spd 12.0 (Q-Value(24))
  - gMotorVars.Ki_spd 0.08 (Q-Value(24))

Valve Control and Temperature Sensing

A C program in CCS was developed for the MSP430FR2155 to test the basic functions of the DRV8847 and TMP1075 devices. The code communicates with two DRV8847S devices through I^2C. One DRV8847 drives up to four unidirectional solenoid valves, the other drives up to two bidirectional solenoid valves. Each valve is switched in a sequence, including the bidirectional valves. The code also communicates with three TMP1075 devices through I^2C to read the temperature.

3.3 Test Results

3.3.1 Motor Test Result

The following motor tests were conducted:

- Motor Identification
  - Wonsmart WS7040_24_V200
  - Boreasa C65MS1_L5
- No-Load Step Response
  - Current Step Response
  - Speed Step Response (10kRPM to 40kRPM and 40kRPM to 10kRPM)

Tests were done at room temperature around 22°C to 23°C, with a PWM of 45 kHz. The current and speed controllers were set to 45 kHz and 3 kHz. The user control parameters are configured in the user.h file.

```
#define USER_PWM_FREQ_kHz                (45.0)
#define USER_NUM_CTRL_TICKS_PER_CURRENT_TICK   (1)
#define USER_NUM_CTRL_TICKS_PER_SPEED_TICK  (15)
```

Motor Identification

When identifying the motor parameters, the proj_lab02c from MotorWare was used. The following parameters were identified for the Wonsmart_WS7040_24_V200 motor:

```
#define USER_MOTOR_TYPE                 MOTOR_Type_Pm
#define USER_MOTOR_NUM_POLE_PAIRS       (1)
#define USER_MOTOR_Rs                   (0.653760076)
#define USER_MOTOR_Ls_d                 (0.000252834143)
#define USER_MOTOR_Ls_q                 (0.000252834143)
#define USER_MOTOR_RATED_FLUX           (0.0168186165)
```

The following parameters were identified for the Boreasa_C65MS1_L5 motor:

```
#define USER_MOTOR_TYPE MOTOR_Type_Pm
#define USER_MOTOR_NUM_POLE_PAIRS (1)
#define USER_MOTOR_Rs (0.348989993)
#define USER_MOTOR_Ls_d (0.000173127264)
#define USER_MOTOR_Ls_q (0.000173127264)
#define USER_MOTOR_RATED_FLUX (0.0160903856)
```

Once the motor parameters are determined from lab02c and saved to user.h, the user can proceed to lab05h for step response testing.

No-Load Step Response

When measuring the step reponse, proj_lab05h was used. The motors tested were Wonsmart_WS7040_24_V200 and Boreasa_C65MS1_L5.

図 3-15 shows the Wonsmart Id current controller PI step response.

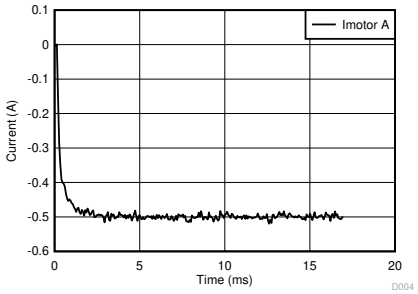


図 3-15. Wonsmart Id Current Controller PI Step Response

図 3-16 shows the Wonsmart speed controller PI step response.

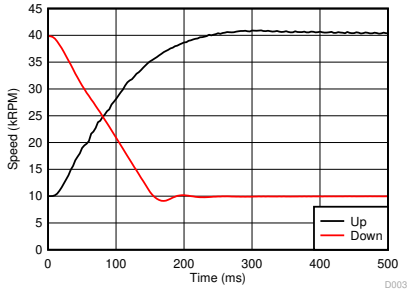


図 3-16. Wonsmart Speed Controller PI Step Response

表 3-5. PI Controller Parameters to Generate No-load Step Responses

CONTROLLER	KP	KI
Current controller at 45 kHz	0.395	0.172
Speed controller at 3 kHz	12	0.08

図 3-17 shows the Boreasa Id current controller PI step response.

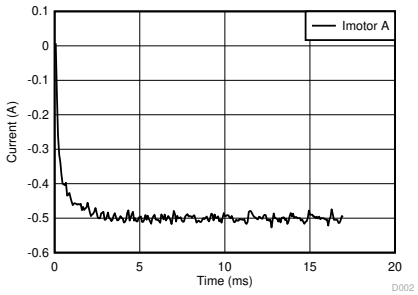


図 3-17. Boreasa Id Current Controller PI Step Response

図 3-18 shows the Boreasa speed controller PI step response.

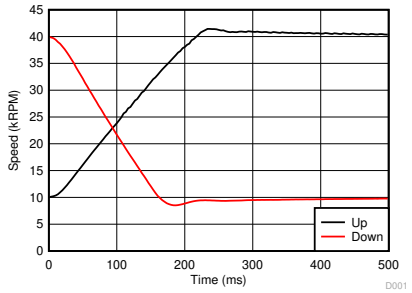


図 3-18. Boreasa Speed Controller PI Step Response

表 3-6. PI Controller Parameters to Generate No-load Step Responses

CONTROLLER	KP	KI
Current controller at 45 kHz	0.27	0.134
Speed controller at 3 kHz	30	0.12

These PI values are optimized for this specific speed range. In reality, the designer may have multiple sets of PI values depending on the specific operation (for example, one set low speed and another set for high speed).

3.3.2 Valve Test Result

The following valve tests were conducted:

- Valve Turn-On Time (Makeblock 59001)
- Valve Turn-Off Time (Makeblock 59001)
- Consecutive Valve operation (2x Makeblock 59001)
- Bidirectional Valve operation (Spartan Scientific 3827-B60-AA82B)

DRV8847 Valve Turn-On Time

The valve turn-on transition (<400 ns) is clean with minimal overshoot as shown in channel 1 in 図 3-19.

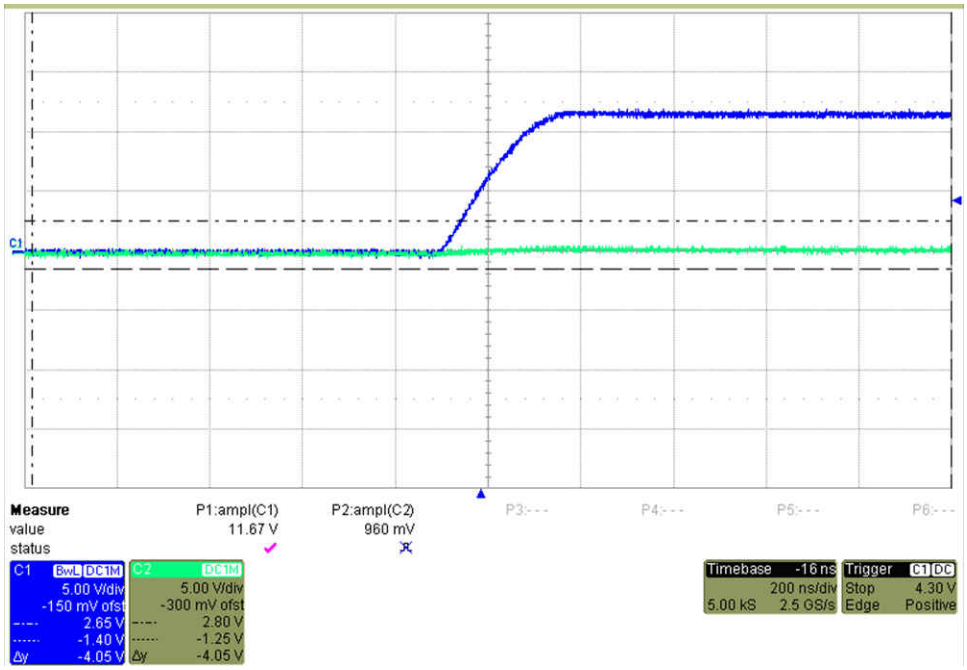


図 3-19. DRV8847 Valve Turn-On Time

DRV8847 Valve Turn-Off Time

The valve turn-off transition (<400ns) is clean with minimal overshoot as shown in channel 1 in 図 3-20.

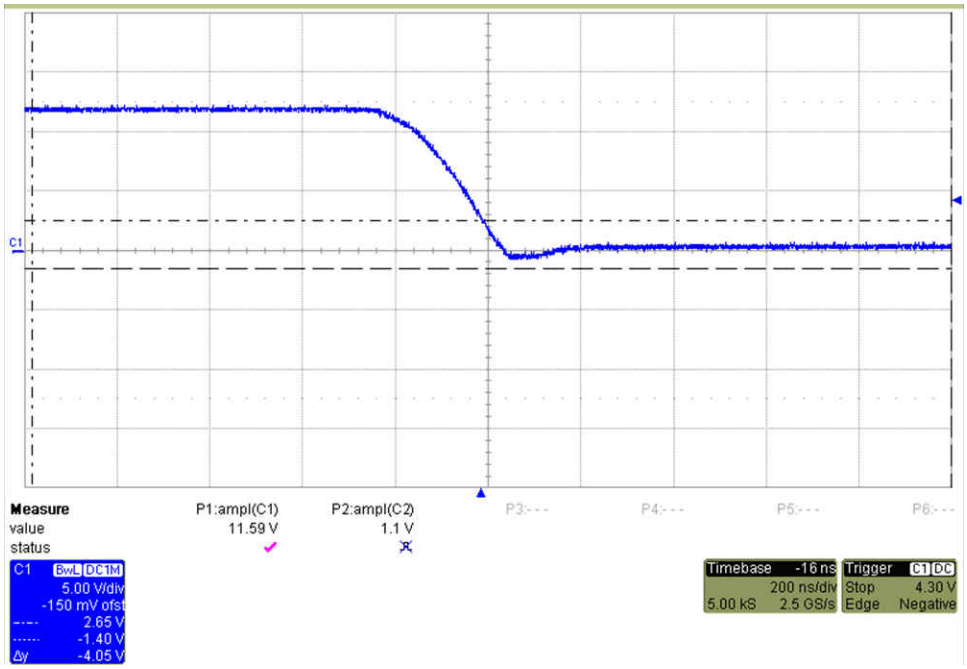


図 3-20. DRV8847 Valve Turn-Off Time

DRV8847 Consecutive Valve Operation

The transition between valves is clean with no overshoot as shown in channel 1 and 2 in 図 3-21. Valve is seen and heard to engage during both events.

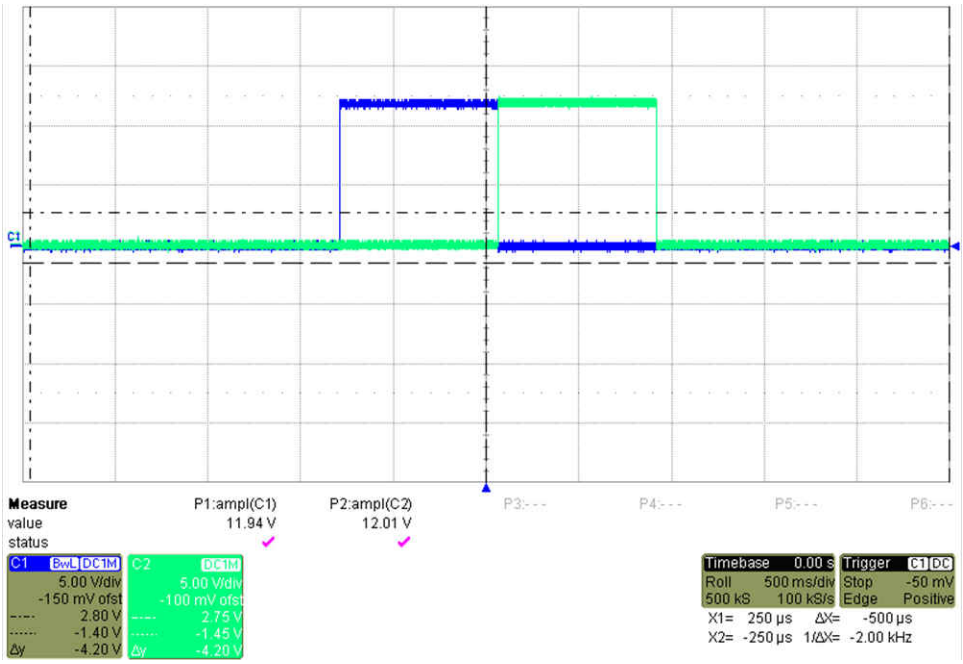


図 3-21. DRV8847 Consecutive Valve Operation

DRV8847 Bidirectional Valve Operation

The voltage waveforms for each side matched as shown in channel 1 and 2 in 図 3-22. The observed current draw was the same for either direction. The valve is seen and heard to engage during both events.

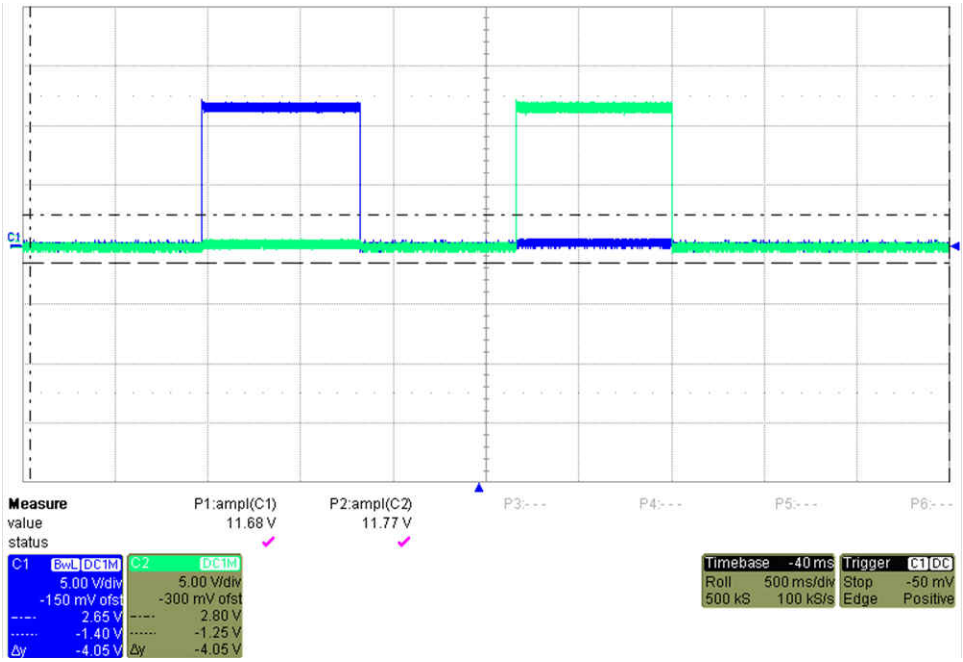


図 3-22. DRV8847 Bidirectional Valve Operation

3.3.3 Power Tree Test Result

The following power tree tests were conducted:

- Efficiency
  - LM5122
  - LMR33630

  - DRV8323RS's Integrated Buck
  - TPS62840
- Thermal distribution imaging

Efficiency

The efficiency plots for the LM5122, LMR33630, DRV8323RS, and TPS62840 devices are shown from 図 3-23 to 図 3-26, respectively.

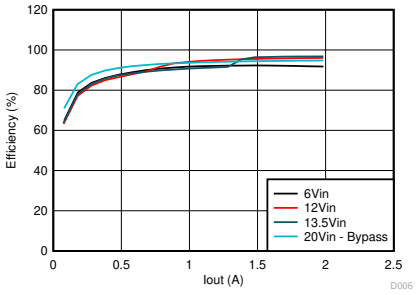


図 3-23. LM5122 Efficiency, Vout = 14 V

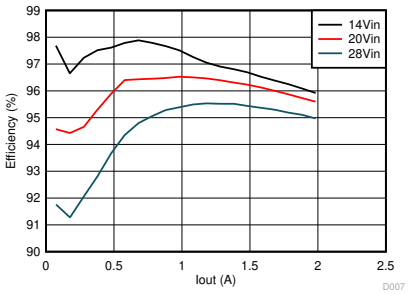


図 3-24. LMR33630 Efficiency, Vout = 12 V

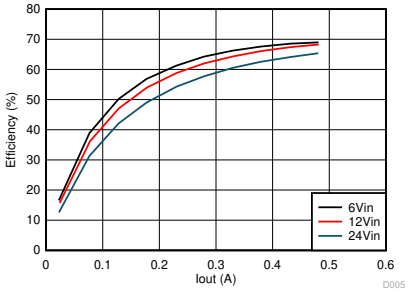


図 3-25. DRV8323RS Integrated Buck Efficiency, Vout = 4 V

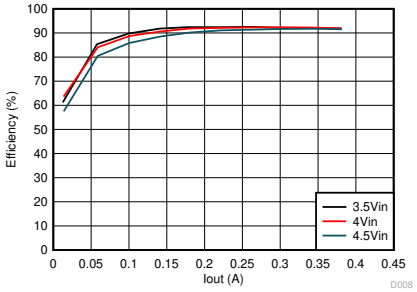


図 3-26. TPS62840 Efficiency, Vout = 3.3 V

Thermal Distribution Imaging

The condition for the thermal image in 図 3-27:

- Vin = 12 V
- Pin = ~4.5 W
- BLDC motor inactive
- DRV8847 cycling 42 ms

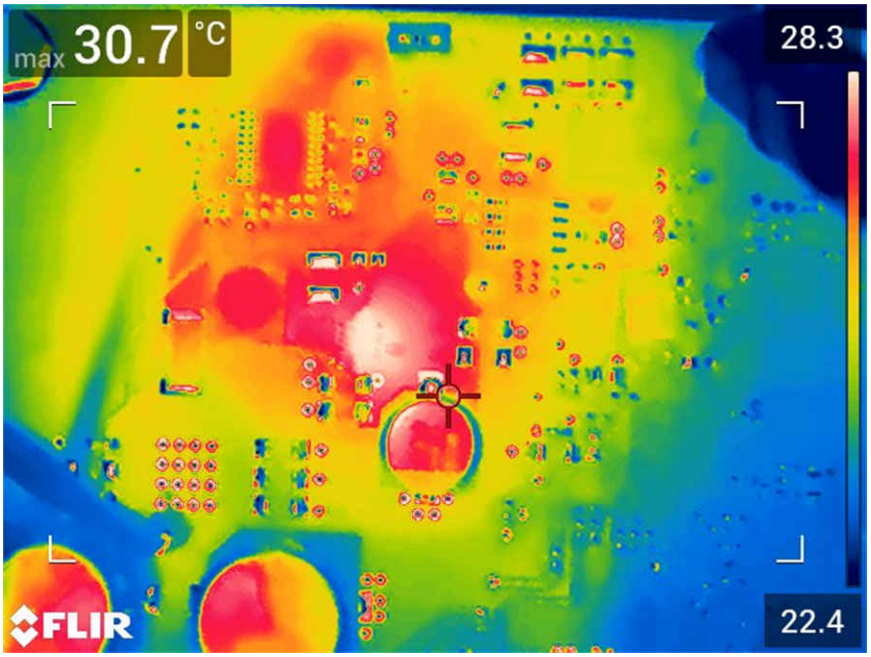


図 3-27. Thermal image for 4.5-W input

The condition for the thermal image in 図 3-28:

- Vin = 12 V
- Pin = ~6 W
- BLDC motor at 2 kRPM
- DRV8847 cycling 800 ms

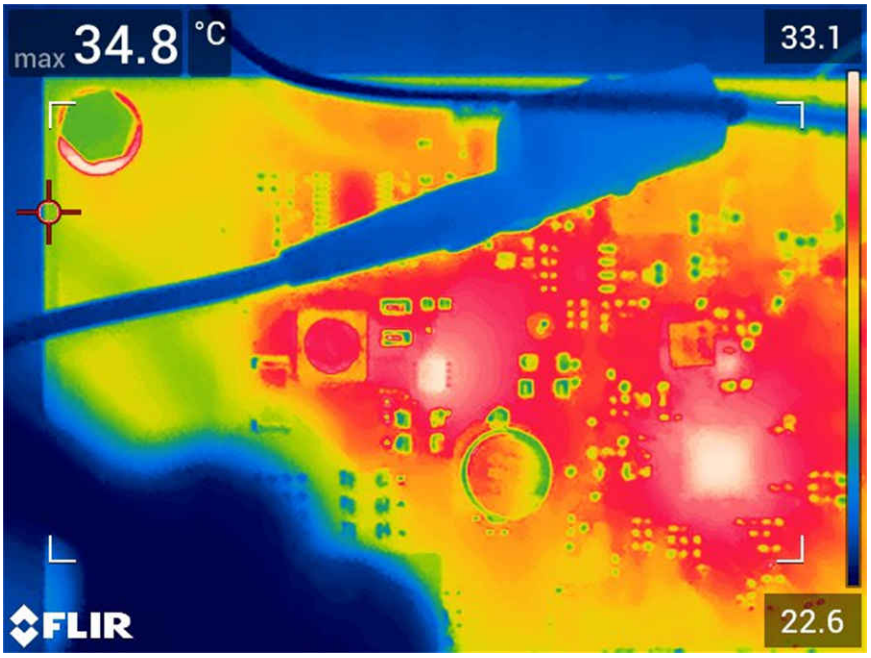


図 3-28. Thermal image for 6-W input

3.3.4 Key Test Summary

Both the Wonsmart and Boreasa motors under test were able to achieve an acceleration of 120 kRPM/s (10 kRPM to 40 kRPM in 250 ms) and a deceleration of 150 kRPM/s (40 kRPM to 10 kRPM in 200 ms). The results were only limited by the motor maximum current ratings and other motor specific speed characteristics. The hardware is capable of supporting up to 200 kRPM/s for motors capable of higher current limits and speeds. The valve driver's turn-on and turn-off times were less than 400 ns, which is faster than the typical application requirement of 5 ms.

This reference design shows how to adapt InstaSPIN-FOC to enable high-speed motor control using TI provided software. This is done by using the special capabilities of the C2000 processor family for advanced system debug capability. This can supplement the simulation effort of the engineers to not need to develop the perfect simulation tool for the system, but simply use the actual hardware to debug the control algorithm issue. This removes the need to build complex simulation algorithms to define specific motor or PCB parasitic effects to the system. The C2000 device can run a full FOC, sensorless, speed, and current closed loop control system up to 1.2 kHz electrically or higher, using TI provided software (for example, MotorWare).

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010072.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010072.

4.2 Documentation Support

1. Texas Instruments, DRV8323R, 65-V max 3-phase smart gate driver with buck regulator and current shunt amplifiers
2. Texas Instruments, LAUNCHXL-F28027F, C2000 Piccolo MCU F28027F LaunchPad™ development kit
3. Texas Instruments, BOOSTXL-DRV8323RS, DRV8323RS Three-Phase Smart Gate Driver With Buck, Shunt Amps (SPI Interface) Evaluation Module
4. Texas Instruments, Sensorless High-Speed FOC Reference Design for Drone ESC
5. Texas Instruments, InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide
6. Texas Instruments, Basic Calculation of a Boost Converter's Power Stage
7. Texas Instruments, Basic Calculation of a Buck Converter's Power Stage
8. Texas Instruments, Reducing Converter Stresses
9. Texas Instruments, MOSFET power losses and how they affect power-supply efficiency
10. Texas Instruments, Compensating the Current-Mode-Controlled Boost Converter
11. Texas Instruments, How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors

4.3 サポート・リソース

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4.4 Trademarks

5 About the Author

KELVIN LE is a systems engineer at Texas Instruments, where he is responsible for developing system solutions for the Medical sector. Kelvin has been with TI since 2015. Kelvin earned his Bachelor of Science in Biomedical Engineering from the University of Central Oklahoma and his Master of Science in Electrical and Computer Engineering from the University of Texas at Austin.

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