参考資料

Design Guide: TIDA-010249

4 チャネルの同期 IEPE 振動センサ・インターフェイスのリファレンス・デザイン

概要

このリファレンス・デザインでは、同期 4 チャネル広帯域高分解能インターフェイスの理論、設計、テストについて説明します。主なターゲット・アプリケーションは振動検出アプリケーションですが、力率測定における 3 相電圧および電流監視など、広帯域を必要とするあらゆるアプリケーションにもこの設計を適用できます。

リソース

TIDA-010249	デザイン・フォルダ
ADS127L11	プロダクト・フォルダ
THS4551	プロダクト・フォルダ
OPA2320	プロダクト・フォルダ
REF6041	プロダクト・フォルダ
OPA4187	プロダクト・フォルダ
TLV431B-Q1	プロダクト・フォルダ

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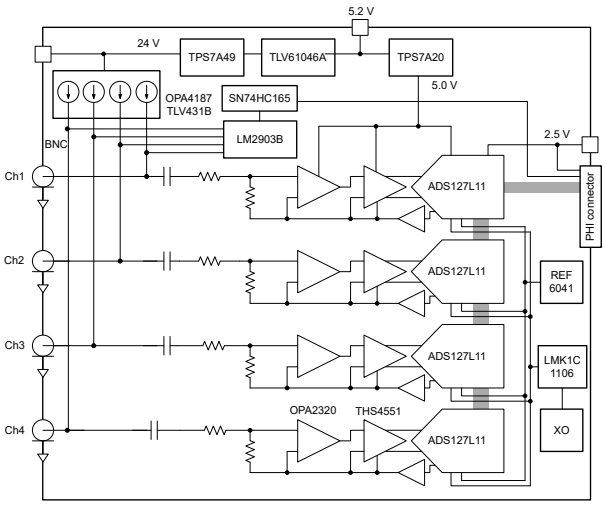
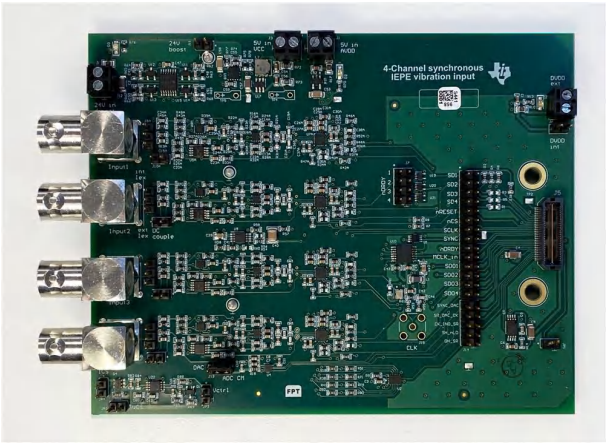
特長

- 同期 4 チャネル、広帯域の統合型電子圧電性 (IEPE) センサ・インターフェイス
- 24 ビット、20kHz の帯域幅変換
- データ・レート: 124kSPS (デイジー・チェーン)、400kSPS (パラレル SPI)
- ±10V AC 入力、320kΩ 入力インピーダンス
- オンボードの 4 つの励起電流 (3.5mA)
- オンボードの非絶縁型での 5V から 24V への昇圧
- 断線と短絡の検出

アプリケーション

- 状況監視モジュール
- スペシャル・ファンクション・モジュール
- データ・アクイジション (DAQ)





1 System Description

This design features four-channel high sampling rate (up to 400 kSPS), wideband, 24-bit resolution, high dynamic range design. The four channels are simultaneously sampled which is required in case of sampling a multi-axis vibration sensor, or in other applications such as power monitoring. Assembly options are used to support both daisy-chain and parallel SPI connections.

1.1 Key System Specification

This reference design is intended for high-end multichannel wideband high-resolution, high-sampling-rate interfaces. Four channels are demonstrating the concept that can be extended to 6 or more channels. The standard IEPE sensors require excitation current > 2 mA and excitation voltage > 22 V and bandwidth > 15 kHz for most applications. The design supports two SPI communication modes:

1. Daisy-chain mode, which enables all ADC devices to connect to a single SPI channel, minimizing the control lines and isolation signals, if applied
2. Parallel mode, which enables the ADCs to run at their maximum data rate but requires a separate data output line per ADC

The low-power consumption enables the design to be used in battery-powered monitoring systems. Wire-break and short-circuit detection is designed for safe and reliable operation of the sensor interface.

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	4
Input signal	±10 V, single-ended
Coupling	AC coupled
Excitation voltage	23 V (minimum)
Excitation current	3.5 mA
Resolution	24 bits
Bandwidth	0.6 Hz to 20 kHz
Data rate	124 kSPS per channel wideband filter, daisy chain SPI 400 kSPS per channel wideband filter, parallel SPI 1000 kSPS per channel sinc filter, parallel SPI
Target SNR	> 100 dB
Gain	0.4 V/V
Sampling clock frequency	16 MHz
SPI clock frequency	16 MHz
Input impedance	> 250 kΩ
Power consumption	< 1 W
Operating temperature	–40°C to 125°C
Diagnostic features	Wire-break and short circuit

2 System Overview

2.1 Block Diagram

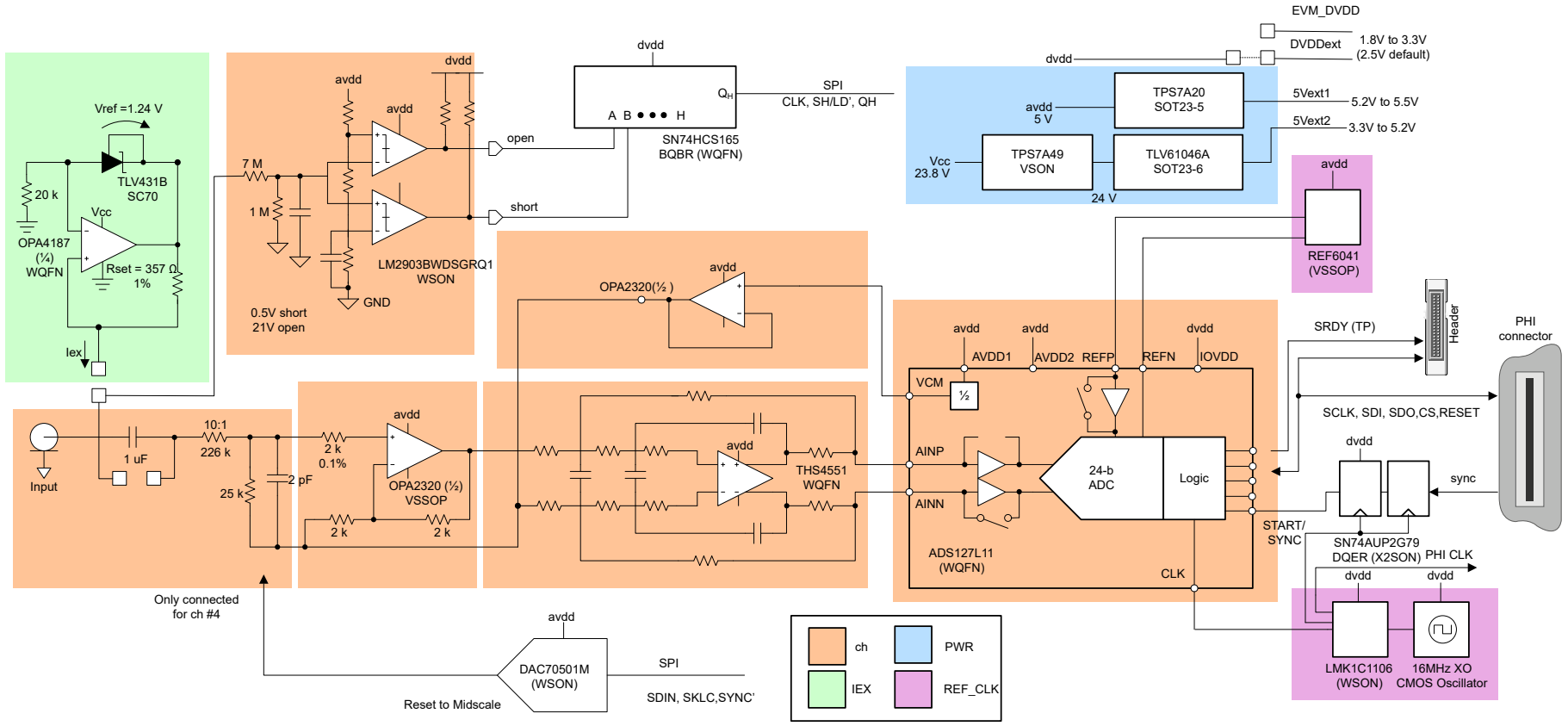


図 2-1. TIDA-010249 Block Diagram

2.2 Design Considerations

2.2.1 Signal-Chain Voltage Levels

According to the target specifications, the input signal can be as high as 23 V. With AC coupling, the maximum signal level is ±10 V, to enable a 5-V signal chain, a resistive divider follows the coupling capacitor, with a scaling factor of 10:1. This brings down the signal to ±1.0 V. The resistive divider is referred to the mid-supply of 2.5 V generated by the ADC to perform level shifting, the output signal becomes 2.5 V ±1.0 V after the shifting. The non-inverting buffer stage has a gain of 2, so the output of the buffer is ±2.0 V. The buffer inverting pin is also referred to the mid-supply of 2.5 V, so the output of the buffer is 2.5 V ±2.0 V.

The fully-differential amplifier converts the single-ended signal into a differential signal and adds a gain of 2. The output common-mode of the differential amplifier is also set to 2.5 V. The maximum differential output of the amplifier is therefore ±4.0 V, while the single-ended outputs are 2.5 V ±2.0 V.

A reference voltage of 4.096 V is used to maximize the DR. With the previously-given signal levels, the proper amplifier devices can be selected that have the required input and output range, and have the least noise contribution.

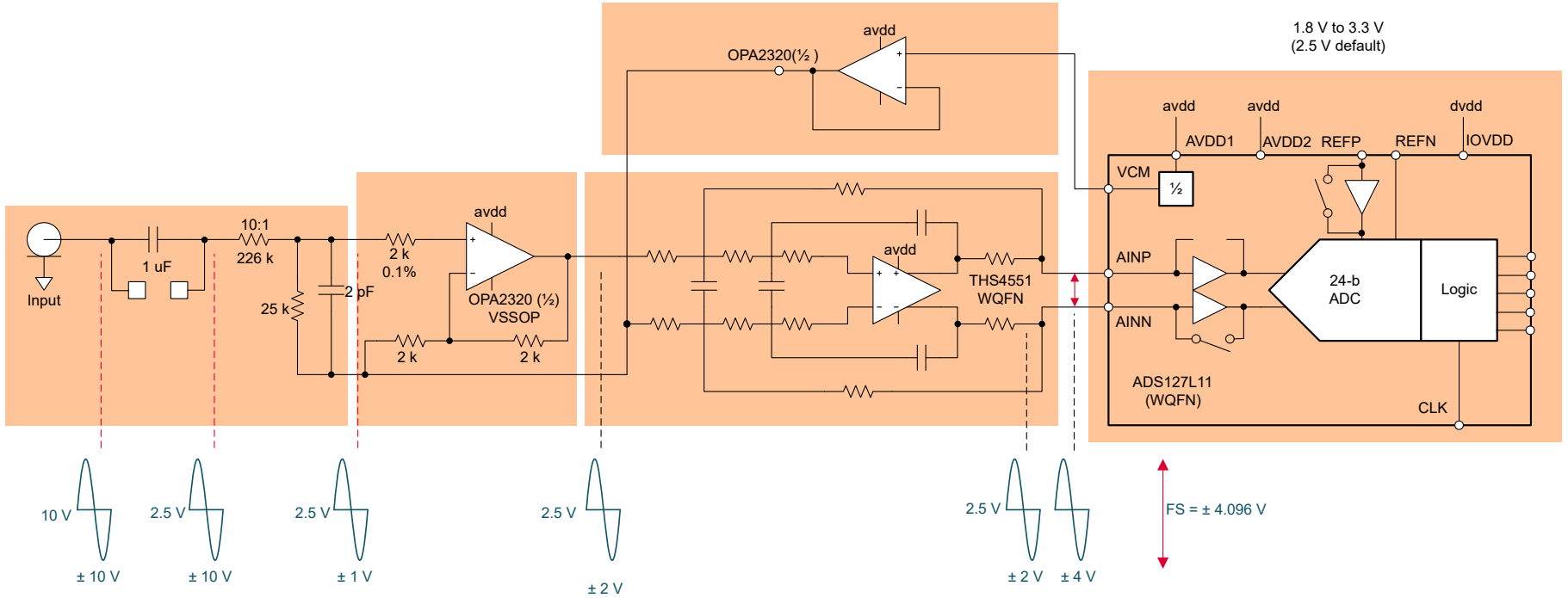


図 2-2. Signal-Chain Voltage Levels

2.2.2 ADC Configuration

As mentioned in the previous section, a 4-V reference is to be used with the ADS127L11 to maximize the dynamic range. A 16-MHz oscillator clock is also selected as clock reference to the ADC as well as an SPI clock. The ADC can run with clocks up to 25 MHz.

To get the best performance out of the signal-chain, the ADS127L11 ADC has to be configured properly. The following list shows the required settings:

- Data Width (resolution) = 24 bits
- Speed Mode= High Speed
- Filter Type= Wide Bandwidth
- INP_RNG= VREF
- REF_RNG= High-reference range
- VCM=Enabled
- AINP_BUF, AINN_BUF=Enabled
- CLK_SEL=External

The ADC can be used either in daisy chain or in parallel SDO modes. 式 1 shows the maximum data rate for daisy-chain mode.

$$\text{Maximum data rate} = \text{SPI Clk} / (\text{devices in the chain} \times \text{bit per frame}) \quad (1)$$

For a 16-MHz SPI clock, 4 devices, and 32b per frame, the maximum data rate is 125 kSPS. To get the output data rate to 125 kSPS, set the OSR=64.

For parallel SDO mode and using the wideband filter, the data rate can be set to a maximum of 400 kSPS. With a 16-MHz clock, only OSR = 64 is possible, and that gives an output data rate of 250 kSPS. To achieve 400 kSPS, replace the onboard 16-MHz oscillator with a 25-MHz oscillator.

For more details about the daisy-chain and parallel connections, see the *ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC* data sheet and *ADS127L11 in Simultaneous-Sampling Systems* application brief.

2.2.3 ADC Clocking and Synchronization

Synchronization of multiple ADS127L11 devices is essential for this design. Two factors are required to maintain full synchronicity. The reference clock used for all ADCs need to be identical, and the START signal for all ADCs have to be identical and synchronized with the ADC reference clock.

For the reference clock, to verify the minimum skew between different clock inputs, the oscillator is buffered through the LMK1C1106, which is a very low-jitter, 6-channel buffer. Four channels are routed to the four ADCs, one output is sent back to the controller, and the sixth output is used for synchronizing the START signal as explained in this section. On the top of the low-jitter buffering, special care is taken to route the four clock signals to the four ADCs with identical trace length and delays on the PCB.

For the START signal, a small logic synchronizer circuit is used to align the START signal with the ADC reference clock, to make sure all ADCs are receiving the START signal on the same time with regard to the reference clock and avoiding one clock cycle of uncertainty.

For more details about the synchronization see the *ADS127L11 in Simultaneous-Sampling Systems* application brief.

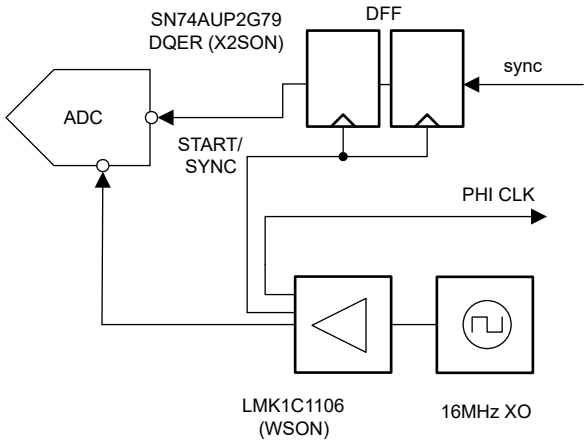


図 2-3. ADC Synchronization Circuit

2.2.4 Differential Low-Pass Filter

The THS4551 stage acts as a single-ended to differential converter with a gain of two to drive the ADC, on top of that the device also acts as a low-pass filter to limit the input bandwidth to 20 kHz. This helps improve the SNR by suppressing the noise signal on the unwanted band.

For details about the differential stage, see the *IEPE Vibration Sensor Interface Reference Design for PLC Analog Input* design guide.

2.2.5 Current Source

IEPE sensors need an excitation current in the range of 2 mA to 20 mA to operate, based on the connecting cable length, and the load capacitance. In most IEPE applications, a static 2–4 mA is sufficient to operate the sensor. The accuracy of the current source is not critical but the compliance range, current noise, and load regulation are important for the interface performance.

For this design, a static 3.5-mA current source is developed using a low-voltage shunt reference and an op amp. Low voltage reference provides low headroom and higher compliance range. A cost-effective design is achieved using a quad op-amp OPA4187 package.

For more details about the current source design, see the *High-side current sources for industrial applications* Analog Design Journal article.

Since this application runs from a 5-V source, a booster stage is required to generate the high voltage for the current source. A TLV61046A compact boosting stage is used followed by the TPS7A49 LDO to generate a clean 23.8 V for the current sources. The current source has about 1.5-V headroom, leaving a compliance range up to 22 V.

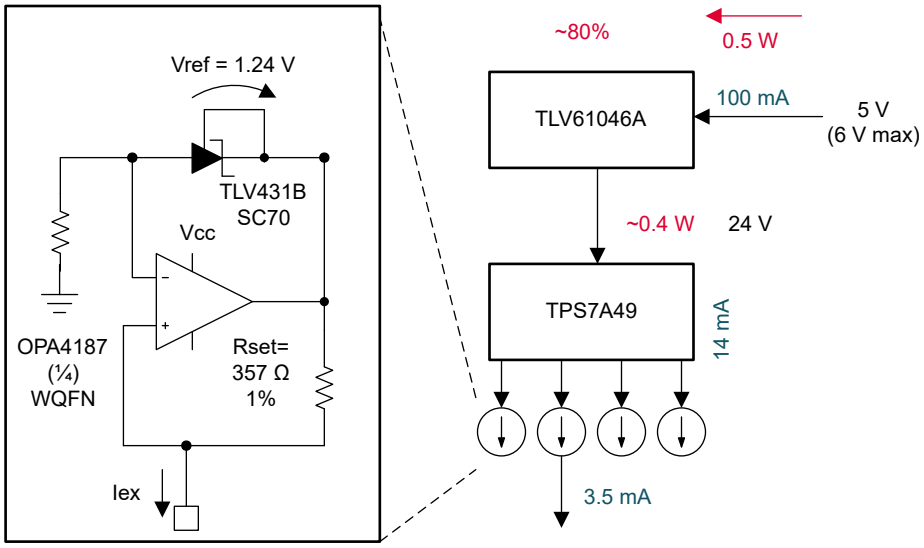


図 2-4. Current Source and Booster Stage

2.2.6 Gain Stage and High-Pass Filter

The sensor is connected to the signal chain through a capacitor followed by a series resistor forming a high-pass filter, which has a cutoff of less than 1 Hz.

The resistor is forming a potential divider with a gain 10 to 1, reducing the input signal of ±10 V to ±1 V.

The resistor is referenced to mid-scale (2.5 V) instead of to ground to shift the signal.

A non-inverting gain stage is buffering and amplifying the signal to ±2 V + 2.5 V at the input of the fully-differential amplifier stage.

The dual op amp OPA2320 device is used for gain stage, and common-mode buffer. An op amp with an output swing reaching to 0.5 V from supplies is needed for that stage. A linear amplifier that does not suffer from crossover distortion is essential for good THD performance.

2.3 Highlighted Products

2.3.1 ADS127L11

The ADS127L11 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with data rates up to 400 kSPS using the wideband filter and up to 1067 kSPS using the low-latency filter. The device offers an excellent combination of AC performance and DC precision with low power consumption (18.6 mW in high-speed mode).

The device integrates input and reference buffers to reduce signal loading. The low-drift modulator achieves excellent DC precision with low in-band noise for outstanding ac performance. The power-scalable architecture provides two speed modes to optimize data rate, resolution, and power consumption.

The digital filter is configurable for wideband or low-latency operation, allowing wideband AC performance or data throughput for DC signals to be optimized, all in one device.

The serial interface features daisy-chain capability to reduce the SPI I/O over an isolation barrier. Input and output data and register settings are validated by a cyclic-redundancy check (CRC) feature to enhance operational reliability.

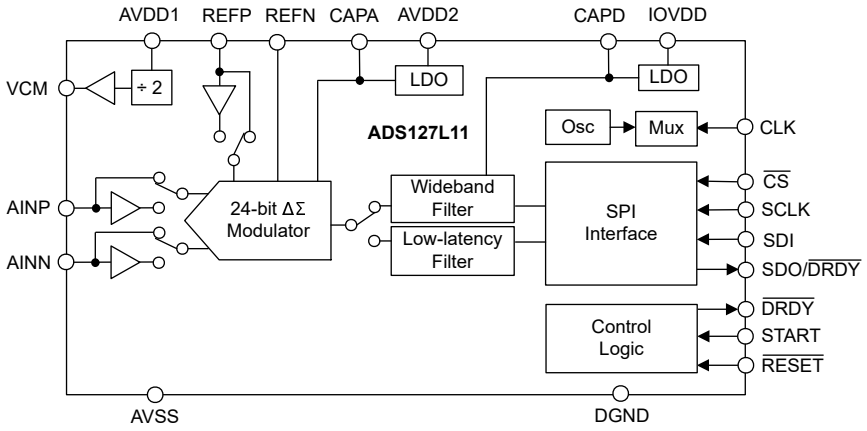


図 2-5. ADS127L11 Block Diagram

2.3.2 THS4551

The THS4551 fully-differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision analog-to-digital converters (ADCs). Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is an excellent choice for data acquisition systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging 16- to 20-bit successive-approximation register (SAR) input requirements. A wide-range output common-mode control supports the ADC running from 1.8-V to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

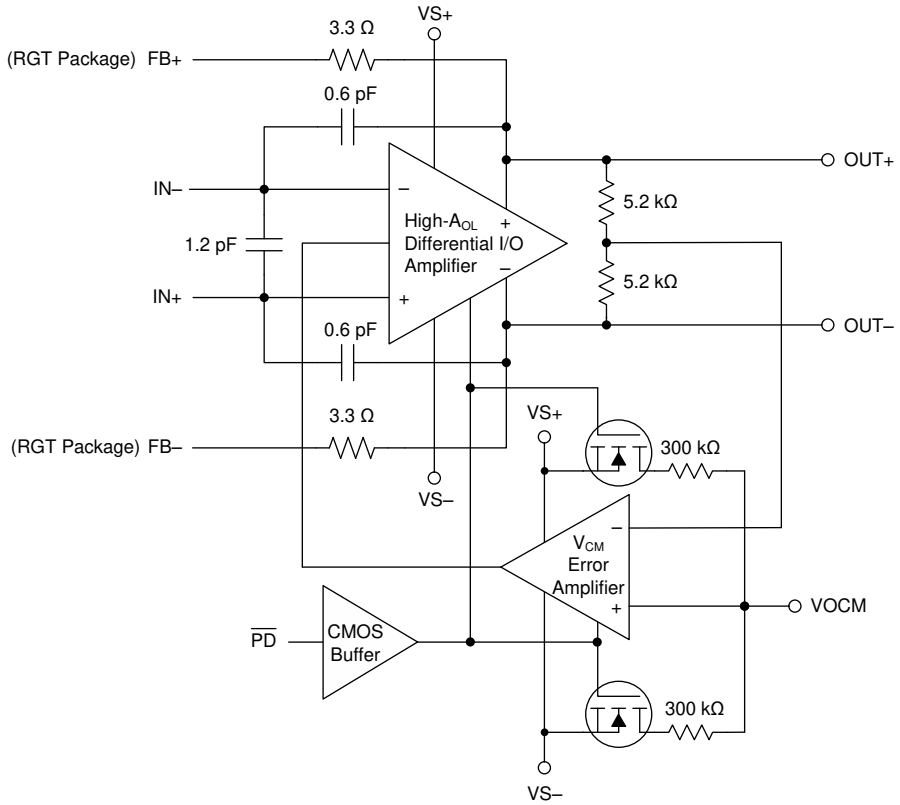


図 2-6. THS4551 Block Diagram

3 System Design Theory

3.1 IEPE Sensor

The integrated electronic piezoelectric (IEPE) sensor is a piezoelectric vibration transducer with integrated charge amplifier and impedance converter (see 図 3-1). Integrating the amplifier close to the sensor greatly reduces the sensor noise. One major advantage of the IEPE sensor is that the sensor is interchangeable.

The IEPE sensor is also commercially known as an Integrated Circuit Piezoelectric (ICP®), Constant Current Line Drive (CCLD), Isotron®, DeltaTron®, and Piezotron®.

Uniaxial, biaxial, and triaxial IEPE accelerometers are available in the market typically with a two-wire connector per axis. Sensors with an output proportional to acceleration is more common (accelerometer), although a velocity-proportional output is also available.

Constant current is applied to the two-wire connection from which the IEPE sensor is drawing power and establishing a constant DC offset around 10 V. A vibration-sensing value is superimposed of this DC signal at the output of the sensor, which is typically AC-coupled to the sensor interface circuit.

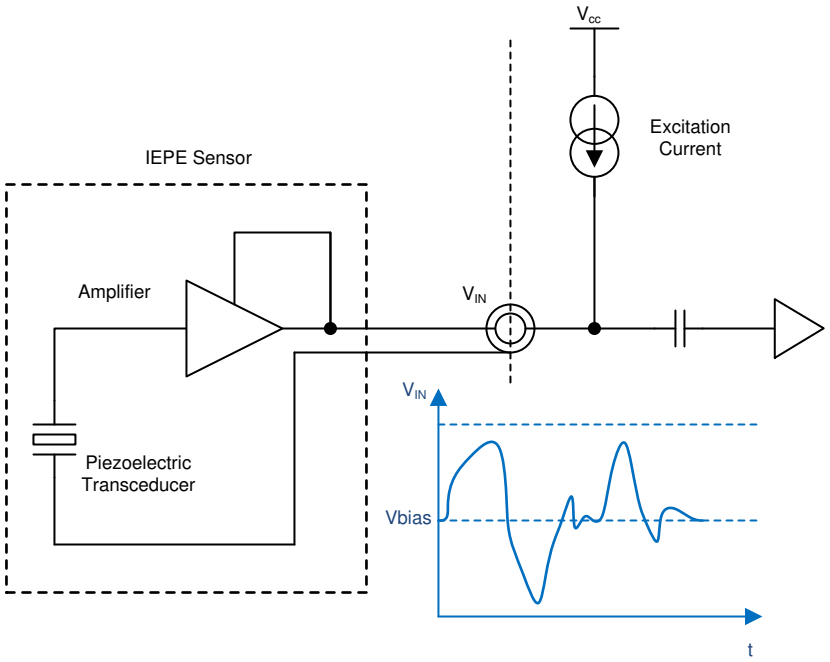


図 3-1. IEPE Sensor Conceptual Circuit

3.1.1 IEPE Sensor Parameters

IEPE accelerometer sensors are available with a wide range of performance parameters for different applications. Understanding those parameters and their relation to the sensor interface circuit performance is important. The following subsections describe these parameters and addresses their relevance.

3.1.1.1 Sensitivity and Measurement Range

Sensitivity is the output voltage change corresponding to a specific mechanical acceleration input. This parameter is commonly measured in *mV/g*, where g is the gravity of earth. Accelerometer data sheets typically report a single nominal sensitivity value. However, note that sensitivity changes with temperature, input frequency, and input acceleration level, which is why sensitivity tolerance is also stated in the sensor data sheet.

IEPE accelerometer sensitivity falls in the range of tens of mV/g to a few thousands of mV/g, with a tolerance of 5% or 10%.

The measurement range is the minimum and maximum of acceleration inputs that can be converted by the sensor to a voltage output without saturation or clipping, which is what determines the maximum output voltage (see 式 2).

$$\text{Output Voltage Range} = \text{Measurement Range} \times \text{Sensitivity} \quad (2)$$

For a measurement range of 10 g and sensitivity of 100 mV/g, the output range is ±5 V. The sensor output voltage range is typically 5 V or 10 V, maximum.

3.1.1.2 Excitation, Output Bias Voltage, and Output Impedance

As previously mentioned, the output voltage of the IEPE sensor can be as large as ±10 V. To avoid the requirement of a dual supply, the AC output of the IEPE sensor is shifted with a certain constant voltage called *output bias voltage*, which is typically in the range of 9 V to 12 V. Having the AC signal superimposed on the DC output bias voltage dictates a minimum compliance voltage from the current source supplying the sensor not to have signal clipping. This compliance voltage is also called *excitation voltage*. Excitation voltage is simply the maximum possible output bias voltage added to the maximum AC voltage output.

$$\text{Excitation Voltage}_{MIN} = \text{Bias Voltage}_{MAX} + \text{Sensitivity}_{MAX} \times \text{Input}_{MAX} \quad (3)$$

A value of 18 V to 22 V is typical for excitation voltage. An upper maximum also exists for the excitation voltage that must not be exceeded to avoid damaging the sensor electronics.

Output impedance is the effective AC output impedance seen by the interface circuit. Typical values are 300 Ω down to below 100 Ω. A lower impedance means less error in measurement when considering the finite input impedance of the interface circuit.

3.1.1.3 Linearity and Temperature Variance

As previously mentioned, sensitivity varies with input level and temperature.

Variation with input level is measured by the linearity (or non-linearity) of the sensor. Temperature variation is also measured by using the sensitivity deviation from the nominal sensitivity over the operating temperature range. The operating temperature range extends from 120°C to 280°C.

Both linearity and temperature variance are expressed as a percentage of the full-scale input range. A 10-g range sensor with a nominal sensitivity of 100 mV/g and 1% linearity has a maximum error of 0.1 g for the voltage reading.

3.1.1.4 Frequency Response

The sensitivity of the sensor changes with the frequency of the acceleration excitation. The sensitivity is generally considered as being constant over a certain frequency range as defined by the minimum and maximum 3-dB frequencies. Beyond the maximum frequency, the sensor has a mechanical resonance frequency that must be avoided in an application. The usual frequency range is sub-Hz to 10 kHz, 20 kHz, or 30 kHz. The sensor interface circuit must have the same bandwidth of the targeted sensor and the ADC converter sampling frequency must be more than twice this bandwidth.

Note that the designer can extend the frequency range for some sensors by increasing the excitation current. For this reason, a variable current source is required for a versatile IEPE sensor interface circuit.

3.1.1.5 Noise and Dynamic Range

The IEPE sensor has intrinsic mechanical and electrical noise, which must be considered if detecting low-level signals. Output noise is represented as root-mean square (RMS) noise voltage.

This ratio of the maximum output range to the noise level constitutes the effective dynamic range of the sensor.

4 Hardware, Software, Testing, and Test Results

4.1 Hardware Description

図 4-1 shows a top view of the reference design PCB, indicating different circuit blocks from the TIDA-010249 Block Diagram.

図 4-1. PCB Layout

4.1.1 Board Interface

図 4-2 shows various connectors and jumpers used to interface with the design PCB.

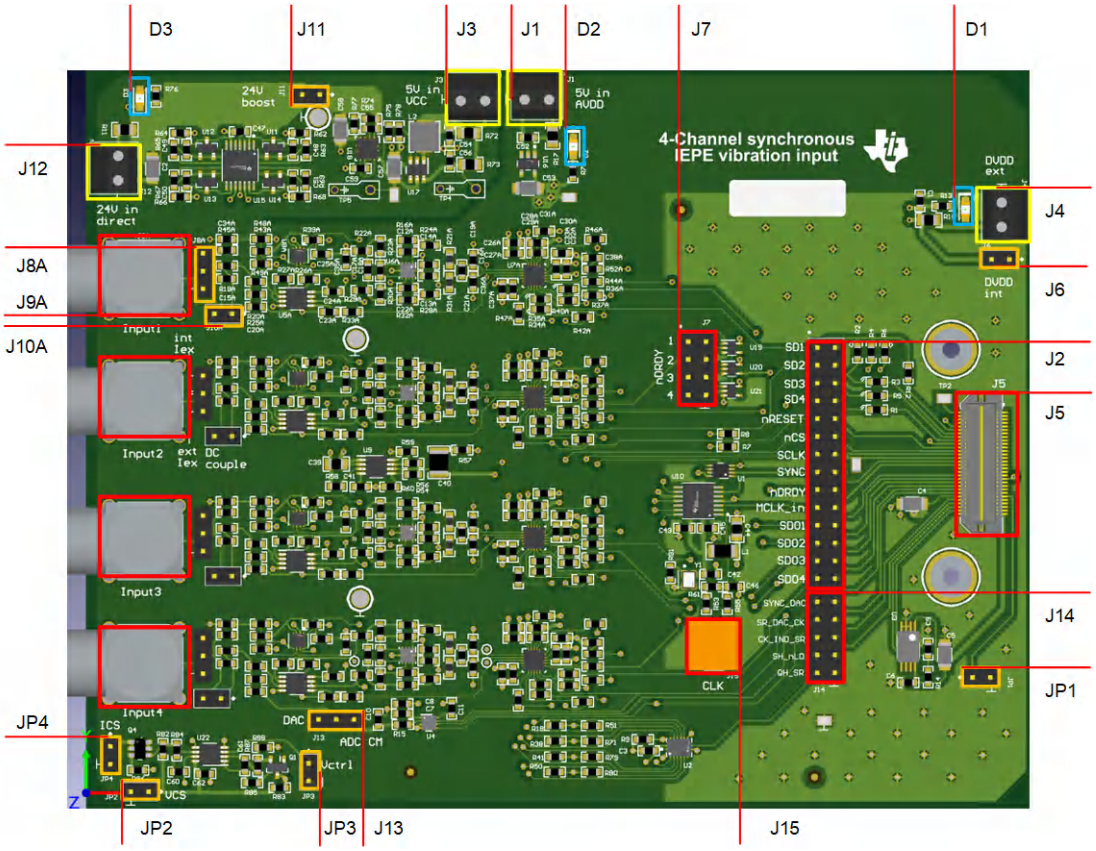


図 4-2. PCB Interface

表 4-1. Board Connectors and Headers

CONNECTOR	DESCRIPTION
J9A…J9D	Ch1 to Ch4 sensor input (BNC connector, with shield grounded)
J8A…J8D	Ch1 to Ch4 excitation current source selector Short (3,2) top and middle, to use onboard current source (make sure it is powered) Connect external current source (2,1) middle and bottom, to use external current source Leave open to evaluate the channel without excitation current (no sensor is connected)
J10A…J10D	Ch1 to Ch4 coupling selection Short: DC coupling, use for Ch4 in case of DC coupling, other channels for testing Open: AC coupling, default configuration
J5	QHS connector connect to PHI, best practice is to power the board before connection
J2	SPI signals header, use for debugging and probing, or to connect to another board (if no QHS)
J14	DAC and SR signals header, use for driving (no QHS) or monitoring auxiliary signals
J7	nRDY signal header, use for checking the synchronization between ADCs
J15	SMA connector for Clk, based on the assembly can be used either as clock input (crystal is removed), or as a clock output
JP1	Used for EEPROM programming if needed. Not used for the PHI board
J12	External supply for excitation current, if used, make sure J11 is open, D3 indicates active supply
J11	Short to use onboard booster supply for excitation current, make sure J12 is open
J3	Input supply for onboard booster stage, valid input range is 1.8 V to 5.5 V, typically use 5.2 V
J1	Input supply for onboard LDO generating 5 V, valid input range is 5.2 V to 6 V, use 5.2 V

表 4-1. Board Connectors and Headers (continued)

CONNECTOR	DESCRIPTION
J4	External digital supply, recommended to use 2.5 V. When used make sure J6 is open and that the MCU or controller connected is 2.5-V compatible.
J6	Short to use PHI digital supply (make sure 2.5 V, and J4 is open), open if external supply is to be used
J13	DAC connection short (1,2, right) to use ADC CM (2.5 V) as input attenuator common-mode short (2,3, left) to use DAC as common-mode source for the attenuator use pin1 to monitor ADC CM, pin3 to monitor, use DAC output, pin2 to connect external source
JP3	Control connection for variable current source, connect J13, pin3 to use the DAC
JP2	Supply connection for the variable current source (note ground sign)
JP4	Output connection for variable current source, connect to J8x(1,2) to use as channel I_{SOURCE}

4.1.2 Power Configuration

The board has three different main supplies: digital supply, analog supply, and excitation current supply. Analog supply requires external source. Digital and excitation current supplies can be connected directly to external sources, or use onboard stages.

The following sections describe jumper settings to run in various configurations.

4.1.2.1 Power Sequence

To avoid damage to the devices, please follow the following sequence when powering the board:

- Connect the analog supply (D2 on)
- Connect the digital supply (D1 on) either externally, or by turning the PHI board on
- Connect the excitation current supply (D3 on)

Observe the absolute maximum ratings for all supply inputs.

4.1.2.2 Analog Supply

The board relies on an onboard LDO to supply the required 5 V to the analog circuits. The input source is connected to J1, and try valid input range is 5.2 V to 6 V (5.1 V can also be tried)

D2 turns on if the supply is active.

The estimated current from the analog supply is below 100 mA.

4.1.2.3 Digital Supply

The board can run from 2.5-V up to 3.3-V digital supply (a 1.8-V supply also works with the diagnostic features unavailable, D1 does not turn on in that case). Use 2.5 V for signal integrity, EMC, and power consumption reasons.

The board is designed to use the PHI digital supply by default when connected. In that mode:

- PHI is connected to J5 and powered, the best practice is to power the analog supply before that
- J6 is shorted, J4 is left unconnected

Digital power supply at different speeds of ADC can be measured by attaching an ammeter on J6 instead of short.

If the external power supply is used:

- Make sure J6 is open if PHI is connected to J5
- Make sure analog supply is connected and active (D2 on)
- Connect voltage source to J4, with maximum level of 3.3 V, recommended voltage is 2.5 V
- Make sure digital controller is compatible with the supply level provided

If power supply is active, D1 is on.

The estimated current from the digital supply is below 30 mA.

4.1.2.4 Excitation Current Supply

The onboard excitation current section requires high voltage to satisfy high compliance range. The board features an onboard booster stage that generates 24 V out of the input which can range from 1.8 V to 5.5 V, best practice is using the use of the same source of the analog LDO, 5.2 V.

To use the onboard booster:

- Make sure the analog supply is connected (D2 is on)
- Connect the external source (5.2 V) to J3
- Short J11, verify that J12 is unconnected, D3 turns on when the supply is active
- Current can be measured using an ammeter instead of the short on J11. The estimated current is about 16 mA. The voltage when measured at J11 is not exactly 24 V but is about 23.8 V due to LDO drop.

The estimated current from the 5.2-V analog supply of the booster is below 100 mA.

If external supply is used:

- Make sure the analog supply is connected
- Make sure J11 is open
- Connect the external high voltage source (8 V to 36 V, typical 24 V) to J12, D3 turns on

The estimated current from the high voltage external supply is 16 mA.

注

To measure the input and output ripples of the booster stage, use test points TP5, TP6.

4.1.2.5 SPI Connectivity Modes and Their Assembly Variants

4.1.2.5.1 Daisy-Chain Mode

In this mode, the four ADCs are connected in a daisy-chain fashion 図 4-3 shows. The maximum SPI clock rate in this mode is 16 MHz.

The following board assembly is required to enable the daisy-chain mode:

- R40x, R36x (all channels), remove R3, R5, and R1

注

図 4-3 shows that all of those resistors are indicated by small parallel lines on the top left corner of the resistor.

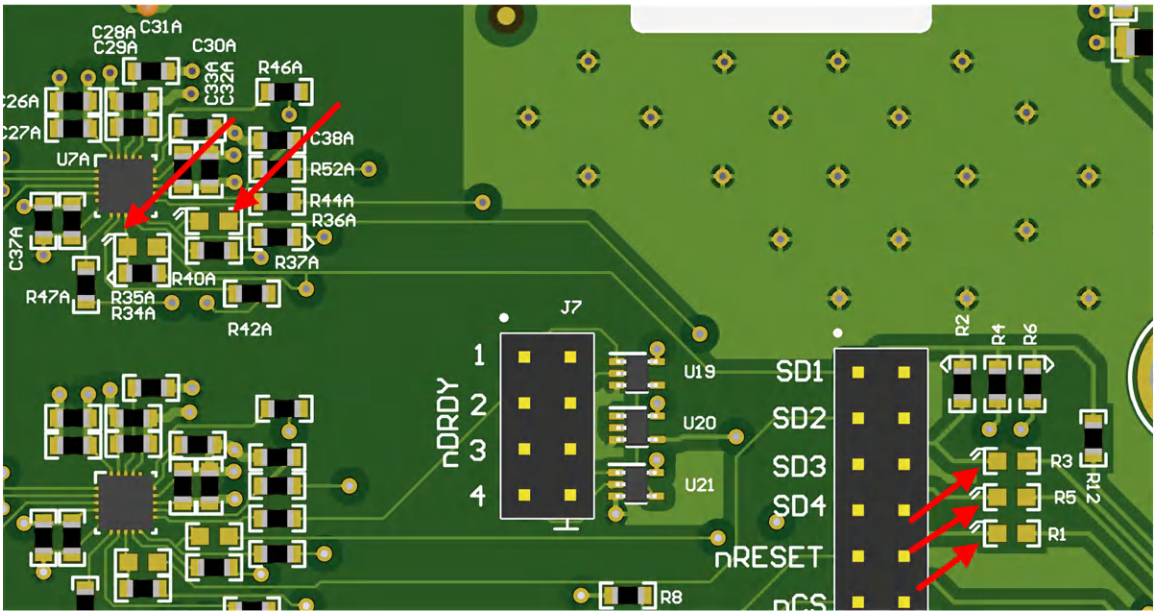


図 4-3. Daisy-Chain Variant

4.1.2.5.2 Parallel SDO Mode

In parallel SDO mode, the four ADCs are connected in parallel, with a single shared SDI input, and four parallel SDO outputs as 図 4-4 shows.

This mode reduces the signal lines required by the controller when high speed is needed but the ADC configuration is similar. The SPI clock can reach 25 MHz allowing data rates at 1 MSPS per channel.

The following board assembly is required to enable the parallel SDO mode:

- R35x, R37x (all channels), remove R3, R5, and R1

注

図 4-4 shows that R35x and R37x are indicated by a small triangle to indicate that the resistors are only used in daisy-chain.

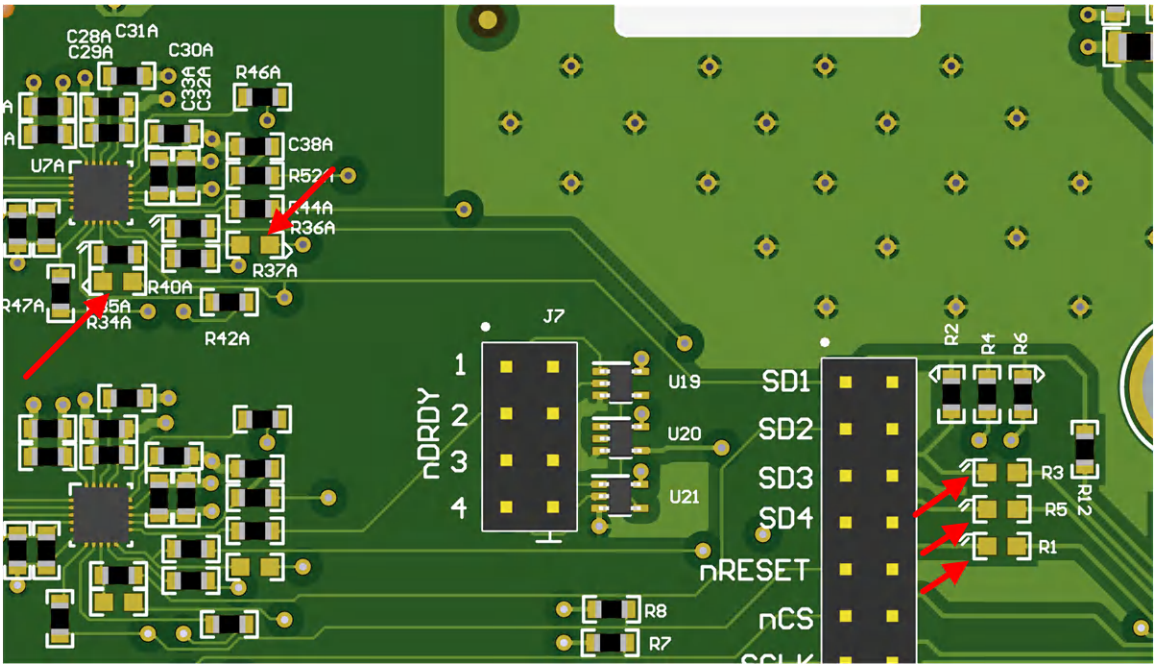


図 4-4. Parallel SDO Variant

4.1.2.5.3 Parallel SDI Mode and Parallel SDO Mode

In parallel SDI mode and parallel SDO mode, CS and SCLK are shared between all ADCs, and separate parallel SDI, SDO lines are used. This allows independent configuration of the ADCs.

The following board assembly is required to enable the parallel SDI and parallel SDO mode:

- R35x, R37x (all channels), remove R2, R4, R6

注

図 4-5 shows that all resistors with the small triangle (daisy) are removed, and all resistors with parallel lines are assembled.

注

The default assembly has a 16-MHz crystal. Using this crystal, parallel modes can only achieve a 600-kSPS data rate from the ADCs. To unlock the full speed of the ADCs, replace the 16 MHz with a 25-MHz crystal.

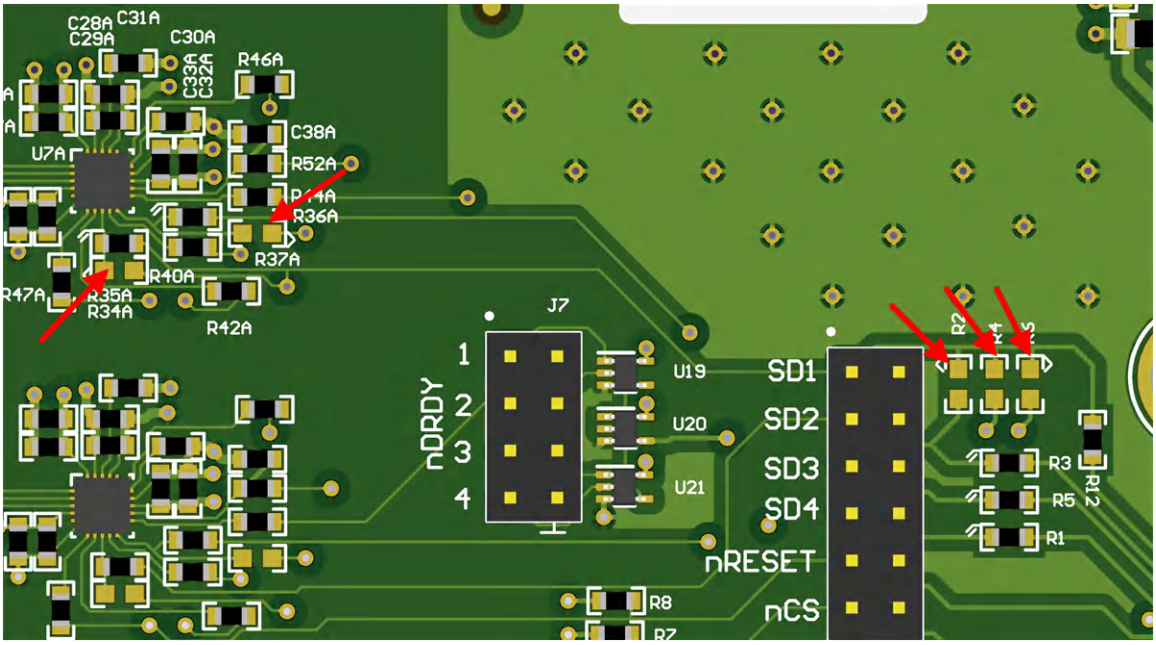


図 4-5. Parallel SDI Variant

4.1.2.5.4 Clocking Modes

The board supports 3 clocking modes as illustrated in 図 4-6:

1. Stand-alone mode: there is no clock line connection to other boards
2. Clock output mode: the onboard clock is connected to the SMA connector
3. External clock input mode: there is no onboard clock, the external clock is connected to the SMA connector

表 4-2 details the board configuration with a minor assembly variant in the clocking section.

表 4-2. Board Clocking Configurations

NO EXTERNAL CLOCK CONNECTIVITY	CLOCK OUTPUT MODE	EXTERNAL CLOCK INPUT MODE
J15 removed	R53 removed	Y1 removed, R55 removed

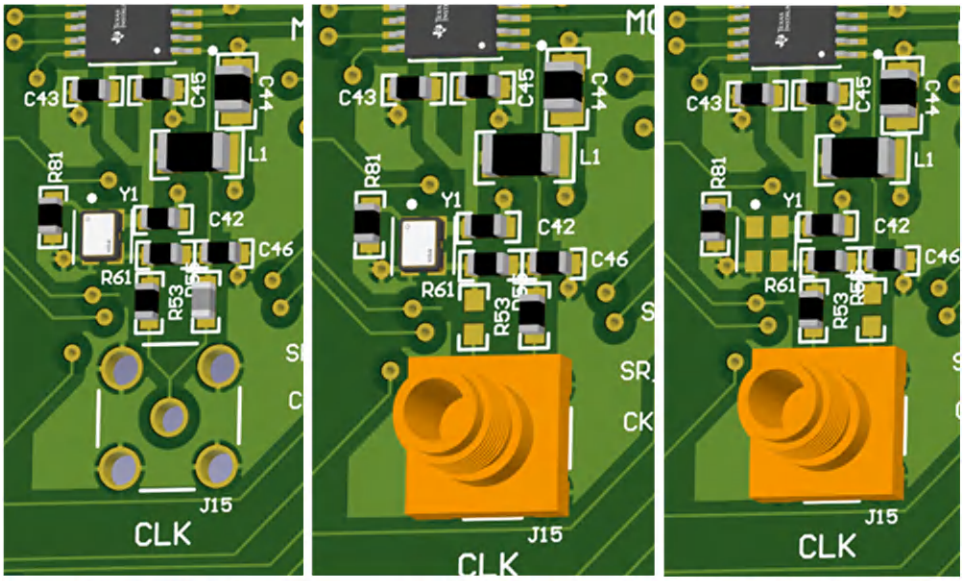


図 4-6. Clocking Assembly Variants

If synchronizing two boards, configure the first board in clock output mode, and configure the second board in external clock input mode. A short coaxial cable connects J15 on both boards, and both boards can be connected to the same controller. Use the controller to handle the difference in nRDY signal.

4.2 Software Requirements

This reference design is intended to be used with a dedicated software: *TIDA-010249 EVM Software* for windows shown in 図 4-7.

図 4-7. TIDA-010249 EVM Software User Interface

4.3 Test Setup and Procedure

Use the basic setup in 図 4-8 to evaluate the design PCB. The board is connected through a PHI board to a PC running the TIDA-010249 software.

The following components are required to run all tests:

- Reference design PCB (with the parallel or daisy-chain assembly configuration)
- 5.2-V power supply, set to a 300-mA limit
- PHI board
- PC running the reference design software
- Shunts, and various loads (100 Ω to 300 Ω, 0.25 W)
- Waveform generator (±10-V output, up to 100 Hz to 15 kHz), for THD measurement the generator must have very low distortion (< –100 dB), 16 MHz needs to be supported for clock rejection
- The PSI EVM is a good and affordable choice to generate a clean 2-kHz signal
- 4-channel analog scope (for the synchronicity test)
- For current source measurement: current source with current sink capability, and output up to 23 V
- For testing with a sensor, a standard IEPE sensor is required, with a shielded cable connected with PCB BNC input. Four sensors can be used for the 4-channel testing.
- For controlled testing with a sensor, use a sensor emulator which can be fed with a known signal to generate deterministic output

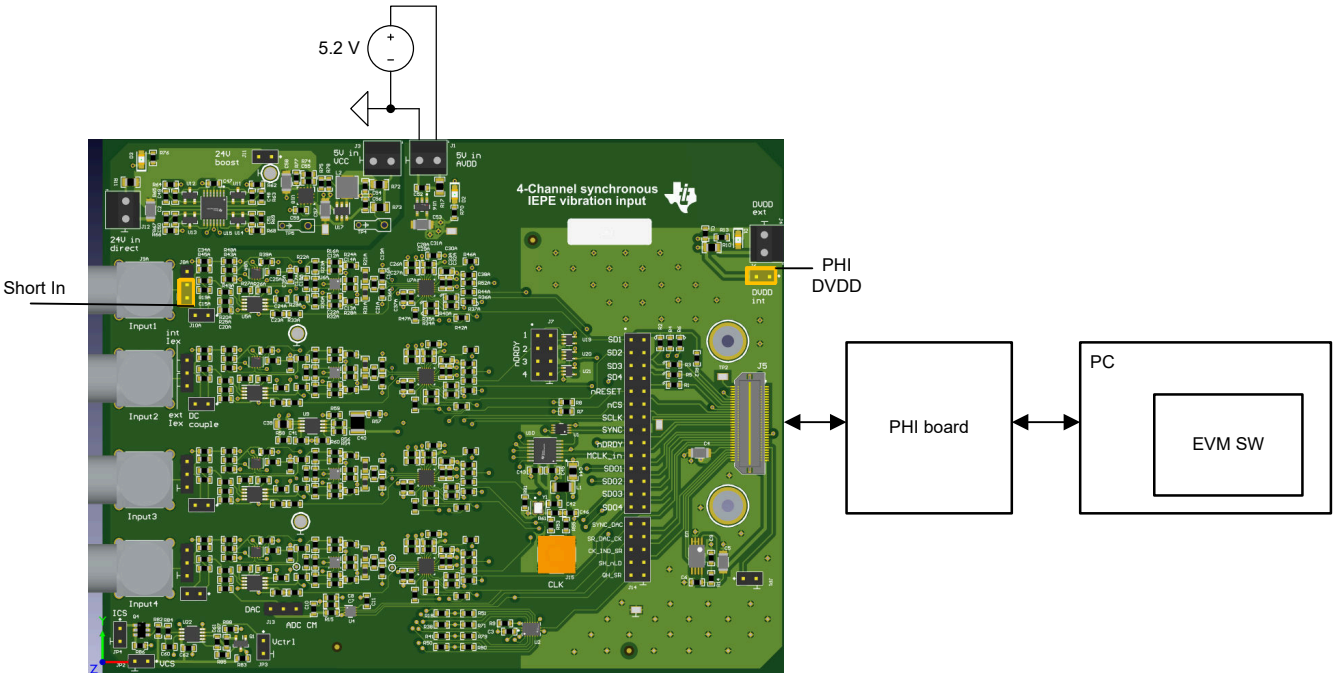


図 4-8. Basic Test Setup

4.3.1 Noise Floor and SNR

For evaluation of signal-chain without excitation current or actual sensors, use the following setup:

- Make sure that the board is in the specific SPI mode (for example, daisy chain) matching that of the software settings
- Channel input is set to AC couple (J10A = open), according to the need and input is shorted to ground (J8A, 2-3 = short)
- Analog supply connector J1 is connected to a 5.2-V supply (booster is off)
- J6 is shorted to use the PHI DVDD (by default, boards are set to 2.5-V digital supply)
- Turn the analog supply on, then connect the PHI board to USB
- Configure the software settings according to the required configuration (Vref = 4.096, OSR = 64, 16384 or 32768 sample)
- Capture the frame (it captures all channels)
- In the histogram or time view, record the peak-to-peak, standard deviation (sigma), and mean values, as well as the effective resolution
- Calculate the channel offset from mean, channel noise from std. deviation in µV (also check peak-to-peak value) and calculate the Dynamic Range of each channel (FS = 4V/RMS Vnoise).
- The previous steps can be repeated for different data rates (OSR) and multiple sample set.
- In the frequency domain view, spectrum is checked for any abnormal noise spikes or interference tones. A histogram view presents a random Gaussian distribution.
- Repeat the measurement with the booster device on, and excitation current loaded with passive load but not connected to the input

4.3.2 Gain and Input Range

For evaluation of signal-chain gain an input range without excitation current or actual sensors, use the following setup:

- Connect the input source to pins (2, 3) of J8A, a low distortion source capable of ±10-V output is recommended, such as R&S Audio Analyzer UPD with THD < –100 dB
- set the output of the source to maximum level Vp-p = 20V, low frequency like 100 Hz
- Capture the ADC time domain and calculate gain (from peak-to-peak value)
- Set the source frequency to 18 kHz and calculate the gain by capturing the ADC output again
- The previous steps can be repeated over different frequencies to draw the frequency response of the channel
- To test channel #4, make sure the attenuator common mode is connected to the ADC common mode. Short J13 (1,2 , right side).
- If required, a differential signal at the input of the ADC can be measured using a differential probe through the test points just before the ADC inputs

Make sure no clipping appears in the signal to verify the signal chain is properly biased.

4.3.3 Crosstalk

Use the following steps to evaluate signal-chain cross-talk:

- Connect a clean source with input (V_{PP} = FS) to channel (for example, channel 1), set the frequency to 2 kHz
- Short the adjacent channel (for example, ch2) and capture ch2 simultaneously with ch1
- In the frequency-domain view, the level of 2 kHz in the spectrum of ch2, calculate the cross-talk
- Repeat the measurement with the frequency set to 18 kHz
- Previous steps can be repeated over multiple frequencies, and different channel pairs

4.3.4 Total Harmonic Distortion

Use the following steps to evaluate the signal-chain total harmonic distortion:

- Set the source at –6 dBFS (11.88 V_{PP}) , and the frequency of 2 kHz of PSI source
- Capture the ADC input
- Using the frequency-domain view in the software, calculate the THD

4.3.5 Clock Image Rejection

Use the following steps to evaluate the signal-chain image rejection:

- Use a high-frequency sinusoidal source (able to produce clean 16-MHz signal)
- Set the source with fin = 16.002 MHz and –6 dBFS
- Capture ADC data in frequency-domain view. The highest spur is monitored in the noise spectrum and image rejection is calculated as the image spur referred to the input level. (A good target is for the spur to be 2 kHz, but complex intermodulation can result in different tones.)

4.3.6 Synchronization of the ADCs

To make sure proper synchronization is maintained between the four ADCs:

- Monitor the four nDRDY signals on J7
- In a good test case, those nDRDYx signals have the exact time for high-to-low transition. Record the delay between those signals using the 4-channel scope.
- Use persistent waveform display to capture variance of nDRDY delay between different channels (use one of the nDRDY signals as trigger)
- Repeat the previous test for each new SPI SCLK frequency and for both daisy and parallel SPI modes

4.3.7 Fault Detection Circuit

The reference design software shows the output of the fault detection circuit as open and short states. However, detection is not continuous in time, but rather is sampled every predefined period. The sampling period can be configured in the software.

Use the following steps to check the levels of the fault detection:

- Connect the input to a DC source
- Sweep the DC source between 0 V and 24 V with arbitrary number of steps
- For each step, make sure to acquire the fault shift register output
- Mark the levels at which open and short faults are triggered
- A reverse sweep can be applied to check hysteresis

Use the following steps to check the delay of the fault detection circuit.

- Input to the fault detection comparators is low-pass filtered which results in some delay between the actual input change and the comparator output change
- Use an input square waveform that crosses one of the detection levels found in the previous step. Probe the input signal and use as a trigger.
- Probe the comparator output of the excited channel
- Measure the delay between the threshold crossing of the input and the output mid-level crossing

4.4 Test Results

This section presents the sample test results. All the test results are done at room temperature 27°C, for daisy-chain configuration, data rate at 125 kSPS, digital supply at 2.5 V(PHI powered), and analog supply at 5.2 V, 32768 sample frame.

4.4.1 Noise Floor and Dynamic Range

The excitation current circuit and booster stage are not powered for the noise floor and dynamic range tests.

Begin by setting the ADC input MUX to offset test mode.

図 4-9. Histogram Plot of ADCs Inputs Shorted (Test Mode)

The ADC intrinsic voltage noise sigma is 7.7 µV, and offset of about 50 µV which is in line with the values in the *ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC* data sheet.

Next, short the front-end input (J8A, 2-3 = short).

図 4-10. Histogram Plot of Front-End Inputs Shorted

The full front-end voltage noise is around 19.8 µV, which is equivalent to 103 dB of Dynamic Range. The frequency plot in 図 4-11 shows a clean spectrum with the highest tone at 94 dBFS.

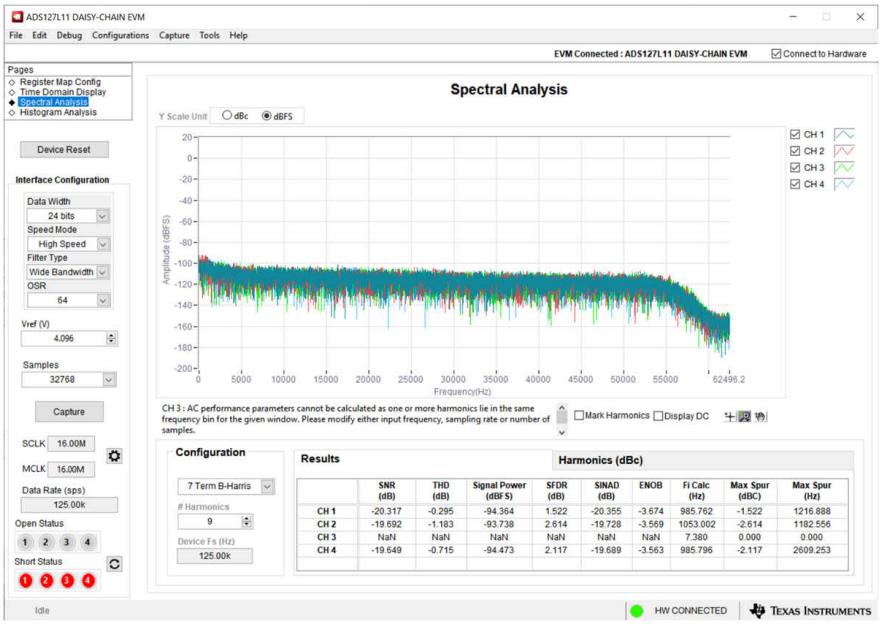


図 4-11. Frequency-Domain Plot of Front-End Inputs Shorted

The time-domain plot (see 図 4-12) verifies that there are no visible tones. The mean value of the channels are well below 0.5 mV which is the estimated offset of the whole channel including the offsets of OPA2320 (with gain of 4) and THS4551 (with gain of 2), and the ADS127L11 offset.

図 4-12. Time-Domain Plot of Front-End Inputs Shorted

4.4.2 Gain and Input Range

The following conditions were applied for the gain and input range testing:

- 20 V_{PP}, 2-kHz sinusoidal input is connected to this input of ch1, excitation current of all channels are on, and loaded but not connected to the input

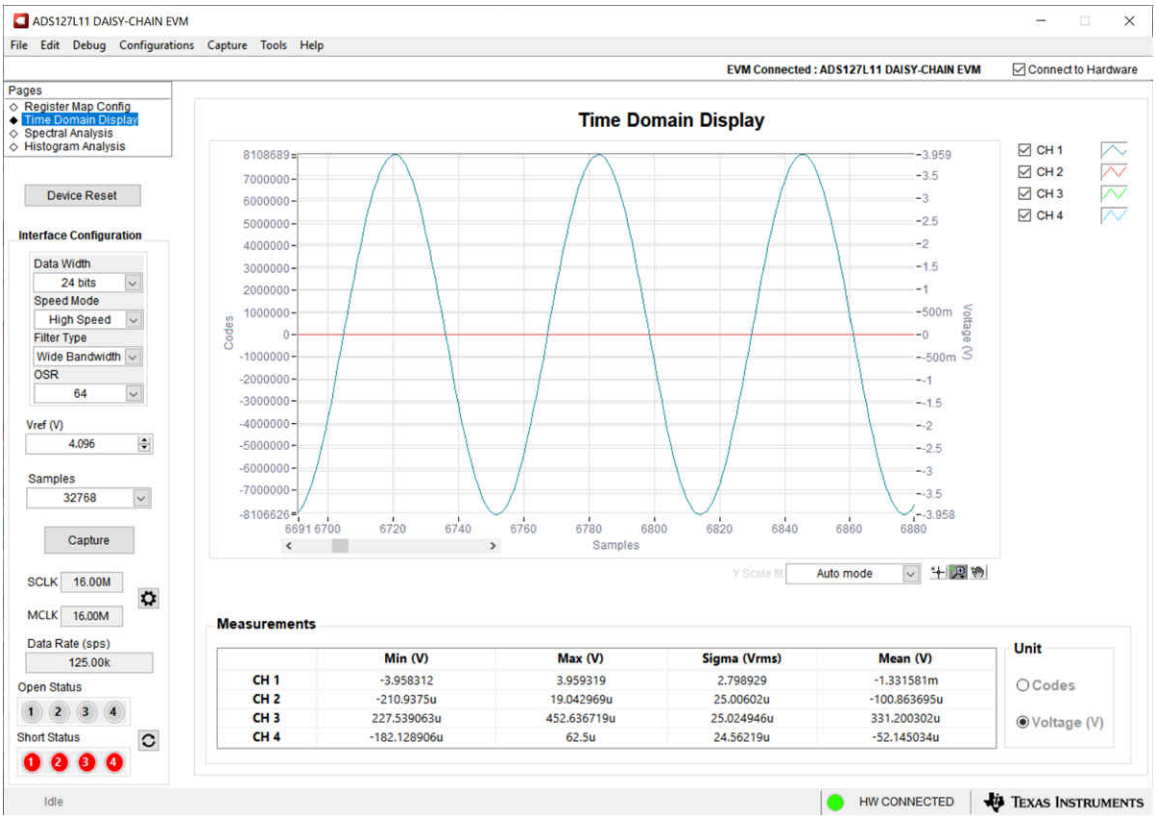


図 4-13. Time-Domain Plot of 20-V_{PP} Input at Channel 1

No sign of clipping appears in the time-domain plot shown in 図 4-13. The clipping results are obvious in the Total Harmonic Distortion test.

4.4.3 Crosstalk

The 20-V_{PP}, 2-kHz sinusoidal inputs applied to ch1 as in the input range test, ch2 signal power is compared to ch1 signal power. The 20 V_{PP}, 2 kHz is not pure and includes multiple high harmonics.

図 4-14. Frequency-Domain Plot of 20-V_{PP} Input at Channel 1

The ch1 signal level is ch1 is –2.8 dB as expected for full-scale input. While ch2 and ch3 signal levels are at –93 dB. These results indicate a cross-talk level below –90 dB.

4.4.4 Total Harmonic Distortion

For the TDH plot shown in 図 4-15, 10-V_{PP}, 2-kHz sinusoidal signal from a very clean source (PSI EVM) is applied to ch1 directly, this is equivalent to –6 dBFS. The total harmonic distortion is less than –97 dB showing the high linearity of the front-end.

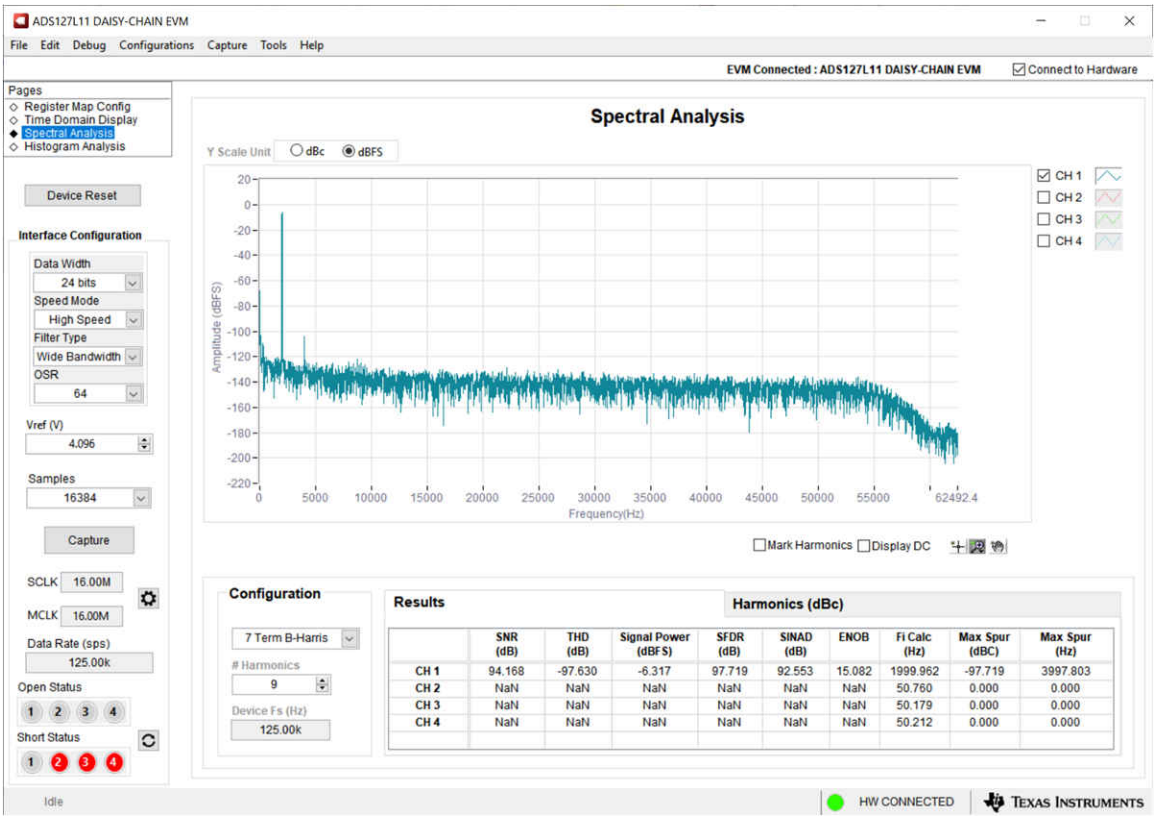


図 4-15. Frequency-Domain Plot of 2-kHz, 10-V_{PP} Input at Channel 1

4.4.5 Clock Image Rejection

The frequency-domain plot shown in 図 4-16 were taken at 10-V_{PP}, 16.002-MHz sinusoidal signal applied to ch1. This setting simulates the clock image frequency at the input. Output spectrum shows no sign of clock intermodulation, and that the clock rejection is below the noise level.

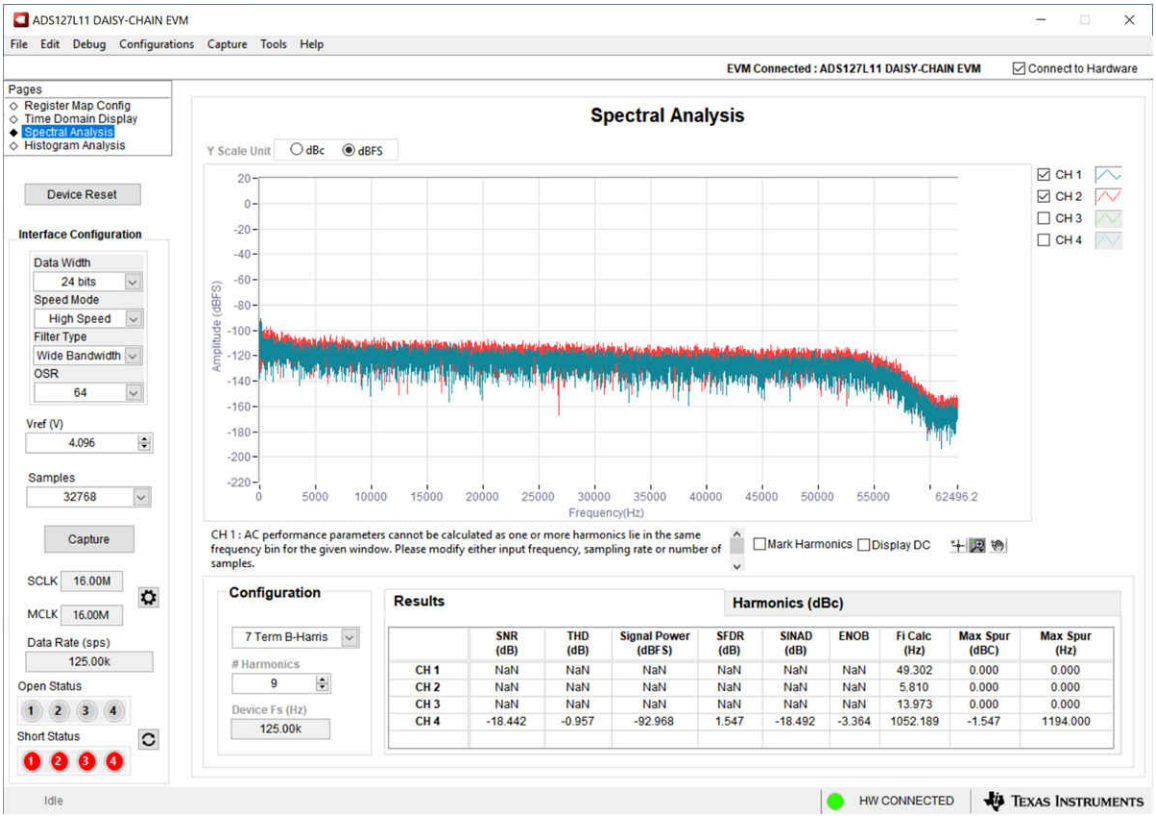


図 4-16. Frequency-Domain Plot of 10-V_{PP} Clock Image Input at Channel 1

4.4.6 Synchronization of the ADCs

図 4-17 shows the time domain waveform of nDRDY signals indicating four aligned signals.

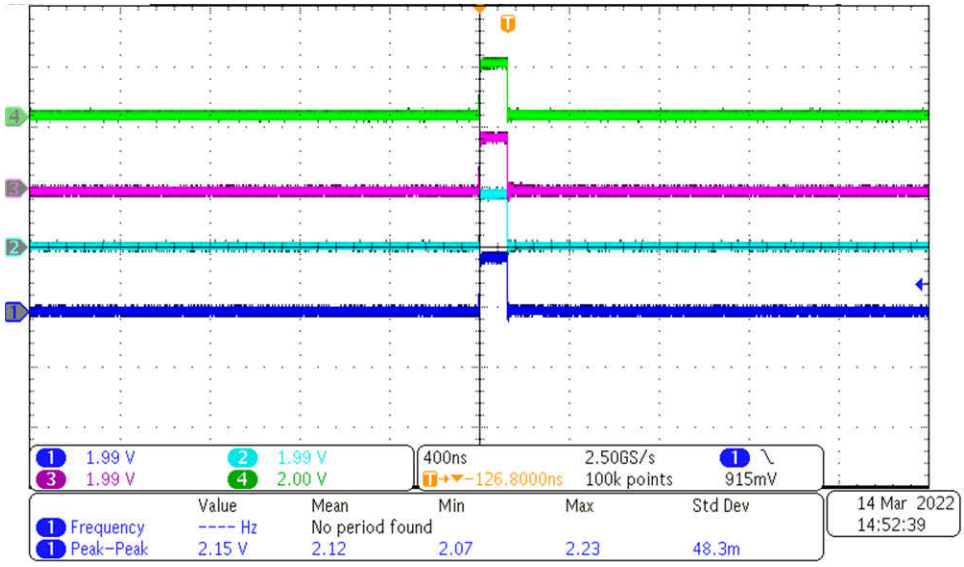


図 4-17. Time-Domain Plot of Data Ready Signal

The zoomed-in plot in 図 4-18 shows that the signals are synchronized down to pic-seconds level.

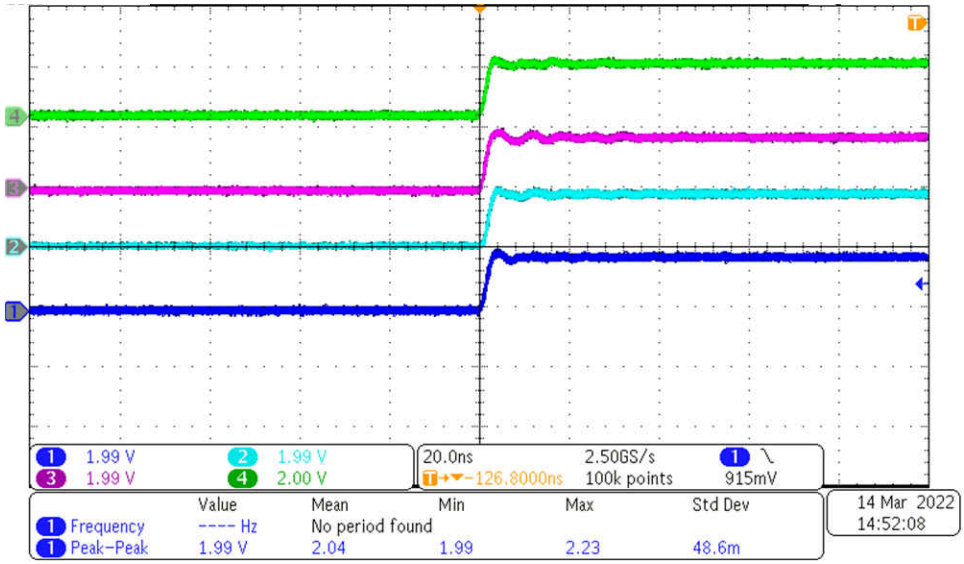


図 4-18. Zoomed-in Time-Domain Plot of nDRDY Signals

4.4.7 Fault Detection Circuit

Sweeping the input voltage results in the following thresholds for a fault-detection circuit:

- 0.5 V is the short detection threshold
- 20.1 V is the open detection threshold

The input signal stepped down from 10 V to 0 V, and the output of the short detection comparator is probed. The plot in 図 4-19 shows a delay of 1.5 ms until the comparator output goes low.

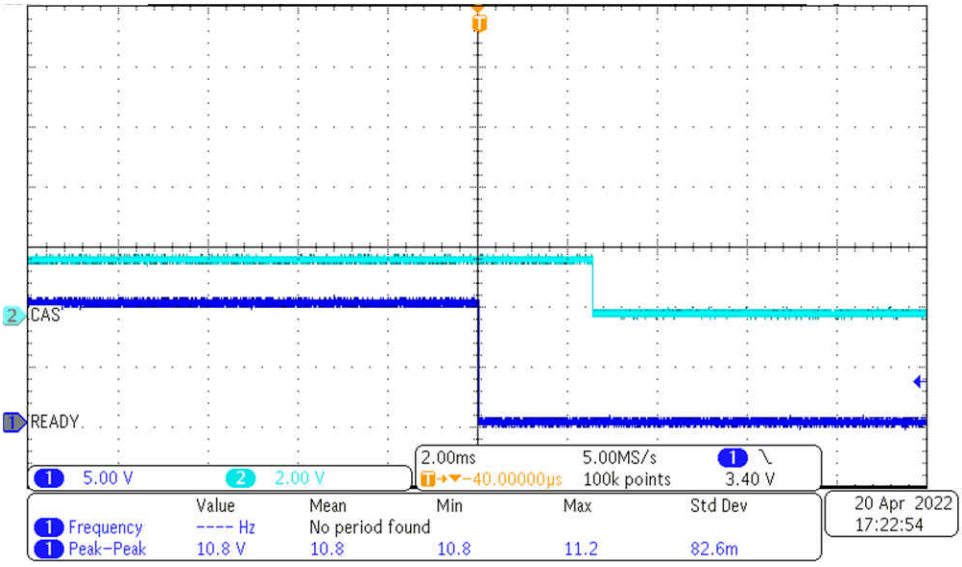


図 4-19. Time-Domain Plot of Fault Detection Circuit Delay

4.4.8 Test With Actual IEPE Sensor

An IEPE sensor, the Innomic ICS80 1741, is connected to ch1 contacting an audio vibration source of the same amplitude at 1 kHz and 5 kHz, respectively. The spectrum is captured to show the sensitivity of the interface to such input. The low frequency has the setup and environment mechanical vibration.

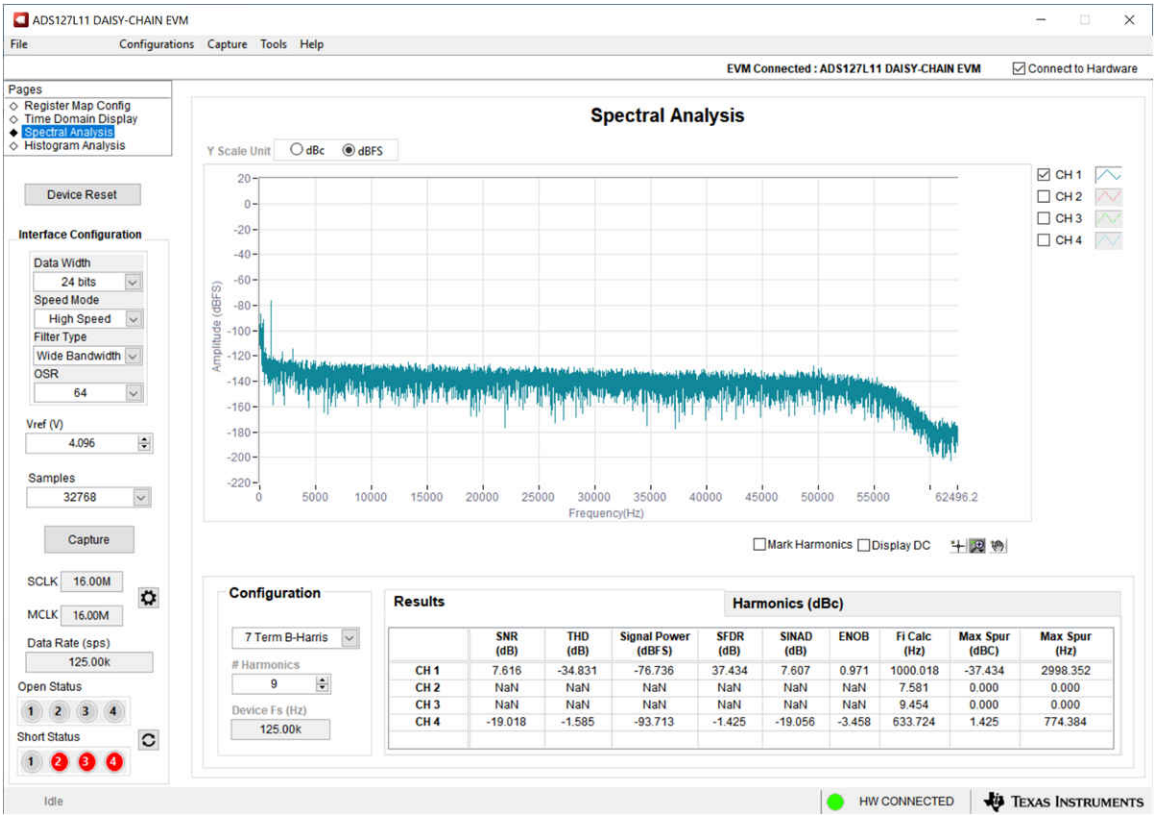


図 4-20. Frequency-Domain Plot of 1 kHz Applied to the IEPE Sensor

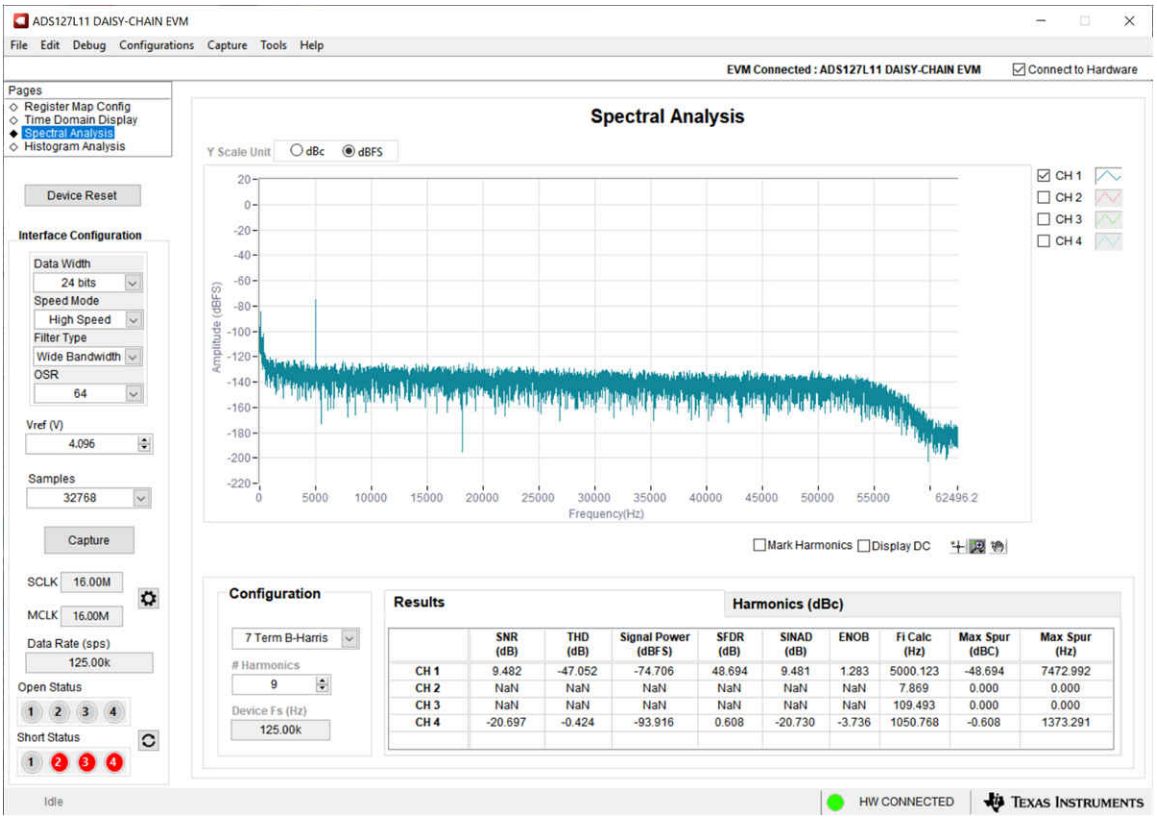


図 4-21. Frequency-Domain Plot of 5 kHz Applied to the IEPE Sensor

4.4.9 Measurement Results Summary

表 4-3 shows the key system specifications.

表 4-3. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	4
Input signal	±10 V, single-ended
Coupling	AC coupled
Resolution	24 bits
Input range	1.7 V to 22.2 V
Excitation current	3.458 mA
Excitation voltage	23.8 V
Excitation load regulation	9.25 µA/V = 0.26%
System input noise RMS	19.8 µV
System dynamic range	103 dB
Cross-talk	–90 dB
Total harmonic distortion	–97 dB
Clock image rejection	–100 dB
Short detection threshold	0.5 V
Open detection threshold	20.1 V
Fault-detection delay	1.5 ms

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010249.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010249.

5.2 Software

Software

TIDA-010249 EVM Software User Interface	This reference design is intended to be used with the dedicated TIDA-010249 EVM Software for windows.

5.3 Documentation Support

1. Texas Instruments, *ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC* data sheet
2. Texas Instruments, *ADS127L11 in Simultaneous-Sampling Systems* application brief
3. Texas Instruments, *IEPE Vibration Sensor Interface Reference Design for PLC Analog Input* design guide
4. Texas Instruments, *High-side current sources for industrial applications* Analog Design Journal article

5.4 サポート・リソース

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6 About the Author

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