
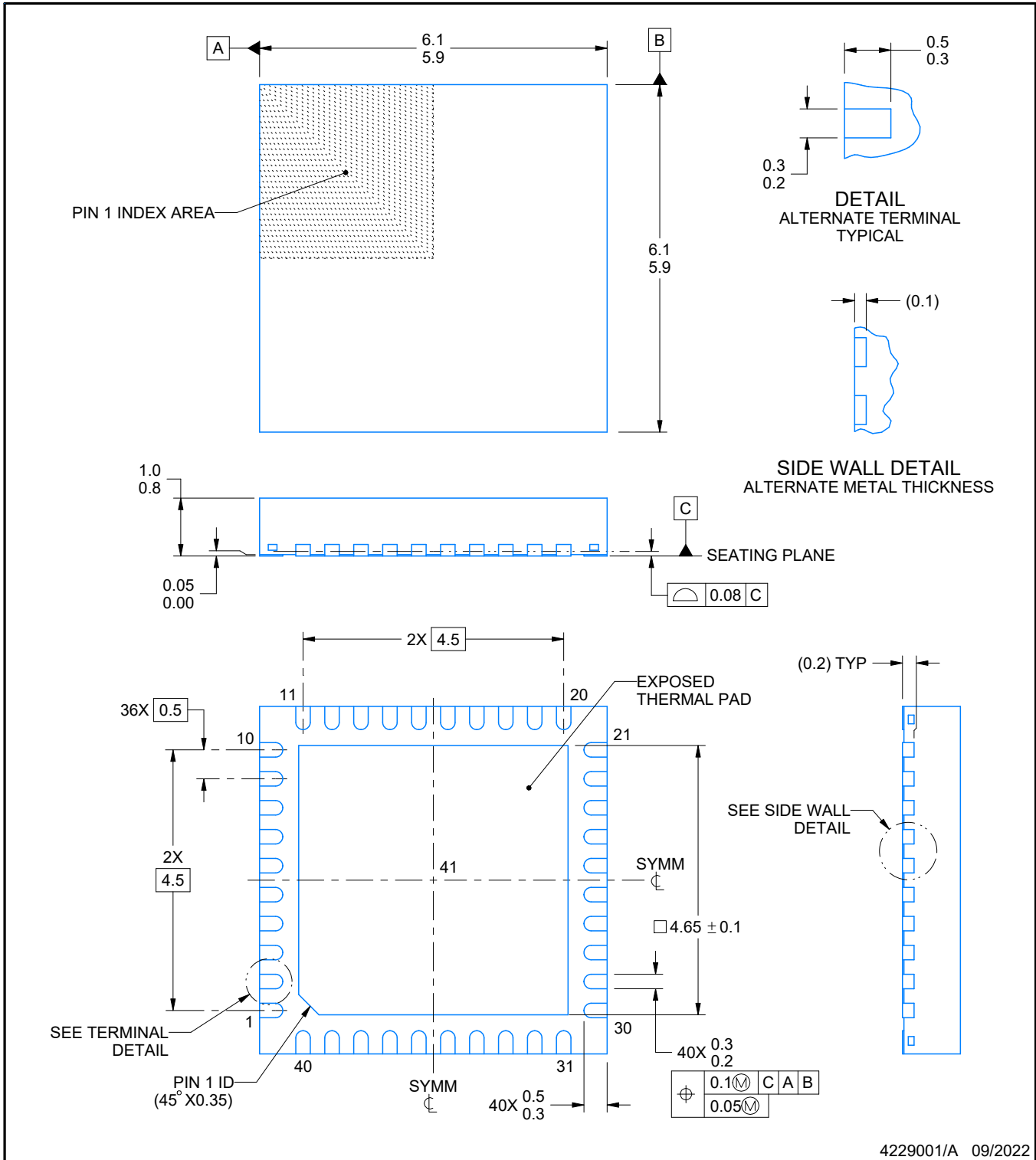
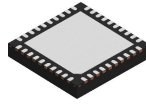


DATA BOOK PACKAGE OUTLINE

DRAFTER: K. SINCERBOX	DATE: 09/01/2022			DIMENSIONS IN MILLIMETERS		
DESIGNER:	DATE:	 TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS		CODE IDENTITY NUMBER 01295		
CHECKER: K. SINCERBOX	DATE: 09/01/2022	ePOD, RHA0040R / VQFN, 40 PIN, 0.5 MM PITCH				
ENGINEER: S. KUMMERL	DATE: 09/01/2022					
APPROVED: D. CHIN & D. KAN	DATE: 09/01/2022					
RELEASED: K. SINCERBOX	DATE: 09/01/2022					
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016	SCALE NTS	SIZE A	4229001	REV A	PAGE 1 OF 5



NOTES:

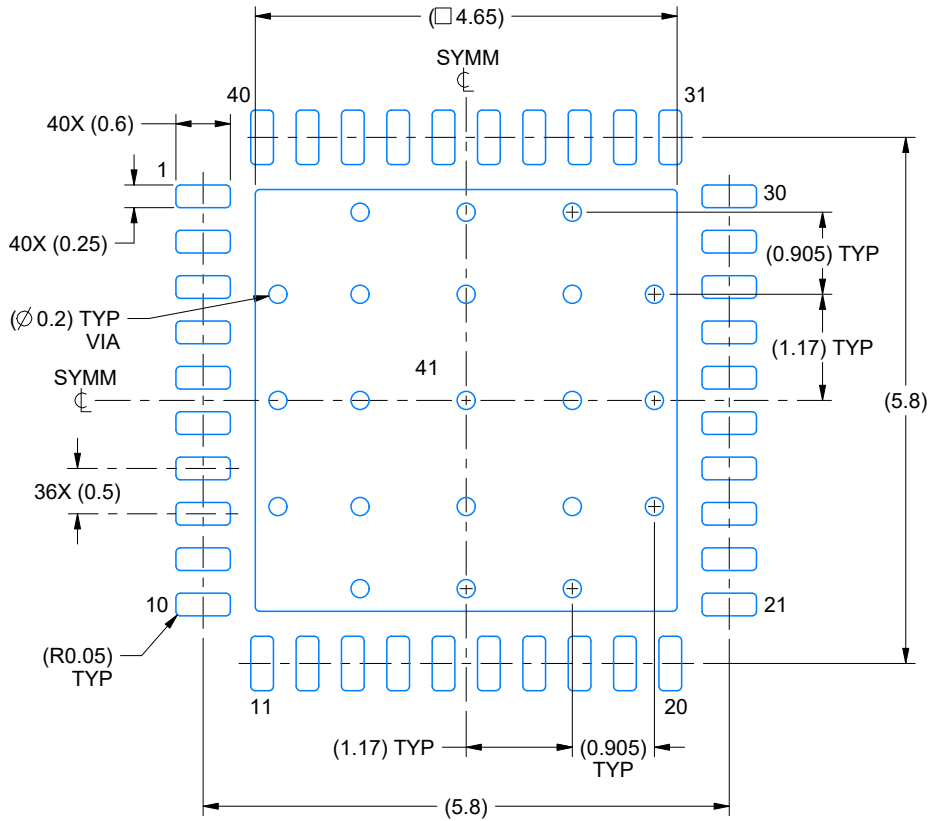
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

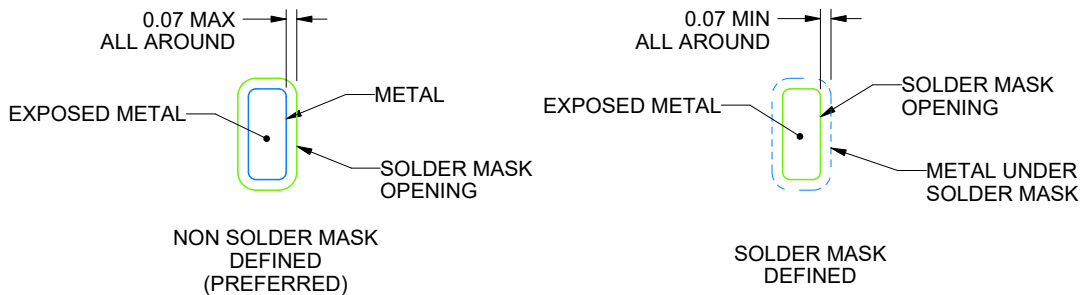
RHA0040R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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NOTES: (continued)

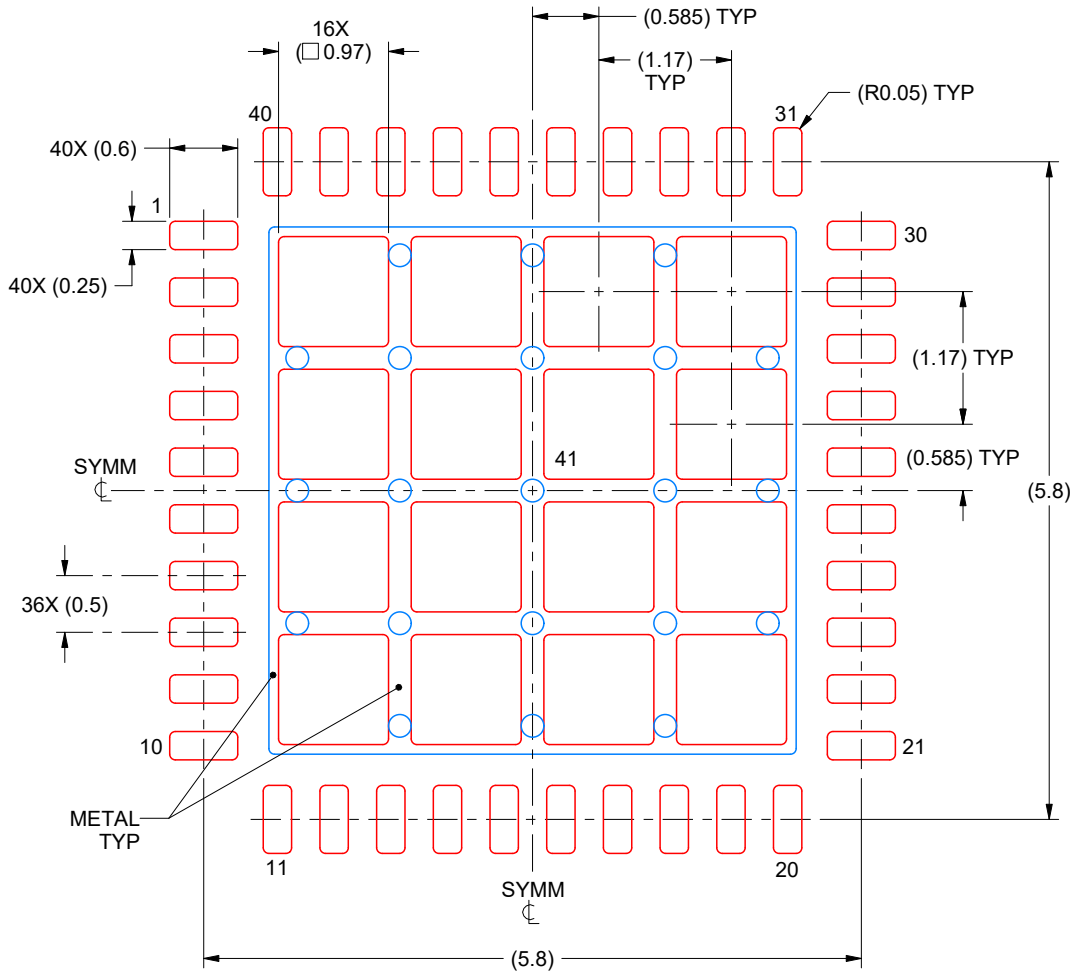
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHA0040R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2201054	09/01/2022	S. KUMMERL / K. SINCERBOX

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