Application Report
SBAA193–October 2011

POR and Resets in TSC2004/5/6

Wendy Fang, James Wang — *High-Performance Analog*

ABSTRACT

The TSC2004, TSC2005, and TSC2006 are a series of nanopower, four-wire resistive touch screen controllers (TSCs), with either an I²C™ (TSC2004) or SPI™ (TSC2005 or TSC2006) digital interface. To ensure that the TSCs power up at a known default working state, the proper power-on-reset (POR) requirements should be implemented. In addition to the POR option, the TSC2004/5/6 also feature a hardware or software reset that can bring up the device to a specific default state from any operating conditions.

This application report discusses the specific requirements for the POR and hardware and software resets with the TSC2004/5/6 devices. Unless otherwise noted, all references to the *TSC2004/5/6* apply to all three of these TSC devices.

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1 TSC2004/5/6 Power-On-Reset

Based on design principles and extensive tests with TSC2004/5/6, and to prevent any unexpected response, the device power must meet a specific ON/OFF timing and sequence in order to ensure that the Power-On-Reset (POR) function is implemented each and every time the TSC2004/5/6 powers on.

1.1 Functions of TSC2004/5/6 POR

During the TSC2004/5/6 SNSVDD power-on process, the POR brings the TSC2004/5/6 into a known default working state by initializing the internal state machine, data and control registers, and setting the conditions of several output pins. Without the POR function enabled correctly, TSC2004/5/6 could start up in a random state and even cause the TSC $\overline{\text{PINTDAV}}$ pin to not respond correctly.

The TSC2004/5/6 POR circuit was designed so that it does not consume power during normal operation of the TSC device; additionally, the power-down current is kept as low as possible (maximum power-down supply current: 0.8 µA; see Ref. 1, Ref. 2, and Ref. 3).

However, the POR circuit in the TSC2004/5/6 requires a specific power-up/-down ramp and sequence.

1.2 TSC2004/5/6 Power Cycle Requirements

Figure 1 and Table 1 show the recommended specifications for both power-off and ON-/OFF-RAMP times.

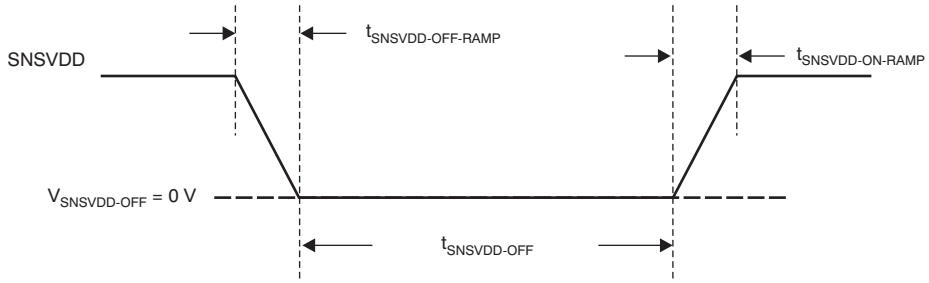

Figure 1. Power Cycle Sequence

Table 1. Recommended Power Cycle Timings

Temperature Range	Minimum $t_{SNSVDD-OFF-RAMP}$	Minimum $t_{SNSVDD-ON-RAMP}$	Minimum $t_{SNSVDD-OFF}$ (1)
-40°C to -21°C	12 kV/sec	12 kV/sec	1.2 sec
-20°C to +85°C	2 kV/sec	12 kV/sec	200 ms

(1) $t_{SNSVDD-OFF}$ time starts when the TSC2004/5/6 SNSVDD drops to and remains at 0 V.

Why Specify a Minimum $t_{SNSVDD-OFF}$ Time?

The POR circuit of the TSC2004/5/6 contains a capacitor that charges when the device powers up and generates an internal reset signal. This capacitor discharges after the TSC2004/5/6 supply is switched off. The TSC2004/5/6 is designed for low-power operation; therefore, the POR takes time to charge and discharge the capacitor, especially under cold temperatures (less than –20°C).

Why Specify Minimum $t_{SNSVDD-OFF-RAMP}$ and $t_{SNSVDD-ON-RAMP}$ Times?

To ensure the proper initialization of the TSC2004/5/6, it is required that the device reach a certain voltage before the internal POR signal is released. If the power supply ON-RAMP is too slow, the device may come up in a random state and thus not respond correctly

The capacitor within the POR circuit must be discharged through the TSC2004/5/6 SNSVDD pin. To support a proper discharge, it is recommended to have a certain $t_{SNSVDD-OFF-RAMP}$ time, and also provide a low-resistance path on the SNSVDD pin when the TSC2004/5/6 supply switches off.

1.3 Effects on TSC2004/5/6 POR

If any situation given in Section 1.2 cannot be ensured, it could affect the TSC2004/5/6 POR circuit; the TSC2004/5/6 might then enter a specific test mode that is only for TI internal testing purposes. If this event happens accidentally as a result of an irregular power condition, certain software workarounds are then required to escape this condition and remediate the event.

1.3.1 Effect from TSC2004/5/6 Digital Pins

Many applications use the same power supply for both analog and digital power supplied to the TSC2004/5/6. In practical terms, the TSC2004/5/6 SNSVDD is connected with the IOVDD. In such cases, the logic high status on the TSC2004/5/6 digital pins before device power up becomes a concern for the proper TSC2004/5/6 POR operation.

The TSC2004/5/6 has several digital IO pins, as listed in Table 2 and Table 3.

Table 2. TSC2004 Digital IO Pins

TSC2004 Pin Name	Description
$\overline{\text{PINTDAV}}$	Digital output; an interrupt on touch/data status
$\overline{\text{RESET}}$	Digital input; hardware reset to the TSC.
SCL	Open drain; I^2C bus clock.
SDA	Open drain; I^2C bus data.
A0	Digital input; I^2C address bit A0 for TSC2004.
A1	Digital input; I^2C address bit A1 for TSC2004.

Table 3. TSC2005/6 Digital IO Pins

TSC2005/6 Pin Name	Description
$\overline{\text{PINTDAV}}$	Digital output; an interrupt on touch/data status
$\overline{\text{RESET}}$	Digital input; hardware reset to the TSC.
SCLK	Digital input; SPI bus clock.
SDO	Digital output; SPI bus output data.
SDI	Digital input; SPI bus input data.
$\overline{\text{CS}}$	Digital input; SPI bus chip select input.

The TSC2004/5/6 has the best electrostatic discharge (ESD) protection on the market. Every TSC2004/5/6 pin (except the SDA and SCL pins of the TSC2004) is well-protected against both positive and negative ESD shocks. Consider the TSC2004/5/6 $\overline{\text{RESET}}$ pin as an example: internally, there is an ESD protection diode between $\overline{\text{RESET}}$ and the ground pin, and a second diode between $\overline{\text{RESET}}$ and the SNSVDD pin, as shown in Figure 2.

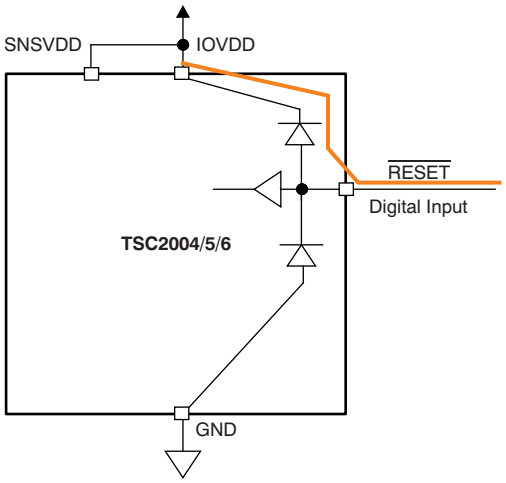

Figure 2. Internal ESD Protection Diodes at TSC2004/5/6 $\overline{\text{RESET}}$ Pin

If by any chance a TSC2004/5/6 digital input pin (such as $\overline{\text{RESET}}$) powers up while the device SNSVDD power is not applied, the TSC2004/5/6 would be *powered up* from the $\overline{\text{RESET}}$ pin through the connected internal diode between the pin and the SNSVDD pin. This internal connection is shown by the orange line in Figure 2.

Such *false* power up cannot ensure the required power supply to TSC2004/5/6; therefore, the TSC2004/5/6 POR circuit would not be ensured, and some unexpected behavior of the TSC2004/5/6 may occur as a result.

1.3.2 Effect from SNSVDD Glitches During Normal Operation

A TSC2004/5/6 SNSVDD power glitch during normal operation may cause an incorrect device response. Therefore, it is important that the system is able to power up according to the requirements described in Figure 1 and Table 1.

1.3.3 Effect from Power Cycles During Normal Operation

The TSC2004/5/6 is a low-power device, and therefore it is not necessary to switch off the TSC2004/5/6 during normal operation. Each power cycle must meet the requirements shown in Figure 1 and Table 1. Otherwise, proper POR operation may not be achieved during the power cycle sequence, and the TSC may not be in its default working state.

2 TSC2004/5/6 Hardware or Software Reset

There are three ways to reset the TSC2004/5/6 to its default working state. In addition to the POR process, discussed in Section 1, there are also two additional techniques to perform a device reset:

- A hardware reset through the TSC2004/5/6 $\overline{\text{RESET}}$ pin
- A software reset by the SWRST bit in the TSC2004/5/6 Control Byte 1

As Section 1 notes, the requirements for ensuring a proper TSC2004/5/6 POR are very stringent and may be very hard to meet in many applications. As a workaround, users may apply a proper hardware or software reset instead of (or in addition to) the POR process described earlier.

2.1 TSC2004/5/6 Hardware Reset

An active low (equal to or longer than 10 µs or 13 µs) applied to the $\overline{\text{RESET}}$ pin triggers the TSC2004/5/6 hardware reset. The reset signal is specified in Figure 3 and Table 4. See the respective product data sheets as well.

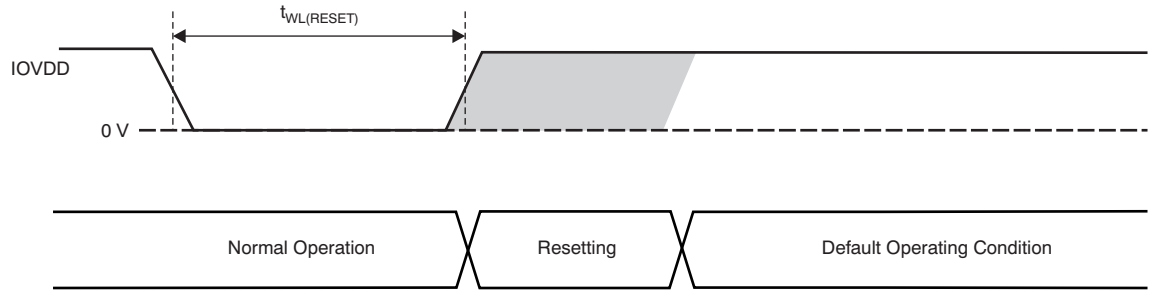

Figure 3. Hardware Reset Signal Specification

Table 4. Required Hardware Reset Timings

SNSVDD	Minimum $t_{WL(RESET)}$
≥ 1.6 V	10 µs
≥ 1.2 V and < 1.6V(1)	13 µs

(1) For TSC2004 and TSC2006 only.

A hardware reset in any mode or condition returns the TSC to its default working state (that is, the exact same state as the POR process does), except to terminate a specific test mode (this mode is only for TI internal testing purposes and may be a random outcome from an improper POR).

A power cycle is necessary if by any chance the TSC2004/5/6 was brought into the specific test mode. A specific software reset sequence can also terminate the specific test mode, as the next section explains.

2.2 TSC2004/5/6 Software Reset

A software reset can be sent from the host processor to the TSC device through setting the SWRST bit to '1'. The SWRST bit is bit D1 in the Control Byte 1 (see Ref. 1, Ref. 2, and Ref. 3).

Note that **the SWRST bit in the TSC2005/6 is not self-cleared**. It is required to set the SWRST to '0' to cancel the software reset and resume normal device operation. On the other hand, **the SWRST bit in the TSC2004 is self-clearing**; it returns back to '0' and automatically resumes normal operation after the software reset is complete.

After the power cycle, if the TSC2004/5/6 has randomly entered the specific test mode through an improper POR sequence, users can then apply the software reset through a special sequence to bring the TSC device back to the known default working state.

2.2.1 TSC2004 Software Reset Sequence to Terminate Test Mode

The TSC2004 reset sequence after the power cycle is categorized into two cases, depending on the connection of the AD0 pin. Refer to Table 5 for cases when the AD0 pin is connected to '0', and Table 6 for situations when the AD0 pin is connected to '1'. Some steps in these sequences are optional and can be ignored without deactivating the SW reset. Removing the optional steps can simplify the reset sequence if it is necessary. Although the AD0 pin connection makes the resetting sequence slightly different, it is only a one-case scenario once AD0 pin connection is determined on the system.

Table 5. Case 1:TSC2004 AD0 Pin is Connected to '0'

Step	Sequence	Description
1	$\overline{\text{RESET}}$ = 'L'	The power cycle starts.
2	$\overline{\text{RESET}}$ = ('L' → 'H')	It may be pulled up by a pull-up resistor or directly set to 'H' by the host processor (see Figure 4).
3	$\overline{\text{RESET}}$ = ('H' → 'L' → 'H')	It should meet the HW reset requirement. This step is optional but recommended if $\overline{\text{RESET}}$ is pulled up by a resistor.
4	SW reset (matched with AD0 pin)(1)	START → I2Cwrite = 0x10010(AD1)**0**0 → Ack → CB1 = 0x10000010 → Ack → STOP
5	Set the internal register starting address to 7h for reading Status Register (optional)	START → I2Cwrite = 0x10010(AD1)00 → Ack → CB0 = 0x00111001 → Ack → STOP
6	Verify Status Register (optional)	START → I2Cread = 0x10010(AD1)01 → Ack → Status Register Content (8bit+Ack+8bit+NAck) → STOP Its content is 0x0004.
7	TSC2004 initialization procedure	It includes setting the contents of configuration registers and setting the internal register starting address to 0h.
8	Touch screen normal operation	

(1) Bit changes noted in **boldface**.

Both Step 4 and Step 5 in Table 6 can proceed without checking the acknowledge bit (Ack) of the I²C bus and branching the sequence, because either step receives a not-acknowledge (*Not-Ack*) signal. In this way, the sequence programming can be simplified without deactivating the SW reset.

Table 6. Case 2: TSC2004 AD0 Pin is Connected to '1'

Step	Sequence	Description
1	$\overline{\text{RESET}}$ = 'L'	The power cycle starts.
2	$\overline{\text{RESET}}$ = ('L' → 'H')	It may be pulled up by a pull-up resistor or directly set to 'H' by the host processor (see Figure 4).
3	$\overline{\text{RESET}}$ = ('H' → 'L' → 'H')	It should meet the HW reset requirement. This step is optional but recommended if $\overline{\text{RESET}}$ is pulled up by a resistor.
4	SW reset (matched with AD0 pin)	START → I2Cwrite = 0x10010(AD1)**1**0 → Ack/Not-Ack → CB1 = 0x10000010 → Ack/Not-Ack → STOP
	4.1 If the *Not-Ack* appeared after I²C write command, then the AD0 bit should be set to '0' in the I²C write command (the AD1 bit still follows the hardware setting); go to Step 5.	This state implies that TSC2004 accidently enters the test mode 0 because of the irregular power ramp up.
	4.2 Otherwise, skip Step 5.	If Step 5 proceeds anyway, it only generates a *Not-Ack* and will not confuse the TSC.
5	SW reset with AD0 = '0'(1)	START → I2Cwrite = 0x10010(AD1)**0**0 → Ack/Not-Ack → CB1 = 0x10000010 → Ack/Not-Ack → STOP
6	Set the internal register starting address to 7h for reading Status Register (optional)(1)	START → I2Cwrite = 0x10010(AD1)**1**0 → Ack → CB0 = 0x00111001 → Ack → STOP
7	Verify Status Register (optional) (1)	START → I2Cread = 0x10010(AD1)**1**1 → Ack → Status Register Content (8bit+Ack+8bit+NAck) → STOP Its content is 0x0004.
8	TSC2004 initialization procedure	It includes setting the contents of configuration registers and setting the internal register starting address to 0h.
9	Touch screen normal operation	

(1) Bit changes noted in **boldface**.

2.2.2 TSC2005/6 Software Reset Sequence to Terminate Test Mode

Both Step 2 and Step 5 in the TSC2005/6 reset sequence (shown in Table 7) after the power cycle are required to activate the SW reset if the TSC2005/6 has entered the specific test mode. Some steps in these sequences are optional and can be ignored without deactivating the SW reset. Eliminating the optional steps can simplify the reset sequence if it is necessary.

Table 7. Software Sequence for TSC2005/6

Step	Sequence	Description
1	$\overline{\text{RESET}}$ = 'L'	The power cycle starts. Other input conditions should be $\overline{\text{CS}}$ = ('L' → 'H'), SCLK = 'L', and SDI = 'L'.
2	SCLK = ('L' → 'H')	It is set to 'H' by the host processor.
3	$\overline{\text{RESET}}$ = ('L' → 'H')	It may be pulled up by a pull-up resistor or directly set to 'H' by the host processor (see Figure 4).
4	$\overline{\text{RESET}}$ = ('H' → 'L' → 'H')	It should meet the HW reset requirement. This step is optional but recommended if $\overline{\text{RESET}}$ is pulled up by a resistor.
5	SCLK = 'L'	
6	SW reset (CB1.SWRST = 1)	Send CB1 = 0x1000001**1**0 to SDI. $\overline{\text{CS}}$ should be normally toggling (see SPI protocol in Ref. 2 or Ref. 3).
7	Clear SW reset (CB1.SWRST = 0)(1)	Send CB1 = 0x1000001**0**0 to SDI. $\overline{\text{CS}}$ should be normally toggling (see SPI protocol in Ref. 2 or Ref. 3).
8	Verify Status Register (optional)	Send CB0 = 0x00111001 to SDI followed by reading 2 bytes on SDO. $\overline{\text{CS}}$ should be normally toggling (see SPI protocol in Ref. 2 or Ref. 3). Its content is 0x0004.
9	TSC2005/6 initialization procedure	It includes setting the contents of configuration registers.
10	Touch screen normal operation	

(1) Bit changes noted in **boldface**.

3 Suggested Hardware Reset During Power-On

Based on the above discussion, these conclusions can be drawn:

1. The highest precedent reset is the POR, which always brings the TSC into a known default working state. The POR sequence, however, requires a very stringent power cycle sequence.
2. The hardware reset works as the next-highest precedent reset, except if the TSC randomly enters the specific test mode through an improper POR.
3. The software reset works as the lowest precedent reset; however, the software reset can be used in a special sequence to terminate the specific test mode entered through an improper POR.

While it seems that any one of these three reset methods could not work alone, the following hardware reset during power-on is suggested:

The TSC2004/5/6 $\overline{\text{RESET}}$ pin should be held *low* during power-up. Return the pin *high* after the TSC has been completely powered on, where there is no requirement or limitation on the power-up/-down ramps or power sequences.

This hardware reset is illustrated in Figure 4 and Table 4.

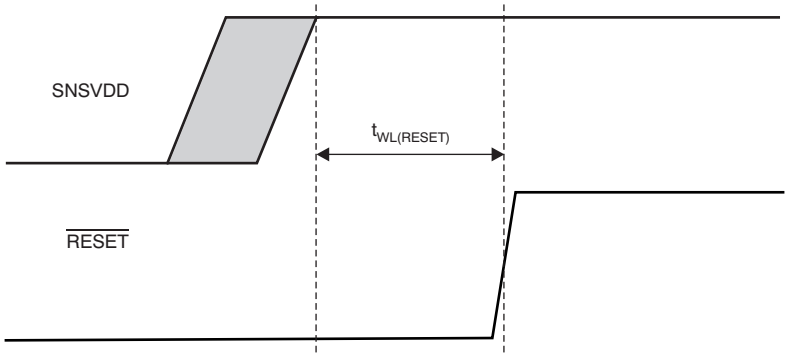

Figure 4. Recommended Hardware Reset During Power Cycle

4 References

Unless otherwise noted, the following documents are available for download at www.ti.com.

1. TSC2004 product data sheet. Literature number SBAS408.
2. TSC2005 product data sheet. Literature number SBAS379.
3. TSC2006 product data sheet. Literature number SBAS415.

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