Application Report

Time Division Duplexing (TDD) in AFE77xx Integrated Transceiver

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ABSTRACT

Time Division Duplexing (TDD) separates uplink and downlink radio frequency channels in the time domain and allows the uplink and downlink channels to share the same radio frequency channel resources while avoiding interference. In the AFE77xx integrated transceiver, external GPIOs are available to switch the transmitter, feedback, and receiver data paths between standby and active modes during TDD. This application note demonstrates how to configure AFE77xx in TDD mode and also how to use the AFE77xxEVM and TSW14J56EVM to make TDD measurements. Basic familiarity with HSDCPRO, TSW14J56EVM, AFE77xx EVM, and Latte GUI is assumed. It is also assumed that the user is familiar with the bring up steps in the AFE77xx Evaluation-Module Quick-Start-Guide.

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Trademarks

1 Introduction

In the AFE77xx integrated transceiver, external GPIOs are provided to switch the transmitter, feedback, and receiver data paths between standby and active modes during TDD. Table 1-1 shows the external GPIOs used in TDD mode on the AFE77xx. There are five total GPIOs used to switch between downlink and uplink when in TDD mode:

- TXEN1
- TXEN2
- RXEN1
- RXEN2
- 1FBEN

Table 1-1. AFE77xx GPIOs Used in TDD Mode

TDD MODE	TXEN1/TXEN2	RXEN1/RXEN2	1FBEN	TRANSMITTER MODE	RECEIVER MODE	FEEDBACK PATH
Downlink	1	0	1	Active	Standby	Active
Uplink	0	1	0	Standby	Active	Standby

The control of the TDD GPIOs is not mutually exclusive so it is possible for uplink and downlink modes to be in standby or active at the same time. In TDD mode, the feedback and receiver ADCs can time share the SERDES lanes to minimize SERDES resource usage in the FPGA and AFE77xx. The information on the SERDES lanes can be dynamically switched between Feedback and Receiver ADCs, depending on the state of RXEN1/RXEN2 and 1FBEN GPIOs. This is summarized in Table 1-2.

Table 1-2. Serdes Lane Sharing in TDD Mode

RXEN1/2	1FBEN	RX CHAIN	FB CHAIN	SERDES LANES TO
1	0	On	Off	RX
0	1	Off	On	FB
1	1	On/Off	On/Off	RX/FB
0	0	Off	Off	

2 Device Overview

The AFE7798 is a high performance multi-channel transceiver, integrating four direct upconversion transmitter chains, four direct downconversion receiver chains, and one wideband RF sampling digitizing auxiliary chain (feedback paths). The high dynamic range of the transmitter and receiver chains allows generating and receiving 2G, 3G, 4G, and 5G signals for a wireless base station. The low power dissipation and large channels integration makes the AFE7798 devices suitable to address the power and size-constrained 4G and 5G massive MIMO base station. The wideband and high dynamic range feedback path can assist the digital pre-distortion (DPD) of the power amplifiers in the transmitter chain. The fast SERDES speed can help reduce the number of lanes required to transfer the data in and out of the device.

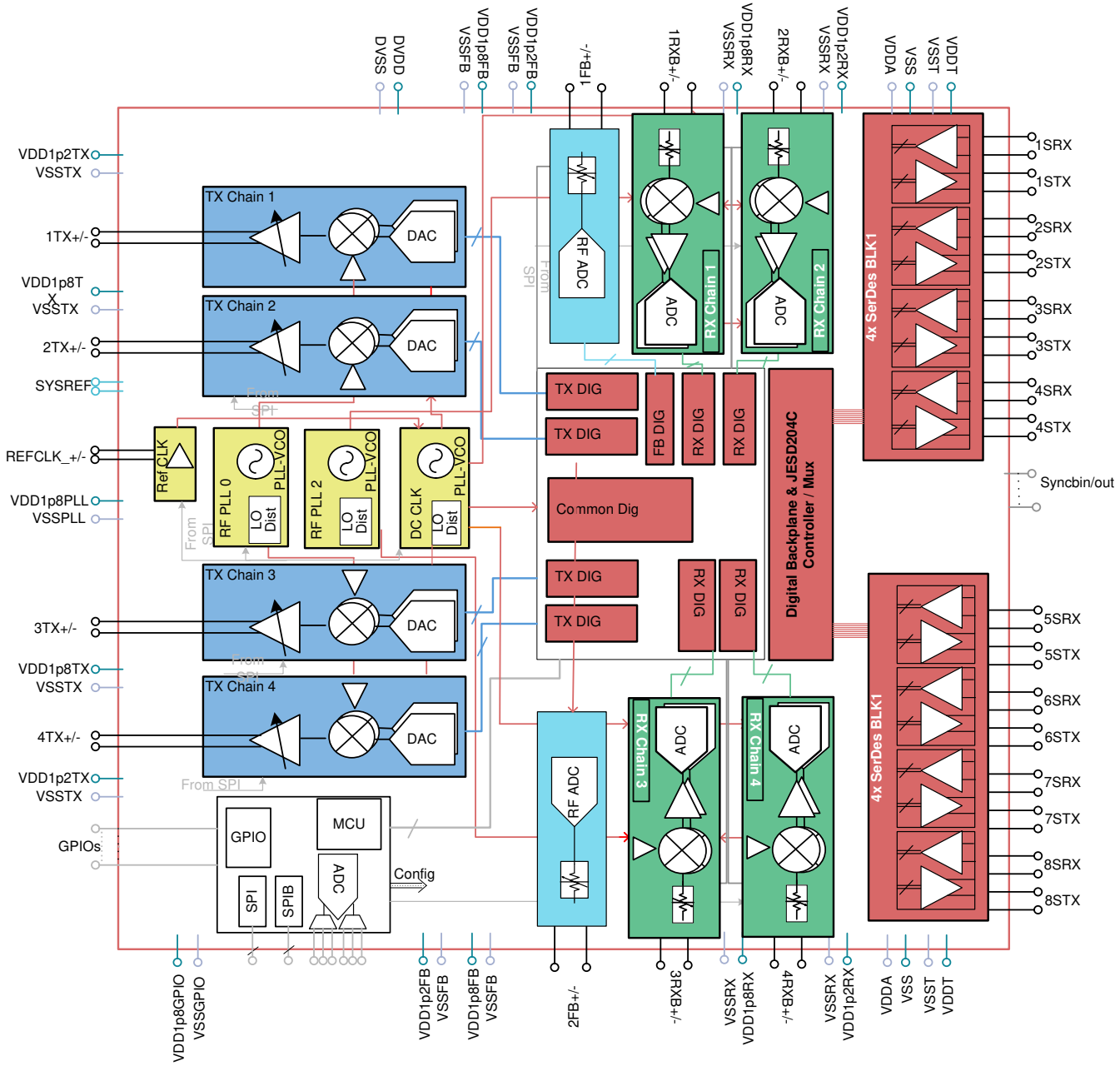

Figure 2-1. Block Diagram of the AFE77xx

3 Hardware and Software Setup for TDD Evaluation

To successfully evaluate the AFE77xx in TDD mode, the following tools are required:

Table 3-1. Software and Hardware Required for TDD Evaluation

EVALUATION TOOL	DESCRIPTION
HSDCPRO	Software to send patterns and capture data from the TSW14J56 arbitrary waveform generator. Software version 2p5 or higher is required.
TSW14J56revD EVM	FPGA-based arbitrary waveform generator used to interface to the AFE77xxEVM for pattern generation to the transmitter and data capture from the receiver and feedback paths.
AFE77xx EVM	Main evaluation board for AFE77xx device
Latte	Software to configure AFE77xxEVM. Version 2p2 or higher is required.
Latte_GUI_TDD_MODE	Software patch to enable TDD evaluation. Can be obtained from local TI support

3.1 Hardware Setup

Figure 3-1 shows an example hardware setup that can be used to make TDD measurements.

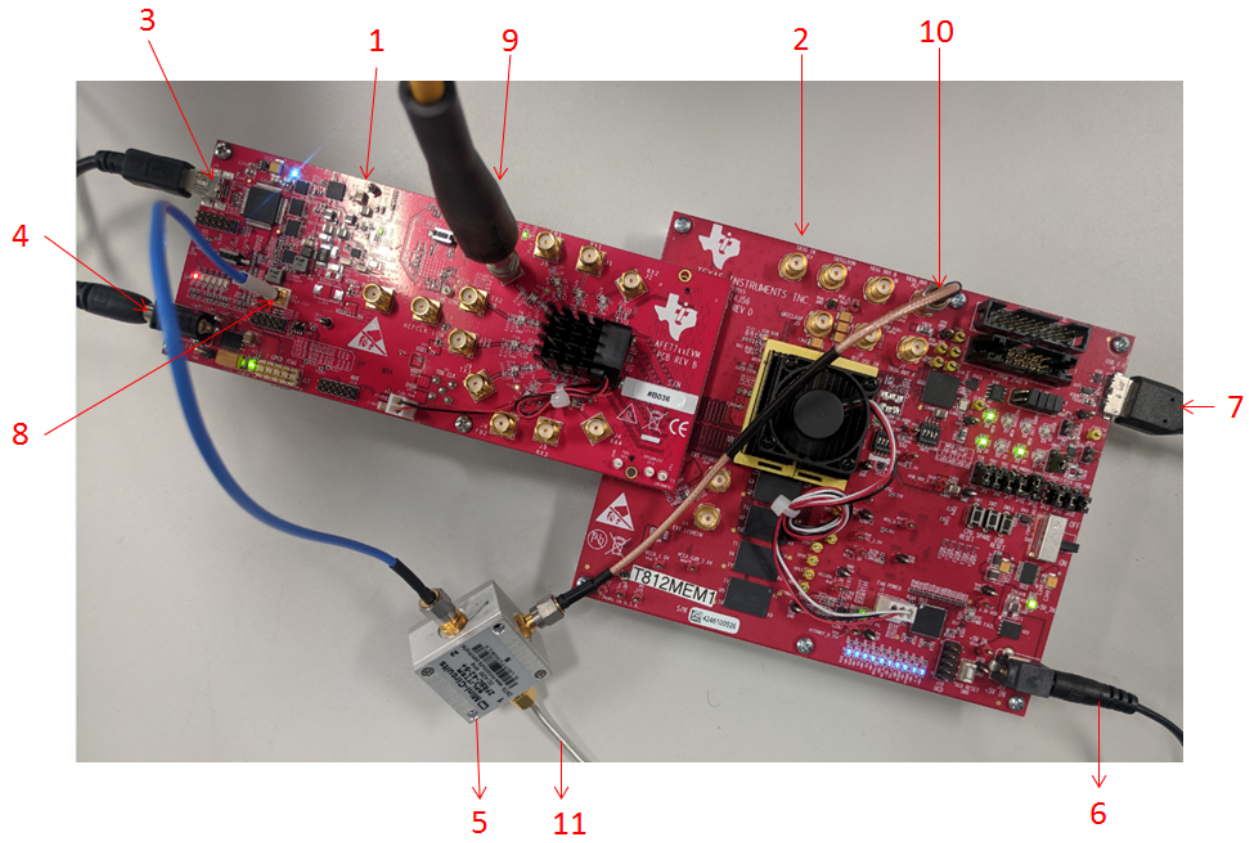

Figure 3-1. Setup for TDD Mode Evaluation

Table 3-2. Description of Hardware Setup for TDD Evaluation

LABEL	DESCRIPTION
1	AFE77xx evaluation module
2	TSW14J56 evaluation module
3	Mini USB 2.0 connector. The opposite end must be connected to a PC running Latte software.
4	Power supply to AFE77xxEVM. Connect to 5.5 V, 5 A bench supply.
5	1 : 2 RF power splitter. Connect the input to SMA J12 on the TSW14J56EVM and the outputs to connector J24 on the AFE77xxEVM and trigger input of spectrum analyzer respectively.
6	Power supply to TSW14J56EVM. Connect to 5.5 V, 5 A bench supply.
7	USB 3.0 connector. Connect the opposite end to PC running HSDCPRO software.
8	TDD control input to AFE77xxEVM
9	Transmitter Output. Connect to RF input of spectrum analyzer.
10	TDD output from TSW14J56EVM
11	TDD control signal to trigger input of spectrum analyzer

3.2 Generating and Loading TDD Test Pattern into HSDCPRO

Table 3-3 gives an example of a test pattern that can be loaded into HSDCPRO. The format of the pattern file must meet the requirements below:

- The pattern file must have three columns with the following definitions:
  1. Column 1: In-phase data (I-data) for the transmitters. The range is from -32767 to 32768.
  2. Column 2: Quadrature phase data (Q-data). The range is also from -32767 to 32768.
  3. Column 3: TDD control pattern. Set to 0 to disable TDD and 1 to enable.
- The number of rows must be a multiple of 512.
- The pattern file can be saved with a .csv file extension and comma as the delimiter or it can be saved with a .txt file extension and tab as the delimiter.

Table 3-3. An Example Transmitter Pattern File for TDD Evaluation

I-DATA	Q-DATA	TDD
9889	31239	0
-6662	32083	0
-21508	24720	0
-30853	11035	0

After saving the test pattern, it can be loaded into HSDCPRO using the “Load External Pattern File” button highlighted in Figure 3-2.

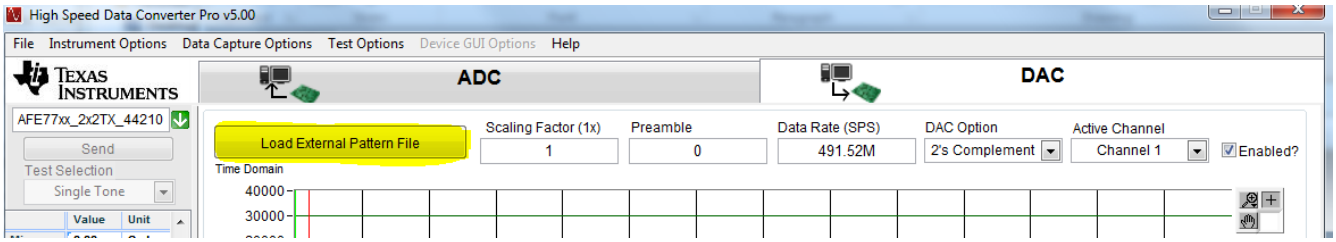

Figure 3-2. Interface of HSDCPRO Showing Button to Load External Test Pattern File

3.3 Device Initialization (.ini) Files for TDD in HSDCPRO

A few parameters must be included in the initialization (.ini) file of the transmitter to enable TDD mode in the firmware running on the TSW14J56EVM. These parameters include the following:

1. Auto duplicate channels = 1
   - This parameter enables the data read from DDR3 memory to be replicated to all four transmitter channels.
2. Number of channels for lane rate = 8
   - This parameter enables accurate calculation of the SERDES bit rate when TDD Auto duplicate channels parameter is set to 1.
3. BCM in channel Data = 1
   - This parameter enables the firmware to treat the signal in the third column as TDD signal and not data to the transmitters.

After installing the software patch Latte_GUI_TDD_MODE, an example .ini file (AFE77xx_2x2TX_44210_tdd.ini) is also installed to the HSDCPRO directory.

For the receiver and feedback ADC initialization files, no extra parameters are needed in the device initialization (.ini) file.

4 Making TDD Measurements

The first step is to setup the hardware as described in Section 3.1. Afterwards, the setup can be configured with the Latte and HSDCPRO software by following the steps described in the AFE77xx Evaluation-Module Quick-Start-Guide. Note that the following .ini files should be used:

- TX DAC: Use AFE77xx_2x2TX_44210_tdd.ini.
- RX ADC: Use AFE77xx_2x2RX_24410_tdd.ini.
- FB ADC: Use AFE77xx_2x1FB_22210_tdd.ini.

All these .ini files are distributed with Latte_GUI_TDD_MODE installer.

4.1 Transmitter TDD Evaluation

The transmit DAC should be set up in HSDCPRO before the receiver or feedback ADC because the TDD ON/OFF pattern is defined in the DAC pattern file. The sequence to evaluate the transmit DAC in TDD mode are as follows:

1. Generate a TDD pattern into HSDCPRO compatible with the format described in Section 3.2.
2. Load the generated test pattern into HSDCPRO and send the loaded pattern to the TSW14J56EVM.

In HSDCPRO, the channel view can be switched to channel 3 to display the TDD pattern ON/OFF times as shown in Figure 4-1. The other channels (1 and 2) show the actual signal waveform.

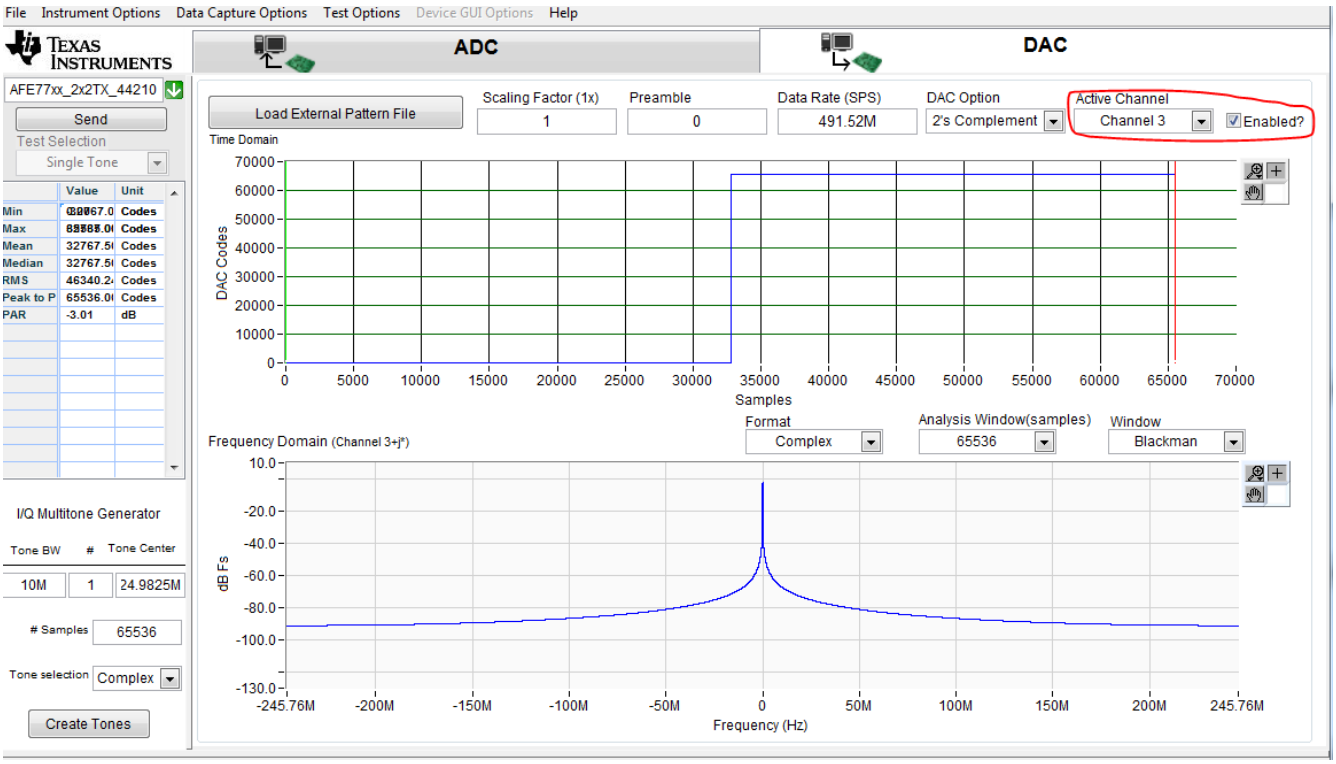

Figure 4-1. HSDCPRO DAC Tab Showing the TDD Test Pattern on Channel 3

4.1.1 Making Time-gated Measurements

Without gating the spectrum analyzer with the TDD test pattern, the spectrum of the TDD signal shows a lot of spurious signals because of the time discontinuity of the signal. The following steps show how to make time-gated measurements with a PXA or MXA spectrum analyzer:

1. Sweep control >> Gate >> ON
2. Sweep control >> Gate View >> Off
3. Sweep control >> Gate Method >> LO
4. Sweep control >> More >> Gate Source >> External 1
   a. Make sure to make the TDD pattern connection to the external trigger 1 input of spectrum analyzer described in Section 3.1.
5. Sweep control >> More >> Gate Source >> External 1 >> Trigger Level >> 500 mV
6. Sweep control >> More >> Control >> Level

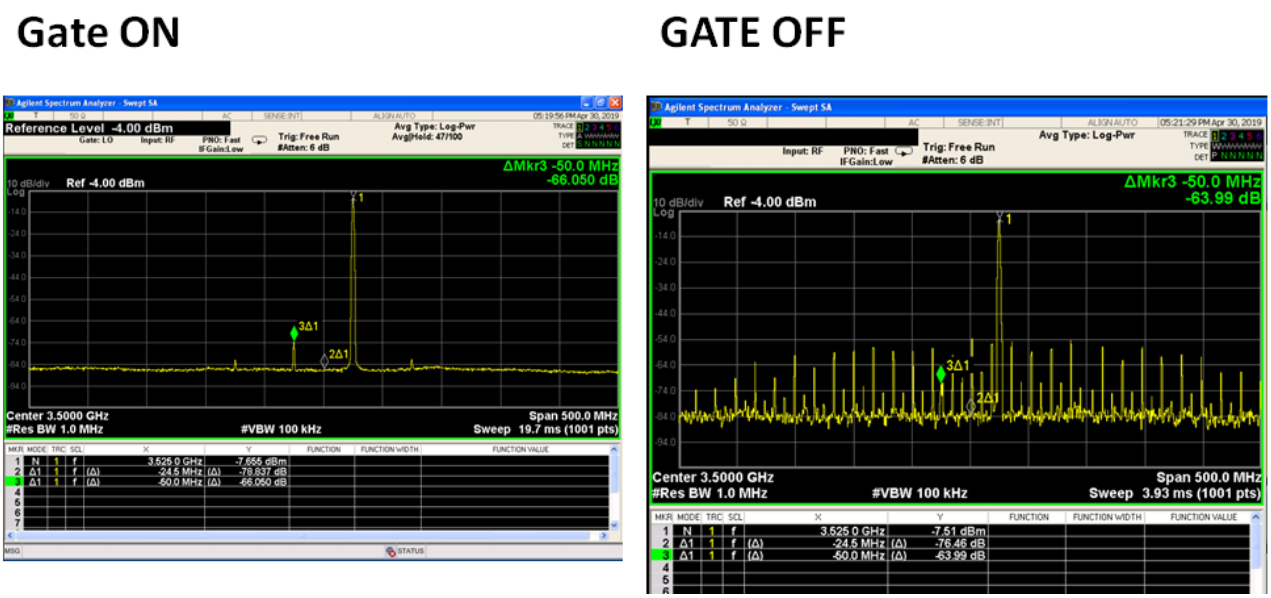

Figure 4-2. Spectrum of Transmitter Output with Gating On vs Off

The gate view can also be enabled in the spectrum analyzer to view the transmitter output power versus time and also to set the gate start and stop times as shown in Figure 4-3.

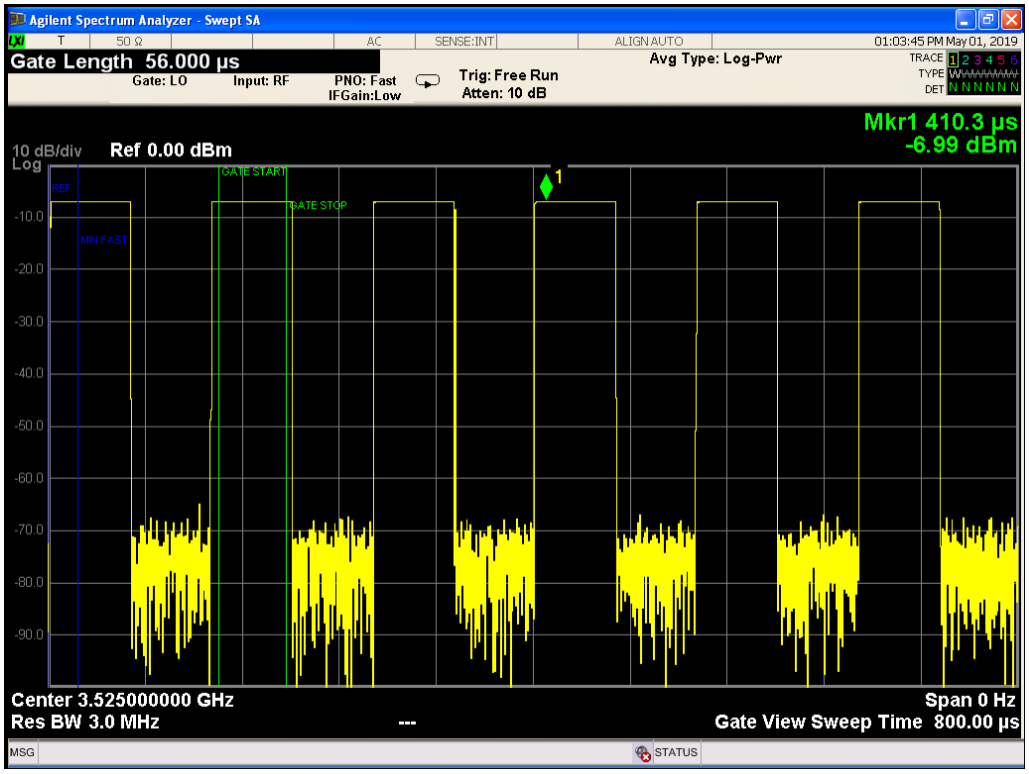

Figure 4-3. Gate View Showing Transmitter Output Power vs Time

4.2 Receiver TDD Evaluation

The sequence below can be used to evaluate the receiver and feedback ADCs in TDD mode.

1. Switch to the ADC tab in HSDCPRO and select the .ini file for receiver or feedback ADC.
2. Set up the data rate and click Capture button to acquire data from the AFE77xx receiver or feedback ADC.
3. In the Codes view (circled in red in Figure 4-4), move the green marker to the start of the data pattern during the time RX TDD signal is ON.
4. Change the Analysis Window size (number of samples to be used for FFT) so that the red marker (in the codes view) is at the end (or within) the data pattern during the time RX TDD is ON.

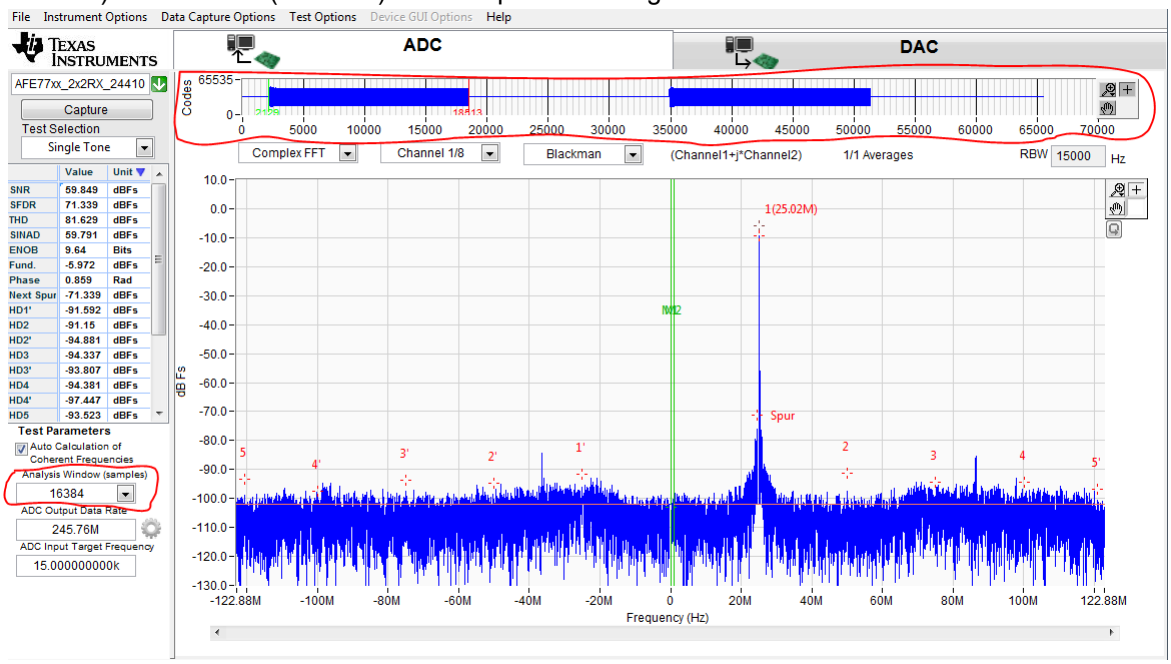

Figure 4-4. Spectrum of Receiver ADC in TDD Mode

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2019) to Revision A (April 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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