

AMC1311-Q1

Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for AMC1311-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

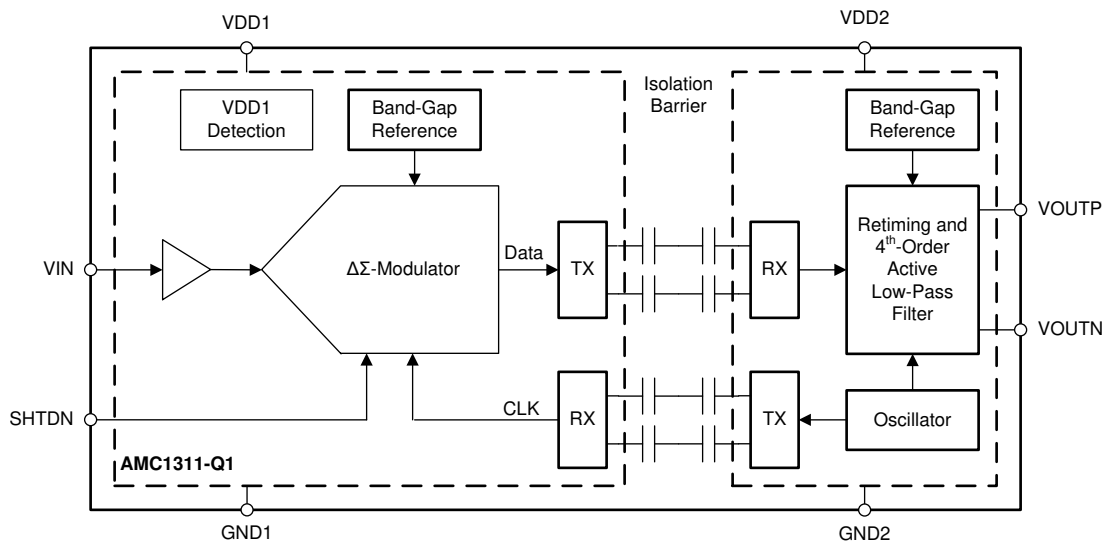


Figure 1. Functional Block Diagram

AMC1311-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for AMC1311-Q1 based on two different industry-wide used reliability standards:

- [Table 1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	17
Die FIT Rate	3
Package FIT Rate	14

The failure rate and mission profile information in [Table 1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 98 mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for AMC1311-Q1 in [Table 3](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output out of specification (gain error)	20%
Output out of specification (offset error)	20%
Output out of specification (differential output at positive or negative full-scale)	20%
VOUTN stuck high or low	10%
VOUTP stuck high or low	10%
Reduced CMTI performance	9%
Output out of specification (spikes, increased noise)	5%
Device behavior undetermined	5%
Output fail-safe function fails to indicate an error ⁽¹⁾	1%

⁽¹⁾ Die faults that lead to a fail-safe indication of an error on the output are excluded.

The FMD in [Table 3](#) excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the AMC1311-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 5](#))
- Pin open-circuited (see [Table 6](#))
- Pin short-circuited to an adjacent pin (see [Table 7](#))
- Pin short-circuited to supply (see [Table 8](#))

[Table 5](#) through [Table 8](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4](#).

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 2](#) shows the AMC1311-Q1 pin diagram. For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the AMC1311-Q1 datasheet.

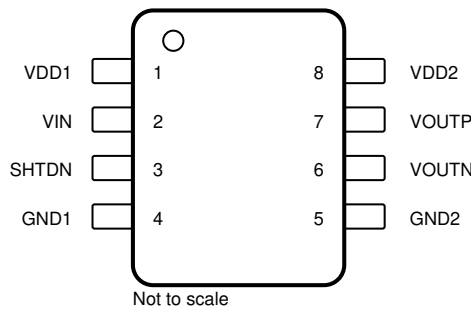


Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- SHTDN pin is permanently tied to GND1 through 10-kOhm pull-down resistor.
- RC filter on VIN.
Series resistor is sized to limit the input currents into VIN to <10 mA in all circumstances, e.g. also in case device is unpowered and input signal is applied.
- For pins on primary side:
'Short-circuited to ground' means short to GND1.
'Short-circuited to supply' means short to VDD1.
- For pins on secondary side:
'Short-circuited to ground' means short to GND2.
'Short-circuited to supply' means short to VDD2.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	Device primary side unpowered. Fail-safe output (see datasheet for more details). Observe that the absolute maximum ratings for VIN of the device are met, otherwise device damage may be plausible.	A
VIN	2	VIN stuck low (GND1). Differential output (VOUTP – VOUTN) = 0 V with common-mode voltage ~1.44 V.	B
SHTDN	3	No effect. Normal operation.	D
GND1	4	No effect. Normal operation.	D
GND2	5	No effect. Normal operation.	D
VOUTN	6	VOUTN stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
VOUTP	7	VOUTP stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	Device secondary side unpowered. VOUTP and VOUTN pins are driven to GND2.	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	Device primary side unpowered. Fail-safe output (see datasheet for more details).	B
VIN	2	Differential output (VOUTP – VOUTN) undetermined.	B
SHTDN	3	Internal 100-kΩ pull-up resistor drives SHTDN pin to VDD1. Device is in shutdown. Fail-safe output (see datasheet for more details).	B
GND1	4	Primary side will be powered through ESD diode on SHTDN pin to GND1. Internal GND1 node of device is lifted by one diode drop compared to external GND1 potential. Differential output (VOUTP – VOUTN) = (VIN – ~300 mV). For VIN close to 0 V the differential output will be negative.	B
GND2	5	Device behavior undetermined. VOUTN and VOUTP undetermined.	B
VOUTN	6	Differential output (VOUTP – VOUTN) undetermined.	B
VOUTP	7	Differential output (VOUTP – VOUTN) undetermined.	B
VDD2	8	Device secondary side unpowered. VOUTP and VOUTN pins are driven to GND2.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	VIN	VIN stuck high (VDD1). VOUTP and VOUTN pins clipped at differential ~+2.516 V.	B
VIN	2	SHTDN	Voltage on VIN smaller than expected because of resistor divider formed by series resistor on VIN and pull-down resistor on SHTDN pin. Result is increased gain error on differential output. VIN will drive the SHTDN pin. Device in shutdown if SHTDN is driven above logic high level. In that case fail-safe output (see datasheet for more details).	B
SHTDN	3	GND1	No effect. Normal operation.	D
GND1	4	GND2	Not considered. Corner pin.	D
GND2	5	VOUTN	VOUTN stuck low (GND2). Excess current consumption from VDD2 source because of short-circuit condition. Device damage plausible if condition is present for extended period of time.	A
VOUTN	6	VOUTP	Differential output (VOUTP – VOUTN) = 0 V with common-mode voltage ~1.44 V. Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VOUTP	7	VDD2	VOUTP stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	VDD1	Not considered. Corner pin.	D

Table 8. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VDD1	1	No effect. Normal operation.	D
VIN	2	VIN stuck high (VDD1). VOUTP and VOUTN pins clipped at differential ~+2.516 V.	B
SHTDN	3	SHTDN stuck high (VDD1). Device is in shutdown. Fail-safe output (see datasheet for more details).	B
GND1	4	Device primary side unpowered. Fail-safe output (see datasheet for more details). Observe that the absolute maximum ratings for VIN of the device are met, otherwise device damage may be plausible.	A
GND2	5	Device secondary side unpowered. VOUTP and VOUTN pins are driven to GND2.	B
VOUTN	6	VOUTN stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VOUTP	7	VOUTP stuck high (VDD2). Excess current consumption from VDD2 source. Device damage plausible if condition is present for extended period of time.	A
VDD2	8	No effect. Normal operation.	D

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