Application Note

TAA52xx Power Consumption Matrix Across Various Usage Scenarios

Pavan Kumar M

ABSTRACT

This application note details the power consumption of TAA52xx devices across various usage scenarios. Applicable devices include:

- TAA5242
- TAA5212

Table of Contents

List of Tables

Trademarks

1 Introduction

Power consumption in TAA52xx devices is highly dependent on the enabled features and usage scenarios. The following tables summarize the power consumption across:

- Supply voltage
- Sampling frequency
- Enabled channel count
- Decimation filter
- Bit clock to frame sync ratio
- PLL state (enabled or disabled)
- Converted word length

The following tables report the average idle-channel current consumed on the analog supply (AVDD). This supply includes all the internal analog and digital circuits but excludes the current consumed by the I/O (input/output) pins due to application dependencies. I/O power is dependent upon:

- Load capacitance of the system bus interface
- Data output clock rate
- Data conversion output activity
- Bus interface pullup or pulldown
- Frequency of I^2C commands sent by the host

2 Target Mode Power Consumption with PLL Disabled

This section describes the typical current consumption of the TAA52xx devices, when the PLL is disabled, with AVDD set to 1.8V and 3.3V.

The PLL is disabled by setting the corresponding bit field B0_P0_R52[7] (PLL_DIS) and enabling (ADC_LOW_PWR_FILT) bit field: B0_P0_R78[2] with PLL disabled.

By default, the bit clock is used as the clock source to the internal block. Alternatively, an external clock source (CCLK) can be used in the device through one of the GPI-capable pins (GPIOx or GPIx), if the system has a low jitter clock available.

- If GPIOx is used for CCLK input, the appropriate GPIOx_CFG bit field in the GPIOx_CFG0 register must be configured for GPI function.
- If GPIx is used for CCLK input, the appropriate GPIx_CFG bit field in the GPI_CFG register must be enabled for GPI function.
- The pin configured for GPI must be configured as CCLK, this is done by configuring B0_P0_R15[6:5] (CCLK_SEL), based on the pin configured.
- With the CCLK configured, the external CCLK must be used as the clock source, this is done by configuring B0_P0_R52[3:1] (CLK_SRC_SEL).
- The CCLK must be synchronized with the frame sync. For example, the CCLK frequency must be an integer multiple of the frame sync frequency.
- Once configured, the device runs on the external CCLK as the clock source.

In Table 2-1, the power consumption measurements have all the biquad filters disabled, the ADC input (or inputs) is (are) grounded, and an external CCLK is provided as the clock source to the device through the GPIO1 pin.

Table 2-1. Target Mode Power Consumption with PLL Disabled

CCLK Frequency (MHz)	Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC CIC 4th Order	ADC DEMRATE OVERLOAD 2X	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)
12.288	8	32	32	1	Disabled	Disabled	2.88	118.75	-106.12	3.21	124.61	-97.04
12.288	8	32	32	1	Disabled	Enabled	2.75	118.8	-107.24	3.08	124.73	-97.74
12.288	8	32	32	1	Enabled	Disabled	2.88	118.78	-105.73	3.21	124.88	-97.22
12.288	8	48	24	2	Disabled	Disabled	4.64	118.95	-105.49	5.14	124.68	-97.39
12.288	8	48	24	2	Disabled	Enabled	4.43	118.5	-107.13	4.93	124.74	-97.64
12.288	8	48	24	2	Enabled	Disabled	4.64	118.63	-105.28	5.15	124.76	-97.31
12.288	16	24	24	1	Disabled	Disabled	3.28	115.34	-104.35	3.62	121.33	-96.9
12.288	16	24	24	1	Disabled	Enabled	3.15	115.37	-106.1	3.48	121.32	-97.66
12.288	16	24	24	1	Enabled	Disabled	3.27	115.49	-104.28	3.61	121.4	-96.94
12.288	16	48	24	2	Disabled	Disabled	5.42	115.42	-103.4	5.92	121.25	-97.21
12.288	16	48	24	2	Disabled	Enabled	5.21	115.39	-105.34	5.71	121.24	-97.64
12.288	16	48	24	2	Enabled	Disabled	5.4	115.41	-103.42	5.9	121.2	-97.04
12.288	24	24	24	1	Disabled	Disabled	3.24	112.46	-103.03	3.57	115.85	-96.78
12.288	24	24	24	1	Disabled	Enabled	3.11	112.52	-104.62	3.43	115.85	-97.54
12.288	24	24	24	1	Enabled	Disabled	3.22	112.24	-103.12	3.56	115.91	-96.79
12.288	24	48	24	2	Disabled	Disabled	5.25	114.06	-103.08	5.75	119.78	-96.91
12.288	24	48	24	2	Disabled	Enabled	5.04	114.05	-104.79	5.54	119.62	-97.91
12.288	24	48	24	2	Enabled	Disabled	5.23	113.95	-103.09	5.73	119.89	-97.07

Table 2-1. Target Mode Power Consumption with PLL Disabled (continued)

CCLK Frequency (MHz)	Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC CIC 4th Order	ADC DEMRATE OVERLOAD 2X	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)
12.288	32	24	24	1	Disabled	Disabled	3.42	113.74	-103.5	3.75	119.61	-96.96
12.288	32	24	24	1	Disabled	Enabled	3.29	113.54	-104.77	3.61	119.31	-97.72
12.288	32	24	24	1	Enabled	Disabled	3.4	113.49	-103.46	3.73	119.61	-96.99
12.288	32	48	24	2	Disabled	Disabled	5.62	113.61	-102.73	6.13	119.57	-96.96
12.288	32	48	24	2	Disabled	Enabled	5.41	113.51	-104.11	5.92	119.24	-97.62
12.288	32	48	24	2	Enabled	Disabled	5.62	113.58	-102.56	6.11	119.52	-96.94
12.288	48	24	24	1	Disabled	Disabled	2.97	109.97	-102.08	3.31	111.24	-96.7
12.288	48	24	24	1	Disabled	Enabled	2.84	107.77	-103.01	3.17	108.44	-97.5
12.288	48	24	24	1	Enabled	Disabled	2.96	107.6	-101.25	3.3	108.2	-96.44
12.288	48	48	24	2	Disabled	Disabled	4.65	110.01	-101.46	5.16	111.2	-96.67
12.288	48	48	24	2	Disabled	Enabled	4.44	107.85	-102.63	4.94	108.42	-97.42
12.288	48	48	24	2	Enabled	Disabled	4.63	107.29	-100.83	5.13	107.58	-96.45
12.288	96	24	24	1	Disabled	Disabled	3.4	87.9	-85.16	3.74	87.33	-84.71
12.288	96	24	24	1	Disabled	Enabled	3.27	87.76	-85.12	3.6	87.36	-84.63
12.288	96	24	24	1	Enabled	Disabled	3.39	86.34	-83.64	3.72	85.97	-83.31
12.288	96	48	24	2	Disabled	Disabled	5.33	88.01	-85.07	5.84	87.22	-84.63
12.288	96	48	24	2	Disabled	Enabled	5.12	87.62	-85.21	5.62	87.04	-84.53
12.288	96	48	24	2	Enabled	Disabled	5.3	86.45	-83.63	5.81	85.69	-83.29
12.288	192	24	24	1	Disabled	Disabled	4.88	113.08	-103.22	5.22	118.09	-96.67
12.288	192	24	24	1	Disabled	Enabled	4.75	113.08	-104.68	5.08	117.78	-97.68
12.288	192	24	24	1	Enabled	Disabled	4.83	113.18	-103.28	5.16	118.11	-96.79
6.144	8	32	32	1	Disabled	Disabled	2.56	118.83	-107.38	2.89	125.12	-98.07
6.144	8	32	32	1	Disabled	Enabled	2.56	119.14	-107.44	2.88	124.75	-97.99
6.144	8	32	32	1	Enabled	Disabled	2.56	118.96	-107.4	2.89	124.95	-98.18
6.144	8	48	24	2	Disabled	Disabled	4.25	118.74	-107.08	4.74	124.63	-98
6.144	8	48	24	2	Disabled	Enabled	4.25	118.89	-106.95	4.74	124.64	-98.08
6.144	8	48	24	2	Enabled	Disabled	4.25	118.85	-106.97	4.74	124.87	-98.08
6.144	16	24	24	1	Disabled	Disabled	2.96	115.4	-106.25	3.29	121.21	-97.9
6.144	16	24	24	1	Disabled	Enabled	2.96	115.42	-106.27	3.29	121.21	-97.97
6.144	16	24	24	1	Enabled	Disabled	2.95	115.58	-106.28	3.28	121.35	-98.09
6.144	16	48	24	2	Disabled	Disabled	5.02	115.38	-105.55	5.52	121.03	-97.96
6.144	16	48	24	2	Disabled	Enabled	5.02	115.21	-105.25	5.52	121.25	-98.07
6.144	16	48	24	2	Enabled	Disabled	5	115.48	-105.46	5.5	121.22	-97.95
6.144	24	24	24	1	Disabled	Disabled	2.87	112.44	-104.69	3.2	115.65	-97.87
6.144	24	24	24	1	Disabled	Enabled	2.87	112.29	-104.69	3.2	115.64	-97.9

Table 2-1. Target Mode Power Consumption with PLL Disabled (continued)

CCLK Frequency (MHz)	Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC CIC 4th Order	ADC DEMRATE OVERLOAD 2X	AVDD = 1.8V			AVDD = 3.3V		
							AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB-Aweighted)	THD+N (dB)
6.144	24	24	24	1	Enabled	Disabled	2.86	112.35	-104.82	3.18	115.71	-97.88
6.144	24	48	24	2	Disabled	Disabled	4.8	114.01	-104.76	5.31	119.41	-98.23
6.144	24	48	24	2	Disabled	Enabled	4.81	113.96	-104.8	5.3	119.45	-97.84
6.144	24	48	24	2	Enabled	Disabled	4.78	113.99	-104.85	5.28	119.35	-97.98
6.144	32	24	24	1	Disabled	Disabled	3.1	113.55	-104.95	3.43	119.23	-97.89
6.144	32	24	24	1	Disabled	Enabled	3.1	113.5	-104.94	3.43	119.28	-98.07
6.144	32	24	24	1	Enabled	Disabled	3.09	113.65	-104.96	3.41	119.41	-97.85
6.144	48	24	24	1	Disabled	Disabled	2.6	107.99	-103.19	2.93	108.54	-97.56
6.144	48	24	24	1	Disabled	Enabled	2.61	107.86	-103.1	2.93	108.52	-97.68
6.144	48	24	24	1	Enabled	Disabled	2.59	105.76	-102.3	2.92	106.32	-97.42
6.144	48	48	24	2	Disabled	Disabled	4.21	107.75	-102.57	4.7	108.37	-97.33
6.144	48	48	24	2	Disabled	Enabled	4.21	107.88	-102.51	4.7	108.38	-97.41
6.144	48	48	24	2	Enabled	Disabled	4.19	105.84	-101.67	4.68	105.86	-97.43
6.144	96	24	24	1	Disabled	Disabled	3.03	87.94	-85.12	3.37	87.4	-84.63
6.144	96	24	24	1	Disabled	Enabled	3.03	87.9	-85.08	3.37	87.47	-84.67
6.144	96	24	24	1	Enabled	Disabled	3.02	86.46	-83.8	3.35	85.92	-83.46
6.144	96	48	24	2	Disabled	Disabled	4.9	87.97	-85.01	5.4	87.08	-84.52
6.144	96	48	24	2	Disabled	Enabled	4.9	87.98	-85.13	5.4	87.12	-84.68
6.144	96	48	24	2	Enabled	Disabled	4.87	86.2	-83.62	5.37	85.64	-83.3

3 Target Mode Power Consumption With PLL Enabled

This section describes the typical current consumption of the TAA52xx when the PLL is enabled with AVDD set to 1.8V and 3.3V.

By default, upon power-up, the PLL is configured as enabled. The bit field corresponding to this configuration is B0_P0_R52[7] (**PLL_DIS**) in the register map.

In Table 3-1, the current consumption measurements have the biquad filters disabled and the ADC inputs are grounded.

Table 3-1. Target Mode Power Consumption With PLL Enabled

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
8	32	32	1	Disabled	Disabled	Disabled	Linear Phase	5.22	118.92	-105.58	5.57	124.75	-97.03
8	32	32	1	Disabled	Disabled	Disabled	Low Latency	5.23	118.85	-105.69	5.57	124.83	-97.1
8	32	32	1	Disabled	Disabled	Disabled	Ultra Low Latency	5.23	118.75	-105.64	5.56	124.79	-97.12
8	32	32	1	Disabled	Disabled	Enabled	Linear Phase	4.95	119.01	-107.65	5.28	124.61	-97.94
8	32	32	1	Disabled	Disabled	Enabled	Low Latency	4.95	118.85	-107.85	5.28	124.79	-98.15
8	32	32	1	Disabled	Disabled	Enabled	Ultra Low Latency	4.95	118.67	-107.75	5.28	125.04	-98.02
8	32	32	1	Disabled	Enabled	Disabled	Linear Phase	5.23	118.74	-105.62	5.56	124.81	-97.02
8	32	32	1	Disabled	Enabled	Disabled	Low Latency	5.23	118.68	-105.7	5.57	124.47	-97.15
8	32	32	1	Disabled	Enabled	Disabled	Ultra Low Latency	5.23	118.84	-105.72	5.56	125.1	-97.18
8	32	32	1	Enabled	Disabled	Disabled	Linear Phase	5.23	118.77	-105.85	5.57	124.89	-97.12
8	32	32	1	Enabled	Disabled	Enabled	Linear Phase	4.95	118.9	-107.68	5.28	124.62	-97.92
8	32	32	1	Enabled	Enabled	Disabled	Linear Phase	5.23	118.65	-105.68	5.57	124.57	-97.05
8	48	24	2	Disabled	Disabled	Disabled	Linear Phase	7.01	119.03	-105.64	7.53	124.78	-97.06
8	48	24	2	Disabled	Disabled	Disabled	Low Latency	7.02	118.79	-105.3	7.52	124.65	-97.09
8	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	7.02	118.85	-105.55	7.53	124.72	-97.15
8	48	24	2	Disabled	Disabled	Enabled	Linear Phase	6.65	118.61	-107.57	7.16	124.54	-98.07
8	48	24	2	Disabled	Disabled	Enabled	Low Latency	6.65	118.73	-107.73	7.16	124.71	-97.99
8	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	6.65	118.97	-107.56	7.16	124.56	-98.01
8	48	24	2	Disabled	Enabled	Disabled	Linear Phase	7.02	118.72	-105.61	7.53	124.63	-97.23
8	48	24	2	Disabled	Enabled	Disabled	Low Latency	7.02	118.51	-105.54	7.53	124.6	-97.25
8	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	7.01	118.95	-105.46	7.53	124.78	-97.14
8	48	24	2	Enabled	Disabled	Disabled	Linear Phase	7.02	118.7	-105.38	7.53	124.77	-97.22

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
8	48	24	2	Enabled	Disabled	Enabled	Linear Phase	6.65	118.65	-107.33	7.16	124.88	-98.2
8	48	24	2	Enabled	Enabled	Disabled	Linear Phase	7.02	118.75	-105.61	7.53	124.8	-97.21
16	24	24	1	Disabled	Disabled	Disabled	Linear Phase	6	115.4	-104.19	6.35	121.15	-96.9
16	24	24	1	Disabled	Disabled	Disabled	Low Latency	6.01	115.42	-104.35	6.35	121.4	-96.98
16	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	6.01	115.3	-104.15	6.35	121.31	-96.96
16	24	24	1	Disabled	Disabled	Enabled	Linear Phase	5.72	115.29	-106.47	6.06	121.27	-98.05
16	24	24	1	Disabled	Disabled	Enabled	Low Latency	5.73	115.37	-106.31	6.06	121.23	-97.85
16	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	5.73	115.34	-106.41	6.07	121.14	-97.79
16	24	24	1	Disabled	Enabled	Disabled	Linear Phase	6	115.43	-104.29	6.34	121.26	-96.98
16	24	24	1	Disabled	Enabled	Disabled	Low Latency	6	115.47	-104.22	6.34	121.18	-96.91
16	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	6	115.33	-104.21	6.35	121.45	-97.02
16	24	24	1	Enabled	Disabled	Disabled	Linear Phase	6.01	115.29	-104.32	6.35	121.2	-96.91
16	24	24	1	Enabled	Disabled	Enabled	Linear Phase	5.73	115.44	-106.39	6.06	121.09	-97.95
16	24	24	1	Enabled	Enabled	Disabled	Linear Phase	6	115.53	-104.27	6.34	121.32	-96.93
16	48	24	2	Disabled	Disabled	Disabled	Linear Phase	8.18	115.41	-103.87	8.7	121.34	-97.03
16	48	24	2	Disabled	Disabled	Disabled	Low Latency	8.18	115.37	-103.71	8.7	121.32	-97.06
16	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	8.18	115.44	-103.86	8.69	121.36	-96.93
16	48	24	2	Disabled	Disabled	Enabled	Linear Phase	7.82	115.37	-106.04	8.33	121.05	-98.12
16	48	24	2	Disabled	Disabled	Enabled	Low Latency	7.82	115.39	-106.33	8.33	121.18	-97.87
16	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	7.82	115.35	-106.25	8.33	121.17	-97.98
16	48	24	2	Disabled	Enabled	Disabled	Linear Phase	8.17	115.49	-103.71	8.68	121.28	-97.07
16	48	24	2	Disabled	Enabled	Disabled	Low Latency	8.17	115.43	-103.49	8.67	121.24	-97.11
16	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	8.17	115.42	-103.64	8.68	121.24	-96.99
16	48	24	2	Enabled	Disabled	Disabled	Linear Phase	8.18	115.35	-103.78	8.7	121.49	-97.02
16	48	24	2	Enabled	Disabled	Enabled	Linear Phase	7.82	115.53	-106.21	8.33	120.87	-97.77
16	48	24	2	Enabled	Enabled	Disabled	Linear Phase	8.17	115.47	-103.85	8.68	121.22	-97.17
24	24	24	1	Disabled	Disabled	Disabled	Linear Phase	6.85	114.13	-103.92	7.2	120.01	-96.96
24	24	24	1	Disabled	Disabled	Disabled	Low Latency	6.84	113.92	-103.78	7.18	119.93	-96.87
24	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	6.75	113.86	-103.68	7.1	119.86	-96.89

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
24	24	24	1	Disabled	Disabled	Enabled	Linear Phase	6.29	114.15	-105.84	6.63	119.99	-98.02
24	24	24	1	Disabled	Disabled	Enabled	Low Latency	6.27	113.98	-105.6	6.61	119.5	-97.92
24	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	6.18	113.93	-105.49	6.53	119.61	-97.87
24	24	24	1	Disabled	Enabled	Disabled	Linear Phase	6.85	114.16	-103.9	7.19	120.07	-96.99
24	24	24	1	Disabled	Enabled	Disabled	Low Latency	6.83	113.91	-103.81	7.17	119.96	-96.93
24	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	6.74	114.02	-103.78	7.09	119.91	-96.98
24	24	24	1	Enabled	Disabled	Disabled	Linear Phase	6.85	114.16	-103.97	7.2	120.1	-97.05
24	24	24	1	Enabled	Disabled	Enabled	Linear Phase	6.29	114.19	-105.71	6.63	119.8	-97.85
24	24	24	1	Enabled	Enabled	Disabled	Linear Phase	6.85	114.16	-103.81	7.19	120.17	-96.91
24	48	24	2	Disabled	Disabled	Disabled	Linear Phase	8.36	114.18	-103.46	8.87	119.99	-96.93
24	48	24	2	Disabled	Disabled	Disabled	Low Latency	8.32	114.08	-103.21	8.83	119.86	-97.13
24	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	8.14	114.05	-103.37	8.66	119.84	-97.04
24	48	24	2	Disabled	Disabled	Enabled	Linear Phase	7.99	114.07	-105.5	8.51	119.78	-97.94
24	48	24	2	Disabled	Disabled	Enabled	Low Latency	7.96	114.05	-105.21	8.47	119.72	-98.04
24	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	7.79	113.94	-105.29	8.29	119.53	-98.07
24	48	24	2	Disabled	Enabled	Disabled	Linear Phase	8.34	114	-103.22	8.85	120.08	-97.15
24	48	24	2	Disabled	Enabled	Disabled	Low Latency	8.3	113.97	-103.21	8.82	119.87	-97.06
24	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	8.13	113.88	-103.1	8.64	120.01	-97.14
24	48	24	2	Enabled	Disabled	Disabled	Linear Phase	8.35	114.19	-103.44	8.87	120.05	-97.15
24	48	24	2	Enabled	Disabled	ENABLED	Linear Phase	8	114.22	-105.4	8.51	119.97	-97.8
24	48	24	2	Enabled	Enabled	Disabled	Linear Phase	8.34	114.13	-103.3	8.85	119.96	-97.01
32	24	24	1	Disabled	Disabled	Disabled	Linear Phase	6.89	113.56	-103.43	7.24	119.36	-96.98
32	24	24	1	Disabled	Disabled	Disabled	Low Latency	6.86	113.41	-103.4	7.21	119.3	-96.81
32	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	6.75	113.46	-103.3	7.09	119.34	-96.92
32	24	24	1	Disabled	Disabled	Enabled	Linear Phase	6.6	113.66	-105.12	6.94	119.05	-97.9
32	24	24	1	Disabled	Disabled	Enabled	Low Latency	6.58	113.3	-105.09	6.92	118.93	-97.82
32	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	6.46	113.33	-104.95	6.81	118.92	-97.95
32	24	24	1	Disabled	Enabled	Disabled	Linear Phase	6.88	113.55	-103.52	7.22	119.38	-97
32	24	24	1	Disabled	Enabled	Disabled	Low Latency	6.86	113.38	-103.28	7.2	119.27	-96.85

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
32	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	6.74	113.4	-103.38	7.09	119.25	-96.89
32	24	24	1	Enabled	Disabled	Disabled	Linear Phase	6.89	113.74	-103.41	7.24	119.22	-96.97
32	24	24	1	Enabled	Disabled	Enabled	Linear Phase	6.6	113.6	-105.12	6.95	119.01	-97.82
32	24	24	1	Enabled	Enabled	Disabled	Linear Phase	6.88	113.61	-103.44	7.22	119.58	-96.9
32	48	24	2	Disabled	Disabled	Disabled	Linear Phase	9.16	113.66	-103.19	9.69	119.44	-96.86
32	48	24	2	Disabled	Disabled	Disabled	Low Latency	9.12	113.35	-102.98	9.64	119.27	-97.09
32	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	8.89	113.36	-102.91	9.41	119.3	-96.96
32	48	24	2	Disabled	Disabled	Enabled	Linear Phase	8.81	113.5	-104.98	9.33	119.07	-97.71
32	48	24	2	Enabled	Enabled	Enabled	Low Latency	8.76	113.46	-104.8	9.27	119.01	-97.82
32	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	8.52	113.4	-104.66	9.04	118.83	-97.91
32	48	24	2	Disabled	Enabled	Disabled	Linear Phase	9.15	113.53	-103.13	9.66	119.29	-97.02
32	48	24	2	Disabled	Enabled	Disabled	Low Latency	9.11	113.35	-102.82	9.63	119.32	-97.02
32	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	8.88	113.45	-102.78	9.4	119.32	-97.02
32	48	24	2	Enabled	Disabled	Disabled	Linear Phase	9.16	113.63	-103.04	9.69	119.45	-97.1
32	48	24	2	Enabled	Disabled	Enabled	Linear Phase	8.81	113.56	-104.75	9.33	119.15	-97.82
32	48	24	2	Enabled	Enabled	Disabled	Linear Phase	9.15	113.48	-103	9.66	119.55	-97.1
48	24	24	1	Disabled	Disabled	Disabled	Linear Phase	8.29	113.3	-103.05	8.64	119.17	-96.85
48	24	24	1	Disabled	Disabled	Disabled	Low Latency	8.17	113.38	-103.01	8.52	119.27	-96.87
48	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	8	113.36	-102.95	8.35	119.19	-96.96
48	24	24	1	Disabled	Disabled	Enabled	Linear Phase	8	113.19	-104.42	8.35	118.83	-97.94
48	24	24	1	Disabled	Disabled	Enabled	Low Latency	7.89	113.31	-104.54	8.23	118.77	-97.73
48	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	7.71	113.25	-104.63	8.05	118.87	-97.93
48	24	24	1	Disabled	Enabled	Disabled	Linear Phase	8.28	113.31	-103.14	8.62	119	-96.82
48	24	24	1	Disabled	Enabled	Disabled	Low Latency	8.16	113.12	-103.06	8.51	119.1	-96.93
48	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	7.99	113.32	-103.1	8.34	119.12	-96.85
48	24	24	1	Enabled	Disabled	Disabled	Linear Phase	7.7	110.27	-102.2	8.04	111.79	-96.67
48	24	24	1	Enabled	Disabled	Enabled	Linear Phase	7.41	108.06	-103.31	7.76	108.71	-97.49
48	24	24	1	Enabled	Enabled	Disabled	Linear Phase	7.69	107.59	-101.24	8.03	108.21	-96.37
48	48	24	2	Disabled	Disabled	Disabled	Linear Phase	10.66	113.26	-102.73	11.18	119.12	-96.84

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
48	48	24	2	Disabled	Disabled	Disabled	Low Latency	10.42	113.31	-102.71	10.95	119.22	-96.95
48	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	10.08	113.31	-102.67	10.59	119.32	-97.05
48	48	24	2	Disabled	Disabled	Enabled	Linear Phase	10.31	113.24	-104.49	10.82	118.6	-98.01
48	48	24	2	Disabled	Disabled	Enabled	Low Latency	10.07	113.13	-104.43	10.59	118.7	-97.67
48	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	9.72	113.27	-104.37	10.24	118.63	-98.04
48	48	24	2	Disabled	Enabled	Disabled	Linear Phase	10.64	113.25	-102.75	11.16	119.14	-97.08
48	48	24	2	Disabled	Enabled	Disabled	Low Latency	10.41	113.3	-102.56	10.92	119.2	-96.91
48	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	10.06	113.22	-102.66	10.58	119.2	-97.09
48	48	24	2	Enabled	Disabled	Disabled	Linear Phase	9.48	110.3	-101.77	10	111.48	-96.71
48	48	24	2	Disabled	Disabled	Enabled	Linear Phase	9.12	107.87	-102.97	9.64	108.57	-97.63
48	48	24	2	Disabled	Enabled	Disabled	Linear Phase	9.46	107.59	-101.13	9.98	107.84	-96.65
96	24	24	1	Disabled	Disabled	Disabled	Linear Phase	11.52	113.45	-103.17	11.87	119.33	-96.84
96	24	24	1	Disabled	Disabled	Disabled	Low Latency	11.27	113.33	-103.09	11.63	119.21	-96.93
96	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	10.92	113.5	-103.11	11.27	119.27	-96.87
96	24	24	1	Disabled	Disabled	Enabled	Linear Phase	11.38	113.34	-104.55	11.72	118.81	-97.76
96	24	24	1	Disabled	Disabled	Enabled	Low Latency	11.13	113.3	-104.45	11.48	118.86	-97.81
96	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	10.77	113.37	-104.49	11.13	118.72	-97.92
96	24	24	1	Disabled	Enabled	Disabled	Linear Phase	11.5	113.23	-103.01	11.85	119.25	-96.8
96	24	24	1	Disabled	Enabled	Disabled	Low Latency	11.26	113.31	-103.03	11.62	119.24	-96.89
96	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	10.91	113.33	-103.2	11.26	119.31	-96.87
96	24	24	1	Enabled	Disabled	Disabled	Linear Phase	10.33	87.98	-85.02	10.68	87.45	-84.71
96	24	24	1	Enabled	Disabled	Enabled	Linear Phase	10.19	87.75	-85.1	10.53	87.17	-84.77
96	24	24	1	Enabled	Enabled	Disabled	Linear Phase	10.32	86.5	-83.58	10.67	85.79	-83.5
96	48	24	2	Disabled	Disabled	Disabled	Linear Phase	14.87	113.32	-102.71	15.4	119.36	-96.87
96	48	24	2	Disabled	Disabled	Disabled	Low Latency	14.39	113.25	-102.7	14.92	119.36	-97.06
96	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	13.69	113.23	-102.61	14.21	119.22	-97.06
96	48	24	2	Disabled	Disabled	Enabled	Linear Phase	14.66	113.25	-104.42	15.18	118.83	-97.72
96	48	24	2	Disabled	Disabled	Enabled	Low Latency	14.18	113.26	-104.21	14.69	118.79	-97.84

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
96	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	13.47	113.13	-104.33	13.99	118.8	-98.03
96	48	24	2	Disabled	Enabled	Disabled	Linear Phase	14.84	113.31	-102.66	15.36	119.24	-96.94
96	48	24	2	Disabled	Enabled	Disabled	Low Latency	14.37	113.39	-102.76	14.9	119.24	-97.14
96	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	13.66	113.42	-102.61	14.19	119.28	-96.98
96	48	24	2	Enabled	Disabled	Disabled	Linear Phase	12.51	87.94	-85.07	13.03	87.32	-84.68
96	48	24	2	Enabled	Disabled	ENABLED	Linear Phase	12.28	87.56	-85.03	12.8	87.05	-84.41
96	48	24	2	Enabled	Enabled	Disabled	Linear Phase	12.47	86.48	-83.67	13	85.71	-83.31
192	24	24	1	Disabled	Disabled	Disabled	Linear Phase	8.88	113.62	-103.12	9.23	119.55	-96.94
192	24	24	1	Disabled	Disabled	Disabled	Low Latency	9.32	113.41	-102.99	9.66	119.32	-96.9
192	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	8.61	113.47	-103.05	8.96	119.39	-96.89
192	24	24	1	Disabled	Disabled	Enabled	Linear Phase	8.74	113.56	-104.65	9.08	118.9	-97.98
192	24	24	1	Disabled	Disabled	Enabled	Low Latency	9.17	113.4	-104.56	9.52	118.98	-97.91
192	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	8.46	113.33	-104.58	8.81	118.9	-97.84
192	24	24	1	Disabled	Enabled	Disabled	Linear Phase	8.83	113.44	-103.14	9.18	119.39	-96.98
192	24	24	1	Disabled	Enabled	Disabled	Low Latency	9.3	113.37	-103.08	9.65	119.17	-96.92
192	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	8.6	113.49	-102.96	8.94	119.35	-96.91
192	48	24	2	Disabled	Disabled	Disabled	Linear Phase	12.15	113.42	-102.34	12.67	119.39	-97.04
192	48	24	2	Disabled	Disabled	Disabled	Low Latency	12.98	113.37	-102.18	13.5	119.34	-97.16
192	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	11.62	113.32	-102.23	12.14	119.33	-97.03
192	48	24	2	Disabled	Disabled	Enabled	Linear Phase	11.93	113.49	-103.81	12.45	118.83	-98.09
192	48	24	2	Disabled	Disabled	Enabled	Low Latency	12.75	113.31	-103.91	13.27	118.71	-97.93
192	48	24	2	Disabled	Disabled	Enabled	Ultra Low Latency	11.39	113.27	-103.79	11.91	118.88	-97.96
192	48	24	2	Disabled	Enabled	Disabled	Linear Phase	12.06	113.4	-102.32	12.58	119.37	-96.92
192	48	24	2	Disabled	Enabled	Disabled	Low Latency	12.94	113.38	-102.34	13.47	119.28	-96.89
192	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	11.59	113.37	-102.44	12.11	119.25	-96.95
384	24	24	1	Disabled	Disabled	Disabled	Linear Phase	9.54	113.43	-103.17	9.88	119.38	-96.9
384	24	24	1	Disabled	Disabled	Disabled	Low Latency	10.49	113.43	-103.12	10.84	119.39	-96.89

Table 3-1. Target Mode Power Consumption With PLL Enabled (continued)

Sampling Frequency (kHz)	BCLK-FS Ratio	Word Length	Enabled Channels	ADC Low Power Filter	ADC CIC 4th Order	ADC DEMRATE OVRLOAD 2x	Decimation Filter	AVDD = 1.8V			AVDD = 3.3V		
								AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)	AVDD Current (mA)	Dynamic Range (dB Aweighted)	THD+N (dB)
384	24	24	1	Disabled	Disabled	Disabled	Ultra Low Latency	9.07	113.43	-103.13	9.42	119.35	-96.85
384	24	24	1	Disabled	Disabled	Enabled	Linear Phase	9.4	113.37	-104.58	9.75	118.9	-97.91
384	24	24	1	Disabled	Disabled	Enabled	Low Latency	10.35	113.2	-104.5	10.7	118.95	-97.97
384	24	24	1	Disabled	Disabled	Enabled	Ultra Low Latency	8.93	113.37	-104.54	9.28	118.89	-97.9
384	24	24	1	Disabled	Enabled	Disabled	Linear Phase	9.49	113.34	-103.11	9.83	119.21	-96.94
384	24	24	1	Disabled	Enabled	Disabled	Low Latency	10.47	113.47	-102.99	10.82	119.4	-97.02
384	24	24	1	Disabled	Enabled	Disabled	Ultra Low Latency	9.06	113.45	-103.1	9.4	119.31	-97
384	48	24	2	Disabled	Disabled	Disabled	Linear Phase	14.34	113.43	-101.85	14.88	119.19	-96.77
384	48	24	2	Disabled	Disabled	Disabled	Low Latency	16.24	113.53	-101.94	16.77	119.23	-96.81
384	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	13.45	113.5	-102	13.98	119.21	-96.55
384	48	24	2	Disabled	Disabled	Enabled	Linear Phase	14.13	113.25	-103.31	14.66	118.71	-97.65
384	48	24	2	Disabled	Disabled	Enabled	Low Latency	16.02	113.43	-103.3	16.56	118.76	-97.37
384	48	24	2	Disabled	Disabled	Disabled	Ultra Low Latency	13.23	113.25	-103.2	13.76	118.89	-97.73
384	48	24	2	Disabled	Enabled	Disabled	Linear Phase	14.24	113.22	-101.99	14.77	119.2	-96.81
384	48	24	2	Disabled	Enabled	Disabled	Low Latency	16.21	113.31	-101.87	16.74	119.2	-96.77
384	48	24	2	Disabled	Enabled	Disabled	Ultra Low Latency	13.42	113.36	-101.93	13.95	119.17	-96.76

4 Digital Microphone Power Consumption

The PDM typical current consumption table describes the typical current consumption of TAA52xx devices when the inputs of the digital microphone are used with an external PDM modulator. The ADC inputs are configured as PDM inputs by:

- Configuring one of the GPIOx or GPOx pins as a PDM clock. This configuration is accomplished by configuring the appropriate GPIOx_CFG or GPOx_CFG bit field, respectively, to PDM clock output.
- Configuring the GPIx or GPIOx as the general-purpose input function.
- Configuring the ADC channels as the PDM inputs (PDM_CHx_SEL). With this configuration, the PDM input data is latched on the edges of the PDM clock input.
- Configuring the PDM_DIN1(for PDM channel 1 and channel 2) and PDM_DIN2 (for PDM channel 3 and channel 4) to the expected GPIOx or GPIx pins (PDM_DINx_SEL).
- Enabling the ASI channel 3 and channel 4 (PASI_TX_CH2_CFG and PASI_TX_CH3_CFG) to the required slots on the ASI bus.
- Configuring the PDM clock frequency, generated by the device, using register P0_R53 (MST_CLK_CFG0).
- Enabling the ADC channels (CH_EN) and powering up the ADC (PWR_CFG).

Table 4-1. Typical Current Consumption with an External PDM 4th Order Modulator

PDM CLOCK		6.144MHz	3.072MHz	1.536MHz	0.768MHz
Sampling Frequency (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3V (mA)			
8	4	5.71	5.41	5.47	5.49
16	4	7.75	7.49	7.53	7.58
24	4	7.66	7.42	7.45	7.51
32	4	9.00	8.72	8.77	8.85
48	4	10.71	10.41	10.53	10.6
96	4	17.04	16.88	17.02	-

Table 4-2. Typical Current Consumption with an External PDM 5th Order Modulator

PDM CLOCK		6.144MHz	3.072MHz	1.536MHz	0.768MHz
SAMPLING FREQUENCY (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3V (mA)			
8	4	5.72	5.43	5.46	5.49
16	4	7.72	7.50	7.54	7.58
24	4	7.66	7.41	7.46	7.52
32	4	8.98	8.72	8.79	8.85
48	4	10.69	10.44	10.54	10.6
96	4	17.08	16.88	17.07	-

5 Settings for Lowest Power Consumption

To minimize the power consumption of the TAA52xx devices, verify that unused modules are disabled, use the lowest sampling rate, bit clock, and controller clock required by the application, and operate at the lowest AVDD and IOVDD supply voltage possible. The following list summarizes the settings and registers for lowest power operation:

- Operate at the lowest supply voltage possible. AVDD and IOVDD support 1.8V or 3.3V supply, independently (AVDD and IOVDD can have different supply voltages).
  - Unused analog inputs, tie to analog ground.
  - Unused digital inputs, tie to digital ground.
- Disable unused ADC channels through the BO_PO_R118 (IN_CH_EN) register.
- Disable MICBIAS power, if unused, through the BO_PO_R120 (PWR_CFG) register.
- Operate at the lowest sample rate possible.
- Disable PLL if the system supplies a low jitter controller clock. Refer to Section 2 for a description of the settings to disable PLL.
- Disable unused post-processing blocks:
  - Disable biquad filters, if unused, through BO_PO_R115[4:3] (DSP_CFG) register.
- Select ultra-low latency over linear phase decimation filters (if the application allows) through the BO_PO_R114[7:6] (DSP_CFG) register.
- Use the smallest word length permissible by the application through the BO_PO_R26[5:4] (PASI_WLEN) register for primary ASI and BO_P3_R26[5:4] (SASI_WLEN) in cases of secondary ASI.

6 Summary

The typical power consumption matrix of the TAA52xx devices, across various usage scenarios, was tabulated in this document and recommendations for lowering power consumption was highlighted.

7 References

For related documentation see the following:

- Texas Instruments, TAA5212 High-Performance Stereo Audio ADC With 119dB Dynamic Range and Configurable Digital Filters, data sheet
- Texas Instruments, TAA5242 Hardware-Control High-Performance Stereo Audio ADC With 119dB Dynamic Range, data sheet

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265