Application Report
SBOA120–November 2009

A Powerline Communication Line Driver Requirement

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ABSTRACT

This application note describes some of the requirements for successful powerline communications, starting with the media and progressing towards more detailled specifications of the amplifier. The goal of this report is to increase the reader's understanding of the physics of the media and the line driver, and to describe the corresponding implications for both the line driver and the overall system performance. The OPA2673, a dual, wideband, high output current op amp with active off-line control, is used as an example throughout this document.

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1 Introduction

The OPA2673 is among the latest amplifiers released by Texas Instruments designed for the powerline communication market. Beyond the necessary bandwidth and distortion requirement for high frequencies, the OPA2673 solves an intermittent loading of the line problem while maintaining the high output voltage and current capability needed to drive a powerline. In this application report, we start looking at the media, then look at some of the line driver requirements during transmission (Tx) , and finally consider some of the system requirements during reception (Rx).

2 Powerline Media

The media used for a powerline can be found in any residential or commercial dwelling because it carries the primary 50Hz or 60Hz power signal. Typically, a powerline modem will connect to this media using a power outlet. This media was originally designed to distribute power throughout a building, carrying the primary 120V - 230V at 50Hz - 60Hz. Since a dwelling must be connected to the broader power distribution grid, it can be subject to lightning surges. Therefore, the following characteristics for the media apply:

- High voltage 50Hz or 60Hz power waveform
- Large transient events occur on the power network with amplitudes up to 6kV likely (for example, lightning strikes, equipment malfunction, abruptly disconnecting a plug from the outlet, etc.)
- Signal path loss range from 0dB to greater than 70dB, depending on how far the remote connection is located and how many times the data signal goes back to the fuse box
- Multi-path propagation exists because this media is not terminated
- The output impedance of the line varies from less than 10Ω (mostly resistive) to greater than 1kΩ (mostly reactive).
- Noise will be present on the line as a result of the power supply of any device connected to the line.

Note that because the powerline modem must be powered externally and does not require additional wiring to transmit data, it is often called *wireless*. For analysis purpose, the load is often considered to a 50Ω load.

3 Line Driver

In order to achieve sufficient linearity with the environment described above for a 15dBm signal into a 50Ω load, the line driver requires a combination of minimal supply headroom and maximum output current capability. All devices that are intended to be used as line drivers should have an output voltage versus current limitation plot provided somewhere in the product data sheet. For the OPA2673 operating on a ±6V supply, this characteristic plot is provided in Figure 1.

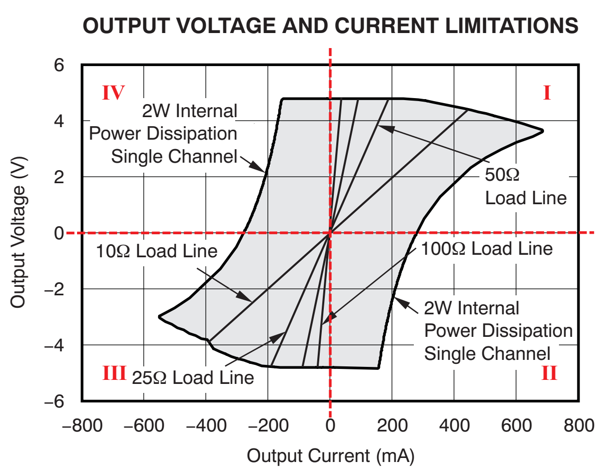

Figure 1. Output Voltage and Current Limitations (OPA2673)

In this graph, we can see four quadrants. Quadrant I shows both that the output voltage is positive and the driver is sourcing current. Quadrant II has the amplifier sourcing current but with a negative output voltage. Quadrant III reflects a negative output voltage and the amplifier sinking current. Quadrant IV illustrates the amplifier as sinking current while the output voltage is positive.

In this graph, for practicality reasons, common-load lines have been included. The 50Ω load line is the typical load for powerline communications; the 10Ω load line corresponds to the worst-case line impedance. With these load lines, a designer can quickly determine if a device can satisfy the worst-case load conditions. A 2W Internal Power Dissipation graph is also shown to enclose the normal operating area of the device. This portion of the graph is calculated using an arbitrary internal power dissipation value. Adjust this number to the specific design constraints, taking into consideration the package junction-to-ambient thermal resistance (θ_{JA}) as well as the layout.

From a power dissipation perspective, the two areas of operation you want to avoid are Quadrants II and IV. Using Figure 2 as a visual aid, we can see that we will have maximum voltage across one of the output transistors while sinking or sourcing current. The model developed in Figure 2 can also help calculate to the first-order internal power dissipation. Table 1 lists the value used for this model.

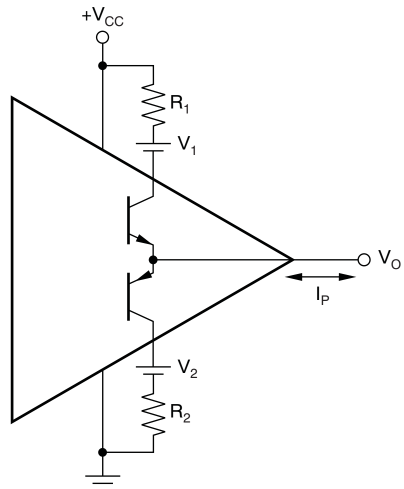

Figure 2. Output Voltage Headroom Model

Table 1. Line Driver Headroom Model Values

Supply Voltage	V_1	R_1	V_2	R_2
+12V	0.9V	2Ω	0.9V	2Ω

Once you have selected a device with sufficient output voltage and output current margin, other design considerations can be analyzed. One such system-level consideration is the operation while in the half-duplex mode, as is the case for powerline communications.

The definition for a half-duplex signal is provided below.[(1)]

A *half-duplex* system provides for communication in both directions, but only one direction at a time (that is, not simultaneously). Typically, once a party begins receiving a signal, it must wait for the transmitter to stop transmitting, before replying.

An example of a half-duplex system is a two-party system such as a *walkie-talkie* style two-way radio, wherein one must use *Over* or another previously-agreed-upon command to indicate the end of transmission. Furthermore, users of this type of system must ensure that only one party transmits at a time, because both parties transmit on the same frequency.

A good analogy for a half-duplex system is a one-lane road with traffic controllers at each end. Traffic can flow in both directions, but in only one direction at a time, regulated by the traffic controllers.

(1) Definition: Wikipedia.com

In automatically-run communications systems, such as two-way datalinks, the time allocation for communications in a half-duplex system is firmly controlled by the hardware. Thus, there is no waste of the channel of bandiwdth for switching. For example, Station A on one end of the datalink could be allowed to transmit for exactly 1 second, and then Station B on the other end could be allowed to transmit for exactly 1 second. This cycle then repeats over and over again.

4 Implications

What do these considerations imply for a powerline communications system?

First, a designer must achieve the performance required with an ideal load, then move to a system-level performance evaluation. At this point, the designer can start to answer questions such as how best to simplify the system while still achieving the same functionality and performance level.

Looking first at the circuit design, the line driver application circuit resembles the circuit shown in Figure 3. The digital-to-analog converter (DAC) or coder-decoder (codec) will provide the analog signal. The DMT signal in the frequency domain will appear as a succession of the carrier frequency, with an amplitude that is associated with the power spectral density spectrum. Figure 4 shows a power spectral density mask example, with Figure 5 showing a detail of the actual carrier frequencies.

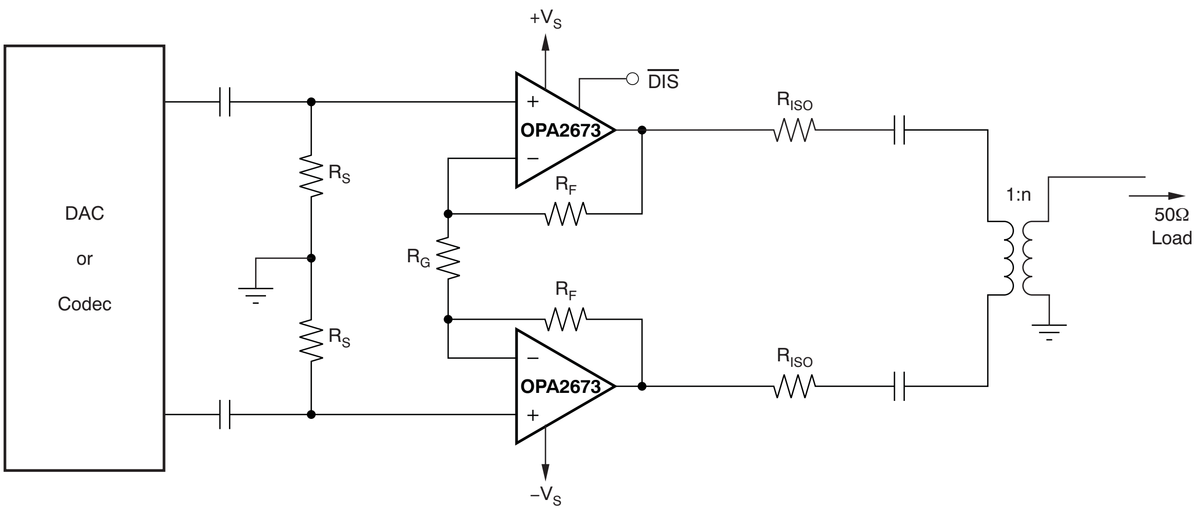

Figure 3. Simplified PLC Line Driver

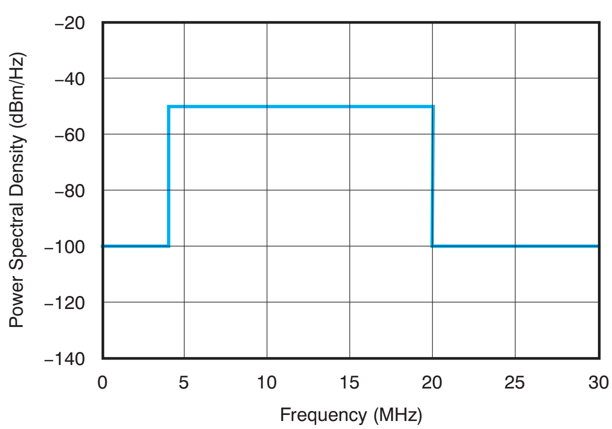

Figure 4. Power Spectral Density Mask

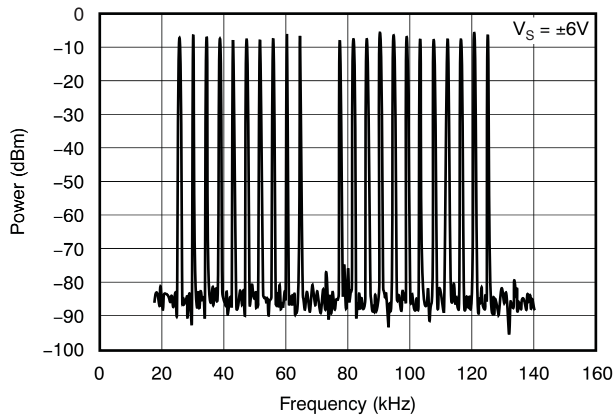

Figure 5. Power Spectral Density: Carrier Detail Example

The output of the DAC/codec is normally ac-coupled and terminated on the amplifier side with fairly high resistor values to limit loading and provide proper biasing. These resistors allow the bias current of the amplifier to circulate while maintaining the advantage of the high input impedance of the noninverting differential configuration. On the amplifier output, we find isolation resistors, an ac-coupled load through an isolation transformer, and series capacitors. Because the isolation resistors that are selected tend to be low impedance, the series capacitors are required to limit dc current flowing through the transformer. The current flowing would be the result of the common-mode voltage mismatch between both amplifiers' output.

As the DAC provides the encoded information in an analog fashion (see Figure 6), the role of the line driver is threefold: provide minimal load on the DAC, amplify the signal to the desired level, and drive the demanding load. These purposes must be done in the most linear way possible; that is, without adding so much distortion and so much noise that the information is lost.

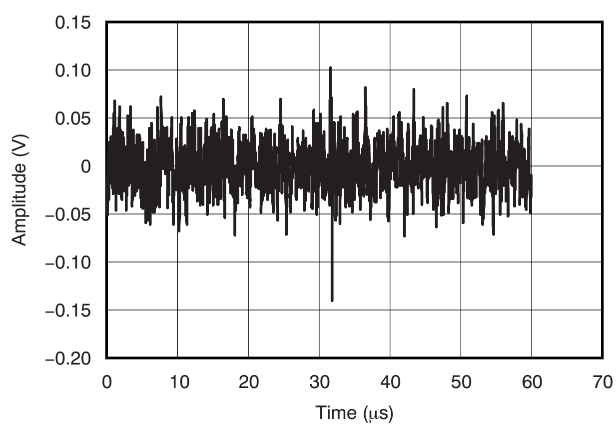

Figure 6. Analog DMT Signal Example

Notice that the analog signal resembles noise.

Broadband PLC systems, such as those used for in-home networking or in-home video distribution or the powerline, often require up to a 30MHz flat frequency response while driving a demanding 50Ω differential load. Line drivers must have very good output power capabilities.

Now looking at the overall system while transmitting information, you will have the circuit shown in Figure 7.

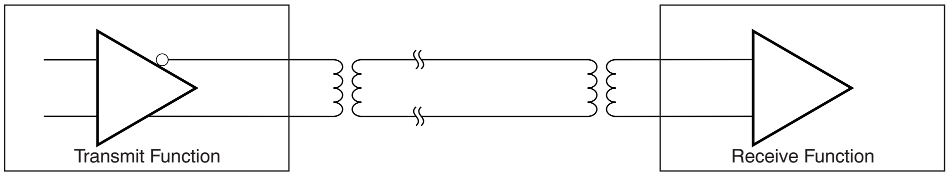

Figure 7. Typical Signal Chain

Figure 7 represents a mono-directional system; but since most powerline modem operation is half-duplex, it is possible to invert the flow of information. This technique produces the circuit configuration shown in Figure 8.

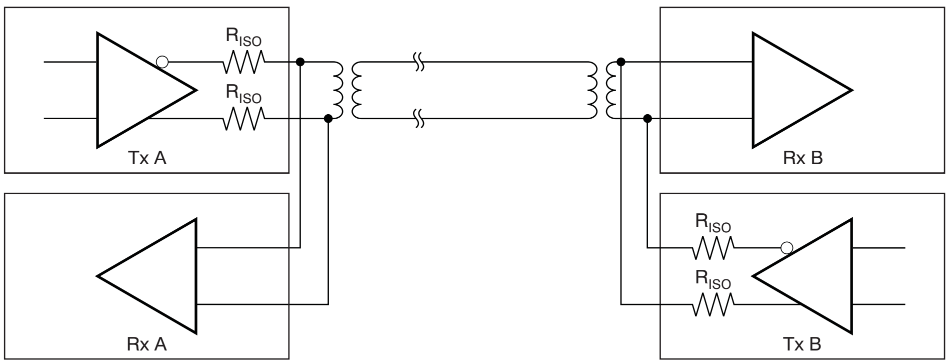

Figure 8. Complete Signal Chain

The system will operate in the following manner:

While TxA is transmitting, RxB is receiving; RxA and TxB are both disabled. This configuration eliminates a low impedance node that would make a harder load to drive as well as attenuate the receive signal. Notice that if both TxA and TxB are active at the same time, the amplifier driving the load would see the two R_{ISO} resistors instead of the 50Ω load of the media as represented in figure 3. Of course, the distortion would be dramatically increased because the Tx amplifier would be loaded very heavily.

Although this scenario may not be considered plausible, it is not far-fetched and if not verified extensively could be encountered during production with resulting yield loss. Also, since this problem will most likely be intermittent, as only the right signal will trigger this mechanism; it will be a difficult to isolate. There are two approach to resolve this issue: 1) insert switches to isolate the line driver in the Rx mode; 2) select a component that does not have this issue or that has an active off-line control. We will next move on to analyzing these two solutions.

The circuit presented in Figure 3 is an ideal circuit; unfortunately more components are required to provide sufficient isolation with the purpose of maintaining good distortion. To ensure adequate isolation, solid state switches are added in series with the Tx output of the line driver and with the Rx input of the receiver, as shown in Figure 9.

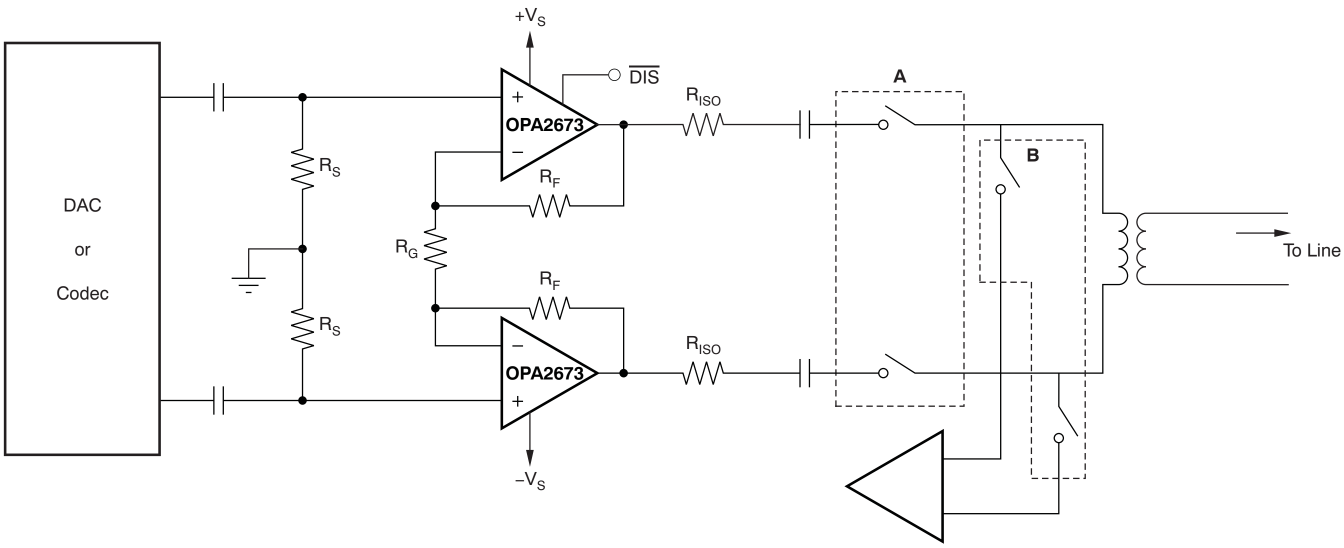

Figure 9. Complete PLC Line Driver Circuit

The operation of such solid-state switches is described below: When Tx is enabled. the A switches are closed and the B switches are open. When Rx is enabled, the B switches are closed and the A switches are open.

Those switches are required as a result of the limitation on most line drivers available on the market today. In effect, the line driver can easily drive $20V_{PP}$ into a 50Ω load from a +12V supply; but if such a large signal is driven directly on the output while in a disable mode; it is possible that the high dV/dt of the signal will casue the output stage of the disbaled line driver to conduct. Under these circomstances, the loading placed on the line by the disbaled amplifier is highly non-linear. This causes a dramatic loss of linearity. An emulation of this undesired mode of operation can be found in Figure 10 and Figure 11 (with the OPA2673 operating in 50% bias mode). The accompanying circuit schematic in shown in Figure 12.

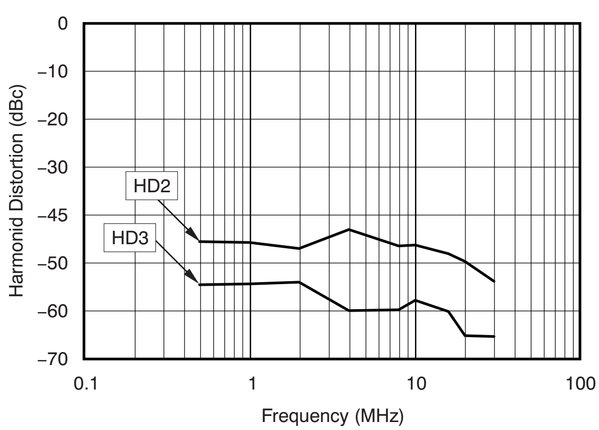

Figure 10. TxA Amplifier Transmitting While TxB Output is in Low-Impedance Mode: Harmonic Distortion vs Frequency Load

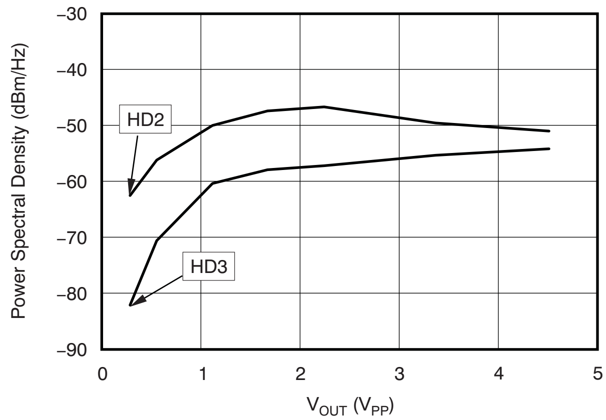

Figure 11. TxA Amplifier Transmitting While TxB Output is in Low-Impedance Mode: Harmonic Distortion vs Output Voltage

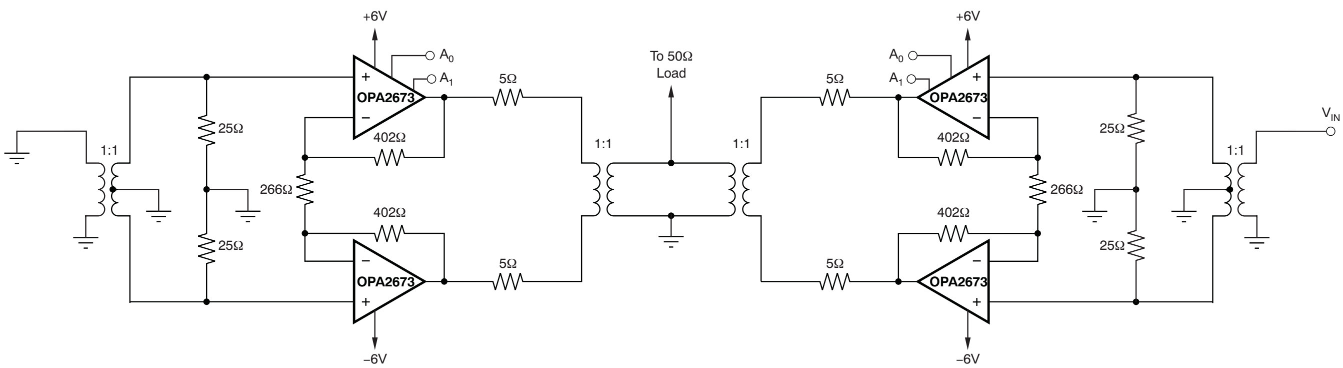

Figure 12. TxA Amplifier Transmitting While TxB Output Stage is in Low-Impedance Mode: Circuit Configuration

An alternative to adding components to ensure that the faulty mode will not exist is to use a line driver that includes an active off-line control. The OPA2673 is such a device.

Using the same test circuit illustrated in Figure 12, but with TxB disabled and TxA driving, you will then observe the dramatic harmonic distortion improvement. Figure 13 and Figure 14 illustrate this effect (with the OPA2673 operating in shutdown mode).

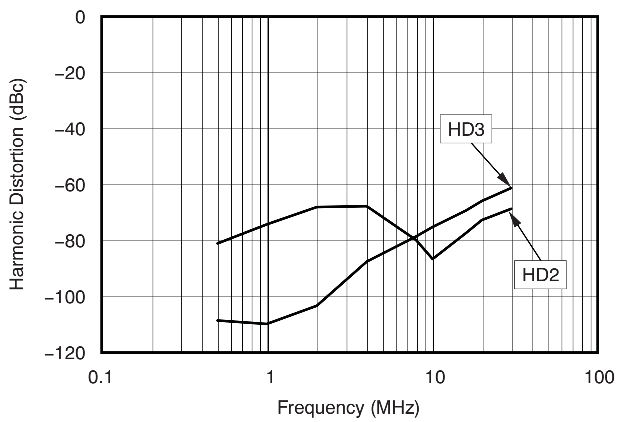

Figure 13. TxA Amplifier Transmitting While TxB Output is Disabled: Harmonic Distortion vs Frequency Load

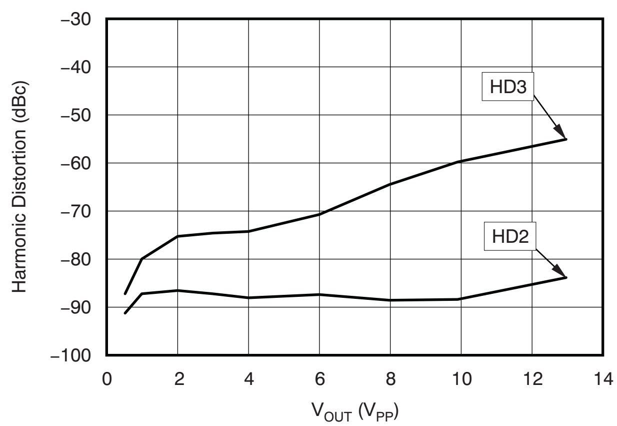

Figure 14. TxA Amplifier Transmitting While TxB Output is Disabled: Harmonic Distortion vs Output Voltage

5 Conclusion

If looking only at the driving capability of an operational amplifier, there are many devices that may constitute a good choice for powerline communications. As the system is better understood, however, the complexity of the architecture adds additional constraints that can be taken advantage of to help design a simpler, more cost-effective solution. The OPA2673 is one step forward in the direction of simpler powerline systems.

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