Application Note

THP210 and ADS127L11 Performance

ABSTRACT

While dynamic range and SNR performance of amplifiers and ADCs can be determined accurately from simulation models, verification of distortion performance from an amplifier driving an ADC is difficult to determine by simulation and is best proven by physical measurement of the exact driver and ADC pairing.

This application note shows the performance of the THP210 fully-differential amplifier driving the ADS127L11 delta-sigma ADC. The focus of this document is on THD, SNR, and gain error performance. In particular, the performance benefits of the ADC input precharge buffers is demonstrated when the ADC is operated in the high-speed mode.

Because of the low THP210 input current noise, the option of increasing the driver gain resistor values to reduce driver power consumption is also examined. Several values of gain resistors are evaluated showing the impact on SNR and the associated power loss.

For applications that vary the ADC clock frequency to set specific sample rates, the sensitivity of gain error change versus clock frequency of the THP210 and ADS127L11 combination is shown.

Table of Contents

Trademarks

A brief introduction of the THP210 and ADS127L11 devices used in this evaluation are shown in the following sections.

1 THP210

The THP210 is a low-noise, low-offset, precision 9.2-MHz gain-bandwidth product, fully-differential input-output amplifier (FDA). Most notable is the low input current noise (0.3 nA/$\sqrt{\text{Hz}}$) with low 10-Hz 1/f noise corner frequency. The low input current noise and 1/f current noise corner enables the option to increase the size of gain resistors to reduce driver power consumption.

2 ADS127L11

The ADS127L11 is a 400-kSPS, wideband delta-sigma ADC featuring low noise, low distortion and low power consumption. The ADC features two power modes with associated sample rates: 400 kSPS with 18.5-mW power consumption in high-speed mode operation and 50 kSPS with 3.3-mW power consumption in low-speed mode operation.

The ADS127L11 integrates optional precharge buffers to reduce input driver loading. Figure 2-1 shows the simplified model of the ADS127L11 input sampling circuit highlighting the precharge buffers.

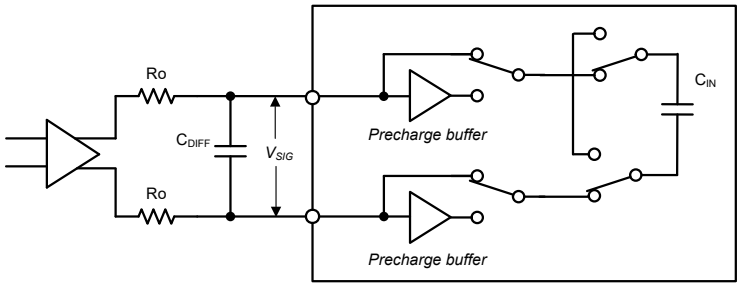

Figure 2-1. ADS127L11 Simplified Input Circuit

With precharge buffers disabled, the ADC samples the input voltage with an internal capacitor (C_{IN}) at the modulator sampling frequency. An input capacitor C_{DIFF} is used at the ADC input to filter the sample pulses from the driver output. The sampling operation causes a kickback transient at the input due to charge transfer between capacitors C_{DIFF} and C_{IN}. The following relates the kickback voltage to the size of capacitor C_{DIFF}.

$$\text{Kickback Voltage (V)} = V_{SIG} \times \frac{C_{IN}}{C_{IN} + C_{DIFF}}$$

The kickback voltage is proportional to V_{SIG} and the ratio of capacitors C_{IN} and C_{DIFF}. With capacitors C_{DIFF} = 2.2 nF, C_{IN} = 7.4 pF, and signal V_{SIG} = 4.096 V, the kickback voltage is 14 mV. Figure 2-2 shows a simulation of the kickback voltage over continuous input samples in high-speed operation with 12.8-MHz modulator sample frequency.

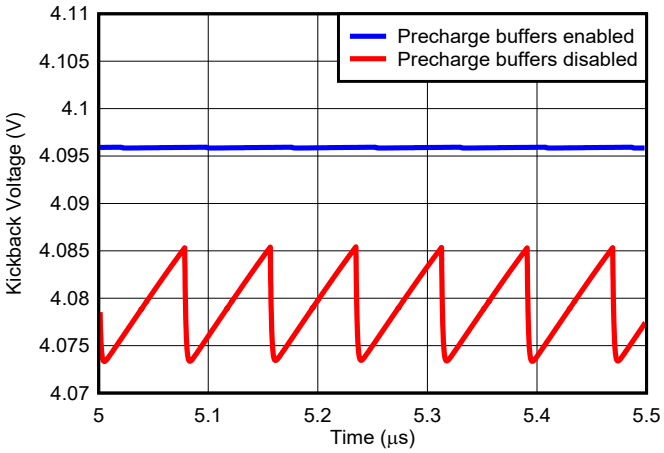

Figure 2-2. Kickback Voltage

After the kickback transient, the driver recharges C_{DIFF} through R_O to restore the charge lost to the sampling operation. Gain error results if the voltage is not restored at the end of the sample phase ½ modulator clock cycle later. Just as important, nonlinear driver current occurs which induces driver distortion.

To reduce the kickback voltage, capacitor C_{DIFF} is typically chosen 300 × C_{IN} (2.2 nF) for a 24-bit ADC such as the ADS127L11. Increasing the size of C_{DIFF} reduces the kickback voltage and resulting driver current which generally improves gain error and distortion performance. However, if C_{DIFF} is increased, driver loading and driver power consumption should be considered if out-of-band signal frequencies are present. See the Driver Power Consumption section for more information.

2.1 ADS127L11 Precharge Buffers

The ADS127L11 integrates precharge buffers to reduce driver loading. For many types of drivers, reducing driver loading improves THD performance and reduces overall gain error. In the first half-cycle of the input sampling phase, the precharge buffers charge the sampling capacitor. In the second half cycle, capacitor C_{IN} is disconnected from the precharge buffers and is connected directly to the input to provide the fine charge. Disconnection of the precharge buffer in the fine-charge phase eliminates precharge buffer noise and distortion when the final voltage is measured at the end of the sample operation. Because capacitor C_{IN} is precharged, the kickback voltage is reduced by factor (k), as shown in the following equation:

$$\text{Kickback Voltage, Buffered (V)} = V_{SIG} \times k \times \frac{C_{IN}}{C_{IN} + C_{DIFF}}$$

Factor (k) is related to the offset and gain error of the precharge buffer. Because k ≤ 0.01 (typical), the kickback voltage is reduced 99%, but more importantly, the peak and average driver output current is also reduced resulting in improved distortion performance.

3 Test Circuit

Figure 3-1 shows the circuit used to evaluate the THP210 and ADS127L11 performance. The THP210 and the ADS127L11 are powered from a single 5-V power supply, with the output common-mode voltage of the THP210 set to 2.5 V, driven by the VCM output of the ADC.

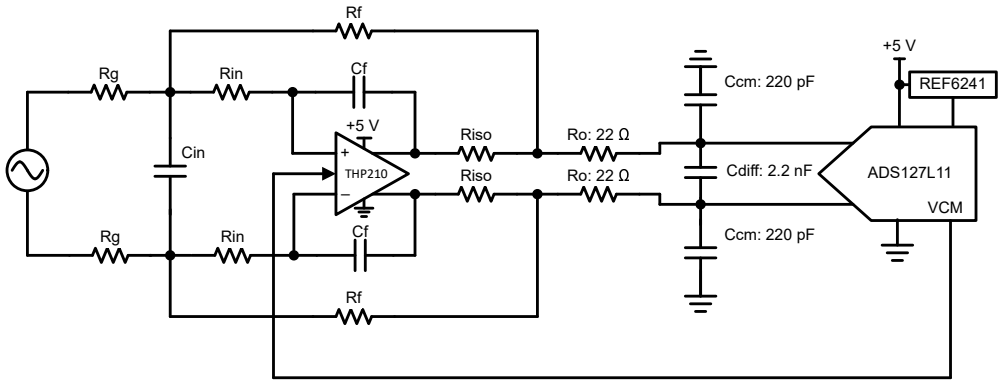

Figure 3-1. Test Circuit

The THP210 driver is implemented as a unity gain, dc-coupled 2nd order low-pass filter. The objective of the filter is to attenuate signal frequencies at the ADC modulator sampling frequency to reduce signal aliasing. The filter is designed for OSR = 32. OSR = 32 requires the filter to attenuate the signal in less than two decades of frequency range between the Nyquist frequency and the modulator sampling frequency. Increasing the OSR value lowers the ADC bandwidth but also increases the frequency range in which the filter can operate. By lowering the filter corner frequency, the filter attenuation is increased at the modulator sampling frequency.

R_O and C_{DIFF} at the ADC input serve two functions. The most important function is the charge reservoir to filter the ADC sample pulses. The second function is an additional filter in the signal path to increase anti-aliasing.

Several filter implementations are evaluated, using 499-Ω, 1-kΩ, and 4.99-kΩ gain resistors with the corner frequency of the filter adapted to the passband of the ADC. Table 3-1 lists the filter components used in the evaluation.

Table 3-1. Filter Components

ADC Mode	Signal Passband	Rg and Rf	Cin	Cf	Rin	Riso
High speed	165 kHz	499 Ω	180 pF	390 pF	275 Ω	47 Ω
	165 kHz	1 kΩ	100 pF	220 pF	500 Ω	47 Ω
	165 kHz	4.99 kΩ	22 pF	47 pF	2.5k Ω	47 Ω
Low speed	20.5 kHz	499 Ω	5.6 nF	2.4 nF	50 Ω	82 Ω
	20.5 kHz	1 kΩ	2.7 nF	1.2 nF	100 Ω	68 Ω
	20.5 kHz	4.99 kΩ	470 pF	240 pF	500 Ω	68 Ω

TINA-TI, a free SPICE-based analog simulation program, the THP210 Spice Model and the ADS127L11 Spice Model are available from TI. The *TINA-TI* program is used to generate the simulation data of the filter frequency response, noise performance, and driver supply current.

The ADS127L11 Evaluation Board is used to acquire the data with modifications for installation of the filter components. The THP210 driver replaces the current THS4551 driver (8-pin VSSOP package) and the 4.096-V REF6241 replaces the current 2.5-V version. The 4.096-V reference voltage is used to maximize the available dynamic range performance.

A low-noise, low-distortion signal source, such as the Audio Precision SYS-2722, is required to achieve high-resolution results. The balanced signal output from the generator drives the differential THP210 inputs for this evaluation. For SNR measurements, a 1-kHz bandpass filter is used to remove noise from the signal generator. Figure 3-2 shows the test setup.

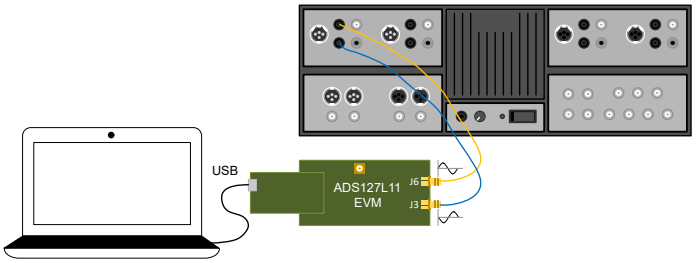

Figure 3-2. Test Setup

Figure 3-3 shows a typical FFT of THD and SNR performance as captured in the ADC high speed mode with precharge buffers enabled. 262,144 ADC samples are used in the analysis to reduce the noise in the FFT harmonic bins to improve measurement resolution.

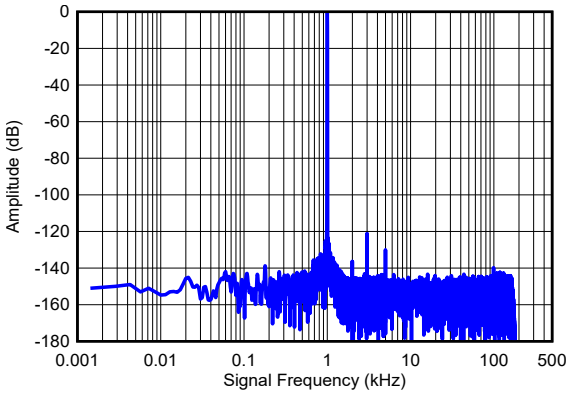

Figure 3-3. Typical FFT Result

3.1 THD Performance

Table 3-2 summarizes THD performance. The data are representative of the THP210 and ADS127L11 combined performance with the THP210 in a low-pass filter configuration using combinations of resistors R_g, R_f, and capacitor C_{DIFF}.

Table 3-2. THD Performance

Rg, Rf	C_{DIFF}	ADC BUFFERS ENABLED		ADC BUFFERS DISABLED	
		THD (f = 1 kHz)	THD (f = 10 kHz)	THD (f = 1 kHz)	THD (f = 10 kHz)
LOW-SPEED OPERATION (1)					
499 Ω	1 nF	–123 dB	–116 dB	–115 dB	–117 dB
1 kΩ	1 nF	–123 dB	–118 dB	–115 dB	–120 dB
4.99 kΩ	1 nF	–119 dB	–122 dB	–104 dB	–124 dB
499 Ω	2.2 nF	–124 dB	–116 dB	–126 dB	–116 dB
1 kΩ	2.2 nF	–125 dB	–121 dB	–121 dB	–122 dB
4.99 kΩ	2.2 nF	–125 dB	–121 dB	–102 dB	–122 dB
4.99 kΩ	10 nF	–124 dB	–124 dB	–122 dB	–123 dB
HIGH-SPEED OPERATION					
499 Ω	1 nF	–113 dB	–109 dB	–97 dB	–97 dB
1 kΩ	1 nF	–114 dB	–112 dB	–104 dB	–104 dB
4.99 kΩ	1 nF	–113 dB	–112 dB	–110 dB	–108 dB
499 Ω	2.2 nF	–118 dB	–111 dB	–105 dB	–104 dB
1 kΩ	2.2 nF	–118 dB	–115 dB	–110 dB	–110 dB
4.99 kΩ	2.2 nF	–118 dB	–115 dB	–113 dB	–110 dB
4.99 kΩ	10 nF	–116 dB	–114 dB	–107 dB	–107 dB

(1) In low-speed operation, 10-kHz input frequency test data includes only the first harmonic in the THD analysis (low speed ADC bandwidth = 20.6 kHz).

The following observations are drawn from the THD data:

Low-Speed Operation

- The precharge buffers provide consistent THD results over the various filter component values. Input capacitor C_{DIFF} = 1 nF can be a consideration to reduce driver current for out-of-band input frequencies, but with a small reduction in THD performance. Operation without the precharge buffers can be considered using C_{DIFF} = 10 nF, however driver output current peaks at a higher value for out-of-band frequencies. See the Driver Power Consumption section for more details.

High-Speed Operation

- Best results over the various filter component values are with precharge buffers enabled. The use of 2.2 nF for input capacitor C_{DIFF} is recommended. See the Driver Power Consumption section if C_{DIFF} is increased beyond 2.2 nF.

3.2 SNR Performance

Table 3-3 summarizes the SNR results. In high-speed operation, the 4.99-kΩ gain resistors degrade SNR performance by –1.5 dB (typical) due to the higher amount of thermal noise generated by the resistors. In low-speed operation, the 4.99-kΩ resistors show little SNR degradation. Operation with or without the precharge buffers yields essentially the same SNR performance. See the Noise Analysis section for details of noise analysis and noise simulation results.

Table 3-3. SNR Performance

Rg, Rf	Cdiff	ADC BUFFERS ENABLED	ADC BUFFERS DISABLED
		SNR	SNR
LOW-SPEED MODE (BANDWIDTH = 21.9 kHz)			
499 Ω	1 nF	106.5 dB	106.5 dB
1 kΩ	1 nF	106.5 dB	106.5 dB
4.99 kΩ	1 nF	106.0 dB	106.5 dB
499 Ω	2.2 nF	106.5 dB	107.0 dB
1 kΩ	2.2 nF	106.5 dB	107.0 dB
4.99 kΩ	2.2 nF	106.5 dB	106.5 dB
4.99 kΩ	10 nF	106.5 dB	106.5 dB
HIGH-SPEED MODE (BANDWIDTH = 175 kHz)			
499 Ω	1 nF	106.0 dB	106.0 dB
1 kΩ	1 nF	106.0 dB	105.5 dB
4.99 kΩ	1 nF	104.0 dB	104.0 dB
499 Ω	2.2 nF	106.0 dB	105.5 dB
1 kΩ	2.2 nF	106.0 dB	105.5 dB
4.99 kΩ	2.2 nF	104.0 dB	104.0 dB
4.99 kΩ	10 nF	104.5 dB	104.5 dB

3.3 Gain Error Performance

Excess gain error will result if the driver is not settled from the kickback voltage by the time the ADC sample phase ends. The driver is normally required to settle within ½ of a modulator clock cycle (39 ns in high-speed operation) for no gain error, which is a difficult requirement to achieve for many types of medium bandwidth drivers.

Another concern is gain change versus ADC clock frequency. In some systems, the ADC clock frequency is changed to set specific sample rates. Ideally the gain should remain constant as the clock frequency is changed. Although to some extent this effect can be characterized to develop a table of clock-frequency correction factors, it is generally preferred to reduce the gain error effect from the onset.

In any case, gain error can be minimized from the system by the use of the ADC precharge buffers. The precharge buffers allow pairing of precision FDA drivers of low-to-medium bandwidth to the ADC.

Figure 3-4 shows gain error performance versus clock period without using the precharge buffers. Gain error plot data for high-speed operation begins at 40-ns clock period, while low-speed operation begins at 156 ns. Gain error changes 3500 ppm over the 40-ns to 500-ns clock period range. Gain error decreases with decreasing clock frequency because more time is available for the driver to settle before the signal is captured for measurement at the end of the sample phase. Note the exponential profile of gain error due to the R-C filter settling at the ADC inputs.

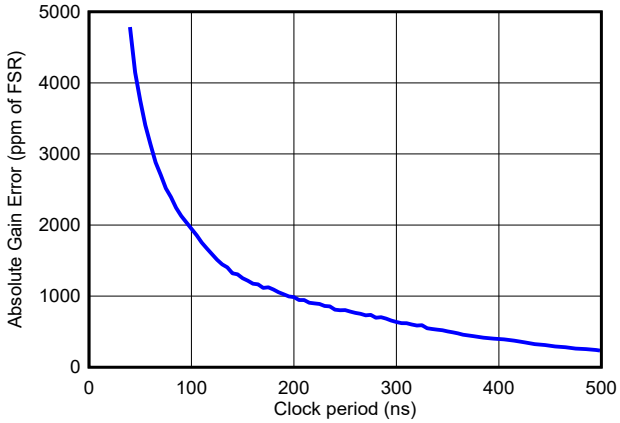

Figure 3-4. Gain Error vs Clock Period *(Precharge Buffers Disabled)*

Figure 3-5 shows gain error performance in the same configuration, this time using the precharge buffers. Gain error is less than 35 ppm peak and also changes less than 35 ppm over the range of clock periods. The decrease in gain error is due to the reduction of kickback voltage at the driver output. The ringing profile of gain error is a result of small-signal settling of the driver at the time the voltage is captured by the ADC at the end of the sample phase.

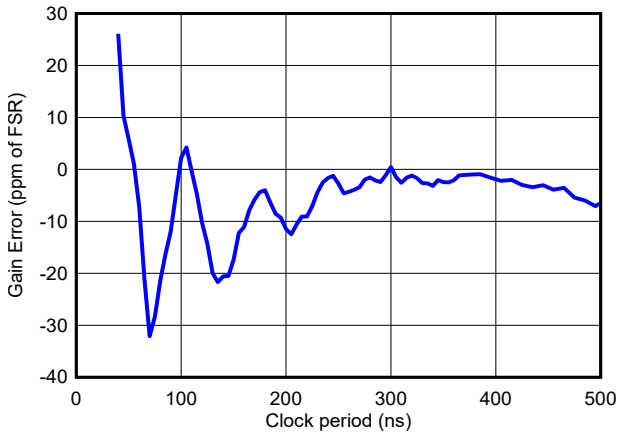

Figure 3-5. Gain Error vs Clock Period *(Precharge Buffers Enabled)*

4 Noise Analysis

Total noise of the system is the sum of noise powers of the driver voltage and current noise, resistor thermal noise and ADS127L11 conversion noise. In addition to the thermal noise of the resistors, the resistors convert THP210 current noise to a voltage noise.

Figure 4-1 shows simulation results of the *integrated noise* performance of the system. Noise is read at the 1-Hz start frequency to the desired ADC bandwidth. For example, at the full 165-kHz high-speed mode bandwidth, total system noise using 1-kΩ gain resistors is 12.1 µV. For comparison purposes, ADS127L11 noise in standalone operation is plotted with the system noise for the three gain resistor values.

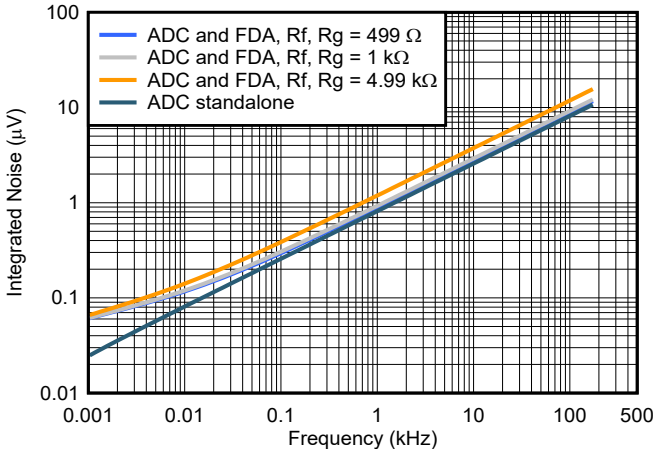

Figure 4-1. THP210 Integrated Noise (High-Speed Operation)

While the lowest absolute noise is with the 499-Ω gain resistors, the 1-kΩ resistors provide essentially the same noise performance but have the advantage of reducing signal power loss in the resistors. The 4.99-kΩ gain resistors increase the integrated noise due to the higher level of thermal noise. Comparing noise of the 4.99-kΩ resistor curve to the 1-kΩ resistor curve at low frequency demonstrates the low current noise of the THP210. Because the THP210 voltage noise dominates over the current noise in this range, gain resistor values in the range 2 kΩ to 4.99 kΩ can be considered since they do not appreciably scale current noise.

In comparison, Figure 4-2 shows simulation noise performance of a conventional FDA. This FDA has a higher level of input current noise, with an associated higher 1/f noise-corner frequency. For example, comparing noise at 10 Hz with 1-kΩ gain resistors, the THP210 noise is nearly 3 times lower. The noise advantage is nearly 10-fold when 4.99-kΩ gain resistors are used.

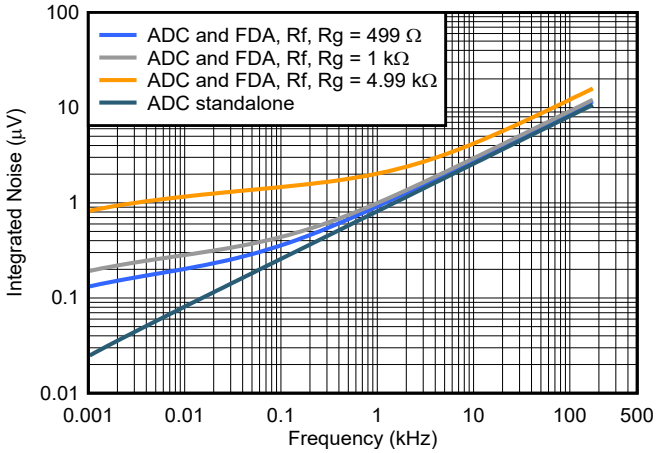

Figure 4-2. Conventional FDA Integrated Noise (High-Speed Operation)

Figure 4-3 shows simulation noise performance in low-speed mode of operation. The signal bandwidth in low-speed operation is 20.6 kHz. Because at the 50-kSPS sample rate, the high-speed operation uses a larger OSR value compared to low-speed operation (256 versus 32), the low-speed noise over the 20-kHz bandwidth is approximately 3 × higher in comparison. The increased ADC noise in low-speed operation dominates the noise produced by the 4.99-kΩ gain resistors.

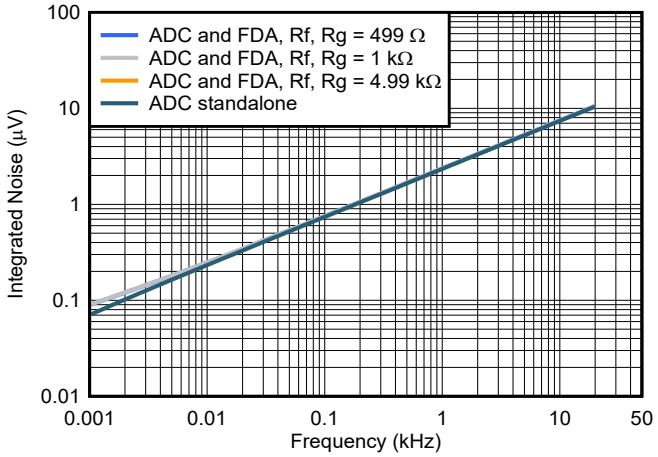

Figure 4-3. THP210 Integrated Noise (Low-Speed Mode)

4.1 SNR and DR

SNR and DR are similar noise parameters, the difference is SNR is tested with a –0.5 dbFS, 1-kHz ac-signal, whereas DR is a calculation based on the ratio of full-scale range to shorted-input noise. The following converts shorted-input integrated noise to dynamic range (DR).

$$\text{Dynamic Range (dB)} = 20\times\log\left[\frac{\text{FSR}}{2\times\sqrt{2}\times e_n}\right]$$

Where:

$\text{FSR} = 2\times V_{REF}$ (1x input range)

e_n = integrated noise

For the ADS127L11, DR typically measures 1-dB better than SNR because DR is not subject to voltage reference noise, clock jitter and most importantly, noise present in the test signal. For example, simulation noise over the 165-kHz bandwidth using 1-kΩ gain resistors is 12.1 µV, resulting in DR = 107.6 dB. The measured SNR in the same condition is 106.6 dB. Likewise, simulation noise using 4.99-kΩ gain resistors is 15.6 µV, resulting in DR = 105.4 dB. The measured SNR in the same condition is 104.6 db.

5 Driver Power Consumption

For battery-operated data acquisition systems, it is worthwhile to investigate power consumed by the driver. Figure 5-1 shows simulation results of the ac-driver current in high-speed operation using the circuit of Figure 3-1. Driver power consumption is a function of the signal frequency and the component values used in filter circuit. The amplitude of driver signal is 2.89 V_{RMS} for operation with a 4.096-V reference voltage.

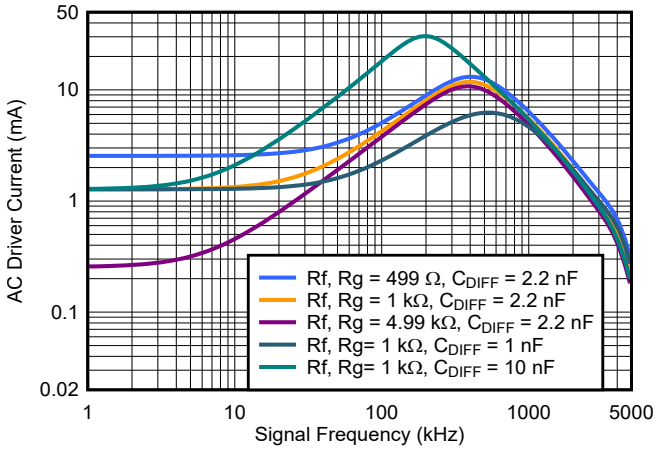

Figure 5-1. THP210 Output Current (High-Speed Operation)

For signal frequencies < 50 kHz, the driver current is mostly a function of the gain resistor size. Above 50 kHz, driver current increases with increasing frequency due to the loading of R_O and C_{DIFF} at the driver output, peaking in the 100-kHz and 400-kHz frequency range. Driver current then decreases due to the signal roll-off of the filter at the driver output. As shown in the plots, driver current reduces if C_{DIFF} = 1 nF and increases if C_{DIFF} = 10 nF, especially the peak value.

Figure 5-2 is the simulated driver current in low-speed operation. The peak current is approximately 50% lower due to the lower corner frequency used for the low-pass filter.

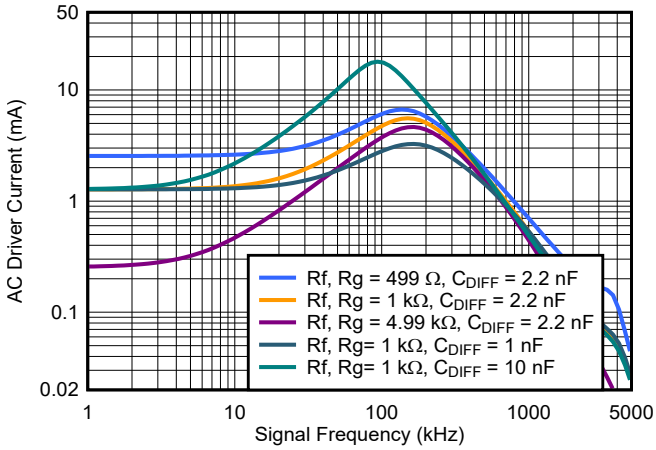

Figure 5-2. THP210 Output Current (Low-Speed Mode)

6 Summary

The THP210 provides good performance driving the ADS127L11 in both operational speed modes. The THP210 demonstrates low input current noise which presents the option of increasing the gain resistor values to reduce low-frequency driver power.

The ADC precharge buffers improve overall THD and gain error performance. In particular, precharge buffers are recommended in high-speed operation. In low-speed operation, the ADC clock operates at 1/8 speed thus allowing more time for driver settling, which leads to improved THD and gain error performance. Optionally, the precharge buffers can be disabled in low-speed operation using C_{DIFF} = 10 nF, however see the Driver Power Consumption section for implications of driver power consumption.

One parameter that is insensitive to precharge buffer operation is SNR performance. From the high-speed mode data, thermal noise generated by the 4.99-kΩ gain resistor dominates over the noise from other components. Interpolating noise data between the 1-kΩ and 4.99-kΩ resistors, 2-kΩ gain resistors could provide a good balance of driver power dissipation versus resistor noise. In low-speed operation, the 4.99-kΩ resistors are not a significant contributor to overall noise.

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