

# Amplifier Performance Development Kit Evaluation Module



## Description

The Amplifier Performance Development Kit (AMP-PDK-EVM) is an evaluation module (EVM) kit to test common operational amplifier (op amp) parameters and is compatible with most op amps and comparators. The EVM kit offers a main board with several socketed daughtercard options to fit package needs, allowing engineers to quickly evaluate and verify device performance.

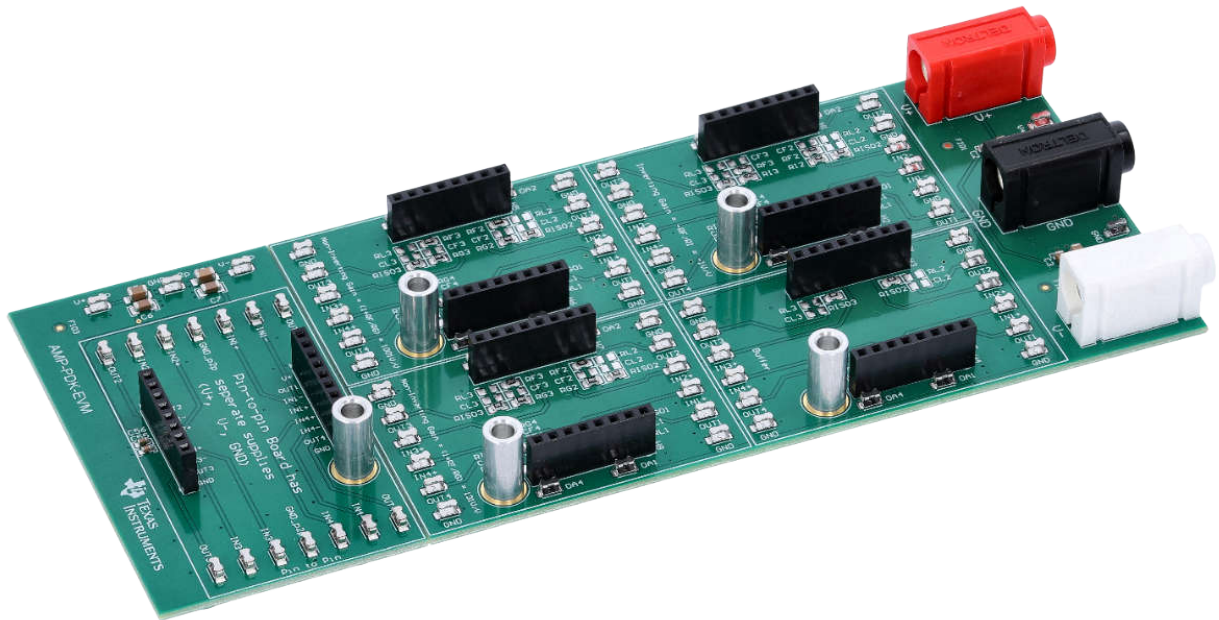
## Get Started

1. Order the main board: [AMP-PDK-EVM](#).
2. Order socketed daughtercard.
3. Order devices to be evaluated from [ti.com](#).

4. For step-by-step instructions, download the user's guide.
5. Reference training videos on [ti.com](#) for common amplifier parameter tests.

## Features

- Solderless platform to quickly evaluate most op amps and comparators
- Four preconfigured op amp circuits of inverting and non-inverting gains
- Optional breakaway pin-to-pin circuit to test both op amps and comparators
- Schematics of preconfigured circuits are provided on the silkscreen of the AMP-PDK-EVM



AMP-PDK-EVM

# 1 Evaluation Module Overview

## 1.1 Introduction

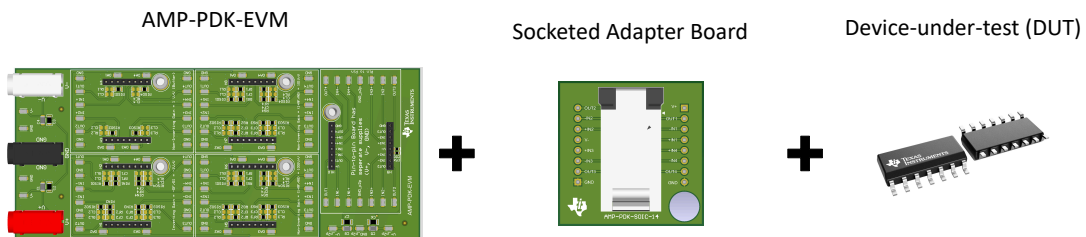
This user's guide contains support documentation for the AMP-PDK-EVM. This EVM kit is compatible with most op amps and comparators in various packages. The EVM is designed for quick evaluation of common op amp parameters and to verify device performance.

This document includes descriptions of how to use the EVM kit, contents, schematics, printed circuit board (PCB) layouts, and bill of materials (BOM).

Throughout this document the terms *evaluation board*, *evaluation module*, *development kit*, *main board*, *motherboard*, and *EVM* are synonymous with the AMP-PDK-EVM. The terms *daughtercard*, *socket board*, *socketed daughtercard*, *socketed adapter board*, and *package variants* are synonymous with the options listed in [Table 1-1](#).

## 1.2 Kit Contents

The orderable AMP-PDK-EVM contains only the main board. The daughtercard options for the different package variants are not included. Ordering the AMP-PDK-EVM main board with at least one daughtercard ([Table 1-1](#)) for full functionality is required. Devices must be ordered separately.



**Figure 1-1. Components Required for Device Evaluation**

The available daughtercards with the package descriptions are listed in [Table 1-1](#), showing each corresponding orderable part number, package family, TI package designator, number of channels, and pin count.

The shutdown and non-shutdown variants of a device are supported (as seen by the pin-count). An example is using the AMP-PDK-SC70-6 with the TLV9001 available in non-shutdown TLV9001DCKR ([SOT-SC70 \(DCK\) | 5](#)) and in shutdown TLV9001SIDCKR ([SOT-SC70 \(DCK\) | 6](#)).

A device's package designators and pin count can be found on [ti.com](http://ti.com).

**Table 1-1. AMP-PDK-EVM Daughtercard Options**

Orderable Part Number	Package Family	TI Package Designator	No. Of Channels in Device	Pin Count (Non-Shutdown   Shutdown Variant)
AMP-PDK-SC70-6	SOT-SC70	DCK	1	5   6
AMP-PDK-SOT23-6	SOT-23	DBV	1	5   6
AMP-PDK-VSSOP-8	VSSOP	DGK	2	8
AMP-PDK-SOIC-8	SOIC	D	2	8
AMP-PDK-SOIC-14	SOIC	D	4	14
AMP-PDK-TSSOP-14	TSSOP	PW	4	14

## 1.3 Specification

The AMP-PDK-EVM is capable of testing op amp or comparators available in the provided package options. The EVM can be used to verify common data sheet parameters and to troubleshoot some application circuits (capacitive load drive).

## 1.4 Device Information

The AMP-PDK-EVM main board contains four preconfigured common amplifier circuits and one pin-to-pin board that can be leveraged by both op amps and comparators. For ease of use, metal alignments have been installed to verify correct daughtercard orientation. If necessary, the prepopulated circuits can be modified to evaluate different gains, loads, and circuit stability compensation options.

## 2 Hardware

### 2.1 Additional Images

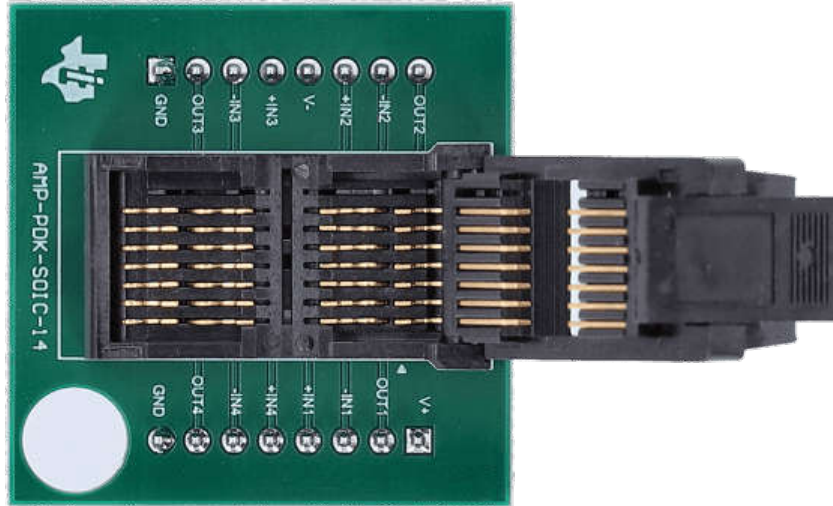


Figure 2-1. AMP-PDK-SOIC-14

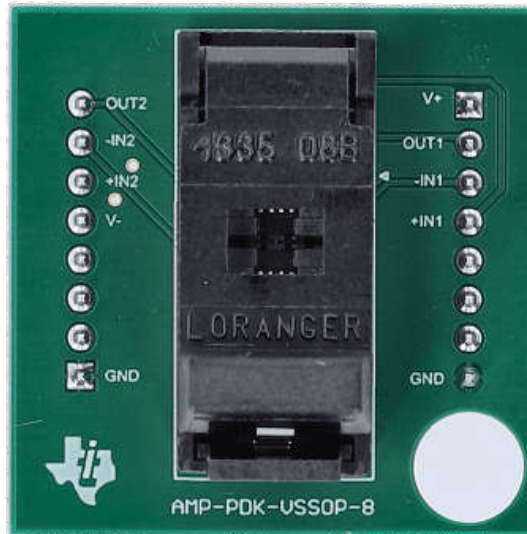


Figure 2-2. AMP-PDK-VSSOP-8

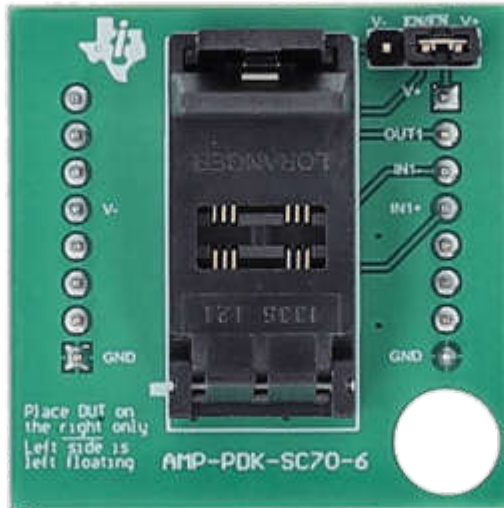


Figure 2-3. AMP-PDK-SC70-6

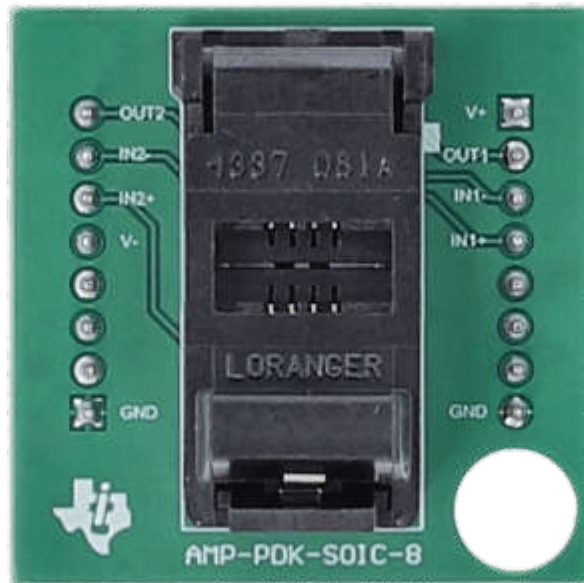


Figure 2-4. AMP-PDK-SOIC-8

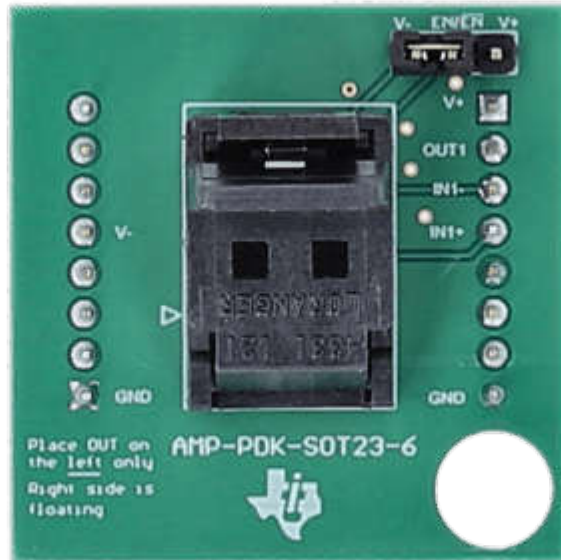


Figure 2-5. AMP-PDK-SOT23-6

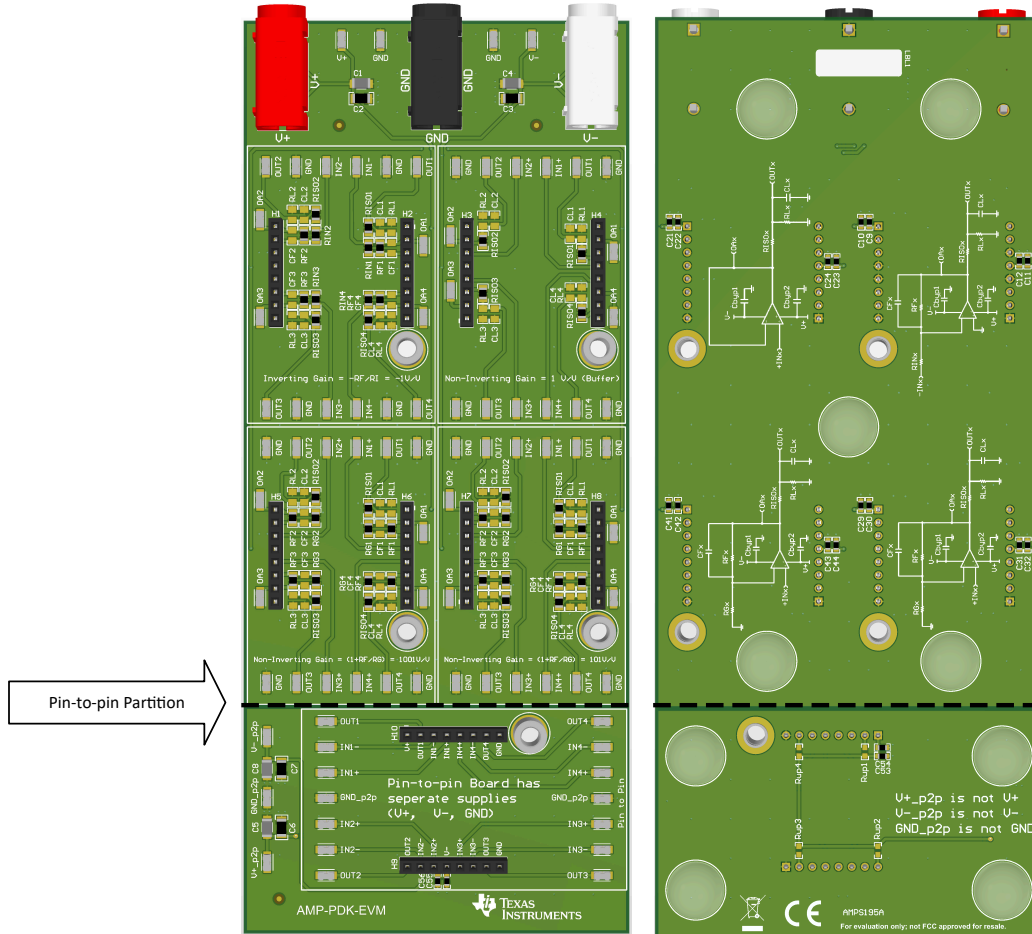


Figure 2-6. AMP-PDK-TSSOP-14

## 2.2 How to Setup

The AMP-PDK-EVM comes with four preconfigured common op amp circuits and one pin-to-pin circuit that can be used to accommodate both op amps and comparators.

The pin-to-pin partition at the bottom can be separated by flexing along the scored edge (shown in [Figure 2-7](#) as a dashed line). There are completely separate power supplies in this partition discussed in further detail in [Section 2.4](#).



**Figure 2-7. AMP-PDK-EVM Main Board - Left (Top), Right (Bottom)**

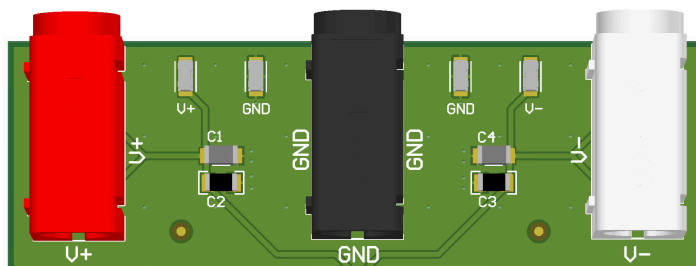
## 2.3 Assembly Instructions

For best practice, follow the recommended assembly procedure:

1. Find which preconfigured circuit or pin-to-pin circuit is most appropriate. Common op amp parameter setups are described in detail in [Section 2.5](#).
2. Install daughtercard onto the selected circuit on AMP-PDK-EVM by aligning both black headers and the alignment metal guide. Apply equal pressure to all four corners of the daughtercard until securely in place.
3. Using [ESD safety precautions](#), place device into the socket with pin 1 alignment. If needed, then reference pin 1 alignment for all daughtercards in [Section 2.7](#).
4. Connect power to the board, this is discussed in further detail in [Section 2.4](#).
5. Connect input and output equipment to the surface mount test points, this is discussed in further detail in the [Section 2.6](#). Common op amp parameter tests setups can be found in [Section 2.5](#).

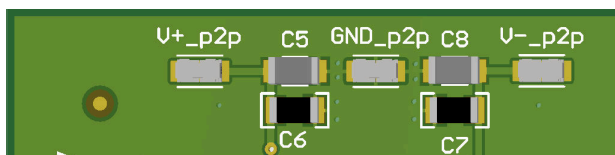
## 2.4 Power Requirements

The four preconfigured op amp test circuits are powered by  $V+$  (positive supply),  $GND$  (ground reference), and  $V-$  (negative supply). The triple power supply connection is required for proper biasing of the preconfigured circuits. The power connection can be accessed either through banana jack connectors or surface mount test points, both are not required.



**Figure 2-8.  $V+$ ,  $V-$ ,  $GND$  Available in Banana Jack Connectors or Surface Mount Test Points**

The pin-to-pin partition has separate power supplies and ground. The pin-to-pin circuit is powered by  $V+_p2p$  (positive supply),  $GND_p2p$  (ground reference), and  $V-_p2p$  (negative supply). A requirement is to access the pin-to-pin power connection through the surface mount test points.



**Figure 2-9.  $V+_p2p$ ,  $V-_p2p$ ,  $GND_p2p$  Available in Surface Mount Connectors**

## 2.5 Setup

To test the parameters of the op amp, the test conditions must match those listed in the electrical characteristics table of the device. The following materials are required for all setup:

- AMP-PDK-EVM main board
- Package variant daughtercard
- Device-under-test (DUT)
- Triple power supply

Once the assembly instructions in [Section 2.3](#) have been implemented, the following test setups can be referenced for common op amp parameters.

In addition to this section, step-by-step instructional videos are available on [ti.com](http://ti.com).

The equipment shown in these examples are for illustration purposes only.

## Quiescent Current per Amplifier ( $I_Q$ )

$I_Q$  is measured in series with the power supply source and the AMP-PDK-EVM.

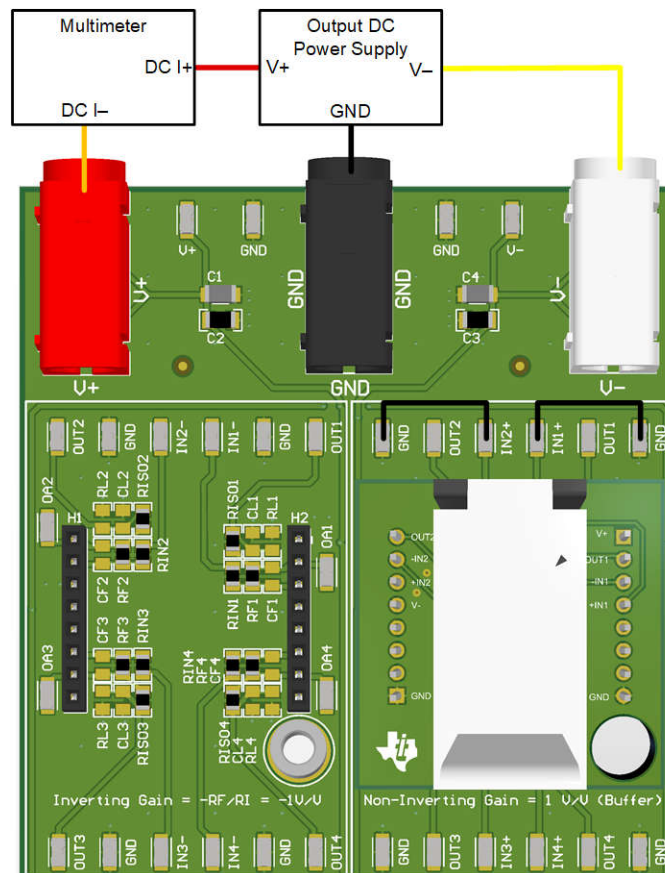
Additional equipment needed for this test:

- Digital multimeter (DMM) or an ammeter

While referencing [Section 2.3](#) to measure  $I_Q$ ,

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit.
2. Connect the positive power supply in series with a DMM:
  - a. Connect  $V^-$  and  $GND$  on AMP-PDK-EVM to the supplies on the triple power supply while matching the device's data sheet conditions. The current limit of the power supply must be set to at least 10 times the  $I_Q$  (considering all channels).
  - b. Connect  $V^+$  on AMP-PDK-EVM to the appropriate port on the DMM.
  - c. Connect the other port from the DMM to the positive power supply on the triple power supply. Limit the output current to at least 10 times the  $I_Q$  (considering all channels).
3. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All  $INx^+$  pins on the sub-circuit must be connected to  $GND$ .
4. Configure the DMM to measure DC current.
5. Turn on the power supply output.
6. On the DMM, divide the observed current by the number of channels in the op amp.

With all other data sheet conditions matched, this test setup helps verify the quiescent current in the data sheet with the one calculated. <sup>1</sup>



**Figure 2-10.  $I_Q$  Measurement Example Setup for a Dual Channel Device**

<sup>1</sup> Some devices have *ultra-low* quiescent currents; therefore require DMM with additional digits (> 6.5 digits).



## Continuity

Most op amp pins have ESD protection diodes to either power supply rail ( $V+$  or  $V-$ ). To check for the presence and operation of these diodes, follow this procedure.

Additional equipment needed for this test:

- Digital multimeter (DMM) or an ammeter

### Note

This is a single supply test and therefore does not require a triple power supply.

While referencing [Section 2.3](#) to measure continuity,

1. Install a daughtercard onto the pin-to-pin circuit.
2. Connect the power supply's positive supply to the appropriate port of the DMM. The current limit of the power supply must be set to 9mA.
3. The ground from the power supply and the other port on the DMM are the two points of continuity, due to the nature of ESD diodes, one must be referenced to a power supply  $V+_p2p$  or  $V-_p2p$ ; the other is the *pin-under-test*.
4. Turn on the power supply output.
5. Manually increase the power supply output voltage in small increments, recording the current between increments, until the measured current reaches a maximum of 9mA. Do not exceed 2-3V in either direction.
6. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All  $INx+$ ,  $INx-$ , and  $OUTx$  pins can be tested against  $V+_p2p$  or  $V-_p2p$ .

Alternatively, this test can be automated with a source meter.

This test setup helps verify the presence and operation of ESD diodes.

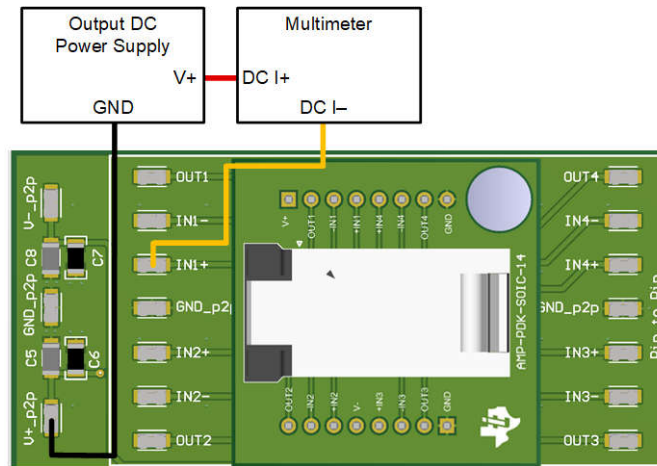


Figure 2-11. Continuity Measurement Example Setup for a Quad Channel Device

## Input Offset Voltage ( $V_{OS}$ )

$V_{OS}$  is an error source at the input stage of the op amp, quantified as the differential input voltage needed to force the op amp's output to 0V.

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter

While referencing [Section 2.3](#) to measure  $V_{OS}$ ,

1. Install a daughtercard onto the *Non-Inverting Gain = 1001V/V* or *Non-Inverting Gain = 101V/V* preconfigured circuit depending on the typical or expected offset voltage of the device. In general, use the *Non-Inverting Gain = 1001V/V* for precision op amps and *Non-Inverting Gain = 101V/V* for general purpose op amps.
2. Connect the triple power supply to the  $V_+$ ,  $GND$ , and  $V_-$  of AMP-PDK-EVM while matching the data sheet conditions of the device. The current limit of the power supply can be set to the  $I_{SC} + I_Q$  of the device (considering all channels).
3. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All  $INx+$  pins on the sub-circuit needs to be connected to  $GND$ .
4. Connect one port of the DMM to  $OUTx$  and the other to  $GND$ .
5. Configure the DMM to measure DC voltage.
6. Turn on the power supply output.
7. Divide the voltage measurement of DMM by the gain of the preconfigured circuit.

With all other data sheet conditions matched, this test setup helps verify the input offset voltage in the data sheet with the one calculated.

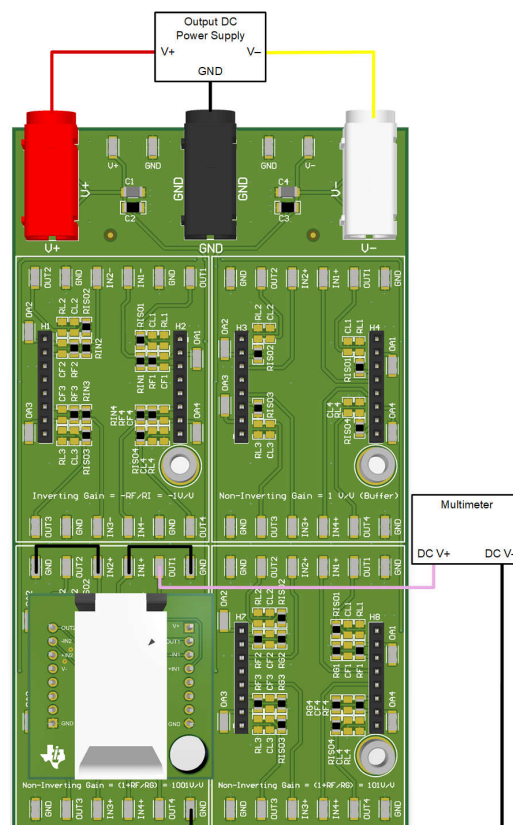


Figure 2-12.  $V_{OS}$  Measurement Example Setup for a Dual Channel Device

## Voltage Output Swing from Supply Voltages ( $V_{OL}/V_{OH}$ )

$V_{OH}$  and  $V_{OL}$  are the voltage limit of the output of the op amp as the output approaches the  $V+$  and  $V-$  of the device.

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter

While referencing [Section 2.3](#) to measure  $V_{OH}$  and  $V_{OL}$

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit. For non-rail-to-rail input op amps, the amplifier needs to be placed in a gain to try to force the output to either rail.
2. Connect the triple power supply to the  $V+$ ,  $GND$ , and  $V-$  of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply needs to be set to the  $I_{SC} + I_Q$  of the device (considering all channels).
3. Connect the single power supply between  $INx+$  pin and  $GND$ . Set the single supply voltage to the  $V+$  value of the op amp. The current limit of the power supply must be set to 9mA.
4. Connect one port of the DMM to  $OUTx$  and the other to  $GND$ .
5. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other  $INx+$  pins on the sub-circuit must be connected to  $GND$ .
6. Configure DMM to measure DC voltage.
7. Turn on the triple power supply first; subsequently, turn on the single power supply.
8. The  $V_{OH}$  is the difference between  $V+$  and the voltage measured on the DMM.
9. Swap the single supply connections listed in Step #3. The positive supply must be connected to  $GND$  and ground from the supply must be connected to  $+INx$  pin.
10. The  $V_{OL}$  is the difference between  $V+$  and absolute value of voltage measured on the DMM.

With all other data sheet conditions matched, this test setup helps verify the voltage output swing from rail in the data sheet with the calculated.

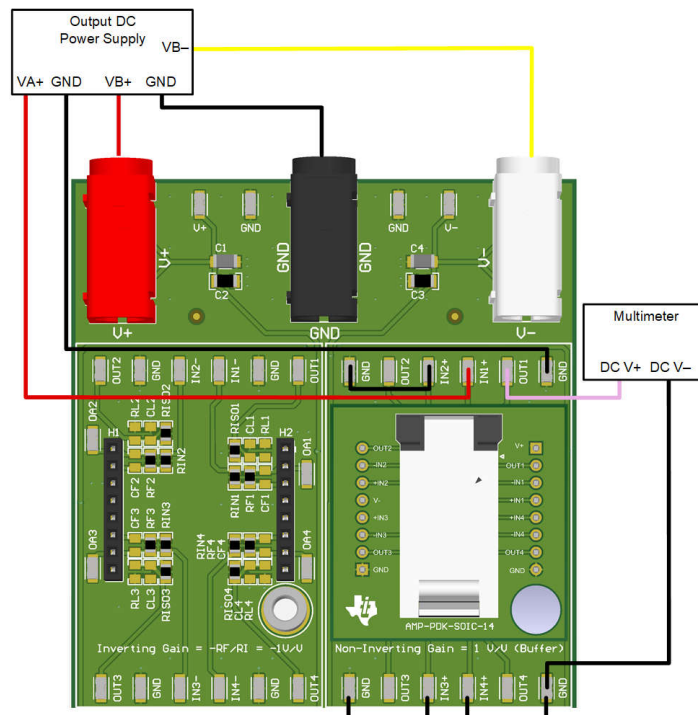


Figure 2-13.  $V_{OH}$  Measurement Example for a Quad Channel Device

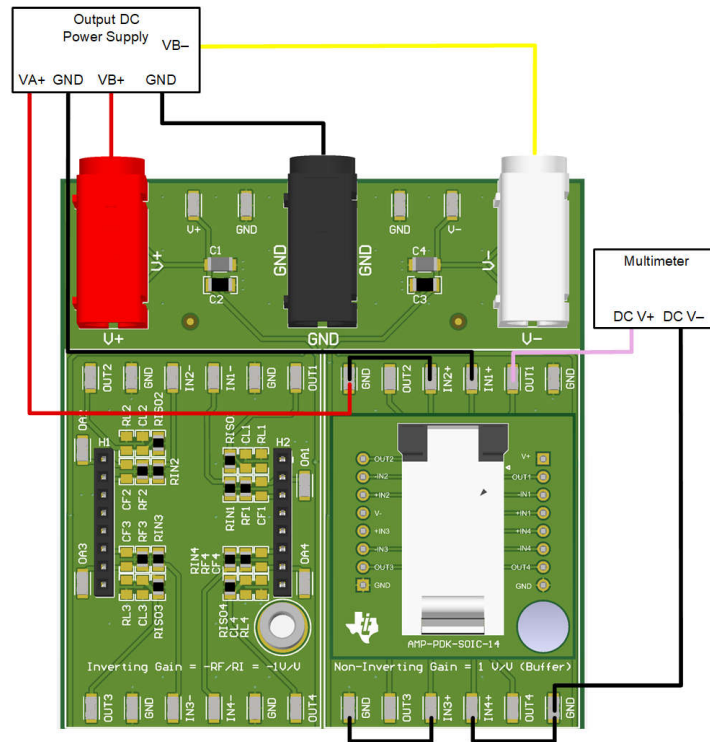


Figure 2-14. VOL Measurement Example for a Quad Channel Device

## Gain Bandwidth Product (GBWP)

Additional equipment needed for this test:

- Digital multimeter (DMM) or a voltmeter
- Waveform function generator

While referencing [Section 2.3](#) to measure GBW,

1. Install a daughtercard onto the *Non-Inverting Gain = 101V/V* preconfigured circuit.
2. Connect the triple power supply to the  $V+$ ,  $GND$ , and  $V-$  of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply must be set to the  $I_{SC} + I_Q$  of the device (considering all channels).
3. Connect the output of the frequency generator to the  $INx+$  pin and reference to  $GND$ .
4. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other  $INx+$  pins on the sub-circuit must be connected to  $GND$ .
5. Connect one DMM port to  $OUTx$  and the other to  $GND$ .
6. Turn on the power supply output.
7. Configure the waveform generator to output a small signal (20mVpp, 100Hz, 0 offset voltage).
8. Turn on the waveform function generator.
9. Configure DMM to measure AC voltage. Record the DMM voltage.
10. Increase the frequency on the waveform generator until the DMM reads 70.7% of the original DMM voltage. Record the frequency of the waveform generator.
11. Divide the frequency by the gain of the preconfigured circuit.

With all other data sheet conditions matched, this test setup helps verify the gain bandwidth product in the data sheet with the calculated.

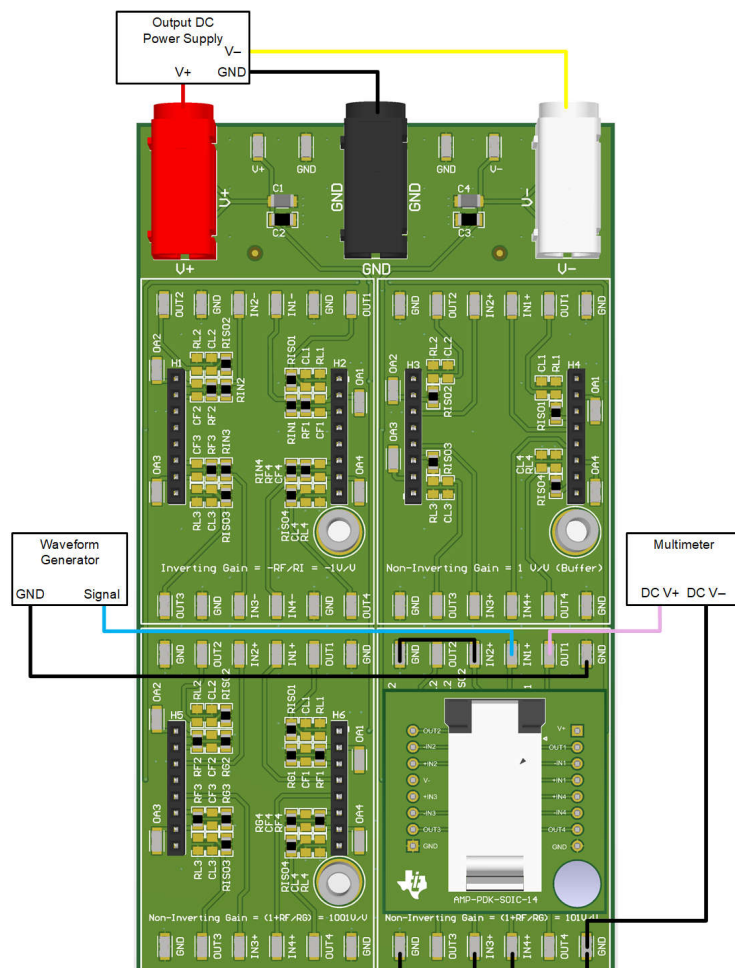


Figure 2-15. BW Measurement Example for Quad Channel Device

## Slew Rate (SR)

SR is the maximum rate of change of an op amp's output voltage in volts per microsecond.

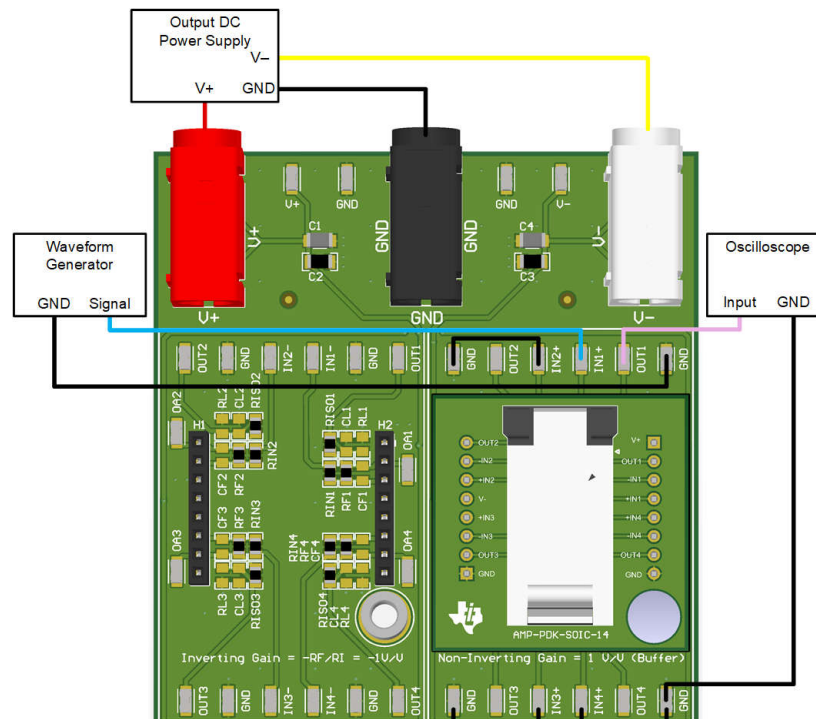
Additional equipment needed for this test:

- Oscilloscope
- Waveform function generator

While referencing [Section 2.3](#) to measure SR,

1. Install a daughtercard onto the *Non-Inverting Gain = 1V/V (Buffer)* preconfigured circuit.
2. Connect the triple power supply to the  $V+$ ,  $GND$ , and  $V-$  of AMP-PDK-EVM while matching the device's data sheet conditions. The current limit of the power supply must be set to the  $I_{SC} + I_Q$  of the device (considering all channels).
3. Connect the waveform generator to the  $INx+$  pin with a reference to  $GND$ . The input signal must be step function the size of the input voltage common mode listed in the data sheet.
4. Depending on how many channels the op amp has, the daughtercard has all possible pins mapped out. All other  $INx+$  pins on the sub-circuit must be connected to  $GND$ .
5. Connect an oscilloscope probe to the  $OUTx$  with a probe referenced to  $GND$ .
6. Turn on the power supply output.
7. Turn on the waveform function generator.
8. Configure the oscilloscope to measure approximately 10% and 90% of the output waveform, note the time differential. Slew rate is the rate of change in volts per microsecond.

With all other data sheet conditions matched, this test setup helps verify the slew rate in the data sheet with the one calculated.



**Figure 2-16. SR Measurement Example for a Single Channel Device**

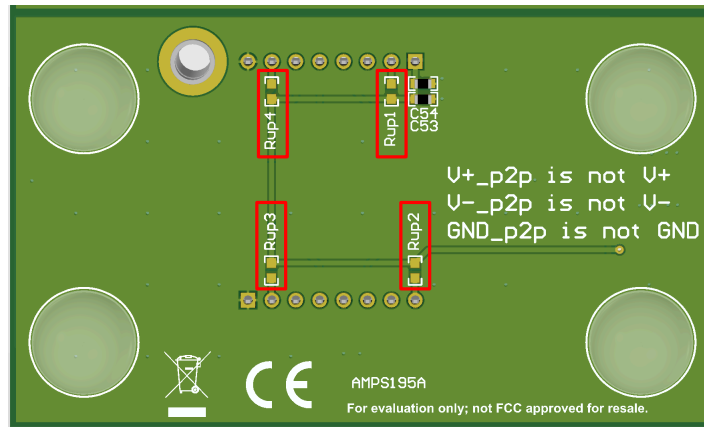
## Comparators Setup

The AMP-PDK-EVM kit has the capability of testing basic functionality of comparators using the pin-to-pin circuit. Do not test a comparator device with any of the other gain configurations as this can result in measurement errors. Positive feedback or hysteresis setup is not available with the board.

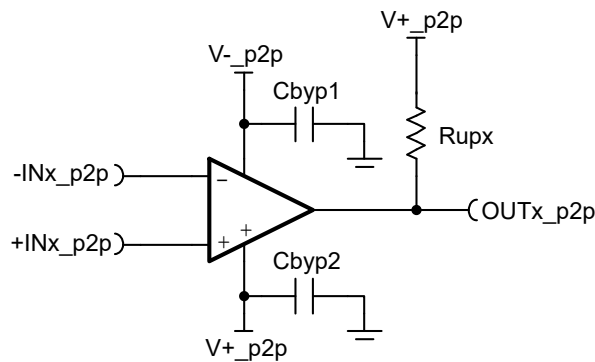
The backside of the pin-to-pin board contains an option to populate pull-up resistors  $R_{upx}$  on the output of the comparator, as shown in [Figure 2-17](#). By default,  $R_{upx}$  are unpopulated.

$R_{upx}$  is required to populate for any comparator that has an open-drain/open-collector output type. Without the pull-up resistor, the output of the comparator can float to an unknown state. This resistor does not need to be populated when using push-pull devices. The output type of the comparator can be verified in the product page and data sheet.

For more information on comparators, please reference [TI Precision Labs](#).



**Figure 2-17. Pin-to-Pin Circuit (Back View)**



**Figure 2-18. Pin-to-pin Schematic with Pull-Up Resistor Option**

## Advanced Test Setup

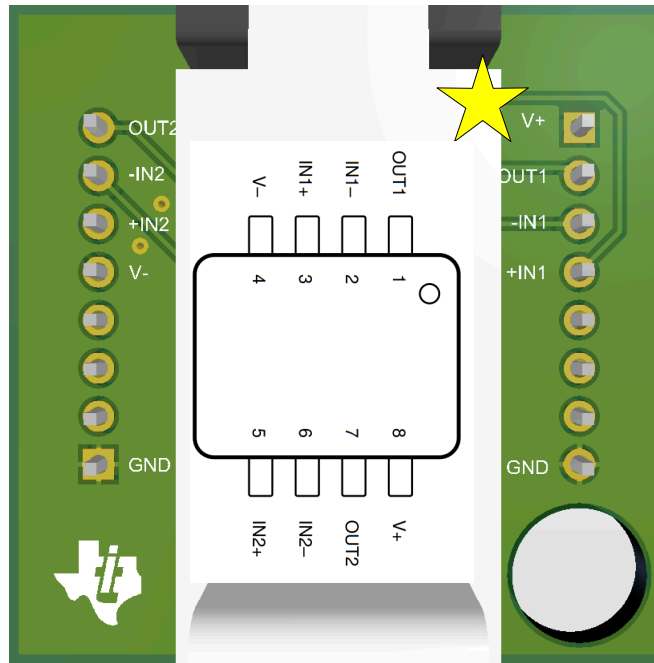
The above test setups are solderless preconfigured op amp designs with the options of a gain of 1, 101, 1001, and -1. The board can also be re-purposed in different gain ratios by changing the passive components. In addition to the existing populated passives, there is compensation circuitry options included to limit noise ( $C_F$ ) and help improve stability ( $R_{ISO}$ ) as seen in [Schematics](#). The  $OAx$  test point is given to help verify amplifier stability. For more resources on op amp noise and stability, please reference [TI Precision Labs](#).

## 2.6 Header Information

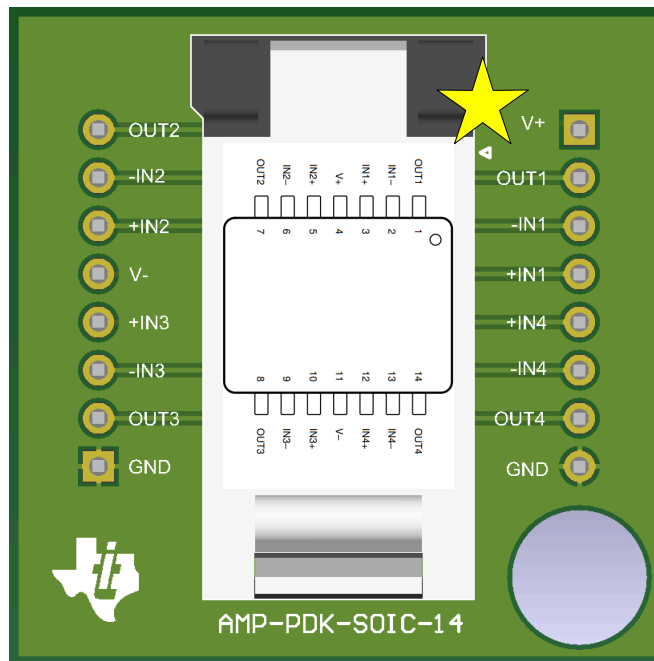
The AMP-PDK-EVM has surface mount test points populated on the board. The surface mount test points best connect to a banana jack to clip cable or an oscilloscope probe. There are also black headers in each circuit to allow the interface between the AMP-PDK-EVM and a daughtercard. If connecting a piece of equipment that has BNC connections, then TI recommends to use a *BNC-to-clip* adapter.

## 2.7 Interfaces

The AMP-PDK-EVM has hardware interfaces between the AMP-PDK-EVM, the daughtercard, and the device as seen earlier in [Figure 1-1](#). The daughtercard can only be plugged in one way due to the metal alignment poles. The device can be plugged in several directions, therefore TI recommends to reference the figures below. Single channel daughtercards have a shutdown enable option via a header on the top right of the board. Refer to the corresponding device data sheet to determine which configuration to set the two-pin jumper to enable or disable shutdown mode.



**Figure 2-19. AMP-PDK-VSSOP-8 - Pin 1 Orientation Example**



**Figure 2-20. AMP-PDK-SOIC-14 - Pin 1 - Orientation Example**



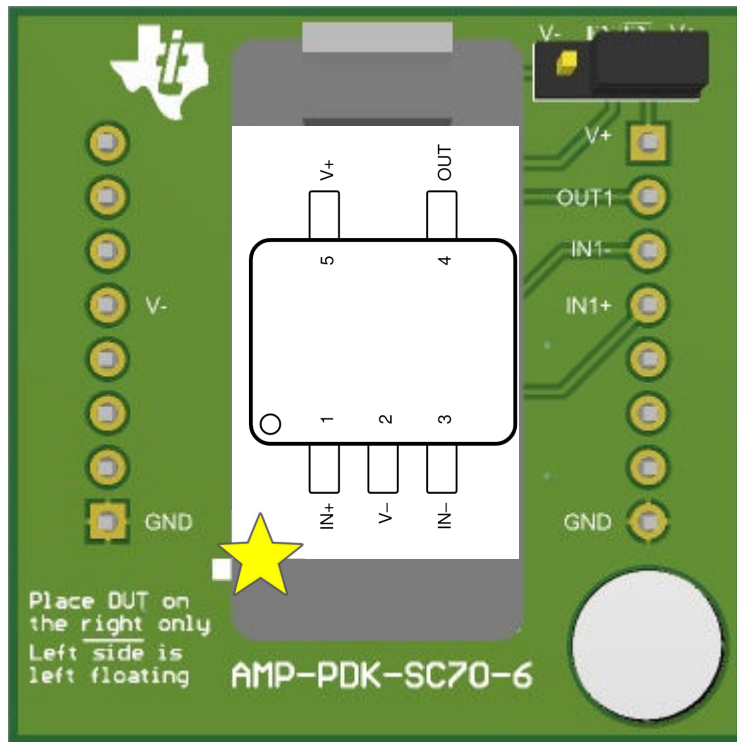


Figure 2-21. AMP-PDK-SC70-6 - Pin 1 - Orientation Example

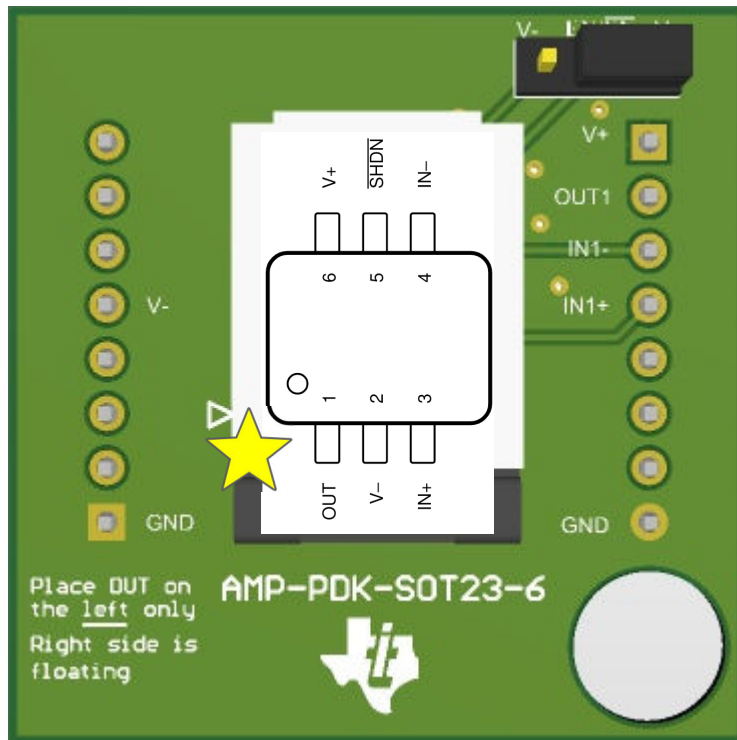


Figure 2-22. AMP-PDK-SOT23-6 - Pin 1 - Orientation Example

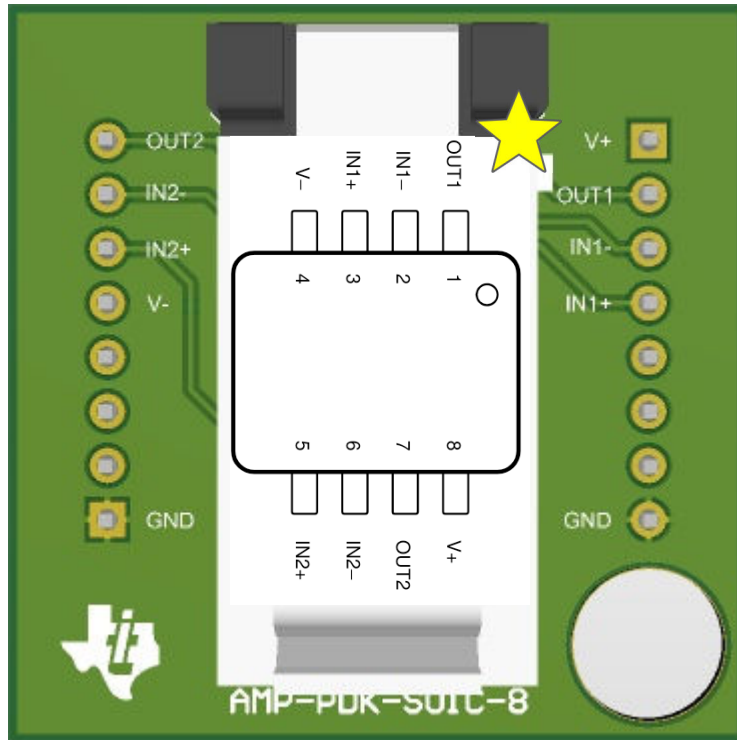


Figure 2-23. AMP-PDK-SOIC-8 - Pin 1 - Orientation Example

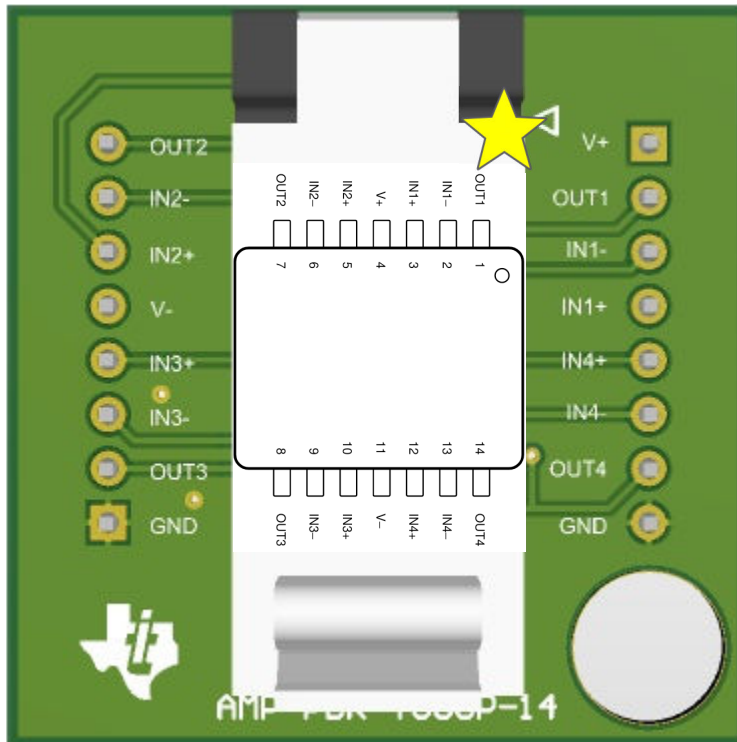


Figure 2-24. AMP-PDK-TSSOP-14 - Pin 1 - Orientation Example

## 2.8 Best Practices

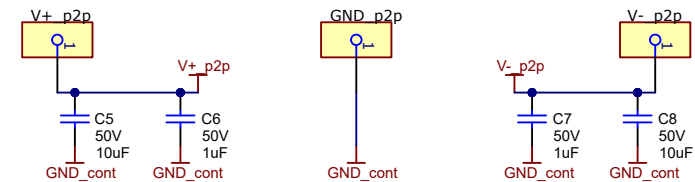
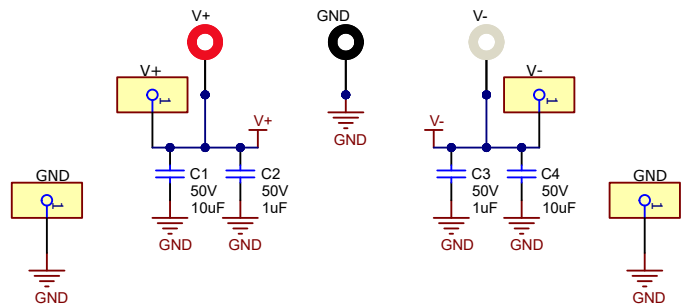
For best user-experience, the following are recommended:

1. Implement [Section 2.3](#).
2. If not already populated, solder on bypass capacitors on daughter card and the main board.
3. Reference stability resources for robust op amp designs.
4. Only utilize the ground surface mount test points as a ground reference. Avoid connecting *GND* and *GND\_p2p* to the metal alignment poles. The alignment metal poles are mechanically but not electrically connected and can introduce a ground shift potential.

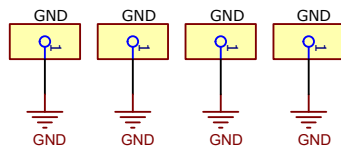
### 3 Hardware Design Files

#### 3.1 Schematics

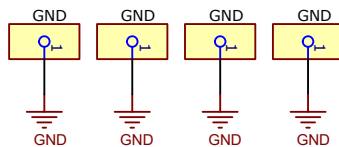
#### Power Supplies



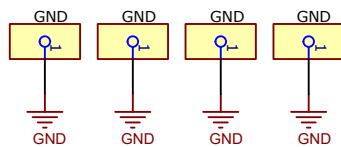
Non-inverting gain of 1 (Buffer)



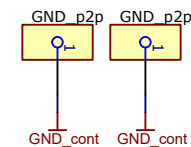
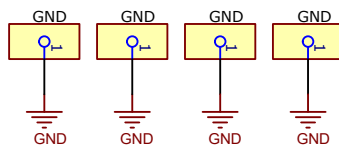
Inverting gain of -1



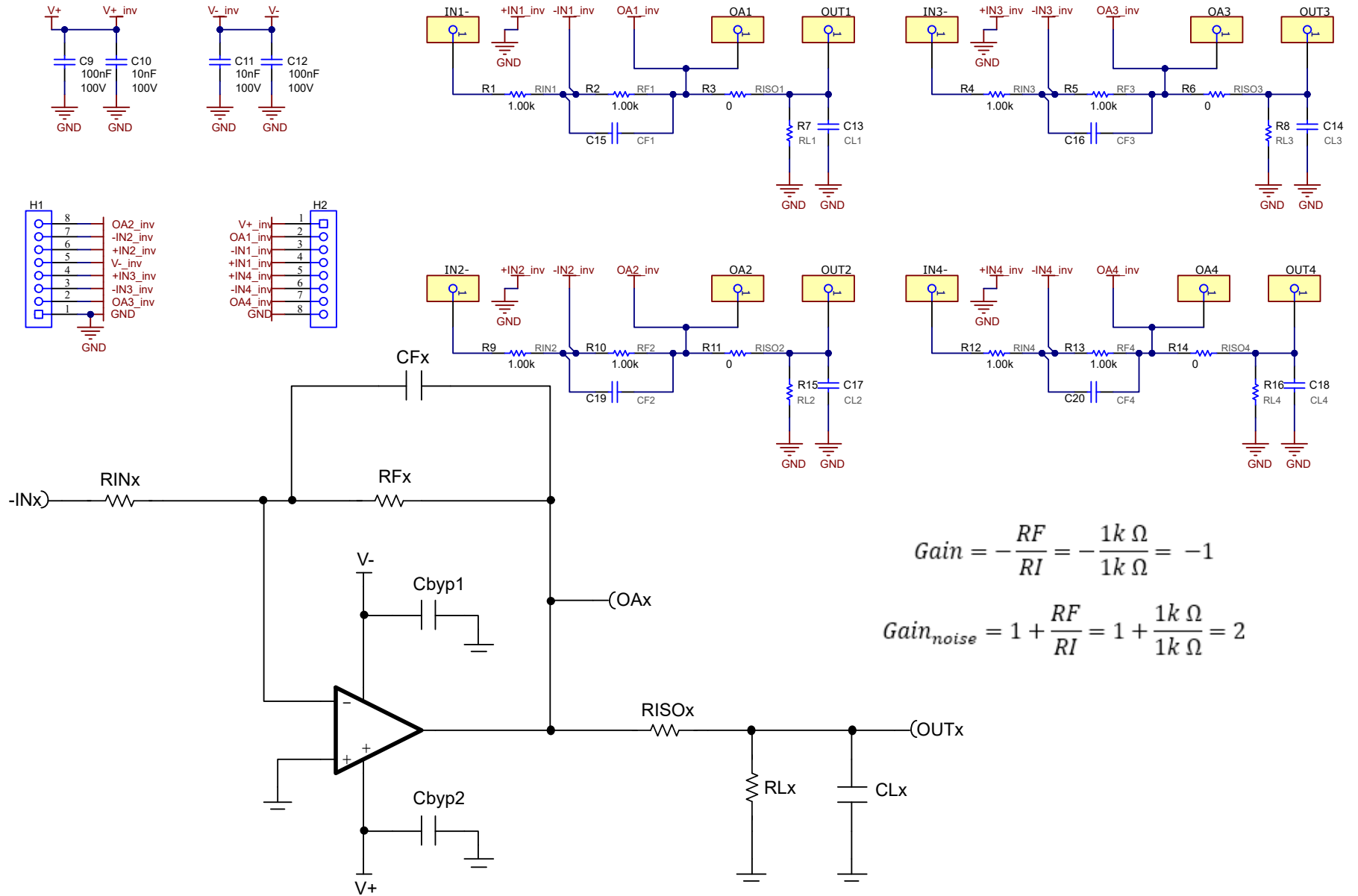
Non-inverting gain of 101



Non-inverting gain of 1001



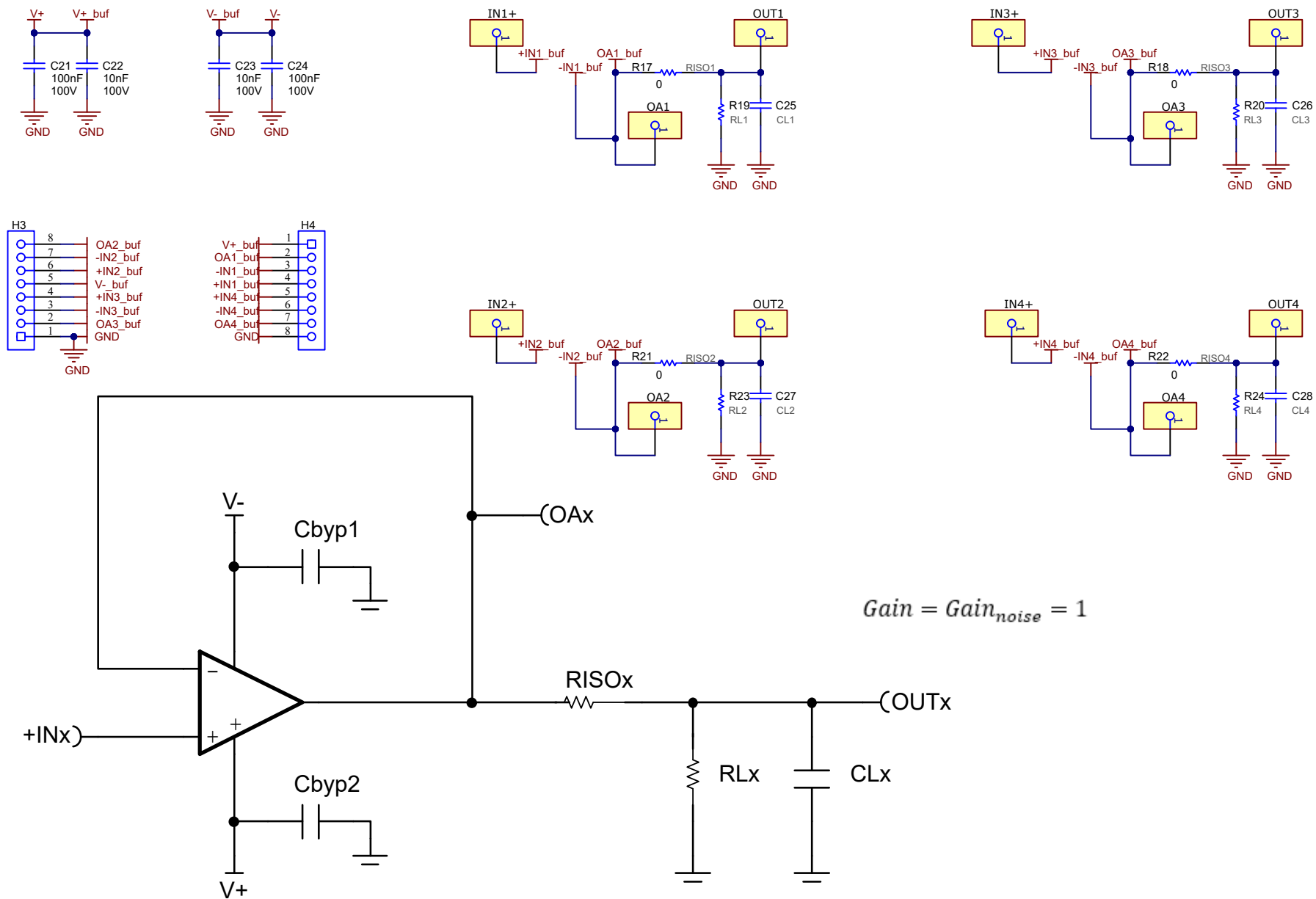
## Inverting Gain of -1



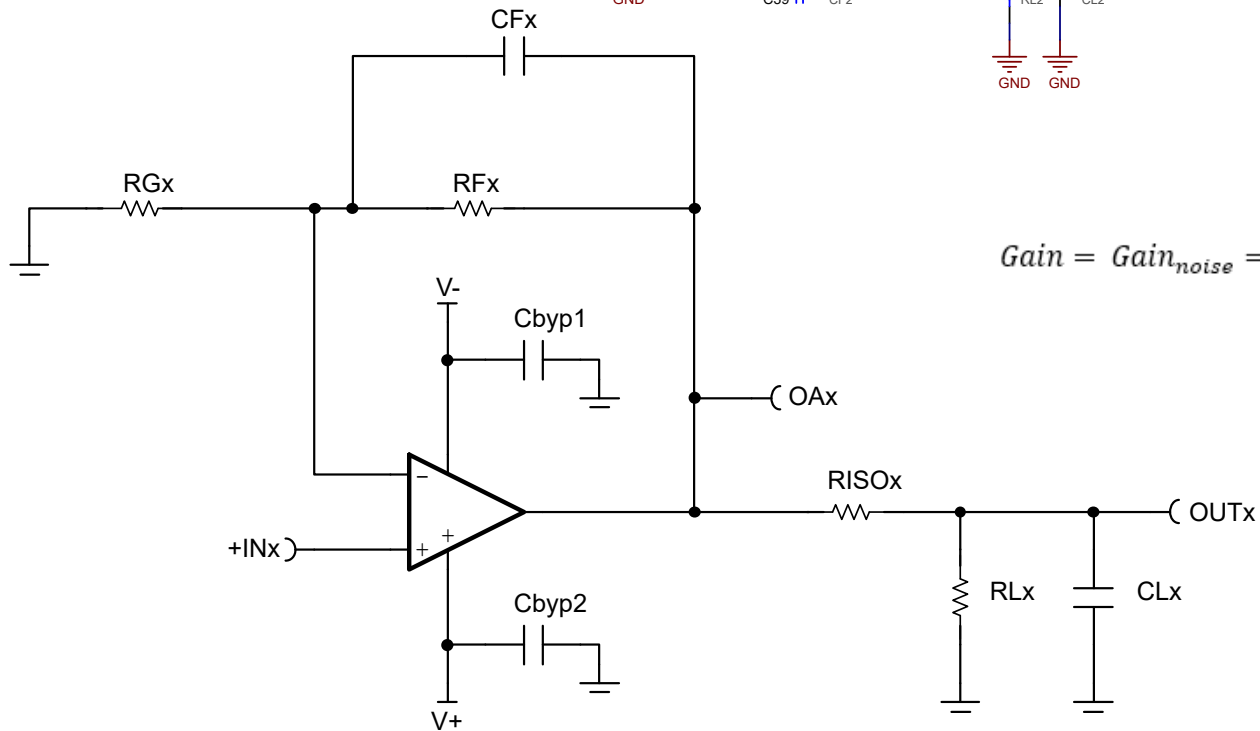
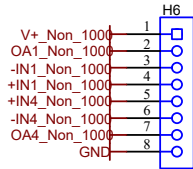
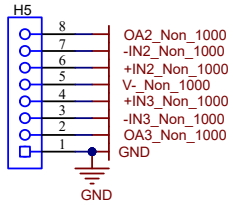
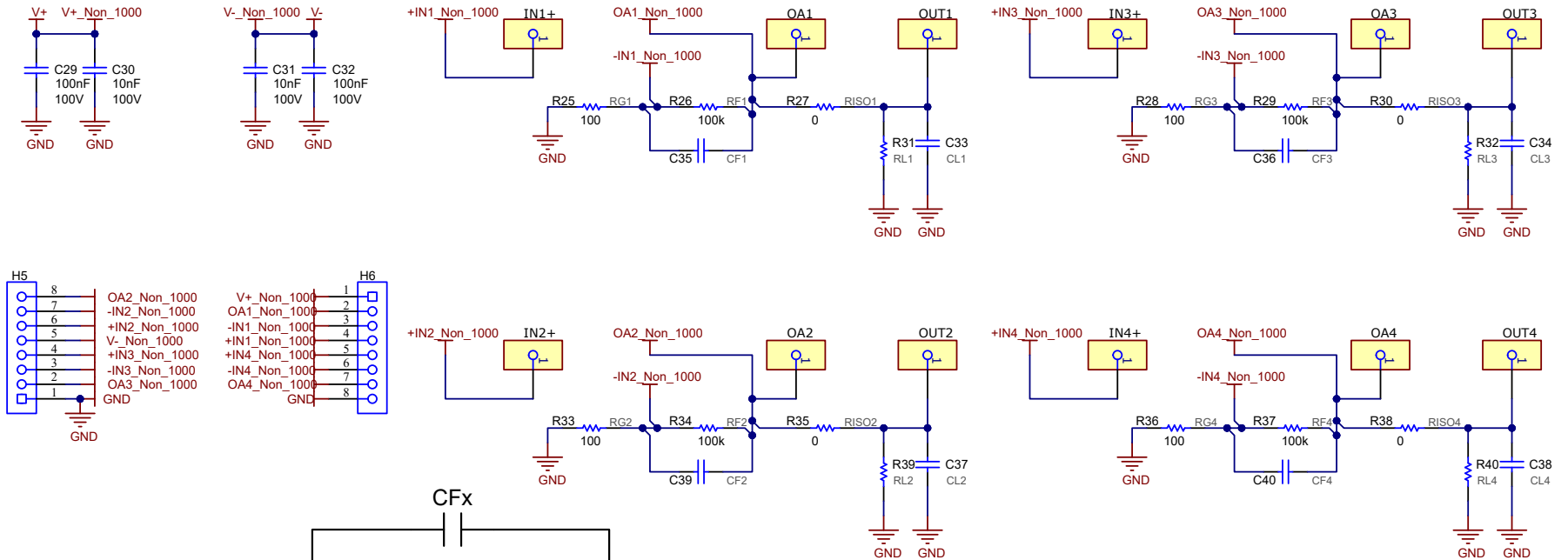
$$Gain = -\frac{RF}{RI} = -\frac{1k\ \Omega}{1k\ \Omega} = -1$$

$$Gain_{noise} = 1 + \frac{RF}{RI} = 1 + \frac{1k\ \Omega}{1k\ \Omega} = 2$$

## Non-inverting gain of 1 (Buffer)

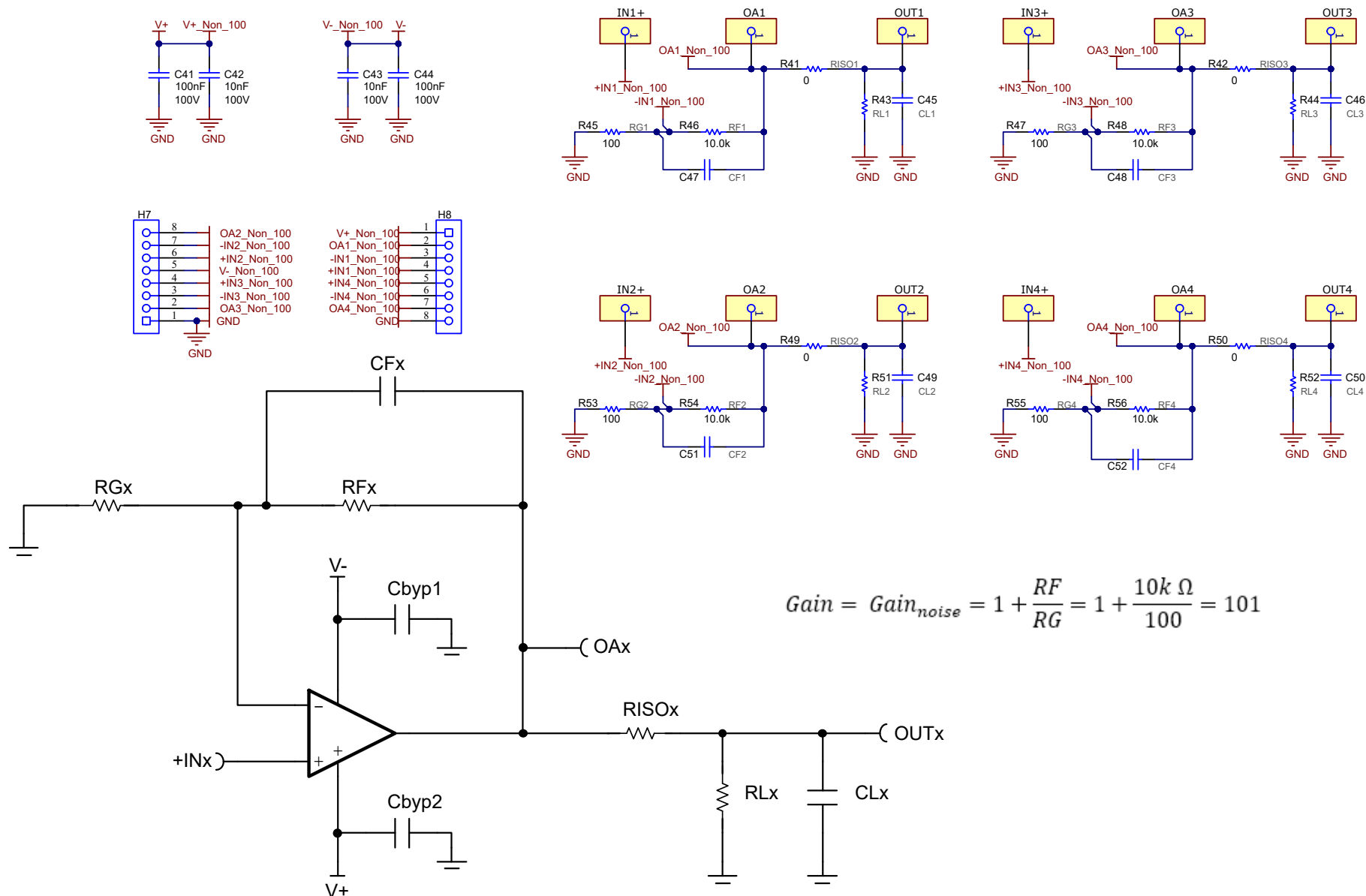


## Non-inverting gain of 1001



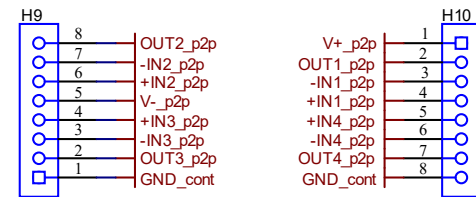
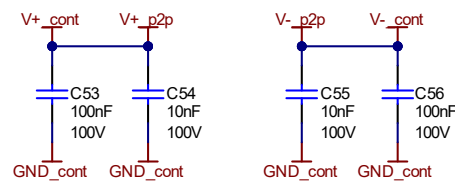
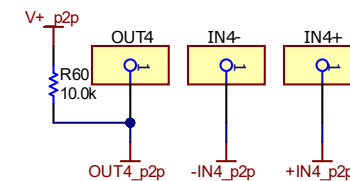
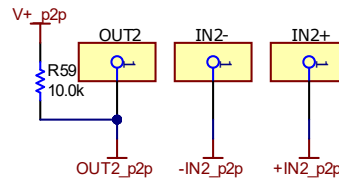
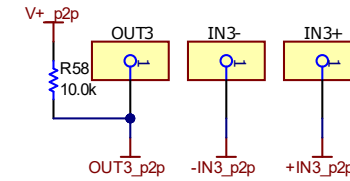
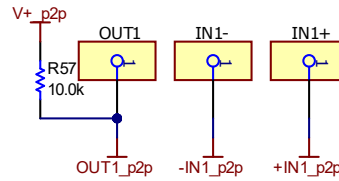
$$Gain = Gain_{noise} = 1 + \frac{RF}{RG} = 1 + \frac{100k\ \Omega}{100\ \Omega} = 1001$$

# Non-inverting gain of 101

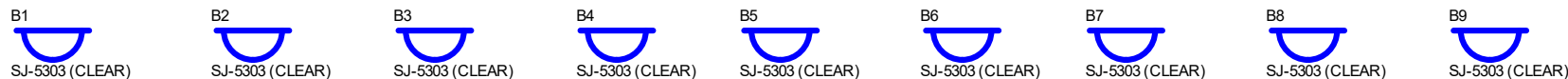
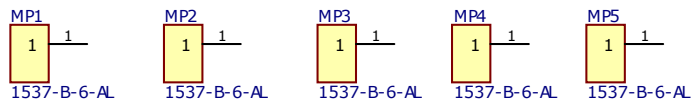




# Pin-to-pin



# Hardware



PCB Number: AMPS195  
PCB Rev: A

PCB  
LOGO  
Texas Instruments



PCB  
LOGO  
FCC disclaimer

PCB  
LOGO  
WEEE logo

LBL1  
PCB Label  
AMPS195A  
Size: 0.65" x 0.20"

Variant/Label Table	
Variant	Label Text
001	AMPS195A

ZZ1  
Assembly Note  
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2  
Assembly Note  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3  
Assembly Note  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4  
Label Assembly Note  
This Assembly Note is for PCB labels only

### 3.2 PCB Layouts

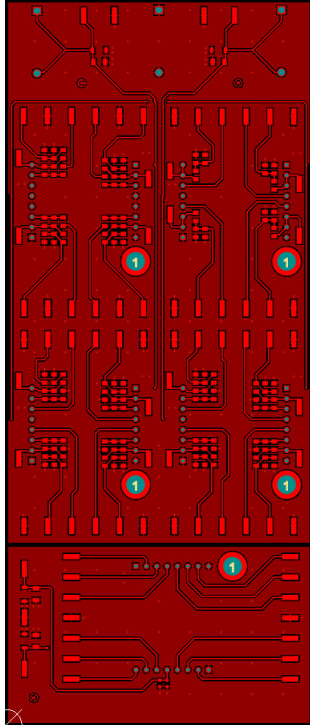


Figure 3-1. AMP-PDK-EVM Top Layer

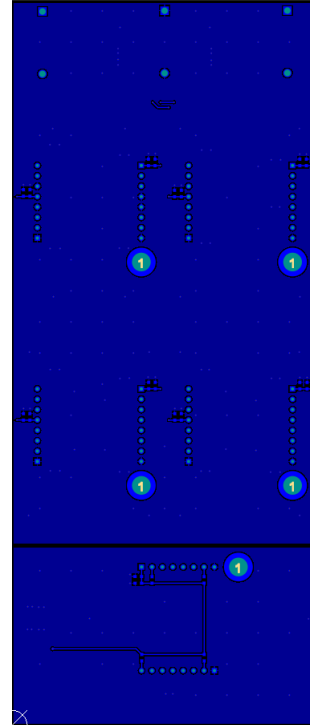


Figure 3-2. AMP-PDK-EVM Bottom Layer

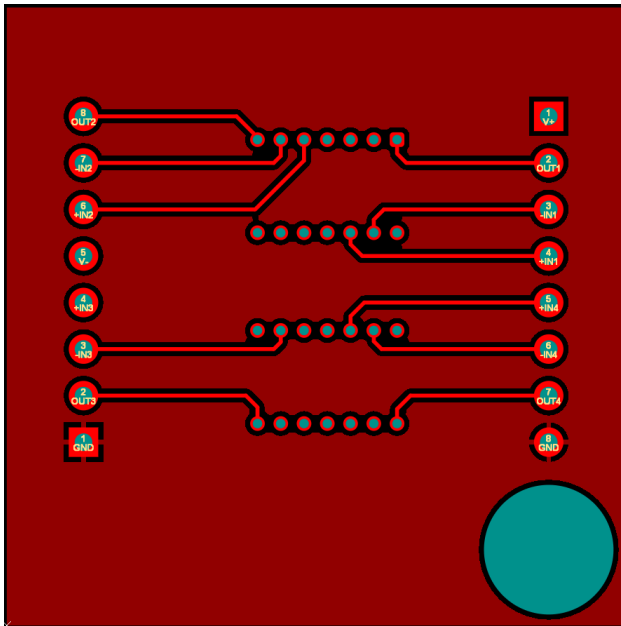


Figure 3-3. AMP-PDK-SOIC-14 Top Layer

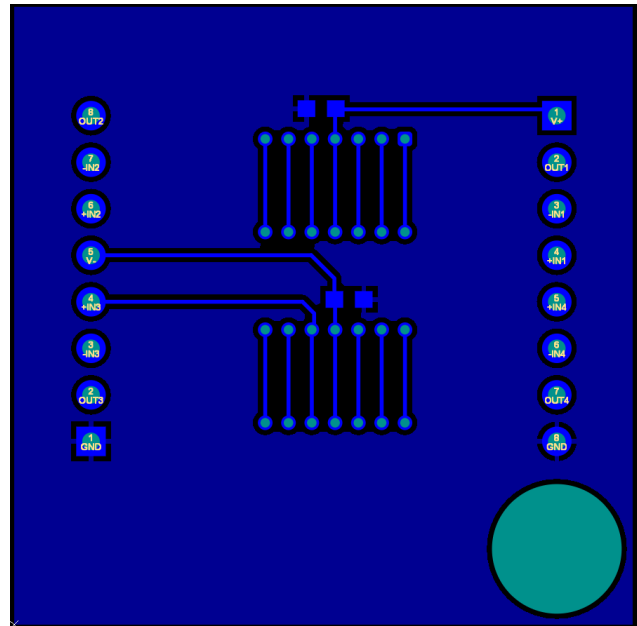


Figure 3-4. AMP-PDK-SOIC-14 Bottom Layer

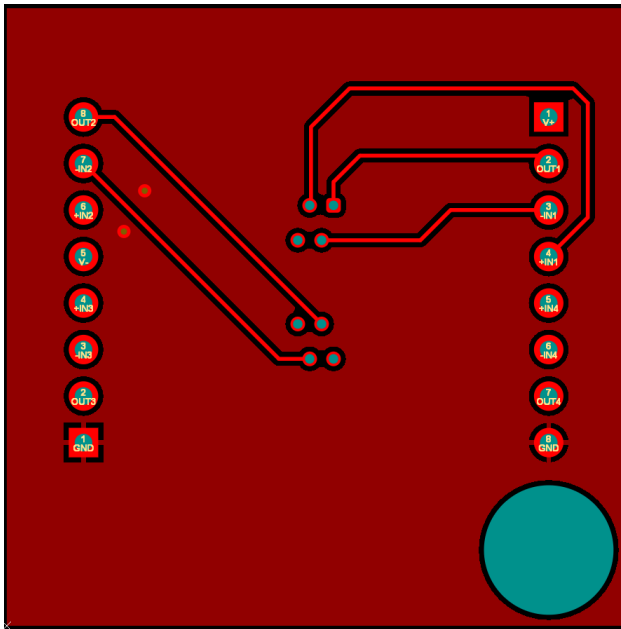


Figure 3-5. AMP-PDK-VSSOP-8 Top Layer

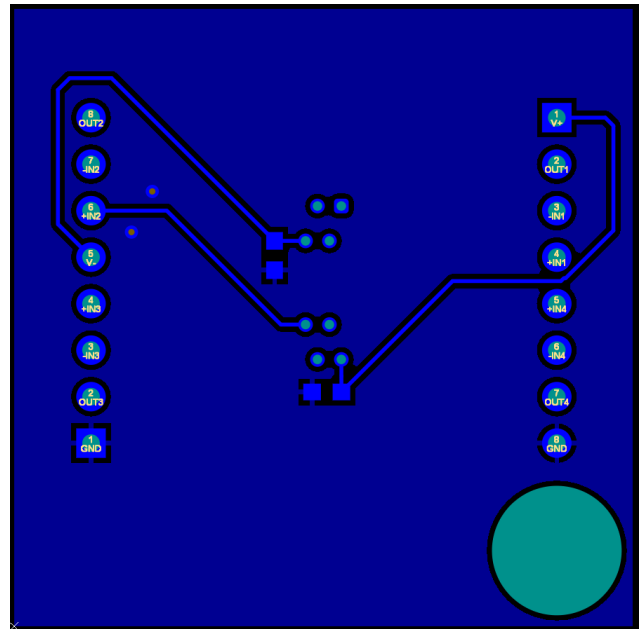


Figure 3-6. AMP-PDK-VSSOP-8 Bottom Layer

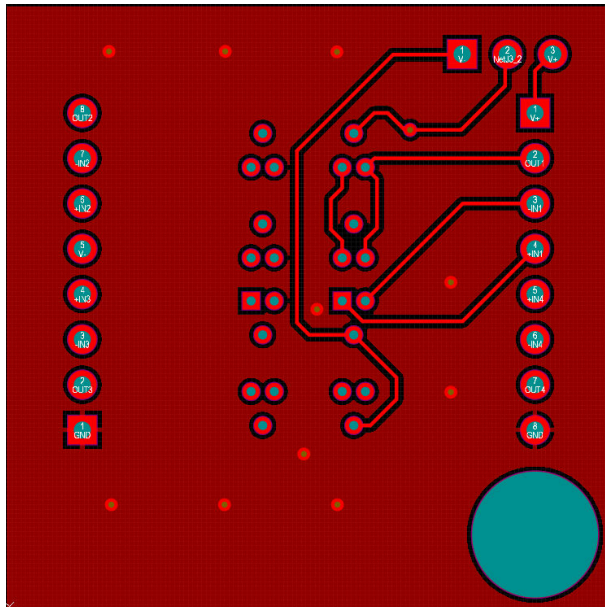


Figure 3-7. AMP-PDK-SC70-6 Top Layer

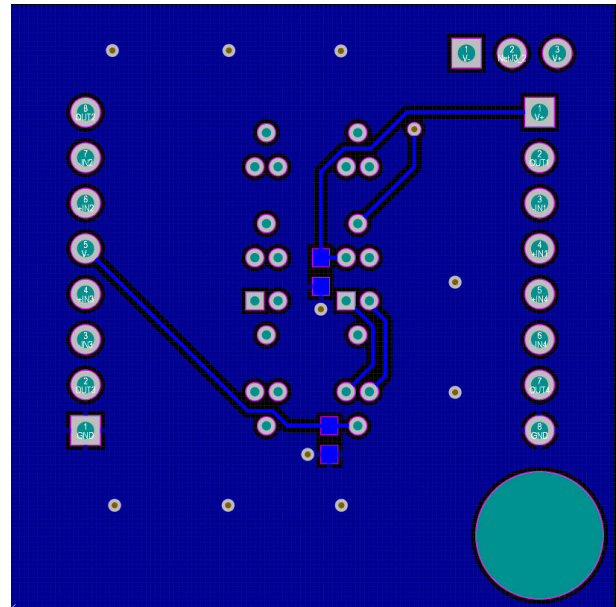


Figure 3-8. AMP-PDK-SC70-6 Bottom Layer

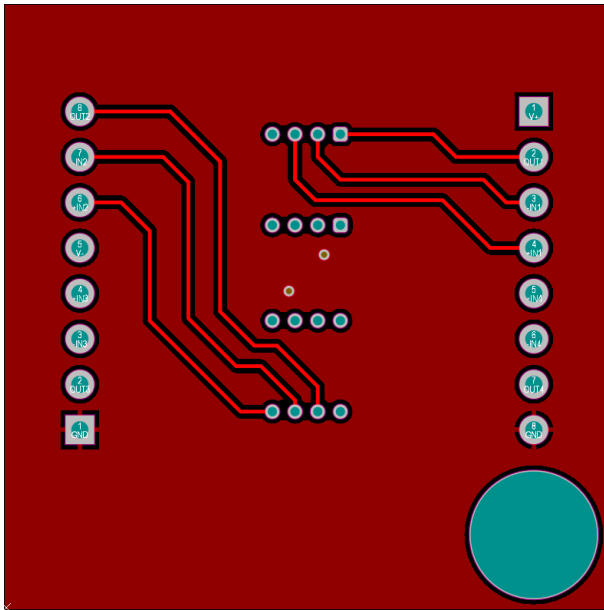


Figure 3-9. AMP-PDK-SOIC-8 Top Layer

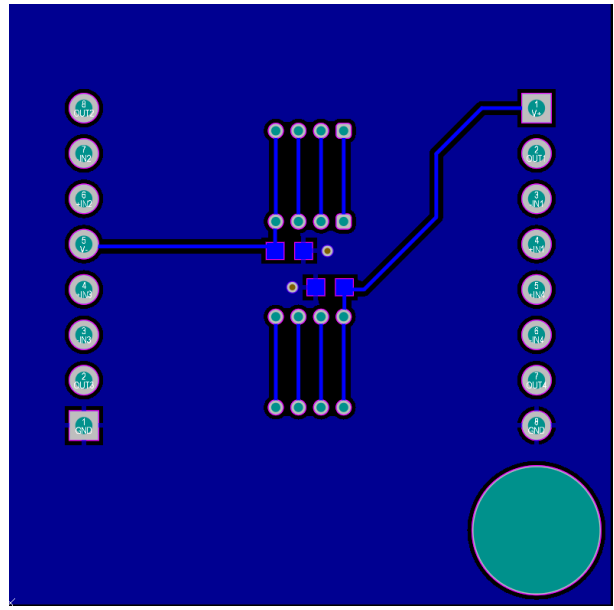


Figure 3-10. AMP-PDK-SOIC-8 Bottom Layer

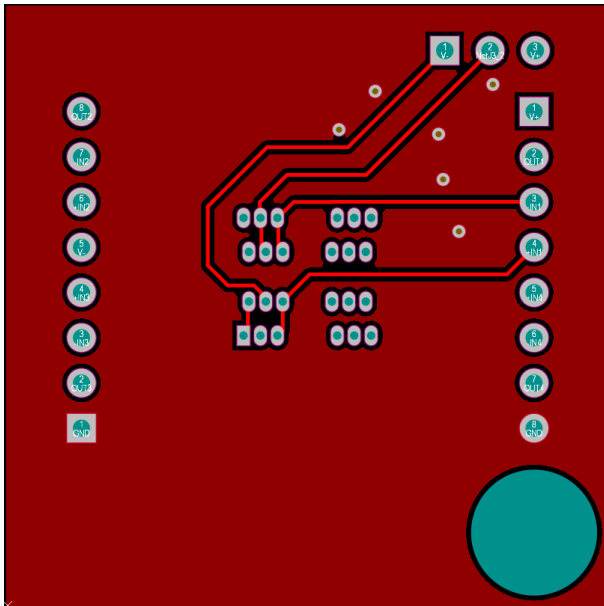


Figure 3-11. AMP-PDK-SOT23-6 Top Layer

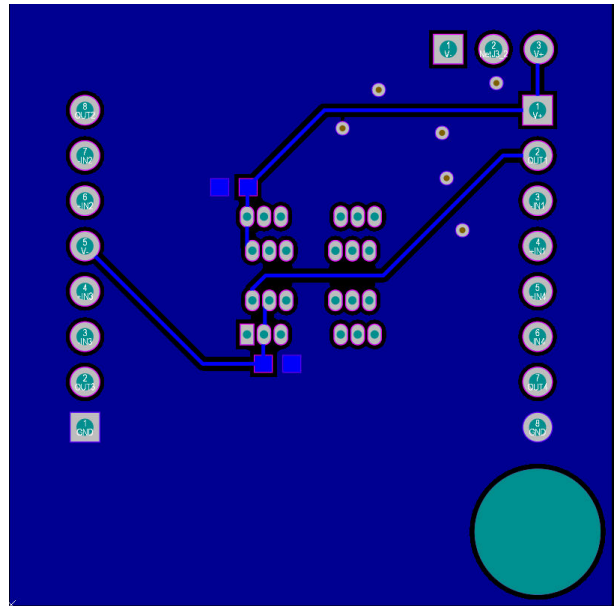


Figure 3-12. AMP-PDK-SOT23-6 Bottom Layer

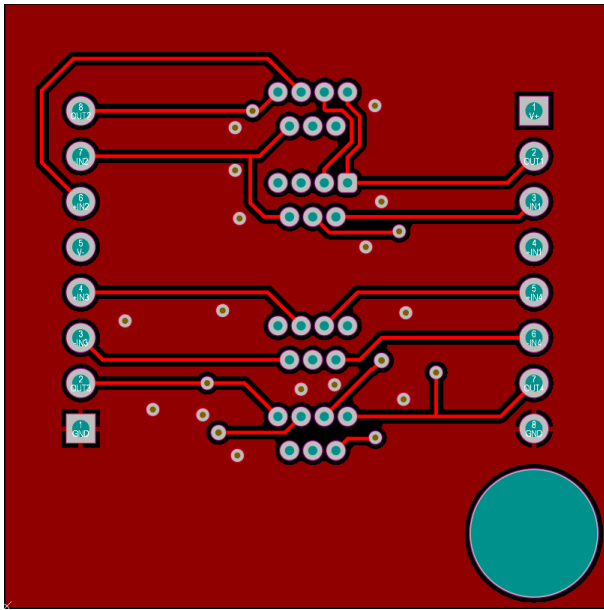


Figure 3-13. AMP-PDK-TSSOP-14 Top Layer

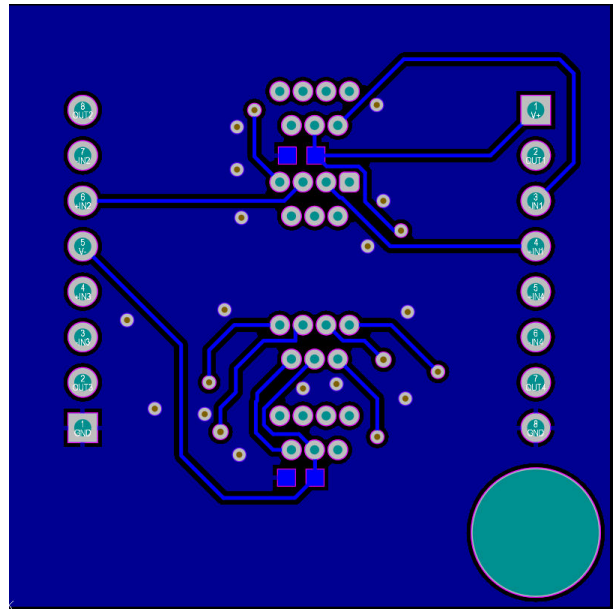


Figure 3-14. AMP-PDK-TSSOP-14 Bottom Layer

### 3.3 Bill of Materials (BOM)

**Table 3-1. AMP-PDK-EVM**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1	AMP-PDK-EVM	Printed Circuit Board		AMP-PDK-EVM	Any
B1, B2, B3, B4, B5, B6, B7, B8, B9	9		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
C1, C4, C5, C8	4	10uF	CAP, CERM, 10uF, 50V, +/- 10%, X5R, AEC-Q200 Grade 1, 1206	1206	GRT31CR61H106KE01L	MuRata
C2, C3, C6, C7	4	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	GCM31MR71H105KA55L	MuRata
C9, C12, C21, C24, C29, C32, C41, C44, C53, C56	10	0.1uF	CAP, CERM, 0.1uF, 100V, +/- 10%, X7R, 0603	603	GRM188R72A104KA35D	MuRata
C10, C11, C22, C23, C30, C31, C42, C43, C54, C55	10	0.01uF	CAP, CERM, 0.01uF, 100V, +/- 10%, X7R, 0603	603	C0603X103K1RACTU	Kemet
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10	10		Receptacle, 2.54mm, 8x1, Tin, TH	Receptacle, 2.54mm, 8x1, TH	PPTC081LFBN-RC	Sullins Connector Solutions
J1	1		Standard Banana Jack, insulated, 10A, red	571-0500	571-0500	DEM Manufacturing
J2	1		Standard Banana Jack, insulated, 10A, black	571-0100	571-0100	DEM Manufacturing
J3	1		Standard Banana Jack, insulated, 10A, white	571-0600	571-0600	DEM Manufacturing
J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88	85		PC Test Point Plating Surface Mount Mounting Type	SMT_TP	RCWCTE	KOA Speer

**Table 3-1. AMP-PDK-EVM (continued)**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1, MP2, MP3, MP4, MP5	5			SPACER_0IN25	1537-B-6-AL	RAF Electronic
R1, R2, R4, R5, R9, R10, R12, R13	8	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic
R3, R6, R11, R14, R17, R18, R21, R22, R27, R30, R35, R38, R41, R42, R49, R50	16	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic
R25, R28, R33, R36, R45, R47, R53, R55	8	100	RES, 100, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEYJ101V	Panasonic
R26, R29, R34, R37	4	100k	RES, 100 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1003V	Panasonic
R46, R48, R54, R56	4	10.0k	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1002V	Panasonic
C13, C14, C15, C16, C17, C18, C19, C20, C25, C26, C27, C28, C33, C34, C35, C36, C37, C38, C39, C40, C45, C46, C47, C48, C49, C50, C51, C52	0	100pF	CAP, CERM, 100pF, 50V,+/- 5%, C0G/NP0, 0805	805	8.85012E+11	Würth Elektronik
R7, R8, R15, R16, R19, R20, R23, R24, R31, R32, R39, R40, R43, R44, R51, R52	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic
R57, R58, R59, R60	0	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0FKEA	Vishay-Dale

**Table 3-2. AMP-PDK-SOIC-14**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS197	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
U1	1		Socket, SOIC-14 Kelvin, 1.27mm Pitch	Socket, SOIC-14, 1.27mm Pitch	04337 161 6218F	Loranger



**Table 3-3. AMP-PDK-VSSOP-8**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS201	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1μF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
XU1	1		Socket, MSOP-8, 25.6mil Pitch	Socket, MSOP-8, 25.6mil Pitch	04335 081 6218B	Loranger

**Table 3-4. AMP-PDK-SC70-6**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS196	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
J3	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
U1	1		Socket, Kelvin, 2x6 Lead SOIC, TH	510x740x1050 mil Socket	04335 121 X215	Loranger

**Table 3-5. AMP-PDK-SOIC-8**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS198	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
U1	1		Socket, SOIC-8 Kelvin, 1.27mm Pitch	Socket, SOIC-8 Kelvin, 1.27mm Pitch	04337 081 6218A	Loranger

**Table 3-6. AMP-PDK-SOT23-6**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS199	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1μF, 25V,+/- 10%, X7R, 0603	603	GRM188R71E104KA01D	MuRata
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
J3	1		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
XU1	1		Socket, 2xSOT-23-6, 0.95mm Pitch	Socket, 2xSOT-23-6, 0.95mm Pitch	04331 121 6217	Loranger

**Table 3-7. AMP-PDK-TSSOP-14**

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		AMPS200	Any
C1, C2	2	0.1uF	CAP, CERM, 0.1uF, 25V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet
J1, J2	2		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions
XU1	1		Socket, TSSOP-14 Kelvin, 0.65mm Pitch	Socket, SOP-14 Kelvin, 0.65mm Pitch	04335 161 6218B	Loranger

## 4 Additional Information

### 4.1 Trademarks

All trademarks are the property of their respective owners.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (April 2024) to Revision A (July 2024)</b>	<b>Page</b>
• Added AMP-PDK-SC70-6, AMP-PDK-SOIC-8, AMP-PDK-SOT23-6, and AMP-PDK-TSSOP-14 throughout document .....	<b>1</b>

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
  - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductor products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
  - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
  - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
  - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
  - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

### **WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

**NOTE:**

**EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.**

### 3 Regulatory Notices:

#### 3.1 United States

##### 3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

##### 3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### **FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

#### 3.2 Canada

##### 3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

#### **Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

#### **Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

#### **Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

### Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

#### 3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_01.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page) 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号  
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see [http://www.tij.co.jp/lstds/ti\\_ja/general/eStore/notice\\_02.page](http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page)

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#### 3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
    - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
    - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
    - 4.3 *Safety-Related Warnings and Restrictions:*
      - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
      - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
    - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
  5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
  6. *Disclaimers:*
    - 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
    - 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
  7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.
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8. *Limitations on Damages and Liability:*

8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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