Application Report
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# VCXO Application Guideline for CDCE(L)9xx Family

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**ABSTRACT**

This application report focuses on the VCXO application, explaining the characteristics that the crystal unit must have in order to meet the device specifications, giving advice on package and assembly to reduce the impact of unwanted effects, and concluding with a list of recommended crystals.

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## 1 Introduction

The CDCE(L)9xx programmable clock generator offers the possibility for the input to be driven either by an LVCMOS clock signal or by a crystal unit.

Because the device has an on-chip integrated VCXO, the output frequency produced can be tuned by means of an analog input voltage, allowing the synchronization of the output signal with the input (i.e., a PWM signal).

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# 2 CDCE(L)9xx VCXO On-Chip Implementation

## 2.1 Architecture Overview

The external crystal unit is attached to the device in order to build a parallel resonant oscillator as depicted in Figure 1.

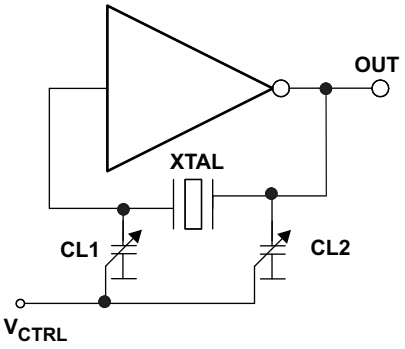



**Figure 1. CDCE(L)9xx VCXO Architecture**

This kind of architecture provides a feedback path through the crystal unit and the load capacitors. Changing the analog control voltage that acts on these capacitors (also called varactors) allows the adjustment of the output frequency. The latter is thus defined by the programmable CL1, CL2 (that are on-chip integrated), and by the crystal unit.

## 2.2 Quartz Crystal: General Theory and Basics Equations

The electrical properties of the crystal unit can be represented by the equivalent circuit depicted in Figure 2.

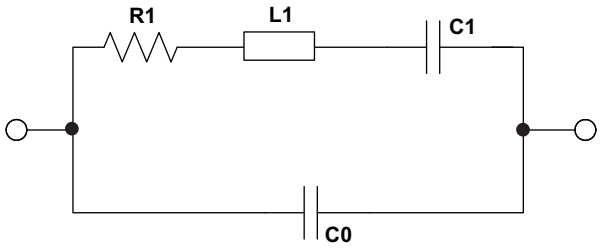
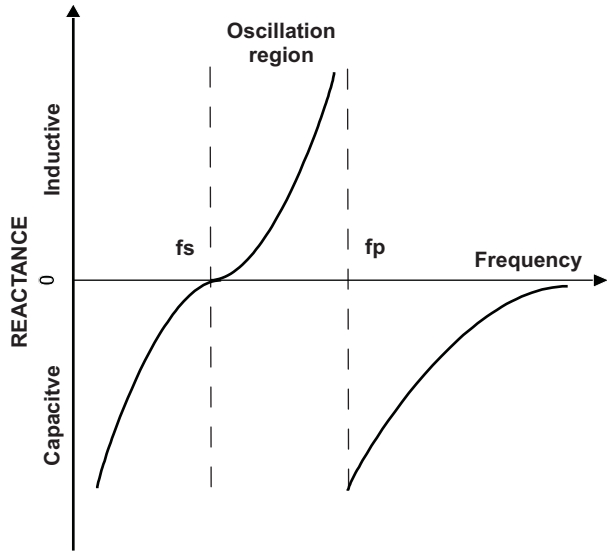



**Figure 2. Crystal Equivalent Circuit**

R1 is the equivalent series resistor (resistive losses), L1 is the motional inductance (oscillating mass), C1 is the motional capacity (elasticity of the oscillating body), and C0 is the shunt capacity (static parallel capacitor). C1 depends on the electrode area and can be changed by changing the cut of the crystal, whereas C0 is the capacity between the vacuum-deposited metal electrodes and the quartz material as a dielectric. By neglecting the resistive losses, the impedance of a quartz crystal can be considered as a pure reactance whose expression is given as the relationship between the voltage difference applied at its terminals and the current flowing, and whose behavior over the frequency range can be seen in Figure 3.




$$fs = \frac{1}{2\pi\sqrt{L_1 \cdot C_1}} \qquad fp = \frac{1}{2\pi\sqrt{L_1 \cdot \frac{C_1 C_0}{C_1 + C_0}}}$$

**Figure 3. Crystal Impedance Characteristic**

The reactance phase is 0 at two frequencies; the first is the series resonant frequency (fs) and the second is the parallel resonant frequency (fp). The frequency region between fs and fp is the oscillation region and the wider this region is, the more pullable the crystal is. The pullability coefficient for any crystal is calculated from the relationship between the shunt capacity and the motional capacity p = C0/C1.

Mathematically fs and fp are linked as follows:

$$fp = fs \times \sqrt{1 + \frac{C_1}{C_0}} \rightarrow fs \times \sqrt{1 + \frac{1}{p}} \tag{1}$$

It is clear that the smaller the pulling coefficient p is, the larger the distance of fp from fs is. Considering the circuit in Figure 1, the effect of the capacitive load is the shifting of the operative frequency of a certain offset over the fs. The operative frequency fl (load) is calculated as follows:

$$fl = fs + fs \times \frac{C_1}{2 \times (C_0 + C_L)} \tag{2}$$

The offset due to the load capacity can also be written as follows:

$$\frac{fl - fs}{fs} = \frac{C_1}{2 \times (C_0 + C_L)} \tag{3}$$

The variation of the offset with the load capacity is another important parameter for a crystal called sensitivity, defined as:

$$S = \frac{\delta_{offset}}{\delta_{C_L}} = \frac{C_1}{2 \times (C_0 + C_L)^2} \tag{4}$$

# 3 CDCE(L)9xx Crystal Specifications

## 3.1 Requirements

So far, some important parameters and mathematical equations of a quartz crystal have been discussed in general. How do these relate to the CDCE(L)9xx requirements? Looking at the 27-MHz video applications for which the device can be used for synchronization purposes, the most important specification of the VCXO is the pulling range. This is the frequency range in which the operative frequency can be swept by sweeping the control voltage. Typical values have an order of magnitude of some ppm (part per million) of the center frequency. The CDCE(L)9xx specifies a typical value of 120 ppm over a voltage that ranges from 0 V to 1.8 V (see Figure 4).

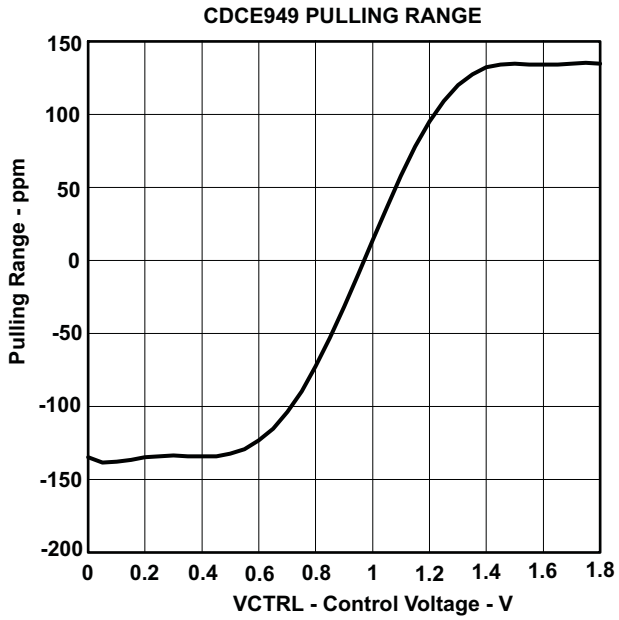



**Figure 4. Pullability Characteristic Versus Control Voltage**

For the crystals (used for the VCXO application) to fulfill this requirement the ratio p = C0/C1 should be close to 220 (or even smaller). Having C1 > 20fF also ensures better performance (pullability > 120 ppm).

The ESR should be as small as possible to ensure the start-up, and the C0 must be smaller than 6 pF. A larger value could have an impact on the start-up capability of the VCXO.

## 3.2 Load Capacitance

The load capacitance is, per definition, the value of capacitance measured, or calculated, across the connection points of the crystal. That is, it takes into account not only CL1 and CL2 but also the stray capacitance Cs (capacity of the crystal socket plus any other parasitic from both PCB and chip across the crystal).

$$C_L = CL_{On-Chip} + Cs \rightarrow CL_{On-Chip} = \frac{CL_1 \times CL_2}{CL_1 + CL_2} \quad (5)$$

$CL_{On-Chip}$ is the on-chip programmable capacitance, also called varactor. The CDCE(L)9xx offers the opportunity to program it from 0 pF up to 20 pF with 1-pF steps, by changing the bit [7:3] of the register 05h (see data sheet SCAS844). The default value is 10 pF.

By knowing the total load capacitance CL from the crystal specification and Cs from the data sheet, it is possible to calculate the value of $CL_{On-Chip}$ by subtraction and program it selecting the appropriate bit configuration.

Once $CL_{On-Chip}$ has been set to the desired value, the variation of the control voltage in the range between 0 V and 1.8 V allows a corresponding sweep of the varactor's value from 1.3 × $CL_{On-Chip}$ (30% higher than starting value) up to 0.3 × $CL_{On-Chip}$ (70% lower than starting value). For further clarification, see the curve appearing in Figure 5.

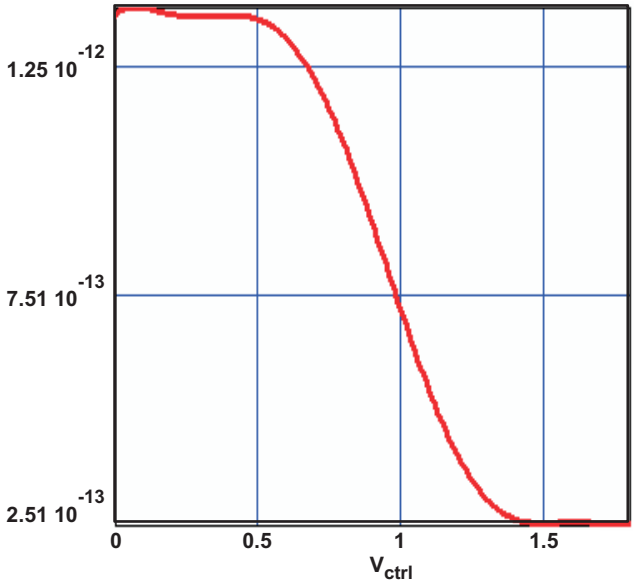



**Figure 5. Varicap Characteristic Versus Control Voltage**

Whether the pulling range requirement is met depends on the sensitivity that the chosen crystal has for that load $CL_{On-Chip}$. The control voltage has an effect on the $CL_{On-Chip}$ only and not on the parasitic, making it clear why is important to reduce them. A high parasitic causes a reduction of pulling range.

Figure 6 shows an example of frequency variation versus load capacitance, also called load capacitance characteristic, for a given crystal that has a trim sensitivity of 25 ppm/pF for a load capacitance of 12 pF.

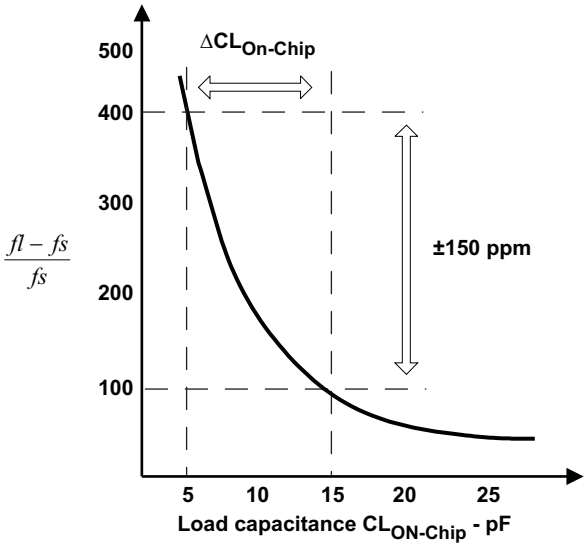



**Figure 6. Load Capacitance Characteristic**

In the upper example of Figure 6, a variation of the control voltage is translated in a variation of the varactor value from its center target value (12 pF) to the corners (3.6 pF and 15.6 pF), for a total delta of 12 pF. Such a change has the effect to make the output frequency drift, giving a final pulling range of (12 pF × 25 ppm/pF) approximately 300 ppm (±150 ppm).

### 3.3 Absolute Pulling Range

The VCXO can also be considered a resonator that locks to its reference (the kick-off) that is the quartz crystal. The VCXO-crystal system is affected from inaccuracy due to temperature stability, aging, circuit variation, and so on. The absolute pulling range is what is left from the nominal pulling range after subtracting all the error contributions. This parameter is an indication of how good the VCXO can follow the crystal and lock to its fundamental mode.

Referring once again to the previous example (±150 ppm) and considering the following error contributions:

| | |
|---|---|
| Frequency tolerance | 20 ppm |
| Temperature stability | 30 ppm |
| Aging | 15 ppm |
| Circuit variation | 15 ppm |

the absolute pulling range is ±70 ppm.

### 3.4 Crystal Specification for Non-VCXO Application

When the VCXO is not employed and the device is driven from a crystal, its requirements are much more relaxed, as a pulling range is unnecessary.

The quartz crystal fundamental frequency ranges from a minimum of 8 MHz up to a maximum of 32 MHz. The requirements for the electrical specification of these crystals concern the equivalent series resistors (ESR) and the shunt capacity (C0).

The first must be smaller than 100 Ω, whereas the latter must be smaller than 6 pF to ensure start-up conditions.

## 4 Layout Considerations

As previously mentioned, any parasitic across the crystal reduces the pullability of the VCXO. Therefore, care must be taken in placing the crystal units on the board. Always place it as close to the device as possible, ensuring that the routing lines from the crystal terminals to XIN and XOUT have the same length. If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of a certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because this can range from 0 pF to 20 pF with steps of 1 pF.

The 0.7-pF capacitor therefore can be discretely added. In order to minimize the inductive influence of the trace, it is recommended to place this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

## 5 Recommended Crystals

Table 1 provides a list of crystals that meet the device requirements.

**Table 1. List of Recommended Crystals for VCXO Application**

| Crystal Manufacturer | Part Number |
|---|---|
| KDS | SMD-49 |
| KDS | DSX530GA |
| KVG | XA 3648 |
| NewXtal | C18P06002 SMD 5032 |
| Pletronics | SMT13T065 |
| Quartzcom | UM-1 MJ |

The pullability of the VCXO for a given crystal can be simulated by inserting its electrical specifications (C0, C1, CL, and L1). TI Pro-Clock™ programming software (available on the TI Web site for the CDCE9xx) offers this feature. Figure 7 shows the comparison between the pullability curve calculated with the platform and measured in the laboratory.

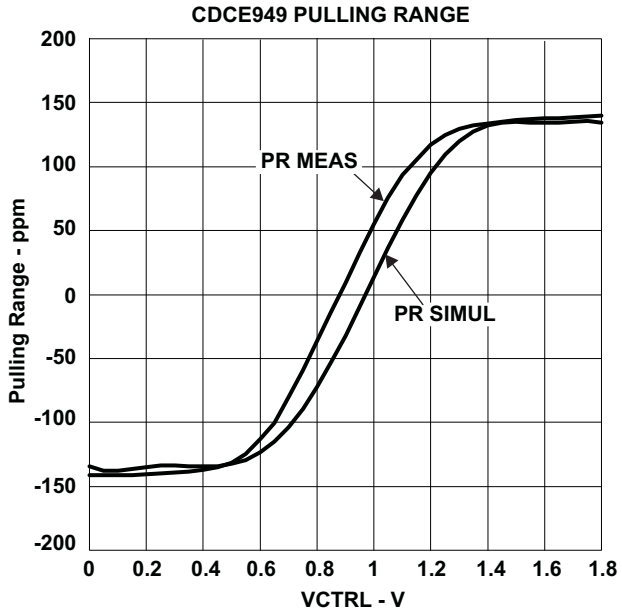



**Figure 7. Pulling Range Curves Comparison**

## 6 References

- Schwingquarze: ein unverzichtbares Bauelement in der Elektronik (Vistas Verlag, Berlin)
- *High-Speed Layout Guidelines* application report (SCAA082)

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