GTL/GTLP Logic
High-Performance Backplane Drivers
Data Book

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INTRODUCTION

Texas Instruments provides an array of advanced bus-interface devices. Designers can select the best solutions for speed, level translation, power consumption, noise rejection, fault tolerance, or simply driving a high-speed local bus or backplane.

Gunning Transceiver Logic (GTL) devices are reduced-voltage-swing, high-speed interface devices between cards operating at LVTTL logic levels and backplanes operating at GTL signal levels. High-speed backplane operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control. TI offers LVTTL-to-GTL translators in SSOP and TSSOP Widebus™ packages to interface with TTL/LVTTL-based subsystems in wireless, remote access, mass storage and legacy telecom/networking applications.

Gunning Transceiver Logic Plus (GTLP) devices are reduced-voltage-swing devices that are designed for high-speed interface between cards operating at LVTTL logic levels and backplanes operating at GTLP signal levels. High-speed backplane operation in excess of 80 MHz is a direct result of the reduced output swing (<1 V), reduced input threshold levels, output edge control, and overshoot-protection circuitry. All devices are optimized for the higher threshold voltage and lower noise margin GTLP derivative of the JEDEC JESD8-3 GTL standard. TI offers LVTTL-to-GTLP translators in low-profile, fine-pitch ball grid array (LFBGA), Widebus, and octal packages to interface with TTL/LVTTL-based subsystems in wireless, remote access, mass storage and legacy telecom/networking applications.

BTL/FB+ transceivers from TI provide high drive and speed, while minimizing skew and ground-bounce noise. BTL devices are compatible with IEEE Std 1194.1-1991. The BTL/FB+ standard uses a greatly reduced output swing and a tighter switching region, improved noise margins, live insertion, bus hold on inputs, series damping resistors on high-drive outputs, and space-saving package options.

ABTE has wider noise margins and is backward compatible with existing TTL logic. ABTE devices support the VME64-ETL specification, with tight tolerances on skew and transition times. ABTE is manufactured using the latest 0.8-μ BiCMOS process by providing high drive up to 90 mA. Other features include a bias pin and internal pullup resistors on control pins for maximum live-insertion protection. Bus-hold circuitry eliminates external pullup resistors on the inputs and series damping resistors on the outputs to damp reflections.

VME complies with VME64 Standard and has 2.94-V regulated output voltage with 1% tolerance at 25°C. VME provides bias for up to 32 lines of active termination for VME buses, –575-mA sourcing current for termination, +475-mA sinking current for active negation drivers, current limit and thermal shutdown protection, and low thermal resistance surface-mount packages.

For more information on these and other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5780, or visit the TI home page at http://www.ti.com

GTL FAMILY SUMMARY

Primary features of the GTL devices:

- 3.3-V or 3.3/5-V V_{CC} operation with 5-V tolerant LVTTL inputs and outputs (I/Os) (except GTL1655), which allows the devices to act as 5-V TTL-to-GTL/GTL+, as well as 3.3-V LVTTL-to-GTL/GTL+, translators.
- GTL1655 supports live insertion with backplane precharge circuitry.
- High point-to-point frequencies with acceptable short-backplane frequencies. The GTL16612 transition device provides for higher distributed load (RLC) frequencies (>60 MHz), due to its optimized edge rate.

DEVICE	FUNCTION	GTL+ DRIVE (mA)	FREQUENCY	
			MAX p-p (MHz)	MAX RLC (MHz)
Medium-Drive Devices				
SN74GTL16612A	18-bit universal bus transceiver	34	85	>60
SN74GTL16616	17-bit universal bus transceiver with buffered clock	50	95	25–33
SN74GTL16622A	18-bit bus transceiver	50	200	25–33
SN74GTL16923	18-bit bus transceiver	50	200	25–33
High-Drive Devices				
SN74GTL1655	16-bit universal bus transceiver	100	160	25–33

Additional features of GTL devices:

- I_{off} circuitry prevents damage to the device during partial power down, a feature of all GTL devices (see I_{off} in the data sheets).
- Power-up 3-state (PU3S) forces outputs to the high-impedance state during power up and power down, which prevents driver conflict during hot swap or hot insertion, a feature of the GTL1655 (see I_{OZPU} and I_{OZPD} in the data sheets).
- BIAS V_{CC} circuitry allows easy internal precharging of backplane I/O pins for true live-insertion applications where active backplane data cannot be suspended or disturbed during circuit-board insertion or removal, a feature of the GTL1655 (see BIAS V_{CC} in the data sheets).
- Bus hold is a feature of all GTL devices. It eliminates floating inputs by holding them at the last valid logic state. This eliminates the need for external pullup and pulldown resistors on unused or undriven inputs, reducing power requirements, cost, and board-layout time. There is no bus-hold circuitry on the B port (GTL/GTL+ side) because this defeats the purpose of open-drain outputs that take on the high-impedance state, which allows the bus to achieve a logic-high state via the pullup resistors.
- OEC™ circuitry controls the rising and falling edges of the GTL16612 GTL/GTL+ outputs, and reduces line reflections and EMI, thereby improving overall signal integrity.
- Edge-rate control (ERC) is featured on the high-drive GTL1655. Fast or slow edge rates are achievable by holding the ERC pin at V_{CC} or GND, respectively.
- GTL devices are available in the shrink small-outline package (SSOP) (56-pin GTL16612 and GTL16616 only) and thin shrink small-outline package (TSSOP) (56 pins or 64 pins).

GTLP FAMILY SUMMARY

Primary features of the GTLP devices:

- 3.3-V V_{CC} operation with 5-V tolerant LVTTL I/Os, which allows the devices to act as 5-V TTL-to-GTL/GTL+, as well as 3.3-V LVTTL-to-GTL/GTL+, translators.
- Optimized OEC circuitry allows clock frequencies of >80 MHz in high-performance, heavily loaded backplane applications.
- Fully supports live insertion with backplane precharge circuitry
- CMOS construction for low-static power consumption
- A-port (LVTTL side) balanced drive of ±24 mA
- B-port (GTL/GTL+ side) drive of 50 mA or 100 mA, which allows the designer flexibility in matching the device to backplane length, slot spacing, and termination resistance
- Each data sheet provides both the lumped-load specified data and resistive/inductive/capacitive (RLC) network data for the designer. The RLC data more closely approximates the device response in a distributed load.
- The SN74GTLP1394 is designed specifically to work with the TSB14AA1 (1394 backplane physical-layer controller) in multiple-slot backplane applications.

DEVICE	FUNCTION	GTL+ DRIVE (mA)	FREQUENCY	
			MAX p-p (MHz)	MAX RLC (MHz)
Medium-Drive Devices				
SN74GTLP817	GTL+-to-LVTTL 1-to-6 fanout driver	50	Not specified	>80
SN74GTLPH306	8-bit bus transceiver	50	Not specified	>80
SN74GTLPH16945	16-bit bus transceiver	50	Not specified	>80
SN74GTLPH16912	18-bit universal bus transceiver	50	TBD	>80
SN74GTLPH32945	32-bit bus transceiver	50	Not specified	>80
SN74GTLPH16916	17-bit universal bus transceiver	50	175	>80
SN74GTLPH16612	18-bit universal bus transceiver	50	80	>80
High-Drive Devices				
SN74GTLP1394	2-bit transceiver	100	Not specified	>80
SN74GTLPH1645	16-bit bus transceiver	100	Not specified	>80
SN74GTLPH1655	16-bit universal bus transceiver	100	175	>80
SN74GTLPH1612	18-bit universal bus transceiver	100	175	>80
SN74GTLPH3245	32-bit bus transceiver	100	Not specified	>80
SN74GTLP1395	Two 1-bit bus transceivers	100	Not specified	>80
SN74GTLP21395	Two 1-bit bus transceivers	100	Not specified	>80
SN74GTLPH1616	17-bit universal bus transceiver	100	175	>80
SN74GTLPH1627	18-bit bus transceiver	100	TBD	>80
SN74GTLP2033	8-bit registered transceiver	100	Not specified	>80
SN74GTLP22033	8-bit registered transceiver	100	Not specified	>80
SN74GTLP2034	8-bit registered transceiver	100	Not specified	>80
SN74GTLP22034	8-bit registered transceiver	100	Not specified	>80

GTLP FAMILY SUMMARY (CONTINUED)

Additional features of GTLP devices:

- I_{off} circuitry prevents damage to the device during partial power down, a feature of all GTLP devices (see I_{off} in the data sheets).
- PU3S forces outputs to the high-impedance state during power up and power down, which prevents driver conflict during hot swap or hot insertion, a feature of all GTLP devices (see I_{OZPU} and I_{OZPD} in the data sheets).
- BIAS V_{CC} circuitry allows easy internal precharging of backplane I/O pins for true live-insertion applications where active backplane data cannot be suspended or disturbed during circuit-board insertion or removal, a feature of all GTLP devices, except GTLPH306 and GTLP817 (see BIAS V_{CC} in the data sheets).
- Bus hold eliminates floating inputs by holding them at the last valid logic state. This eliminates the need for external pullup and pulldown resistors on unused or undriven inputs, reducing power requirements, cost, and board-layout time. Devices with an H in the device name have the bus-hold feature. There is no bus-hold circuitry on the B port (GTL/GTL+ side) because this defeats the purpose of open-drain outputs that take on the high-impedance state, which allows the bus to achieve a logic-high state via the pullup resistors.
- Improved OEC circuitry controls the rising and falling edges of the GTL/GTL+ outputs (a feature of all GTLP devices) and reduces line reflections and EMI, thereby, improving overall signal integrity.
- TI-OPC™ circuitry actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions, thus, improving signal integrity, which allows adequate noise margin to be maintained at higher frequencies.
- ERC is a feature of all high-drive GTLP devices and the medium-drive GTLP817. Fast or slow edge rates are achievable by holding the ERC pin at V_{CC} or GND, respectively.
  - The fast edge rate is useful in point-to-point applications and when the backplane has been optimally terminated.
  - The slow edge rate is used in less than optimally terminated backplane applications where the slow edge reduces overshoot and ringing.
- GTLP devices are available in small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), thin very small-outline package (TVSOP), low-profile, fine-pitch ball grid array (LFBGA), and very low-profile, fine-pitch ball grid array (VFBGA) packages to fit any design requirements.

PRODUCT STAGE STATEMENTS

Product stage statements are used on Texas Instruments data sheets to indicate the development stage(s) of the product(s) specified in the data sheets.

If all products specified in a data sheet are at the same development stage, the appropriate statement from the following list is placed in the lower left corner of the first page of the data sheet.

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>
> PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Contents

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i **Input capacitance**

The capacitance of an input terminal of the device

C_{io} **Input/output capacitance**

The capacitance of an input/output (I/O) terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

C_o **Output capacitance**

The capacitance of an output terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

C_{pd} **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{BHH} **Bus-hold high sustaining current**

The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

I_{BHL} **Bus-hold low sustaining current**

The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

I_{BHHO} **Bus-hold high overdrive current**

An external driver must sink at least I_{BHHO} to switch this node from high to low.

I_{BHLO} **Bus-hold low overdrive current**

An external driver must source at least I_{BHLO} to switch this node from low to high.

I_{CC} **Supply current**

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**

The maximum leakage current into* an output that is in a high state and $V_O = V_{CC}$

$I_{I(hold)}$ **Input hold current**

The input current that holds the input at the previous state when the driving device goes to the high-impedance state

*Current out of a terminal is given as a negative value.

I_{IH} **High-level input current**

The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**

The maximum leakage current into* an input or output terminal of the device with the specified voltage applied to the terminal and V_{CC} = 0 V

I_{OH} **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

I_{OHS} **Static high-level output current**

The static and testable current into* a DOC™ circuit output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive current is not specified for devices with DOC circuit outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

I_{OL} **Low-level output current**

The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output

I_{OLS} **Static low-level output current**

The static and testable current into* a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive current is not specified for devices with DOC circuit outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

I_{OZ} **Off-state (high-impedance state) output current (of a 3-state output)**

The current flowing into* an output with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

I_{OZPD} **Power-down off-state (high-impedance state) output current (of a 3-state output)**

The current flowing into* an output that is switched to or held in the high-impedance state as the device is being powered down to V_{CC} = 0 V

I_{OZPU} **Power-up off-state (high-impedance state) output current (of a 3-state output)**

The current flowing into* an output that is switched to or held in the high-impedance state as the device is being powered up from V_{CC} = 0 V

jitter **Jitter**

Dispersion of a time parameter of the pulse waveforms in a pulse train with respect to a reference time, interval, or duration. Unless otherwise specified by a mathematical adjective, peak-to-peak jitter is assumed.

jitter(RMS) **RMS jitter**

The root mean square jitter, one-sixth of the maximum peak-to-peak jitter

*Current out of a terminal is given as a negative value.
DOC is a trademark of Texas Instruments.

SR **Slew rate**

The average rate of change (i.e., V/ns) for a waveform that is changing from one defined logic level to another defined logic level

t_a **Access time**

The time interval between the application of a specified input pulse and the availability of valid signals at an output

t_c **Clock cycle time**

Clock cycle time is $1/f_{max}$

t_{dis} **Disable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to the high-impedance (off) state

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.

t_{en} **Enable time (of a 3-state or open-collector output)**

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from the high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{OE}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

t_f **Fall time**

The time interval between two reference points (90% and 10%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level

t_h **Hold time**

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

t_{pd} **Propagation delay time**

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_r **Rise time**

The time interval between two reference points (10% and 90%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level

$t_{sk(i)}$ **Input skew**

The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(i)}$ describes the ability of the gate to shape the pulse to the same duration, regardless of the input used as the controlling input.

$t_{sk(l)}$ **Limit skew**

The difference between 1) the greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device. It is calculated from the data-sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time is induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(l)}$ also accounts for process variation. In fact, all other skew specifications [$t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$] are subsets of $t_{sk(l)}$; they are never greater than $t_{sk(l)}$.

$t_{sk(o)}$ **Output skew**

The skew between specified outputs of a single logic device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

$t_{sk(p)}$ **Pulse skew**

The magnitude of the time difference between the propagation delay times, t_{PHL} and t_{PLH}, when a single switching input causes one or more outputs to switch

$t_{sk(pr)}$ **Process skew**

The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, and have identical package styles, identical specified loads, identical internal logic functions, and the same manufacturer

t_{su} **Setup time**

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is specified.

t_w **Pulse duration (width)**

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} **High-level input voltage**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} **Low-level input voltage**

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} **High-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

V_{OHS} **Static high-level output voltage**

The static and testable voltage at a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive voltage is not specified for devices with DOC circuit outputs because of its transient nature.

V_{OL} **Low-level output voltage**

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

V_{OLS} **Static low-level output voltage**

The static and testable voltage at a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive voltage is not specified for devices with DOC circuit outputs because of its transient nature.

V_{T+} **Positive-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}

V_{T-} **Negative-going input threshold level**

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

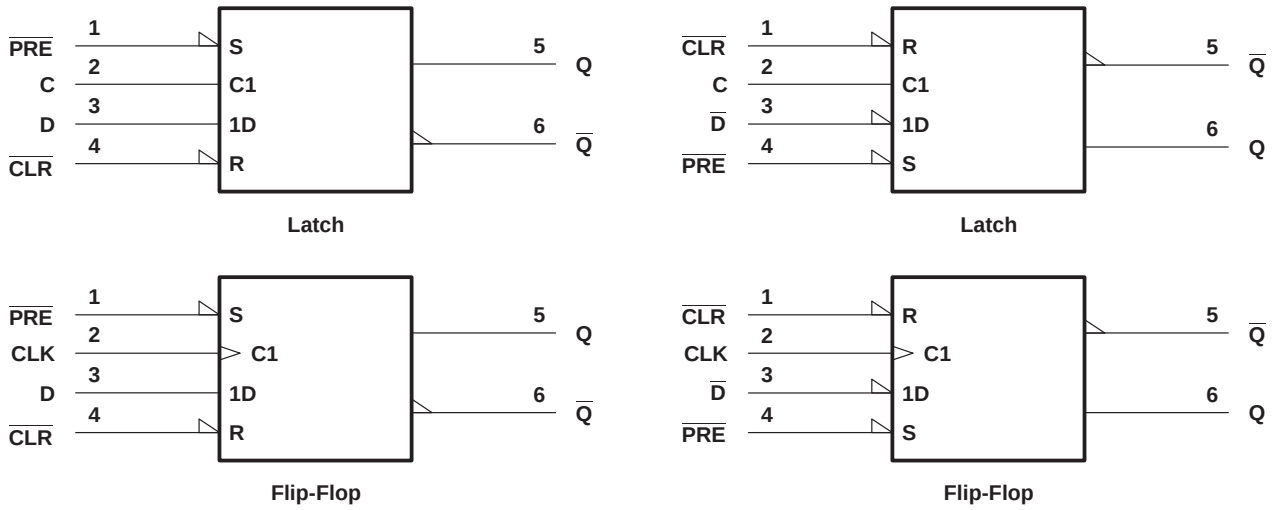
The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function table functional tests do not reflect all possible combinations or sequential modes.

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (◺) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

Example:

SN	74	GTLP	H	16		612		DGG	R
1	2	3	4	5	6	7	8	9	10

1 Standard Prefix

Examples: SN – Standard Prefix
SNJ – Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 – Military
74 – Commercial

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE/ETL – Advanced BiCMOS Technology/ Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALB – Advanced Low-Voltage BiCMOS
ALS – Advanced Low-Power Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
AS – Advanced Schottky Logic
AVC – Advanced Very Low-Voltage CMOS Logic
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CBTLV – Low-Voltage Crossbar Technology
CD4000 – CMOS B-Series Integrated Circuits
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
FCT – Fast CMOS TTL Logic
GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transceiver Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage CMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
PCA/PCF – I^2C Inter-Integrated Circuit Applications
S – Schottky Logic
SSTL/SSTV – Stub Series-Terminated Logic
TVC – Translation Voltage Clamp Logic

4 Special Features

Examples: Blank = No Special Features
C – Configurable V_{CC} (LVCC)
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
K – Undershoot-Protection Circuitry (CBTK)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)
Z – Power-Up 3-State (LVCZ)

5 Bit Width

Examples: Blank = Gates, MSI, and Octals
1G – Single Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank = No Options
2 – Series Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

7 Function

Examples: 244 – Noninverting Buffer/Driver
374 – D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Transceiver

8 Device Revision

Examples: Blank = No Revision
Letter Designator A–Z

9 Packages

Commercial: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBQ – Quarter-Size Outline Package (QSOP)
DBV, DCK, DCT, DCU – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FN – Plastic Leaded Chip Carrier (PLCC)
GKE, GKF – MicroSTAR BGA™ Low-Profile Fine-Pitch Ball Grid Array (LFBGA)
GQL – MicroStar Jr.™ Very-Thin-Profile Fine-Pitch Ball Grid Array (VFBGA)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
NS, PS – Small-Outline Package (SOP)
PAG, PAH, PCA, PCB, PM, PN, PZ – Thin Quad Flatpack (TQFP)
PH, PQ, RC – Quad Flatpack (QFP)
YEA – NanoStar™ Die-Size Ball Grid Array (DSBGA)†

Military: FK – Leadless Ceramic Chip Carrier (LCCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flatpack (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
W, WA, WD – Ceramic Flatpack (CFP)

10 Tape and Reel

Devices in the DB and PW package types include the R designation for reeled product. Existing product inventory designated LE may remain, but all products are being converted to the R designation.

Examples: Old Nomenclature – SN74LVTxxxDBLE
New Nomenclature – SN74LVTxxxADBR

LE – Left Embossed (valid for DB and PW packages only)
R – Standard (valid for all surface-mount packages)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).

In digital-system design, consideration must be given to thermal management of components. The small size of the small-outline packages makes this even more critical. Figures 1–5 show the high-effect (High-K) thermal resistance for the small-outline 14-, 16-, 20-, 24-, and 48-pin packages for various rates of airflow calculated in accordance with JESD 51-7.

The thermal resistances in Figures 1–5 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

T_J = virtual junction temperature (°C)
$R_{\theta JA}$ = thermal resistance, junction to free air (°C/W)
P_T = total power dissipation of the device (W)
T_A = free-air temperature (°C)

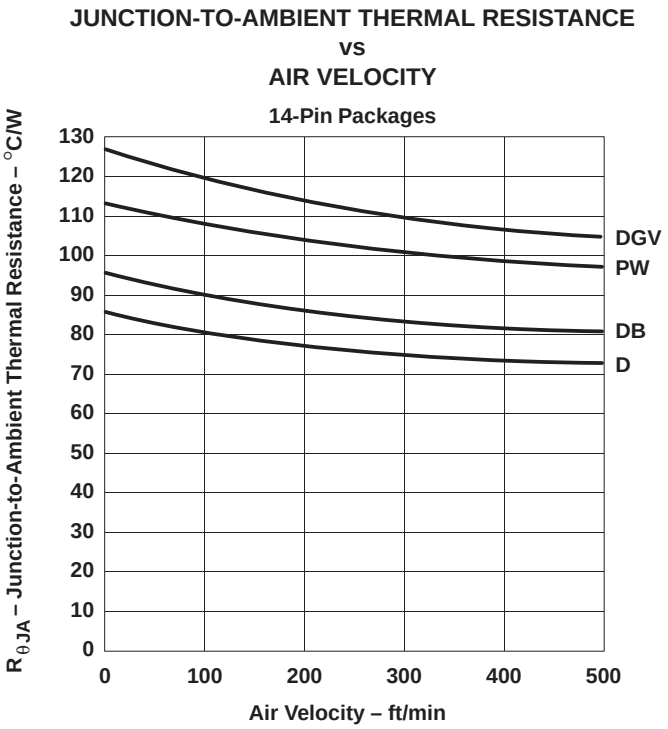


Figure 1

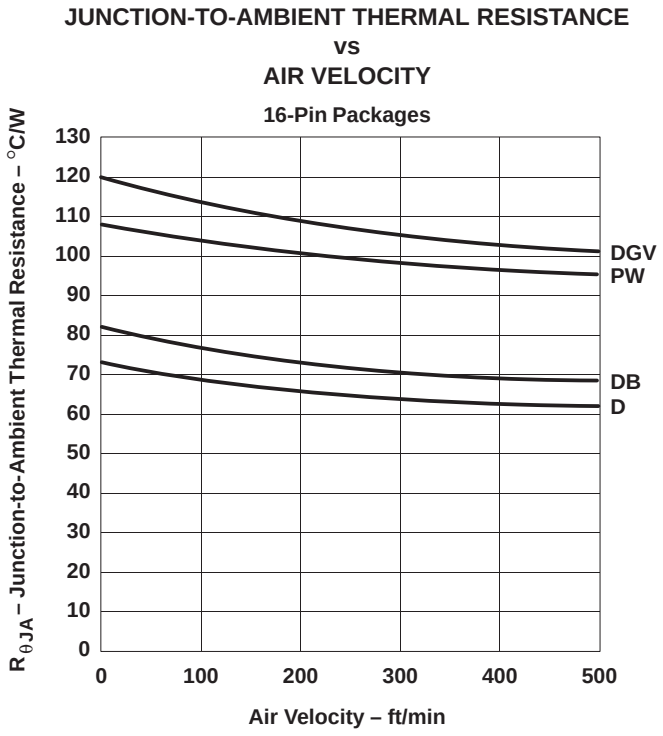


Figure 2

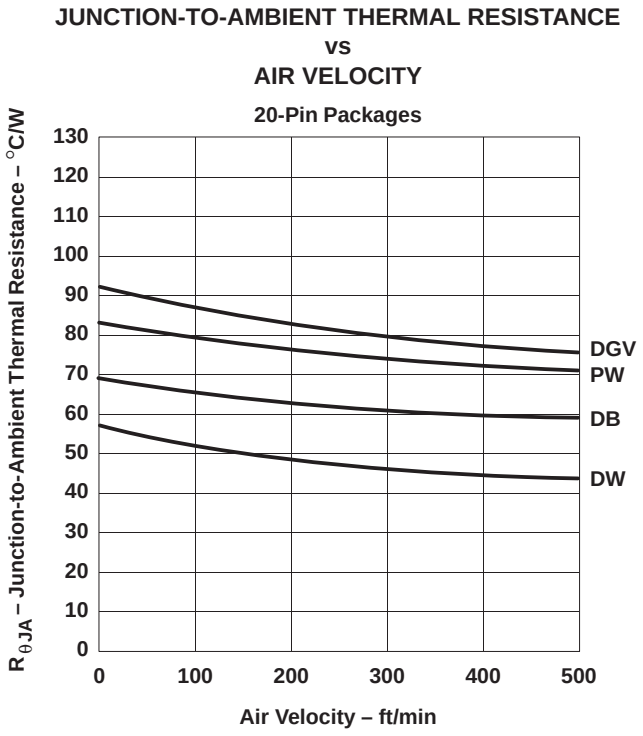


Figure 3

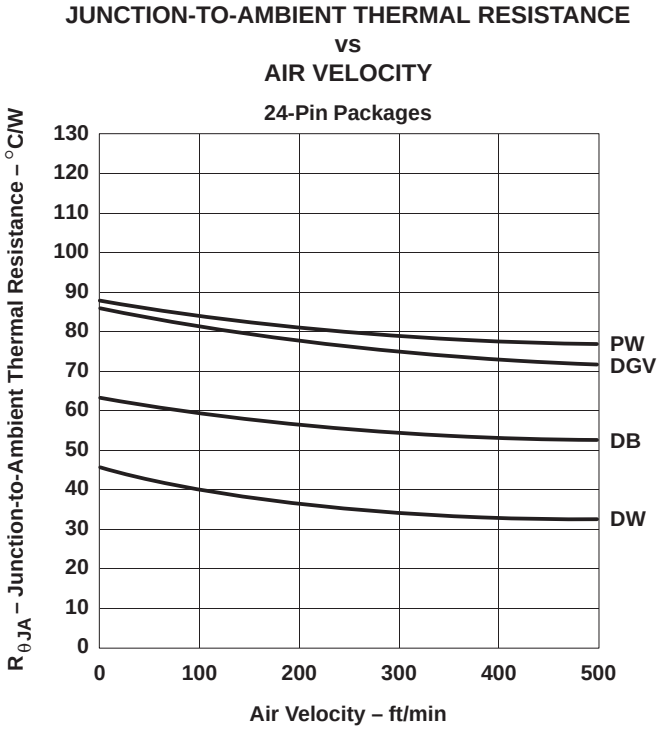


Figure 4

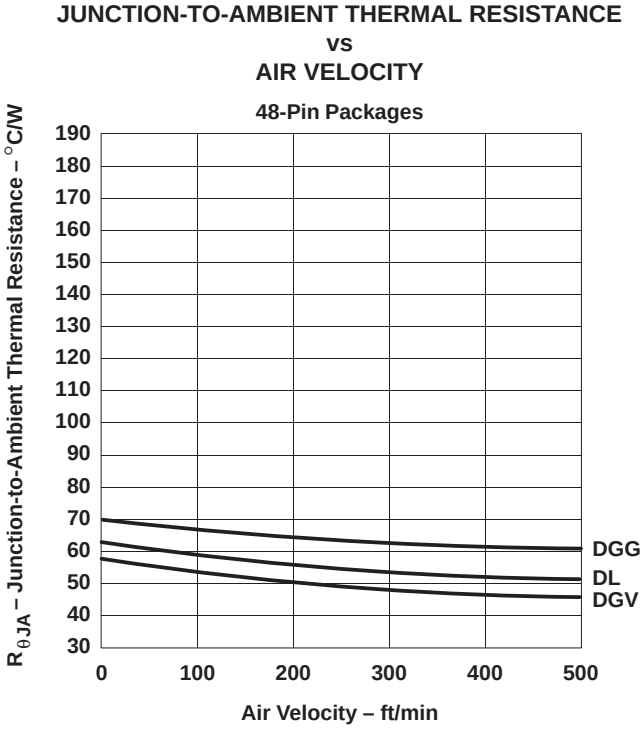
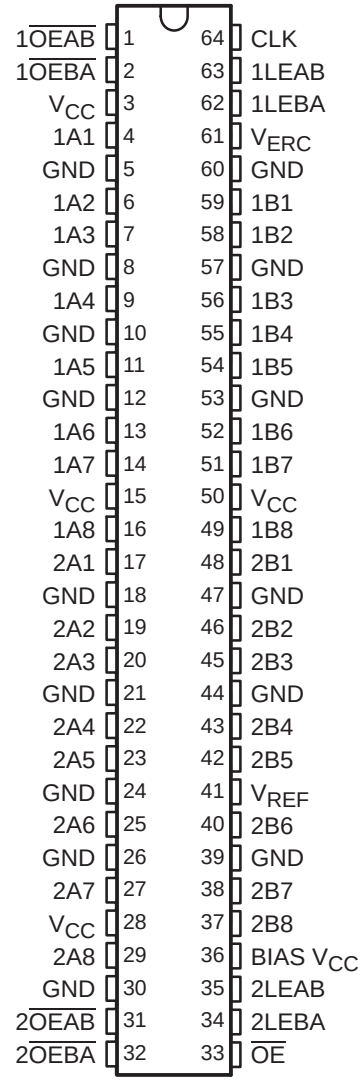


Figure 5

Contents

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Translates Between GTL/GTL+ Signal Level and LVTTL Logic Levels**
- **High-Drive (100 mA), Low-Output-Impedance (12 Ω) Bus Transceiver (B Port)**
- **Edge-Rate-Control Input Configures the B-Port Output Rise and Fall Times**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTL1655 is a high-drive (100 mA), low-output-impedance (12 Ω) 16-bit UBT™ transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two 8-bit transceivers and combines D-type flip-flops and D-type latches to allow for transparent, latched, and clocked modes of data transfer similar to the '16501 function. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

OEC, UBT, and Widebus are trademarks of Texas Instruments.

description (continued)

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels but are not 5-V tolerant. V_{REF} is the reference input voltage for the B port.

This device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output signals, but with a common clock and output enable inputs for both transceiver words.

Data flow for each word is determined by the respective latch enables (LEAB and LEBA), output enables ($\overline{OEAB}$ and $\overline{OEBA}$), and clock (CLK). The output enables ($1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, and $2\overline{OEBA}$) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When $\overline{OEAB}$ is low, the outputs are active. With $\overline{OEAB}$ high, the outputs are in the high-impedance state.

Data flow for the B-to-A direction is identical, but uses $\overline{OEBA}$, LEBA, and CLK. Note that CLK is common to both directions and both 8-bit words. $\overline{OE}$ is also common and is used to disable all I/O ports simultaneously.

The SN74GTL1655 has adjustable edge-rate control (V_{ERC}). Changing V_{ERC} input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize for various loading conditions.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL1655DGGR	GTL1655

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

FUNCTION†

INPUTS				OUTPUT B	MODE
$\overline{OEAB}$	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	H	X	L	L	Transparent
L	H	X	H	H	Transparent
L	L	↑	L	L	Registered
L	L	↑	H	H	Registered
L	L	H	X	B_0‡	Previous state
L	L	L	X	B_0§	Previous state

† A-to-B data flow is shown. B-to-A flow is similar, but uses $\overline{OEBA}$, LEBA, and CLK.
‡ Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

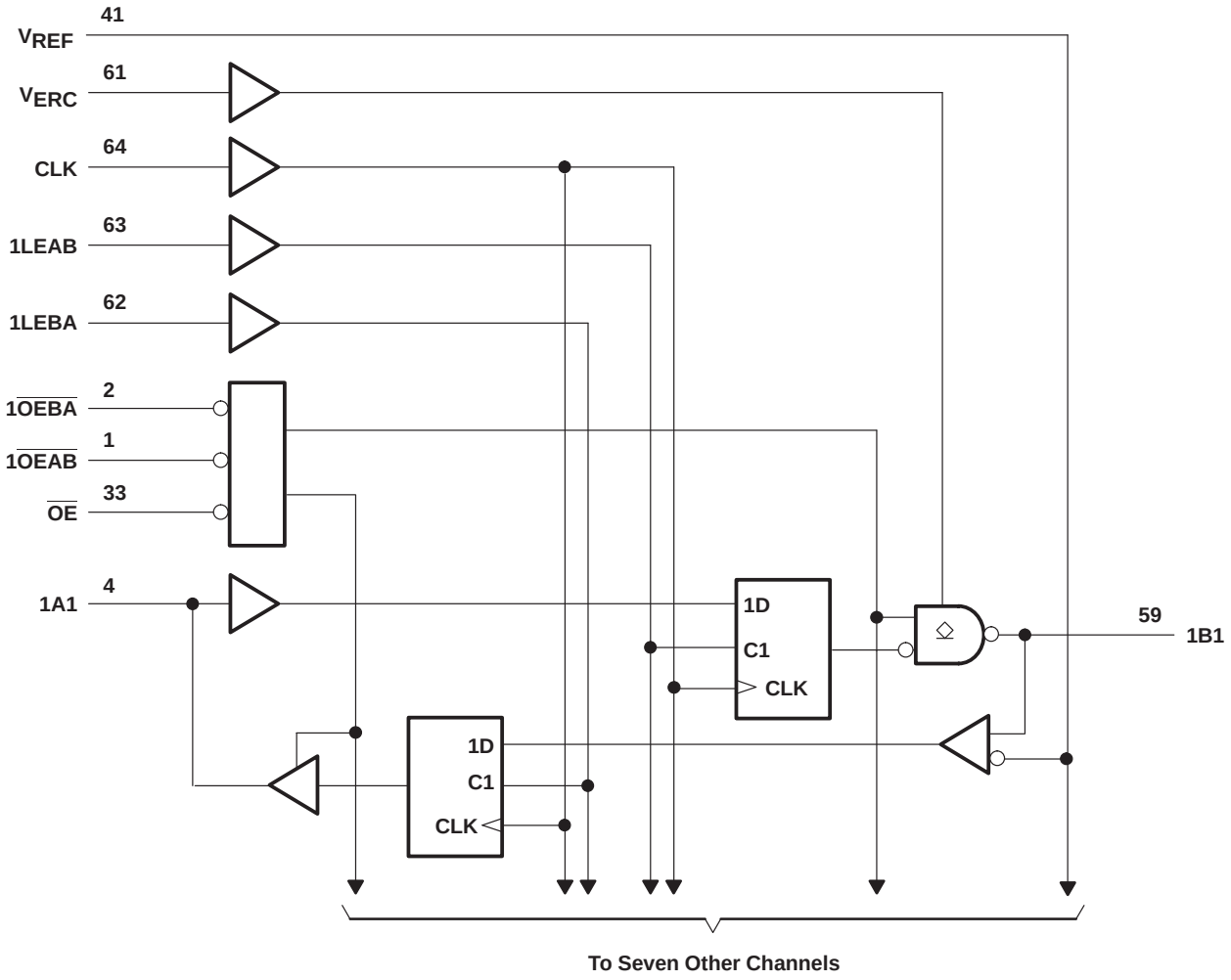
OUTPUT ENABLE

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{OEAB}$	$\overline{OEBA}$	A PORT	B PORT
L	L	L	Active	Active
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

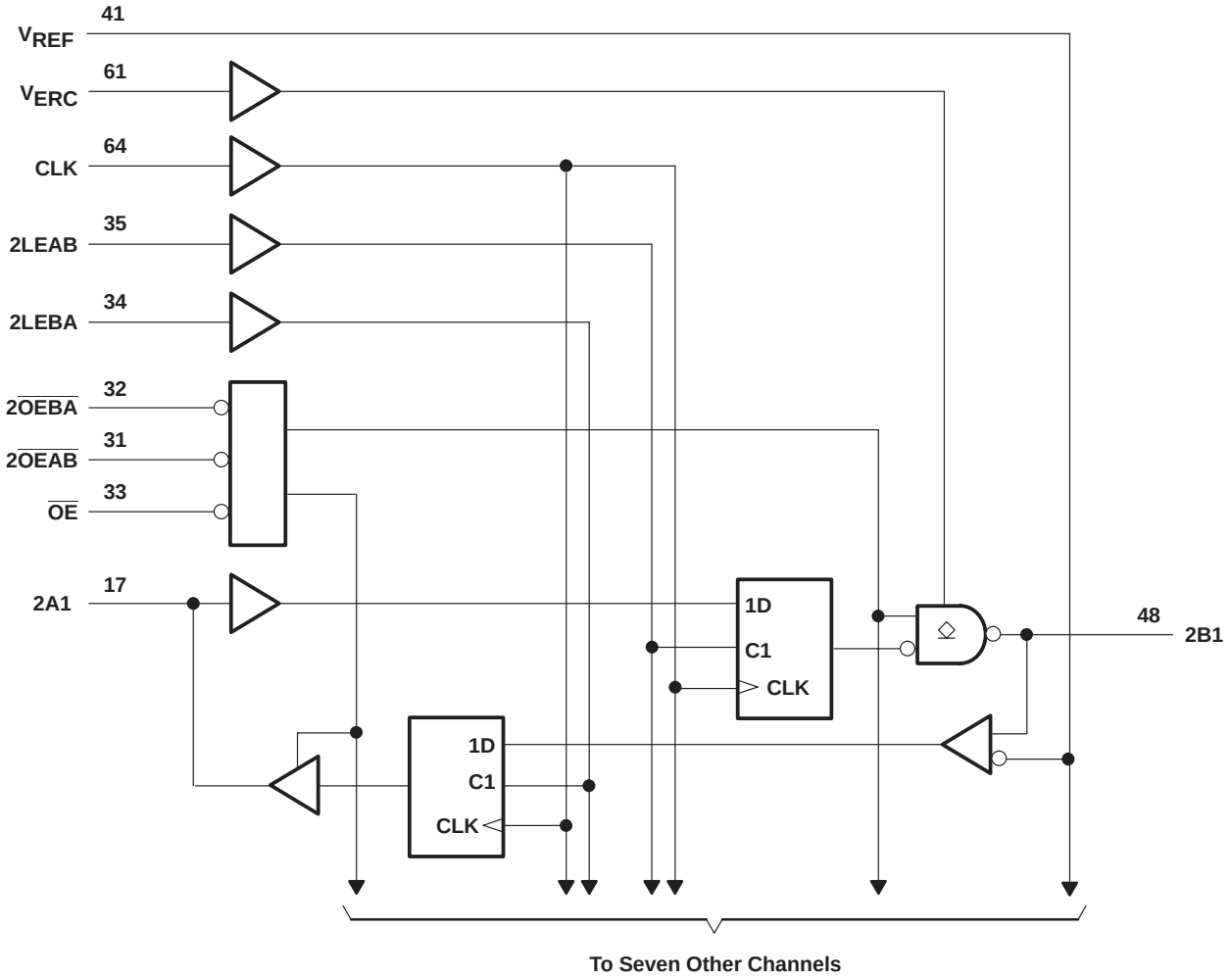
B-PORT EDGE-RATE CONTROL (V_{ERC})

INPUT V_{ERC}		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

logic diagram (positive logic)



logic diagram (positive logic) (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs . . . . . –0.5 V to 4.6 V
B port, V_{ERC}, and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 4.6 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 200 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
BIAS V_{CC}	Supply voltage		3	3.3	3.6	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port	0		V_{TT}	V
		Except B port	0		V_{CC}	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		V_{ERC}	V_{CC}–0.6	V_{CC}		
		Except B port and ERC	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		V_{ERC}		GND	0.6	
		Except B port and ERC			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, BIAS V_{CC} = 3.3 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and V_{CC} = 3.3 V, BIAS V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. When V_{CC} is connected, the BIAS V_{CC} circuitry is disabled.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 1 V and V_{TT} = 1.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2.2			
V_{OL}	A port	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.55	
	B port	V_{CC} = 3 V	I_{OL} = 40 mA			0.2	
			I_{OL} = 80 mA			0.4	
			I_{OL} = 100 mA			0.5	
I_I	Control inputs	V_{CC} = 3.6 V	V_I = V_{CC} or GND			±10	µA
	B port		V_I = V_{TT} or GND			±10	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V			±100	µA
$I_{I(hold)}$	A port	V_{CC} = 3 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.6 V‡,	V_I = 0 to V_{CC}			±500	
I_{OZH}	B port	V_{CC} = 3.6 V,	V_O = 1.5 V			10	µA
I_{OZL}	B port	V_{CC} = 3.6 V,	V_O = 0.4 V			–10	µA
I_{OZ}§	A port	V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{OZPU}	A port	V_{CC} = 0 to 3.6 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = low				±50	µA
I_{OZPD}	A port	V_{CC} = 3.6 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = low				±50	µA
I_{CC}	A or B port	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			80	mA
			Outputs low			80	
			Outputs disabled			80	
ΔI_{CC}¶	Except B port	V_{CC} = 3.6 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				1	mA
C_i	Control inputs	V_I = V_{CC} or 0			3	5	pF
C_{io}	A port	V_O = V_{CC} or 0			5	6	pF
	B port				6	8	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 3 V	V_O (B port) = 0 to 1.2 V,	V_I (BIAS V_{CC}) = 3 V to 3.6 V		5	mA
		V_{CC} = 3 V to 3.6 V				10	µA
V_O	B port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 3.3 V		1	1.2	V
I_O	B port	V_{CC} = 0,	V_O (B port) = 0.4 V,	V_I (BIAS V_{CC}) = 3 V to 3.6 V	–1		µA
		V_{CC} = 0 to 3.6 V,	$\overline{OE}$ = 3.3 V			100	
		V_{CC} = 0 to 1.5 V,	$\overline{OE}$ = 0 to 3.3 V			100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{ERC} = V_{CC} or GND for GTL (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				160	MHz
t_w	Pulse duration	LE high		3		ns
		CLK high or low		3		
t_{su}	Setup time	Data before CLK↑		2.7		ns
		Data before LE↓	CLK high	2.8		
			CLK low	2.6		
t_h	Hold time	Data after CLK↑		0.4		ns
		Data after LE↓	CLK high or low	0.9		

A-to-B switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{ERC} = V_{CC} or GND for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	A, V_{ERC} = V_{CC}	B	3.1	5.2	ns
t_{PHL}			2.6	6.2	
t_{PLH}	CLK, V_{ERC} = V_{CC}	B	3.4	5.5	ns
t_{PHL}			2.4	5.8	
t_{PLH}	LEAB, V_{ERC} = V_{CC}	B	3.5	5.8	ns
t_{PHL}			2.6	6.4	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$, V_{ERC} = V_{CC}	B	3.3	5.4	ns
t_{dis}			2.7	5.9	
t_{PLH}	A, V_{ERC} = GND	B	2.3	4.3	ns
t_{PHL}			1.9	4.3	
t_{PLH}	CLK, V_{ERC} = GND	B	2.7	4.8	ns
t_{PHL}			1.8	4.3	
t_{PLH}	LEAB, V_{ERC} = GND	B	2.8	4.9	ns
t_{PHL}			2	4.8	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$, V_{ERC} = GND	B	2.5	4.5	ns
t_{dis}			2	4.2	
Slew rate (V_{ERC} = V_{CC})	Both transitions, B outputs (0.6 V to 1.3 V)			1	ns/V
Slew rate (V_{ERC} = GND)	Both transitions, B outputs (0.6 V to 1.3 V)			1	ns/V
$t_{sk(o)}$†	Skew between drivers in the same package (switching in the same direction)			1	ns
$t_{sk(o)}$‡	Skew between drivers switching in any direction in the same package			1	ns

† Skew values are applicable for through mode only.
‡ Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

B-to-A switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	B	A	1.8	4.7	ns
t_{PHL}			2.3	4.6	
t_{PLH}	CLK	A	1.6	4	ns
t_{PHL}			1.5	3.4	
t_{PLH}	LEBA	A	1.7	4	ns
t_{PHL}			1.4	3.5	
t_{en}	$\overline{OEBA}$ or $\overline{OE}$	A	1.3	4.2	ns
t_{dis}			2	6.1	
$t_{sk(o)}$†	Skew between drivers in the same package (switching in the same direction)			1	ns
$t_{sk(o)}$‡	Skew between drivers switching in any direction in the same package			1	ns

† Skew values are applicable for through mode only.
‡ Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{ERC} = V_{CC} or GND for GTL+ (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				160	MHz
t_w	Pulse duration	LE high		3		ns
		CLK high or low		3		
t_{su}	Setup time	Data before CLK↑		2.7		ns
		Data before LE↓	CLK high	2.8		
			CLK low	2.6		
t_h	Hold time	Data after CLK↑		0.4		ns
		Data after LE↓	CLK high or low	0.9		

A-to-B switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{ERC} = V_{CC} or GND for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	A, V_{ERC} = V_{CC}	B	3	5.1	ns
t_{PHL}			2.9	6.5	
t_{PLH}	CLK, V_{ERC} = V_{CC}	B	3.4	5.4	ns
t_{PHL}			2.7	6.2	
t_{PLH}	LEAB, V_{ERC} = V_{CC}	B	3.5	5.7	ns
t_{PHL}			2.8	6.7	
t_{en}	$\overline{OEAB}$, V_{ERC} = V_{CC}	B	3.3	5.4	ns
t_{dis}			3	6.3	
t_{en}	$\overline{OE}$, V_{ERC} = V_{CC}	B	3	5.5	ns
t_{dis}			3.6	5.8	
t_{PLH}	A, V_{ERC} = GND	B	2.3	4.3	ns
t_{PHL}			2	4.4	
t_{PLH}	CLK, V_{ERC} = GND	B	2.7	4.8	ns
t_{PHL}			1.9	4.5	
t_{PLH}	LEAB, V_{ERC} = GND	B	2.8	4.9	ns
t_{PHL}			2.1	4.9	
t_{en}	$\overline{OEAB}$, V_{ERC} = GND	B	2.5	4.5	ns
t_{dis}			2.1	4.4	
t_{en}	$\overline{OE}$, V_{ERC} = GND	B	2.5	4.6	ns
t_{dis}			2.9	4.9	
Slew rate (V_{ERC} = V_{CC})	Both transitions, B outputs (0.6 V to 1.3 V)			1	ns/V
Slew rate (V_{ERC} = GND)	Both transitions, B outputs (0.6 V to 1.3 V)			1	ns/V
$t_{sk(o)}$†	Skew between drivers in the same package (switching in the same direction)			1	ns
$t_{sk(o)}$‡	Skew between drivers switching in any direction in the same package			1	ns

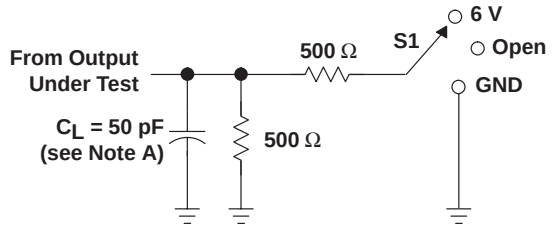
† Skew values are applicable for through mode only.
‡ Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

B-to-A switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	B	A	2	4.8	ns
t_{PHL}			2.4	4.7	
t_{PLH}	CLK	A	1.6	4.4	ns
t_{PHL}			1.5	3.4	
t_{PLH}	LEBA	A	1.7	4	ns
t_{PHL}			1.4	3.5	
t_{en}	$\overline{OEBA}$	A	1.3	4.2	ns
t_{dis}			2	6.1	
t_{en}	$\overline{OE}$	A	2.2	4.7	ns
t_{dis}			4.1	6.3	
$t_{sk(o)}$†	Skew between drivers in the same package (switching in the same direction)			1	ns
$t_{sk(o)}$‡	Skew between drivers switching in any direction in the same package			1	ns

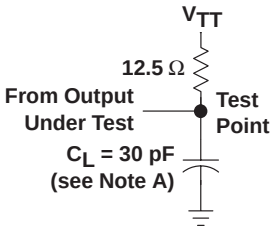
† Skew values are applicable for through mode only.
‡ Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

PARAMETER MEASUREMENT INFORMATION

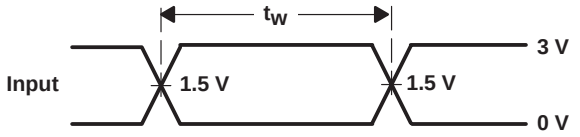


LOAD CIRCUIT FOR A OUTPUTS

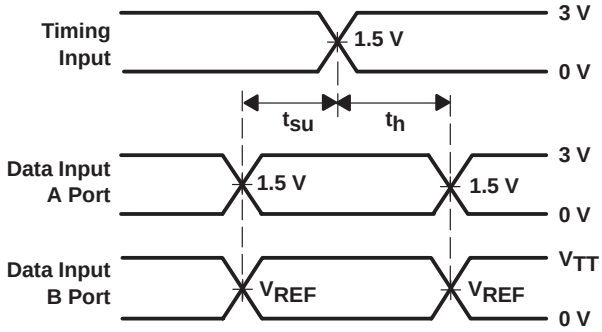
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



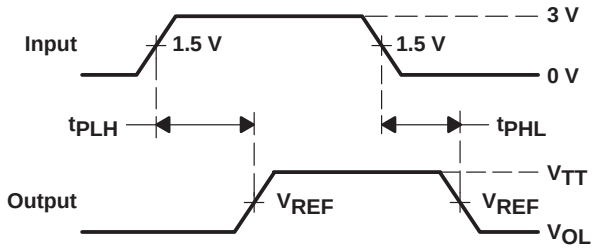
LOAD CIRCUIT FOR B OUTPUTS



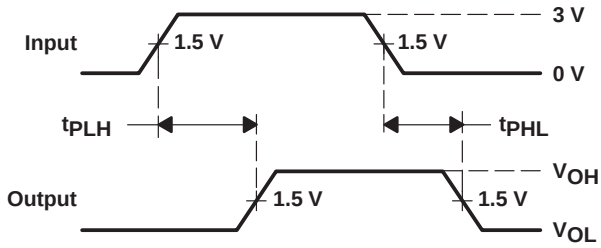
VOLTAGE WAVEFORMS
PULSE DURATION



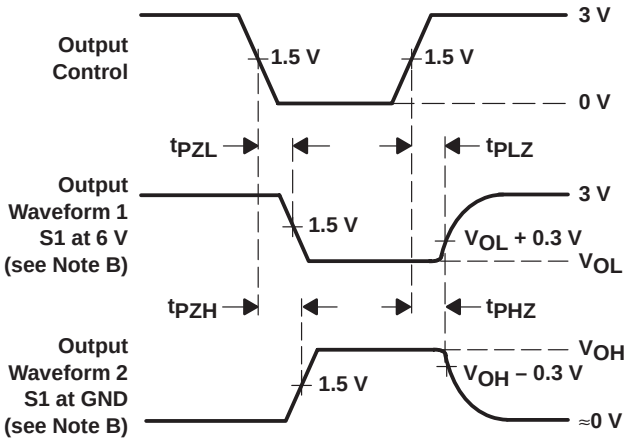
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLK to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLK to A port)



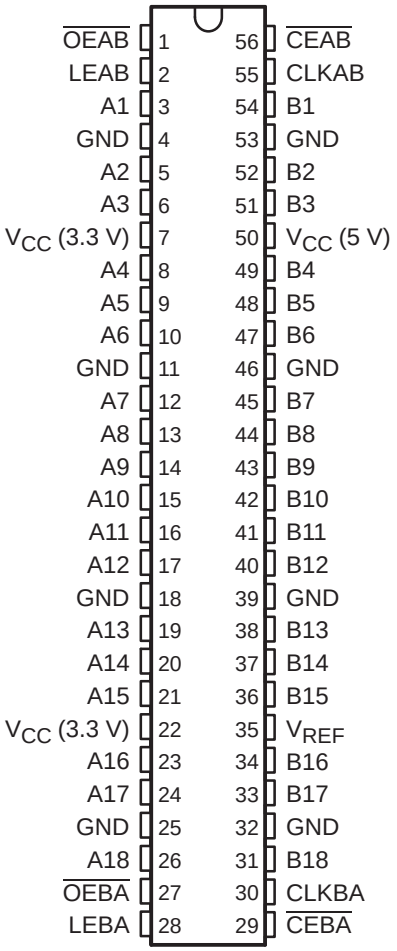
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Load Circuits and Voltage Waveforms

- **Members of Texas Instruments' Widebus™ Family**
- **UBT™ Transceivers Combine D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Translate Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **Identical to '16601 Function**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

SN54GTL16612 . . . WD PACKAGE
SN74GTL16612 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'GTL16612 devices are 18-bit UBT™ transceivers that provide LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. They combine D-type flip-flops and D-type latches to allow for transparent, latched, clocked, and clock-enabled modes of data transfer identical to the '16601 function. The devices provide an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using these devices at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

V_{CC} (5 V) supplies the internal and GTL circuitry while V_{CC} (3.3 V) supplies the LVTTL output buffers.

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description (continued)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable(LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTL16612DL	GTL16612
		Tape and reel	SN74GTL16612DLR	
	TSSOP – DGG	Tape and reel	SN74GTL16612DGGR	GTL16612
–55°C to 125°C	CFP – WD	Tube	SNJ54GTL16612WD	SNJ54GTL16612WD

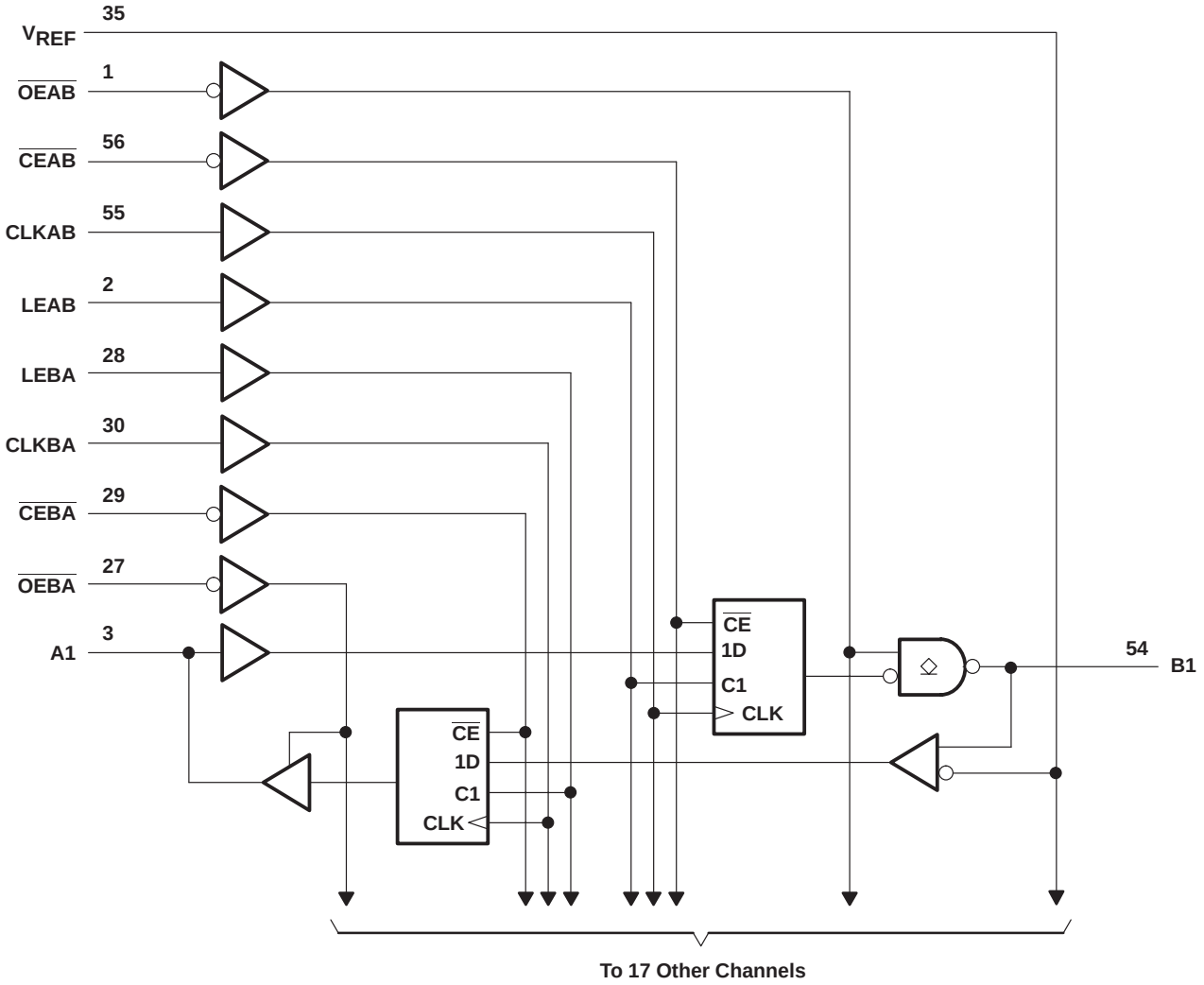
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE‡

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0§	Latched storage of A data
L	L	L	L	X	B_0¶	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0¶	Clock inhibit

‡ A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
¶ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . . –0.5 V to 4.6 V
5 V . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A-port and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 128 mA
B port . . . . . 80 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 64 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 64°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			SN54GTL16612			SN74GTL16612			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}			V_{TT}	V
		Except B port			5.5			5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V_{REF}+50 mV			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV			V_{REF}–50 mV	V
		Except B port			0.8			0.8	
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–32			–32	mA
I_{OL}	Low-level output current	A port			64			64	mA
		B port			40			40	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16612			SN74GTL16612			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V)= 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V	I_{OH} = –100 µA	V_{CC} (3.3 V)–0.2			V_{CC} (3.3 V)–0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			2.4			
			I_{OH} = –32 mA	2			2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 64 mA			0.6			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V, I_{OL} = 40 mA				0.5			0.4	
I_I	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V, V_{CC} (5 V) = 0 or 5.25 V	V_I = 5.5 V			10			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			1000			20	
			V_I = V_{CC} (3.3 V)			1			1	
			V_I = 0			–30			–30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5			5	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			1000			100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
			V_I = 0 to V_{CC} (3.3 V)‡			±500			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 3 V				1			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 1.2 V				10			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.5 V				–1			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, V_O = 0.4 V				–10			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			1			1	mA
			Outputs low			5			5	
			Outputs disabled			1			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND	Outputs high			120			120	mA
			Outputs low			120			120	
			Outputs disabled			120			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A-port or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V				1			1	mA
C_i	Control inputs	V_I = 3.15 V or 0			3.5	12		3.5		pF
C_{io}	A port	V_O = 3.15 V or 0			12	18		12		pF
	B port					10			5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (unless otherwise noted) (see Figure 1)

			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	1.3		1.3		ns
		B before CLKBA↑	3.4		2.5		
		A before LEAB↓	1.2		0		
		B before LEBA↓	1		1		
		$\overline{CEAB}$ before CLKAB↑	2.1		2		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.2		
t_h	Hold time	A after CLKAB↑	2.9		1.6		ns
		B after CLKBA↑	4.1		0.3		
		A after LEAB↓	4.5		4		
		B after LEBA↓	4.3		3.6		
		$\overline{CEAB}$ after CLKAB↑	2		0.8		
		$\overline{CEBA}$ after CLKBA↑	1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t_{PHL}			1	2.5	4.5	1.3	2.5	4	
t_{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t_{PHL}			1	3.5	6	1.9	3.5	5.4	
t_{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t_{PHL}			1	3.4	5.5	1.9	3.4	5.4	
t_{en}	$\overline{OEAB}$	B	1	3.3	5.5	2	3.3	5.5	ns
t_{dis}			1	3.4	5.5	2	3.4	5.1	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.3			1.3		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.5			0.5		ns
t_{PLH}	B	A	2	4.1	6.9	2.1	4.1	6.3	ns
t_{PHL}			1	2.9	5.1	1.2	2.9	4.6	
t_{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t_{PHL}			1	3	5.1	1.8	3	4.8	
t_{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t_{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t_{en}	$\overline{OEBA}$	A	1	5	7.5	2.3	5	7.4	ns
t_{dis}			2	4.3	6.9	2.5	4.3	6.4	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 1)

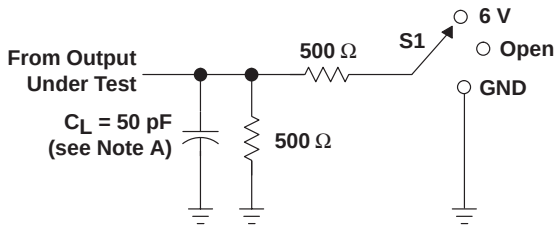
			SN54GTL16612		SN74GTL16612		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			95		95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		3.3		ns
		CLKAB or CLKBA high or low	5.6		5.6		
t_{su}	Setup time	A before CLKAB↑	1.3		1.3		ns
		B before CLKBA↑	3.2		2.3		
		A before LEAB↓	1.2		0		
		B before LEBA↓	1.3		1.3		
		$\overline{CEAB}$ before CLKAB↑	2.1		2		
		$\overline{CEBA}$ before CLKBA↑	2.6		2.2		
t_h	Hold time	A after CLKAB↑	2.9		1.6		ns
		B after CLKBA↑	4.4		0.3		
		A after LEAB↓	4.5		4		
		B after LEBA↓	4.3		3.6		
		$\overline{CEAB}$ after CLKAB↑	2		0.8		
		$\overline{CEBA}$ after CLKBA↑	1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

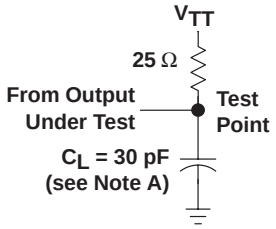
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16612			SN74GTL16612			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1	2.8	4.5	1.5	2.8	4.1	ns
t_{PHL}			1	2.5	4.6	1.3	2.5	4.1	
t_{PLH}	LEAB	B	1	3.6	5.5	2	3.6	5.3	ns
t_{PHL}			1	3.5	6.1	1.9	3.5	5.5	
t_{PLH}	CLKAB	B	1	3.7	5.5	2.3	3.7	5.3	ns
t_{PHL}			1	3.4	5.6	1.9	3.4	5.5	
t_{PLH}	$\overline{OEAB}$	B	1	3.4	5.5	2	3.4	5.1	ns
t_{PHL}			1	3.3	5.6	2	3.3	5.6	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.5			1.5		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.8			0.8		ns
t_{PLH}	B	A	1.9	4	6.9	2	4	6.3	ns
t_{PHL}			0.9	2.8	4.9	1.1	2.8	4.4	
t_{PLH}	LEBA	A	2	3.7	6.1	2.3	3.7	5.7	ns
t_{PHL}			1	3	5.1	1.8	3	4.8	
t_{PLH}	CLKBA	A	2	3.8	6.4	2.5	3.8	6.1	ns
t_{PHL}			2	3.3	5.6	2.3	3.3	5.2	
t_{en}	$\overline{OEBA}$	A	1	5	7.5	2.3	5	7.4	ns
t_{dis}			2	4.3	6.9	2.5	4.3	6.4	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+

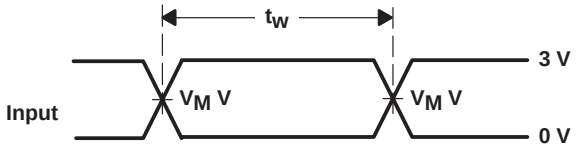


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

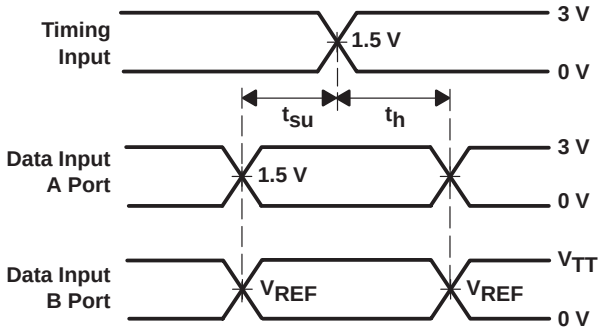


LOAD CIRCUIT FOR A OUTPUTS

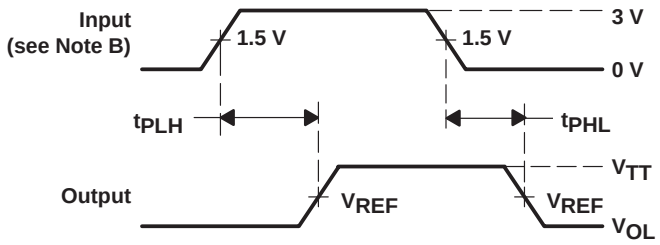
LOAD CIRCUIT FOR B OUTPUTS



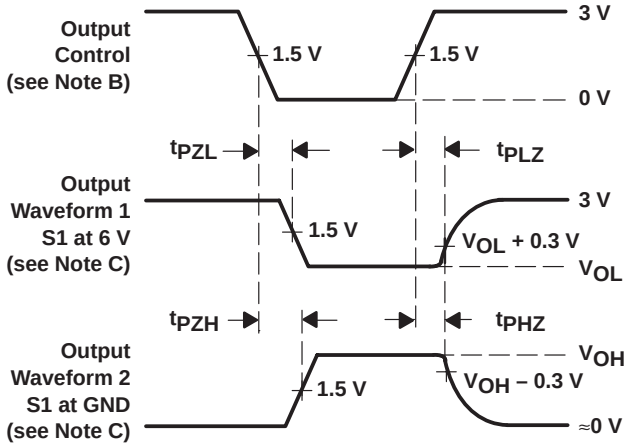
VOLTAGE WAVEFORMS
PULSE DURATION
(V_M = 1.5 V for A port and V_{REF} for B port)†



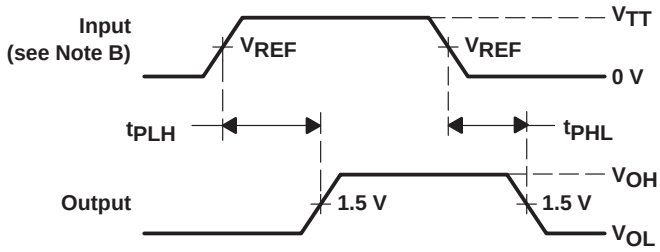
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)†

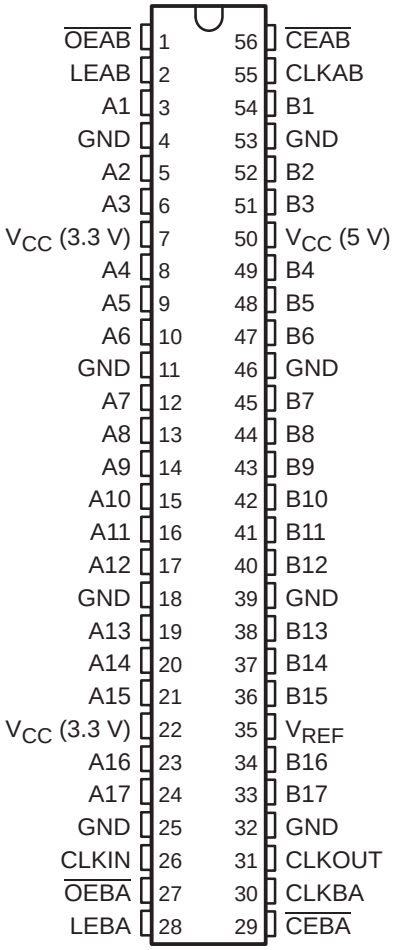
† All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveform

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **GTL Buffered CLKAB Signal (CLKOUT)**
- **Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Supports Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **Equivalent to '16601 Function**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  – 2000-V Human-Body Model (A114-A)

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTL16616 is a 17-bit UBT™ transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. Combined D-type flip-flops and D-type latches allow for transparent, latched, clocked, and clocked-enabled modes of data transfer identical to the '16601 function. Additionally, this device provides for a copy of CLKAB at GTL/GTL+ signal levels (CLKOUT) and conversion of a GTL/GTL+ clock to LVTTL logic levels (CLKIN). This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port. V_{CC} (5 V) supplies the internal and GTL circuitry while V_{CC} (3.3 V) supplies the LVTTL output buffers.

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description (continued)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ also is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTL16616DL	GTL16616
		Tape and reel	SN74GTL16616DLR	GTL16616
	TSSOP – DGG	Tape and reel	SN74GTL16616DGGR	GTL16616

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE‡

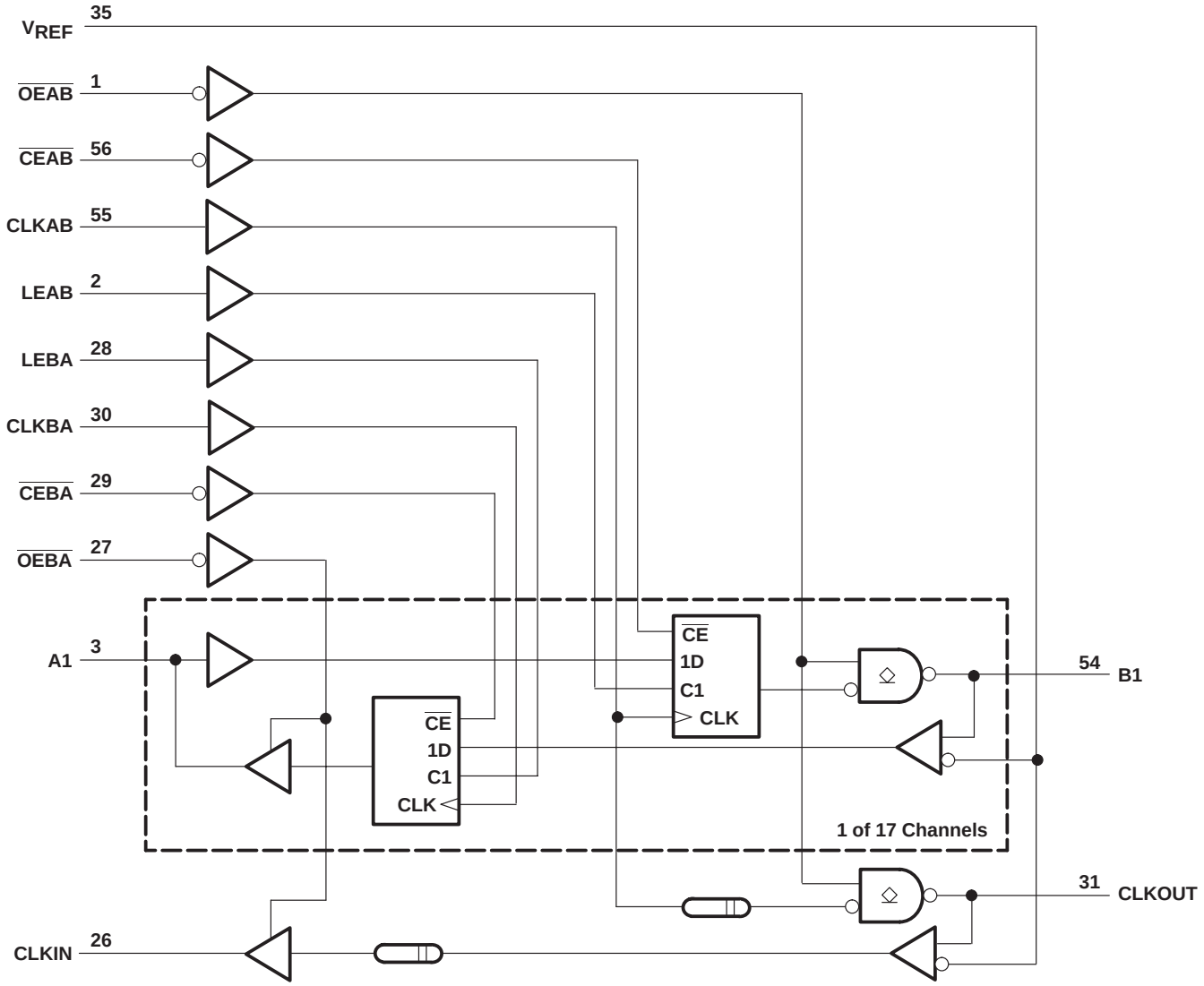
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0§	Latched storage of A data
L	L	L	L	X	B_0¶	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0¶	Clock inhibit

‡ A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

¶ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . . –0.5 V to 4.6 V
5 V . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A-port and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 128 mA
B port . . . . . 80 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 64 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 64°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–32	mA
I_{OL}	Low-level output current	A port			64	mA
		B port			40	
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V,		I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V,		I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V		I_{OH} = –8 mA	2.4			
				I_{OH} = –32 mA	2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V		I_{OL} = 100 µA			0.2	V
				I_{OL} = 16 mA			0.4	
				I_{OL} = 32 mA			0.5	
				I_{OL} = 64 mA			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V,		I_{OL} = 40 mA			0.4	
I_I	Control inputs	V_{CC} = 0 or 3.45 V, V_{CC} (5 V) = 0 or 5.25 V,		V_I = 5.5 V			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V		V_I = 5.5 V			20	
				V_I = V_{CC} (3.3 V)			1	
				V_I = 0			–30	
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V		V_I = V_{CC} (3.3 V)			5	
				V_I = 0			–5	
I_{off}		V_{CC} = 0, V_I or V_O = 0 to 4.5 V					100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V		V_I = 0.8 V	75			µA
				V_I = 2 V	–75			
				V_I = 0 to V_{CC} (3.3 V)‡			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V,		V_O = 3 V			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V,		V_O = 1.2 V			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V,		V_O = 0.5 V			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V,		V_O = 0.4 V			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND		Outputs high			1	mA
				Outputs low			5	
				Outputs disabled			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND		Outputs high			120	mA
				Outputs low			120	
				Outputs disabled			120	
ΔI_{CC}§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, A-port or control inputs at V_{CC} (3.3 V) or GND, One input at 2.7 V					1	mA
C_i	Control inputs	V_I = 3.15 V or 0				3.5		pF
C_{io}	A port	V_O = 3.15 V or 0				12		pF
	B port	Per IEEE Std 1194.1					5	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.5		
t_{su}	Setup time	A before CLKAB↑	1.3		ns
		B before CLKBA↑	2.5		
		A before LEAB↓	0		
		B before LEBA↓	1.1		
		$\overline{CEAB}$ before CLKAB↑	2.2		
		$\overline{CEBA}$ before CLKBA↑	2.7		
t_h	Hold time	A after CLKAB↑	1.6		ns
		B after CLKBA↑	0.4		
		A after LEAB↓	4		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.1		
		$\overline{CEBA}$ after CLKBA↑	0.9		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			95			MHz
t_{PLH}	A	B	1.7	3	4.4	ns
t_{PHL}			1.4	2.8	4.5	
t_{PLH}	LEAB	B	2.3	3.8	5.4	ns
t_{PHL}			2.2	3.7	5.3	
t_{PLH}	CLKAB	B	2.4	4	5.7	ns
t_{PHL}			2.1	3.7	5.4	
t_{PLH}	CLKAB	CLKOUT	4.7	6.1	8.1	ns
t_{PHL}			5.7	7.9	11.3	
t_{PHL}	$\overline{OEAB}$	B or CLKOUT	2.1	3.6	5.1	ns
t_{PLH}			2.1	3.8	5.6	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.2		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			0.7		ns
t_{PLH}	B	A	1.7	4	6.7	ns
t_{PHL}			1.4	2.9	4.7	
t_{PLH}	LEBA	A	2.4	3.8	5.8	ns
t_{PHL}			2	3	4.6	
t_{PLH}	CLKBA	A	2.6	4	6	ns
t_{PHL}			2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.4	10	14.4	ns
t_{PHL}			6.1	8.1	11.7	
t_{en}	$\overline{OEBA}$	A or CLKIN	2.8	5.3	7.8	ns
t_{dis}			2.7	4.3	6.4	

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 1)

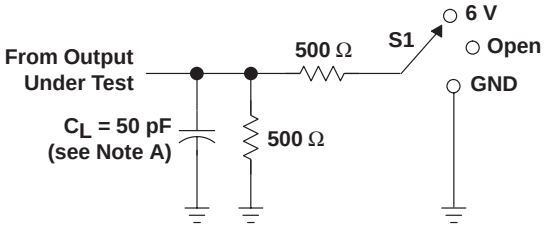
			MIN	MAX	UNIT
f_{clock}	Clock frequency			95	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.5		
t_{su}	Setup time	A before CLKAB↑	1.3		ns
		B before CLKBA↑	2.3		
		A before LEAB↓	0		
		B before LEBA↓	1.3		
		$\overline{CEAB}$ before CLKAB↑	2.2		
		$\overline{CEBA}$ before CLKBA↑	2.7		
t_h	Hold time	A after CLKAB↑	1.6		ns
		B after CLKBA↑	0.6		
		A after LEAB↓	4		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.1		
		$\overline{CEBA}$ after CLKBA↑	0.9		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			95			MHz
t_{PLH}	A	B	1.7	3	4.4	ns
t_{PHL}			1.4	2.9	4.6	
t_{PLH}	LEAB	B	2.3	3.8	5.4	ns
t_{PHL}			2.2	3.7	5.4	
t_{PLH}	CLKAB	B	2.4	4	5.7	ns
t_{PHL}			2.1	3.8	5.5	
t_{PLH}	CLKAB	CLKOUT	4.7	6.1	8.1	ns
t_{PHL}			5.7	8	11.4	
t_{PLH}	$\overline{OEAB}$	B or CLKOUT	2.1	3.6	5.1	ns
t_{PHL}			2.1	3.8	5.7	
t_r	Transition time, B outputs (0.5 V to 1 V)			1.4		ns
t_f	Transition time, B outputs (1 V to 0.5 V)			1		ns
t_{PLH}	B	A	1.6	3.9	6.6	ns
t_{PHL}			1.3	2.8	4.5	
t_{PLH}	LEBA	A	2.4	3.8	5.8	ns
t_{PHL}			2	3	4.6	
t_{PLH}	CLKBA	A	2.6	4	6	ns
t_{PHL}			2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.3	9.9	14.3	ns
t_{PHL}			6	8	11.5	
t_{en}	$\overline{OEBA}$	A or CLKIN	2.8	5.3	7.8	ns
t_{dis}			2.7	4.3	6.4	

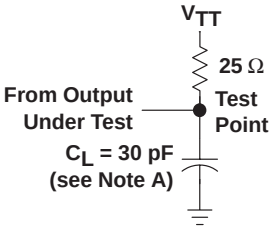
† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+

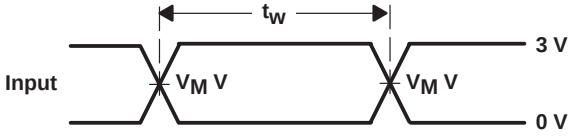


LOAD CIRCUIT FOR A OUTPUTS

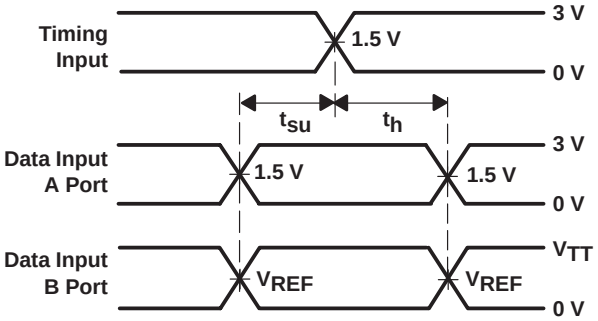
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



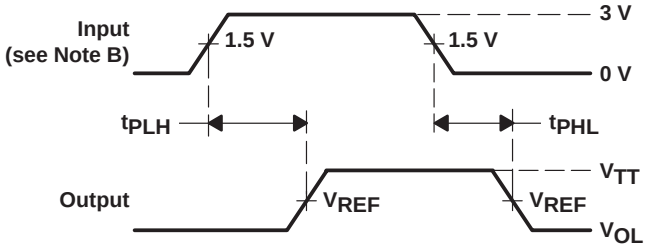
LOAD CIRCUIT FOR B OUTPUTS



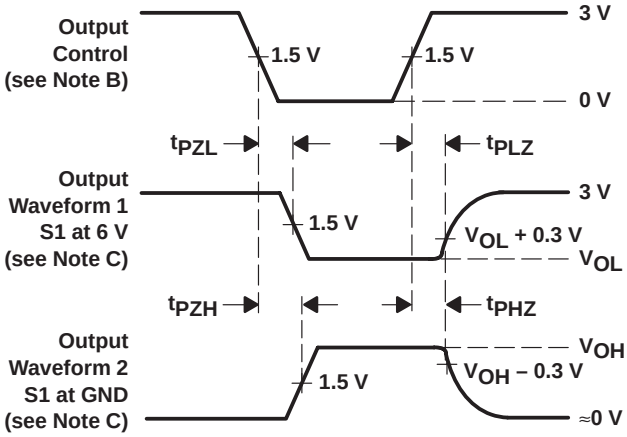
VOLTAGE WAVEFORMS
PULSE DURATION
(V_M = 1.5 V for A port and V_{REF} for B port)†



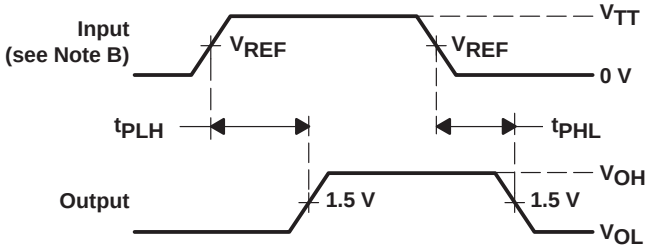
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port and CLKIN)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

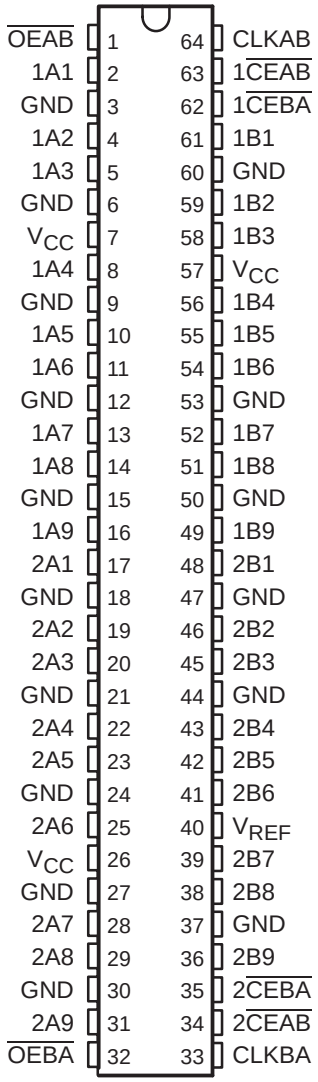
† All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Member of Texas Instruments' Widebus™ Family**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Supports Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Noise**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTL16622A is an 18-bit registered bus transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two separate 9-bit transceivers with individual clock-enable controls and contains D-type flip-flops for temporary storage of data flowing in either direction. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

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description (continued)

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL16622ADGGR	GTL16622A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

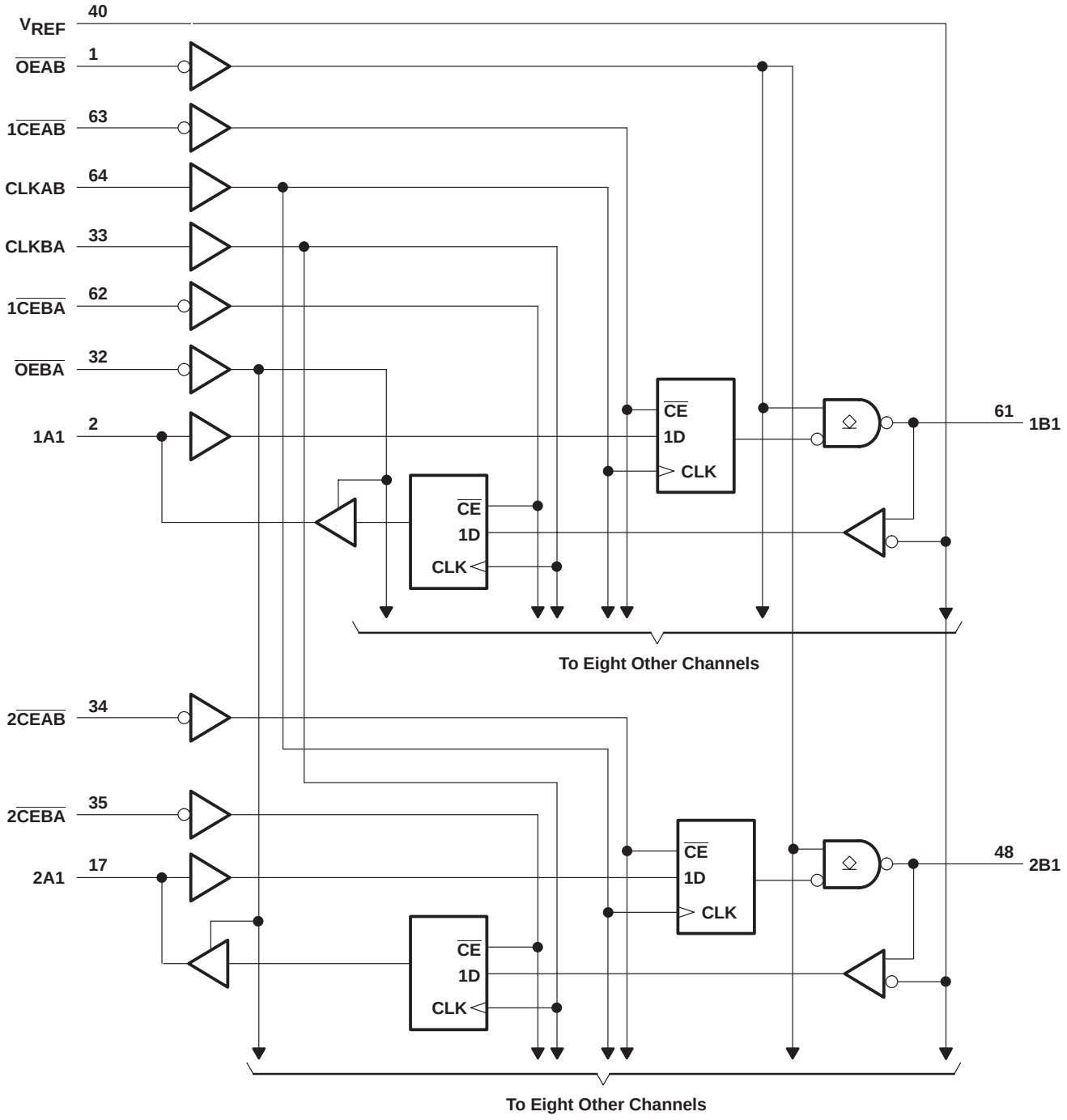
FUNCTION TABLE‡

INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	B_0§	Latched storage of A data
X	L	H or L	X	B_0§	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

‡ A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

§ Output level before the indicated steady-state input conditions are established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs . . . . . –0.5 V to 6.5 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 6.5 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I	B port	V_{CC} = 3.45 V,	V_I = V_{TT} or GND			±5	µA
	A-port and control inputs	V_{CC} = 3.45 V	V_I = V_{CC} or GND			±5	
			V_I = 5.5 V or GND			±20	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			100	µA
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.45 V‡,	V_I = 0.8 V to 2 V			±500	
I_{OZ}§	A port	V_{CC} = 3.45 V,	V_O = V_{CC} or GND			±10	µA
I_{OZH}	B port	V_{CC} = 3.45 V,	V_O = 1.5 V			10	µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			60	mA
			Outputs low			60	
			Outputs disabled			60	
ΔI_{CC}¶		V_{CC} = 3.45 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				500	µA
C_i	Control inputs	V_I = 3.15 V or 0			2.5	3	pF
C_{io}	A port	V_O = 3.15 V or 0			6	8	pF
	B port				6.5	8.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.1		ns
		$\overline{CE}$ before CLK↑	3.3		
t_h	Hold time	Data after CLK↑	0.3		ns
		$\overline{CE}$ after CLK↑	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.5		5.5	ns
t_{PHL}			2.2		5.5	
t_{dis}	$\overline{OEAB}$	B	1.7		4.8	ns
t_{en}			2.2		5.2	
Slew rate	Both transitions (B port)			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.6		2.2	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.4		1.5	ns
t_{PLH}	CLKBA	A	2.1		5.3	ns
t_{PHL}			2.1		5	
t_{en}	$\overline{OEBA}$	A	1.7		5	ns
t_{dis}			2.3		5.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

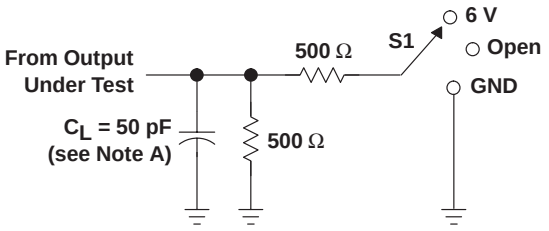
			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.4		ns
		$\overline{CE}$ before CLK↑	3.2		
t_h	Hold time	Data after CLK↑	0.2		ns
		$\overline{CE}$ after CLK↑	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.6	4	5.6	ns
t_{PHL}			2.3	4	5.7	
t_{PLH}	$\overline{OEAB}$	B	2.4	3.8	5.2	ns
t_{PHL}			1.8	3.4	5	
Slew rate	Both transitions (B port)			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)		1	1.6	2.7	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)		0.5	1.1	3.2	ns
t_{PLH}	CLKBA	A	2	3.8	5.3	ns
t_{PHL}			1.9	3.6	5	
t_{en}	$\overline{OEBA}$	A	1.9	3.6	5	ns
t_{dis}			2.1	4	5.5	

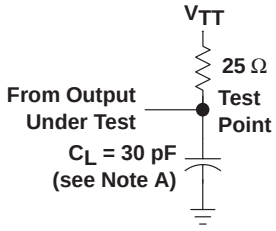
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

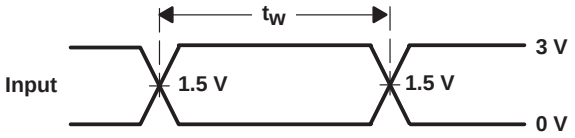


LOAD CIRCUIT FOR A OUTPUTS

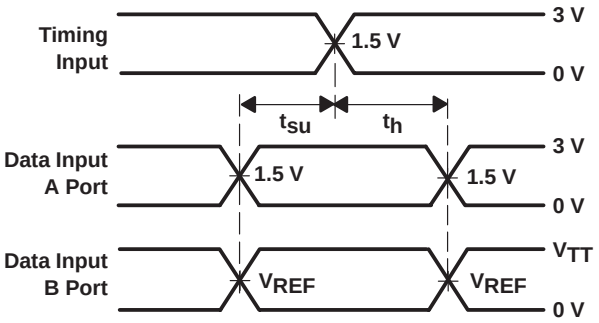
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



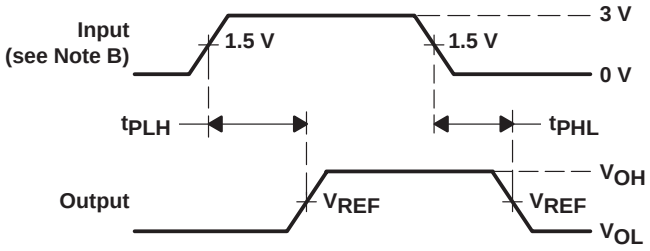
LOAD CIRCUIT FOR B OUTPUTS



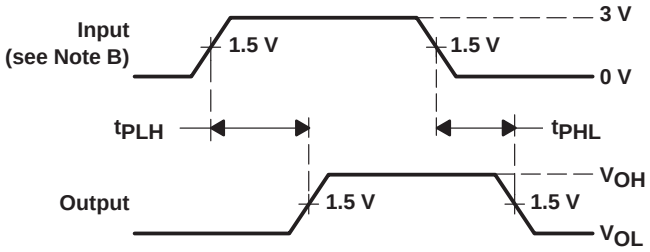
VOLTAGE WAVEFORMS
PULSE DURATION



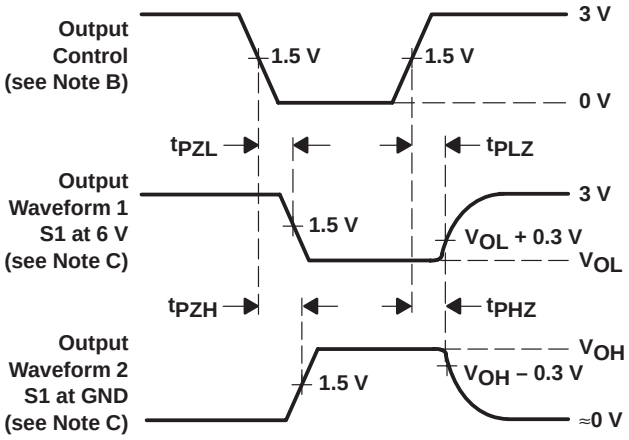
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



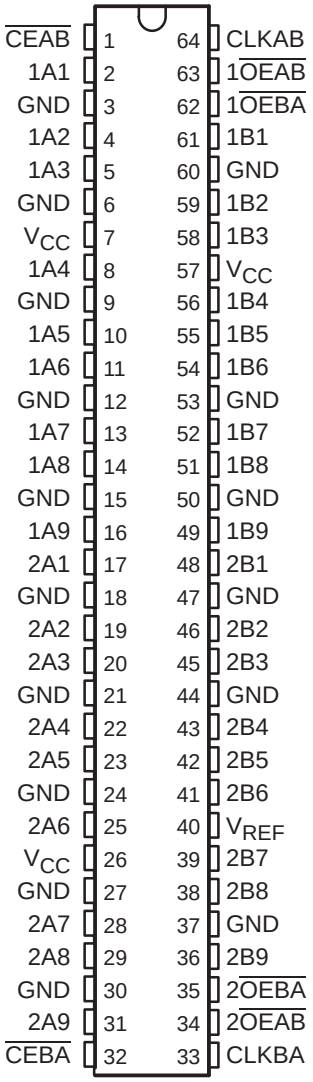
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
($\overline{OEBA}$ to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Member of Texas Instruments' Widebus™ Family**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **D-Type Flip-Flops With Qualified Storage Enable**
- **Translates Between GTL/GTL+ Signal Levels and LVTTL Logic Levels**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltages With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTL16923 is an 18-bit registered bus transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two 9-bit transceivers with individual output-enable controls and contains D-type flip-flops for temporary storage of data flowing in either direction. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry.

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels. All inputs can be driven from either 3.3-V or 5-V devices, which allows use in a mixed 3.3-V/5-V system environment. V_{REF} is the reference input voltage for the B port.

OEC and Widebus are trademarks of Texas Instruments.

description (continued)

Data flow in each direction is controlled by the output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock (CLKAB and CLKBA) inputs. The clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs enable or disable the clock for all 18 bits at a time. However, $\overline{OEAB}$ and $\overline{OEBA}$ are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the device operates on the low-to-high transition of CLKAB if $\overline{CEAB}$ is low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL16923DGGR	GTL16923

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

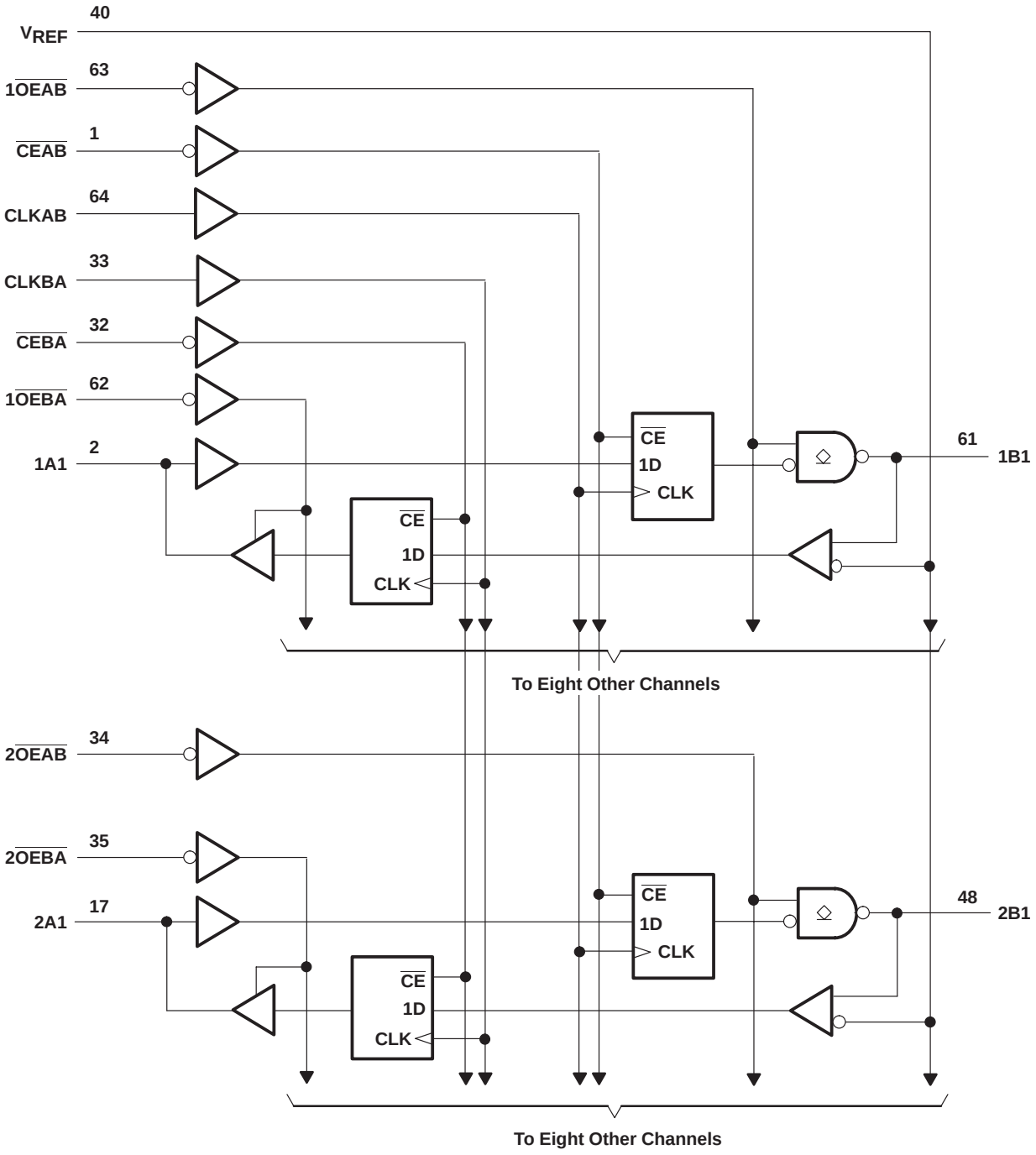
FUNCTION TABLE‡

INPUTS				OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	CLKAB	A		
X	H	X	X	Z	Isolation
H	L	X	X	B_0§	Latched storage of A data
X	L	H or L	X	B_0§	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

‡ A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, CLKBA, and $\overline{CEBA}$.

§ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Current into any A-port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port	0		V_{TT}	V
		Except B port	0		5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTL/GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I	B port	V_{CC} = 3.45 V,	V_I = 5.5 V or GND			±5	µA
	A-port and control inputs	V_{CC} = 3.45 V	V_I = V_{CC} or GND			±5	
			V_I = 5.5 V or GND			±20	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			±100	µA
$I_{I(hold)}$	A port	V_{CC} = 3.15 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.45 V‡,	V_I = 0.8 V to 2 V			±500	
I_{OZ}§	A port	V_{CC} = 3.45 V,	V_O = V_{CC} or GND			±10	µA
I_{OZH}	B port	V_{CC} = 3.45 V,	V_O = 1.5 V			10	µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			60	mA
			Outputs low			60	
			Outputs disabled			60	
ΔI_{CC}¶		V_{CC} = 3.45 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				500	µA
C_i	Control inputs	V_I = 3.15 V or 0			2.5	3	pF
C_{io}	A port	V_O = 3.15 V or 0			6	8.5	pF
	B port	V_O = 3.15 V or 0			7	9.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.6		ns
		$\overline{CE}$ before CLK↑	3.3		
t_h	Hold time	Data after CLK↑	0.1		ns
		$\overline{CE}$ after CLK↑	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.2		5.8	ns
t_{PHL}			2.1		6.3	
t_{dis}	$\overline{OEAB}$	B	1.7		5.3	ns
t_{en}			2		5	
Slew rate	Both transitions			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1 V)		0.3		2.9	ns
t_f	Transition time, B outputs (1 V to 0.6 V)		0.1		3.9	ns
t_{PLH}	CLKBA	A	1.8		5	ns
t_{PHL}			1.7		4.8	
t_{en}	$\overline{OEBA}$	A	1.3		4.8	ns
t_{dis}			2		4.8	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

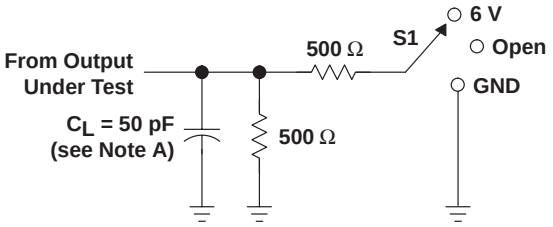
			MIN	MAX	UNIT
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK high or low		2.5		ns
t_{su}	Setup time	Data before CLK↑	2.3		ns
		$\overline{CE}$ before CLK↑	3.3		
t_h	Hold time	Data after CLK↑	0.1		ns
		$\overline{CE}$ after CLK↑	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			200			MHz
t_{PLH}	CLKAB	B	2.2	4	5.9	ns
t_{PHL}			2.1	4	6.1	
t_{PLH}	$\overline{OEAB}$	B	1.9	3.4	5.2	ns
t_{PHL}			1.7	3.1	5.1	
Slew rate	Both transitions			0.5		V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)		0.6	1.3	2.6	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)		0.4	1.3	3	ns
t_{PLH}	CLKBA	A	1.8	3.5	5.1	ns
t_{PHL}			1.7	3.3	4.9	
t_{en}	$\overline{OEBA}$	A	1.3	2.9	4.8	ns
t_{dis}			2	3.2	5	

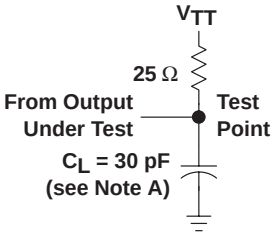
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.5 V, V_{REF} = 1 V

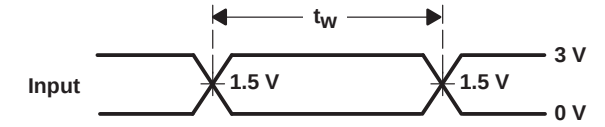


LOAD CIRCUIT FOR A OUTPUTS

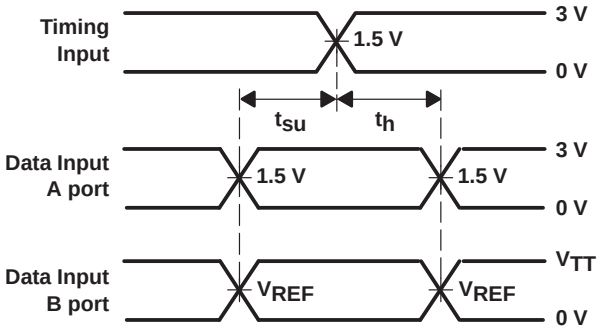
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



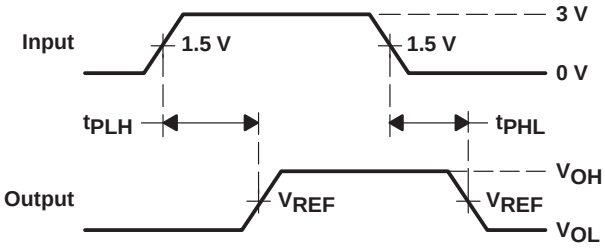
LOAD CIRCUIT FOR B OUTPUTS



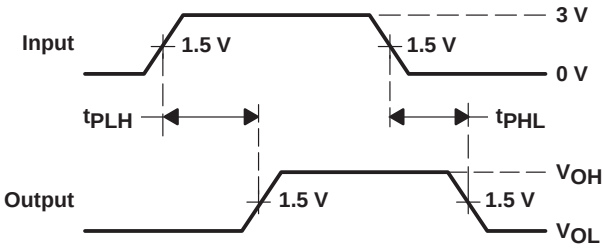
VOLTAGE WAVEFORMS
PULSE DURATION



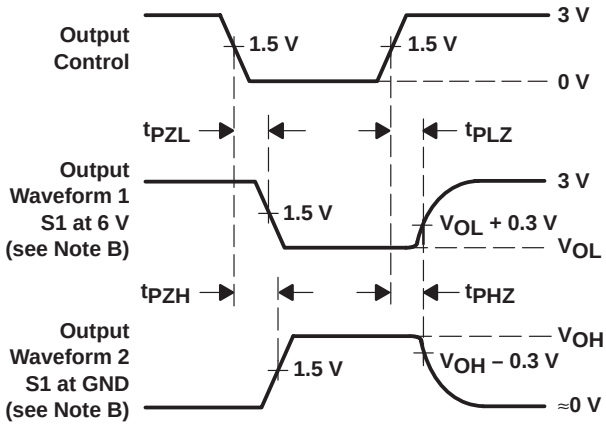
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKAB to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLKBA to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

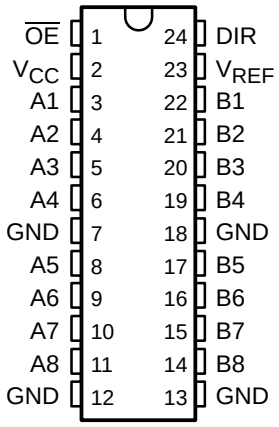
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Contents

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLPH306 is a medium-drive, 8-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH306 is given only at the preferred higher-noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

OEC, TI, and TI-OPC are trademarks of Texas Instruments.

description (continued)

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLPH306DW	GTLPH306
		Tape and reel	SN74GTLPH306DWR	
	TSSOP – PW	Tape and reel	SN74GTLPH306PWR	GH306
	TVSOP – DGV	Tape and reel	SN74GTLPH306DGVR	GH306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH306 is an 8-bit bus transceiver and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

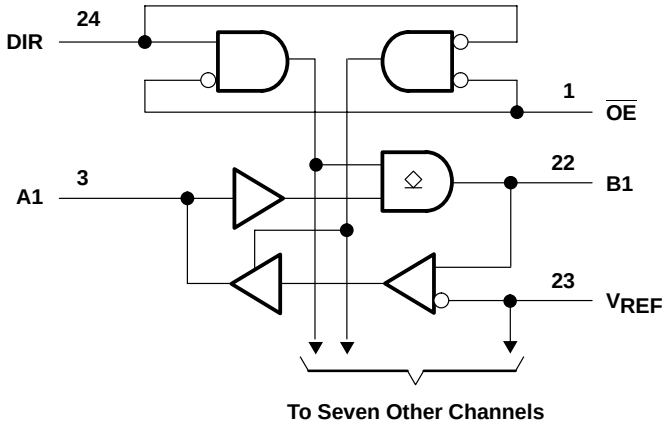
For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except $\overline{OE}$ and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 100 mA
Current into any A port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package . . . . . 86°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±5	µA
			V_I = 5.5 V			±20	
	B port		V_I = 0 to 1.5 V			±5	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4.5	5	pF
C_{io}	A port	V_O = 3.15 V or 0			7.5	9	pF
	B port	V_O = 1.5 V or 0			7.5	9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

hot-insertion specifications for B port over recommended operating free-air temperature range

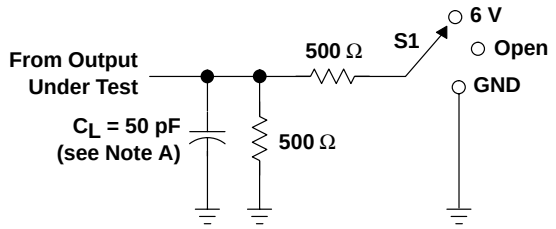
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	B	1		7.5	ns
t_{PHL}			1		7.5	
t_{en}	$\overline{OE}$	B	1		8	ns
t_{dis}			1		8	
t_r	Rise time, B outputs (20% to 80%)			2.2		ns
t_f	Fall time, B outputs (80% to 20%)			2.1		ns
t_r	Rise time, A outputs (10% to 90%)			4.1		ns
t_f	Fall time, A outputs (90% to 10%)			3.3		ns
t_{PLH}	B	A	1		7	ns
t_{PHL}			1		7	
t_{en}	$\overline{OE}$	A	1		8	ns
t_{dis}			1		8	

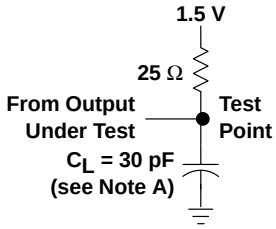
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

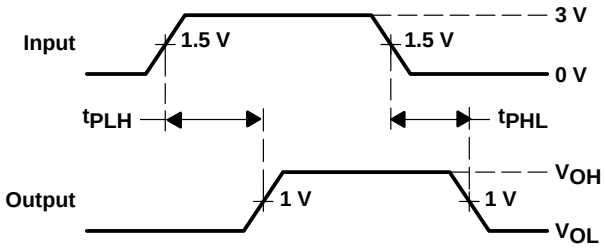


LOAD CIRCUIT FOR A OUTPUTS

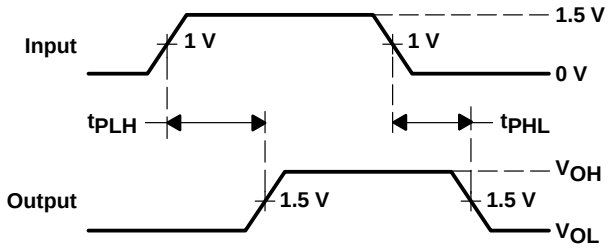
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



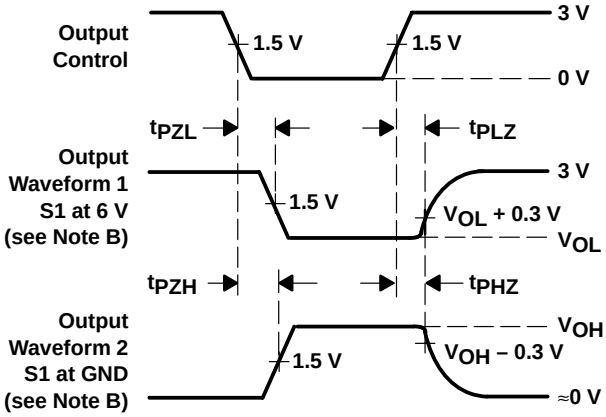
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

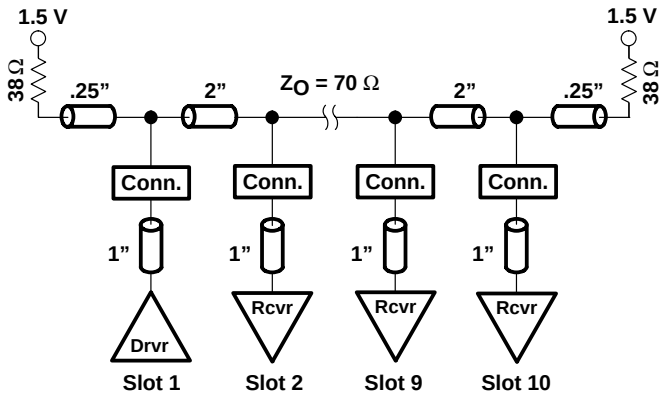


Figure 2. Medium-Drive Test Backplane

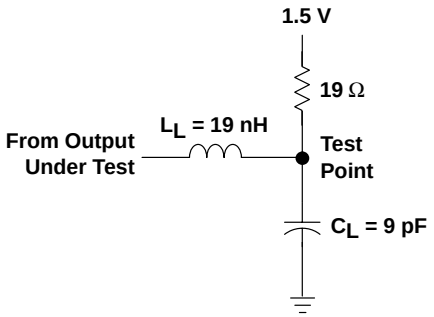


Figure 3. Medium-Drive RLC Network

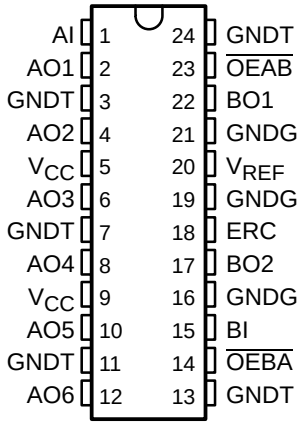
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	3.6	ns
t_{PHL}			4.1	
t_{en}	$\overline{OE}$	B	4.4	ns
t_{dis}			4.6	
t_r	Rise time, B outputs (20% to 80%)		1.2	ns
t_f	Fall time, B outputs (80% to 20%)		2.2	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP-to-LVTTL 1-to-6 Fanout Driver**
- **LVTTL-to-GTLP 1-to-2 Fanout Driver**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **Reduced-Drive LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGV, DW, OR PW PACKAGE (TOP VIEW)



description

The SN74GTLP817 is a medium-drive fanout driver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, and OEC™ circuitry. The improved GTLP OEC circuitry minimizes bus settling time and has been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω. BO1 and BO2 can be tied together to drive an equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP817 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

GNDT is the TTL output ground, while GNDG is the GTLP output ground, and both may be separated from each other for a quieter device.

description (continued)

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

This device features adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load. ERC automatically is selected to the same speed as alternate source 1-to-6 fanout drivers that use pin 18 for 3.3-V or 5-V V_{CC}.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP817DW	GTLP817
		Tape and reel	SN74GTLP817DWR	
	TSSOP – PW	Tape and reel	SN74GTLP817PWR	GT817
	TVSOP – DGV	Tape and reel	SN74GTLP817DGVR	GT817

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP817 is a fanout driver providing LVTTL-to-GTLP translation and GTLP-to-LVTTL translation in the same package.

The LVTTL-to-GTLP direction is a 1-to-2 fanout driver with a single output enable ($\overline{OEAB}$).

The GTLP-to-LVTTL direction is a 1-to-6 fanout driver with a single output enable ($\overline{OEBA}$).

Data polarity is inverting for both directions.

Function Tables

OUTPUT CONTROL (A to B)

INPUTS		OUTPUT BOn	MODE
AI	$\overline{OEAB}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

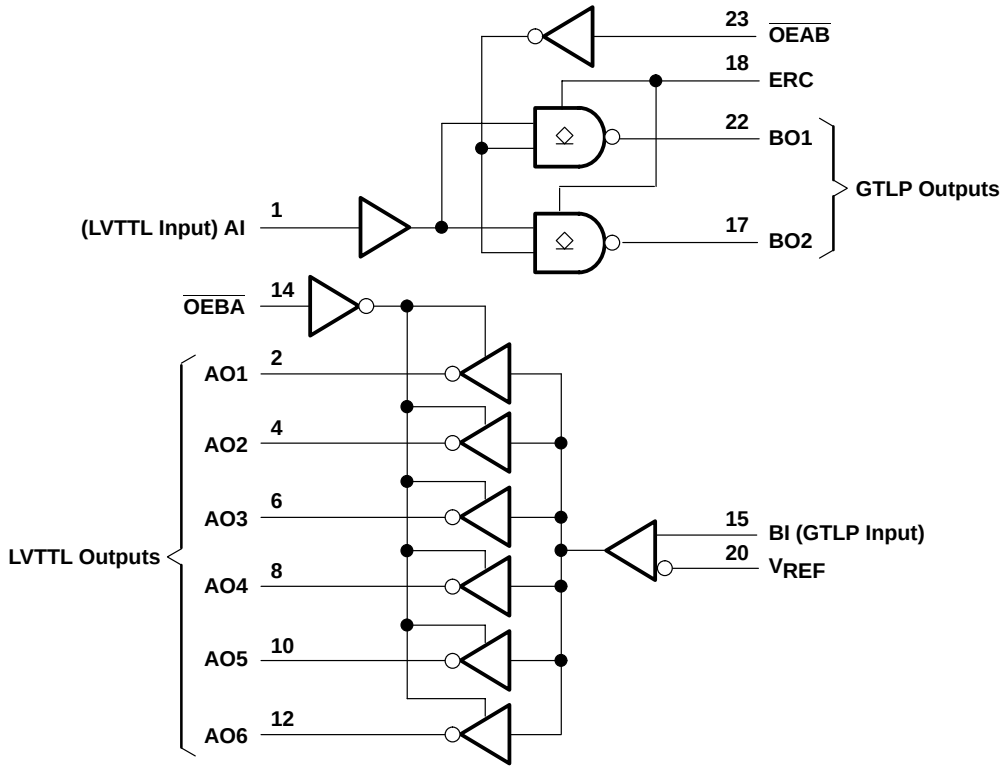
OUTPUT CONTROL (B to A)

INPUTS		OUTPUT AOn	MODE
BI	$\overline{OEBA}$		
X	H	Z	Isolation
H	L	L	Inverted transparent
L	L	H	

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Ground dc voltage difference, ($\lvert V_{GNDG} – V_{GNDT} \rvert$)	0.3 V
Input voltage range, V_I (see Note 1): AI port and control inputs	–0.5 V to 7 V
BI port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): AO port	–0.5 V to 7 V
BO port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port	24 mA
BO port	100 mA
Current into any A output in the high state, I_O (see Note 2)	24 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	BI			V_{TT}	V
		AI, $\overline{OE}$		V_{CC}	5.5	
V_{IH}	High-level input voltage	BI	V_{REF}+0.05			V
		ERC	V_{CC}–0.6	V_{CC}	5.5	
		AI, $\overline{OE}$	2			
V_{IL}	Low-level input voltage	BI			V_{REF}–0.05	V
		ERC		GND	0.6	
		AI, $\overline{OE}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–12	mA
I_{OL}	Low-level output current	AO port			12	mA
		BO port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –100 µA	V_{CC}–0.2			
			I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2.2			
V_{OL}	AO port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 6 mA			0.4	
			I_{OL} = 12 mA			0.5	
	BO port	V_{CC} = 3.15 V	I_{OL} = 100 µA			0.2	
			I_{OL} = 40 mA			0.5	
			I_{OL} = 50 mA			0.55	
I_I	BI, AI, $\overline{OE}$, ERC	V_{CC} = 3.45 V	V_I = 0 or 5.5 V			±5	µA
I_{OZH}	AO port	V_{CC} = 3.45 V	$V_O = V_{CC}$			10	µA
	BO port		V_O = 1.5 V			5	
I_{OZL}	AO port	V_{CC} = 3.45 V	V_O = GND			–10	µA
	BO port		V_O = 5.5 V			–5	
I_{CC}	AO or BO port	V_{CC} = 3.45 V, I_O = 0, V_I (AI or control input) = V_{CC} or GND, V_I (BI input) = V_{TT} or GND	Outputs high			10	mA
			Outputs low			10	
			Outputs disabled			10	
ΔI_{CC}‡	AI, $\overline{OE}$	V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	AI, $\overline{OE}$, ERC	$V_I = V_{CC}$ or 0			4	4.4	pF
	BI	$V_I = V_{TT}$ or 0			3.5	3.9	
C_o	AO port	$V_O = V_{CC}$ or 0			4	4.5	pF
	BO port	$V_O = V_{TT}$ or 0			5	5.4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

hot-insertion specifications for B port over recommended operating free-air temperature range

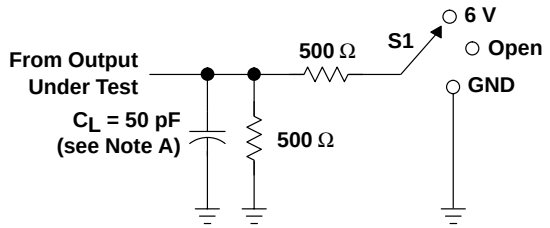
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±30	µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	AI	BO	Slow	3		6	ns
t_{PHL}				1.8		4.7	
t_{PLH}	AI	BO	Fast	2		5	ns
t_{PHL}				1.5		4.2	
t_{en}	$\overline{OEAB}$	BO	Slow	3		6.1	ns
t_{dis}				2		4.7	
t_{en}	$\overline{OEAB}$	BO	Fast	2.1		6	ns
t_{dis}				1.5		4.7	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.4		
t_f	Fall time, B outputs (80% to 20%)		Slow		1.7		ns
			Fast		1		
t_{PLH}	BI	AO	–	2.3		6	ns
t_{PHL}				1.9		4.7	
t_{en}	$\overline{OEBA}$	AO	–	1.1		6.3	ns
t_{dis}				1.2		5	

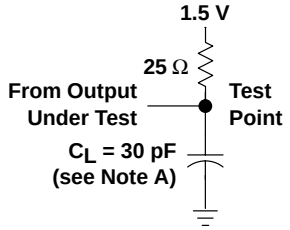
† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

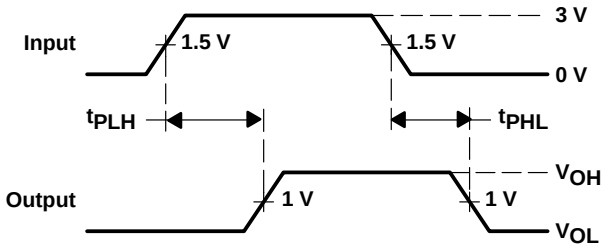


LOAD CIRCUIT FOR AO PORTS

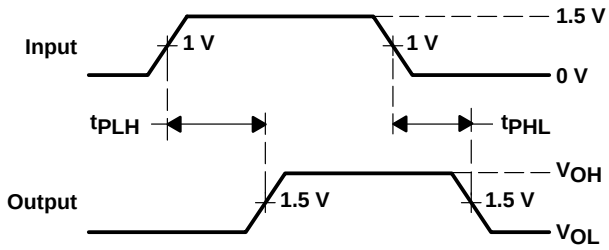
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



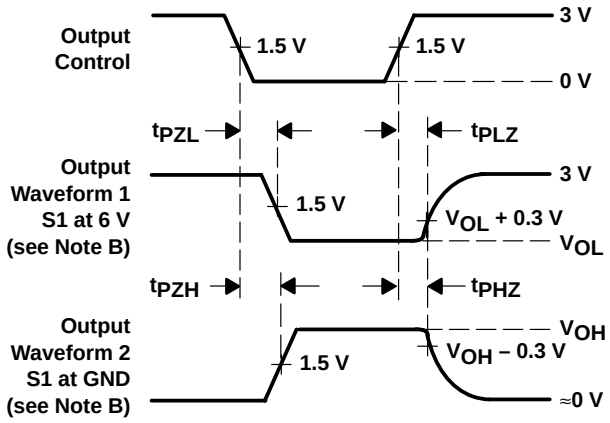
LOAD CIRCUIT FOR BO PORTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to BO port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(BI to AO port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO ports)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

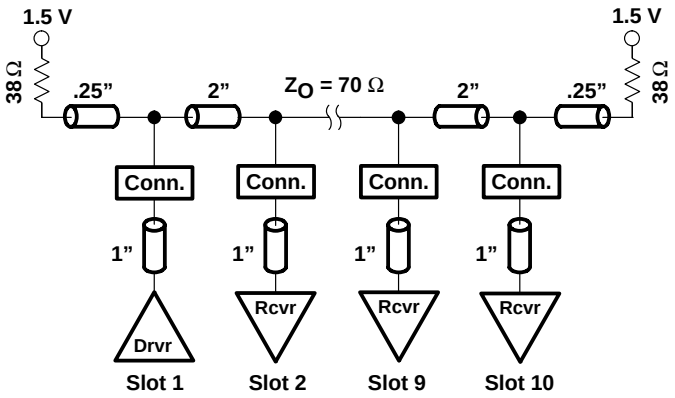


Figure 2. Medium-Drive Test Backplane

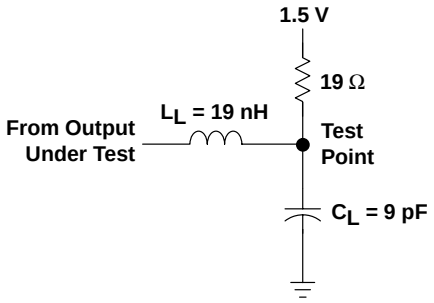


Figure 3. Medium-Drive RLC Network

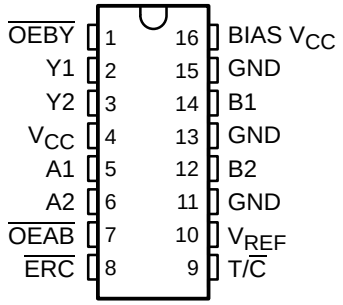
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI	BO	Slow	4.4	ns
t_{PHL}				4.4	
t_{PLH}	AI	BO	Fast	3.2	ns
t_{PHL}				3.2	
t_{en}	$\overline{OEAB}$	BO	Slow	4	ns
t_{dis}				4.4	
t_{en}	$\overline{OEAB}$	BO	Fast	2.9	ns
t_{dis}				3.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	1.8	ns
			Fast	1	
t_f	Fall time, B outputs (80% to 20%)		Slow	2	ns
			Fast	1.6	

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Polarity Control Selects True or Complementary Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

D, DGV, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP1394 is a high-drive, 2-bit, 3-wire bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels, and is especially designed to work with the Texas Instruments 1394 backplane physical-layer controllers. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuitry minimizes bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP1394 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B port differential input reference voltage.

OEC, TI, and TI-OPC are trademarks of Texas Instruments.

description (continued)

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74GTLP1394D	GTLP1394
		Tape and reel	SN74GTLP1394DR	
	TSSOP – PW	Tape and reel	SN74GTLP1394PWR	GP394
	TVSOP – DGV	Tape and reel	SN74GTLP1394DGVR	GP394

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The output-enable ($\overline{OEAB}$) input controls the activity of the B port. When $\overline{OEAB}$ is low, the B-port outputs are active. When $\overline{OEAB}$ is high, the B-port outputs are disabled.

Separate LVTTL input and output pins provide a feedback path for control and diagnostics monitoring. The $\overline{OEBY}$ input controls the Y outputs. When $\overline{OEBY}$ is low, the Y outputs are active. When $\overline{OEBY}$ is high, the Y outputs are disabled.

The polarity-control (T/$\overline{C}$) input is provided to select polarity of data transmission in both directions. When T/$\overline{C}$ is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/$\overline{C}$ is low, data transmission is complementary, and inverted A data goes to the B bus and inverted B data goes to the Y bus.

Function Tables

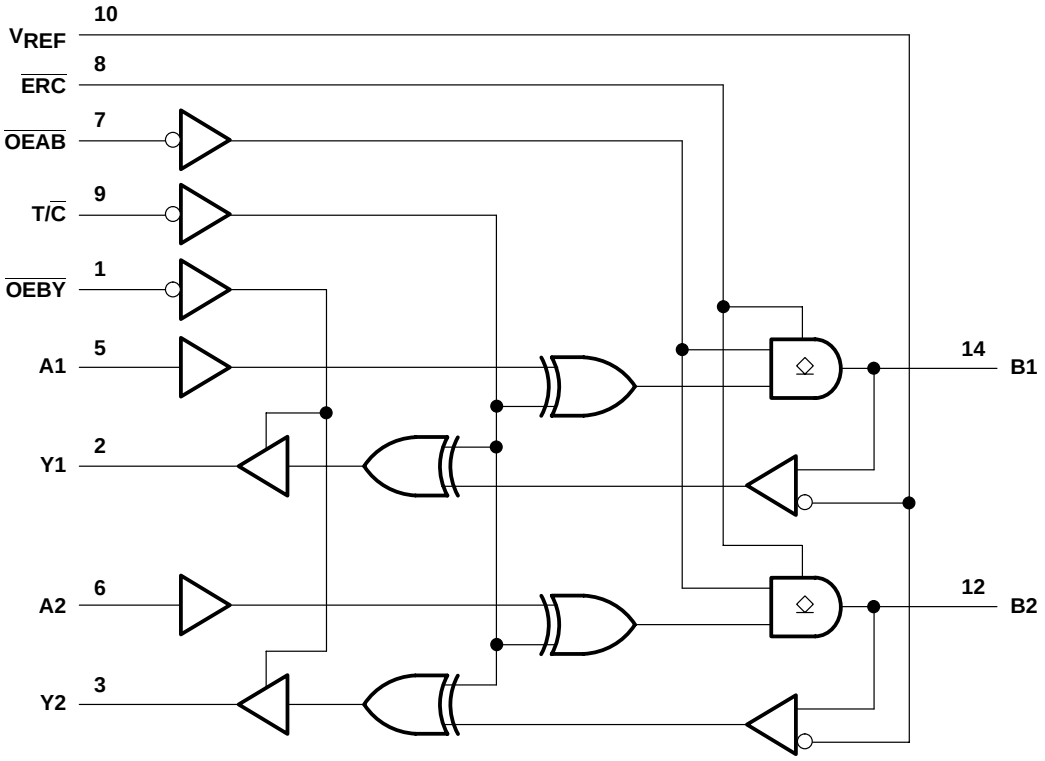
OUTPUT CONTROL

INPUTS			OUTPUT	MODE
T/$\overline{C}$	$\overline{OEAB}$	$\overline{OEBY}$		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True transparent
H	H	L	B data to Y bus	
H	L	L	A data to B bus, B data to Y bus	True transparent with feedback path
L	L	H	Inverted A data to B bus	Inverted transparent
L	H	L	Inverted B data to Y bus	
L	L	L	Inverted A data to B bus, Inverted B data to Y bus	Inverted transparent with feedback path

OUTPUT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A inputs, $\overline{ERC}$, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): Y outputs	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: Y outputs	48 mA
B port	200 mA
Current into any output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DGV package	120°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Y outputs			–24	mA
I_{OL}	Low-level output current	Y outputs			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 to 5.5 V			±10	µA
I_{OZH}‡	Y outputs	V_{CC} = 3.45 V	$V_O = V_{CC}$			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	Y outputs and B port	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{CC}	Y outputs and B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}§		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	A-port inputs	V_I = 3.15 V or 0			3.5	4.5	pF
	Control inputs				4	5	
C_o	Y outputs	V_O = 3.15 V or 0			4.5	5	pF
C_{io}	B port	V_O = 1.5 V or 0			9	10.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A inputs and Y outputs over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

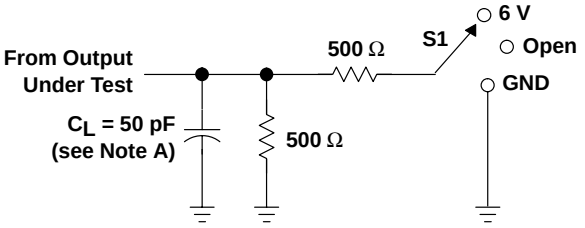
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	A	B	Slow	3.3		5.9	ns
t_{PHL}				3		6.6	
t_{PLH}	A	B	Fast	2.5		5.2	ns
t_{PHL}				1.9		4.8	
t_{PLH}	A	Y	Slow	5.4		9	ns
t_{PHL}				4.9		8.6	
t_{PLH}	A	Y	Fast	4.3		7.9	ns
t_{PHL}				3.9		7.5	
t_{PLH}	T/$\overline{C}$	B	Slow	3		6.5	ns
t_{PHL}				3.1		6.6	
t_{PLH}	T/$\overline{C}$	B	Fast	2.3		5.6	ns
t_{PHL}				1.7		4.9	
t_{en}	$\overline{OEAB}$	B	Slow	3.2		6.2	ns
t_{dis}				3.2		6.4	
t_{en}	$\overline{OEAB}$	B	Fast	1.9		5.3	ns
t_{dis}				2.4		5.7	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.7		ns
			Fast		1.5		
t_f	Fall time, B outputs (80% to 20%)		Slow		3.2		ns
			Fast		2.1		
t_{PLH}	B	Y	–	1.6		4.6	ns
t_{PHL}				1.4		3.9	
t_{PLH}	T/$\overline{C}$	Y	–	1		4.5	ns
t_{PHL}				1.2		4.1	
t_{en}	$\overline{OEBY}$	Y	–	1		4.1	ns
t_{dis}				1.3		4.6	

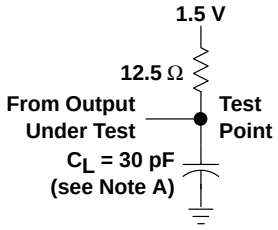
† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

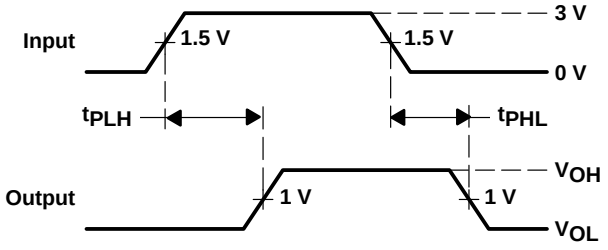


LOAD CIRCUIT FOR Y OUTPUTS

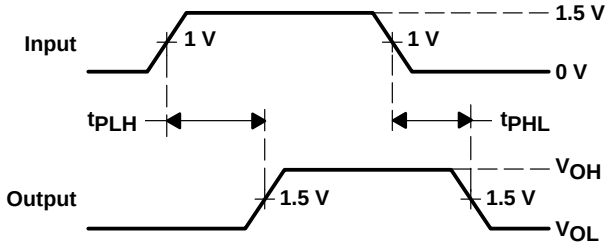
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



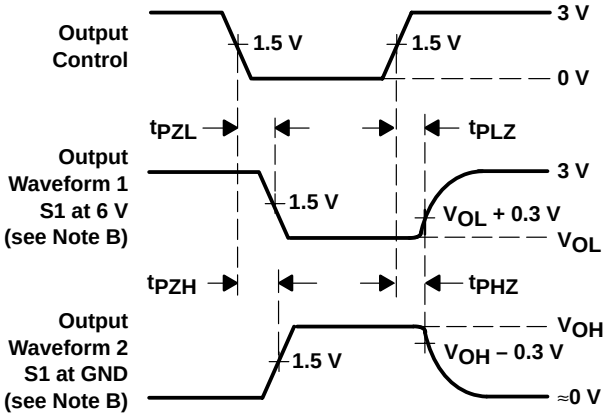
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A input to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to Y output)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A input)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

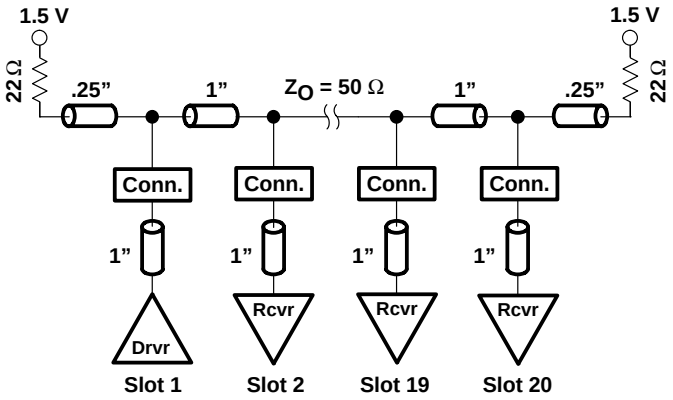


Figure 2. High-Drive Test Backplane

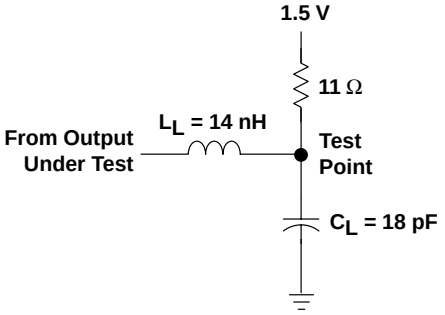


Figure 3. High-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	4.2	ns
t_{PHL}				4.2	
t_{PLH}	A	B	Fast	3.6	ns
t_{PHL}				3.6	
t_{PLH}	A	Y	Slow	5.8	ns
t_{PHL}				5.8	
t_{PLH}	A	Y	Fast	5.2	ns
t_{PHL}				5.2	
t_{PLH}	T/C	B	Slow	4.4	ns
t_{PHL}				4.4	
t_{PLH}	T/C	B	Fast	3.8	ns
t_{PHL}				3.8	
t_{en}	$\overline{OEAB}$	B	Slow	4.2	ns
t_{dis}				4.3	
t_{en}	$\overline{OEAB}$	B	Fast	3.6	ns
t_{dis}				3.3	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

APPLICATION INFORMATION

operational description

The GTLP1394 is specifically designed for use with the Texas Instruments 1394 backplane layer controller family to transmit the 1394 backplane serial bus across parallel backplanes. But, it is a versatile 2-bit device that also is being used to provide multiple single-bit clocks or ATM read and write clock in multislot parallel backplane applications.

The 1394–1995 is an IEEE designation for a high-performance serial bus. This serial bus defines both a backplane (e.g., GTLP, VME, FB+, CPCI, etc.) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 25, 50, or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol. The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The primary application of the backplane version is to provide a robust control interface to each daughter card. The 1394 standard also provides new services such as real-time I/O and live connect/disconnect capability for external devices.

electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as ten bits for bus ID, six bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, with each having up to 63 nodes, each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes can physically reside in a single module, and multiple ports can reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. A maximum of 63 nodes can be connected to one network.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data bit-period, essentially doubling the jitter tolerance with very little additional circuitry overhead in the hardware.

APPLICATION INFORMATION

protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction-layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 µs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus. The cable environment's tree topology is resolved during a sequence of events, triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all the information has been gathered on each node, the bus goes into an idle state, waiting for the beginning of the standard arbitration process.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

backplane features

- 25-, 50-, and 100-Mbps data rates for backplane environments
- Live connection/disconnection possible without data loss or interruption.
- Configuration ROM and status registers supporting plug and play
- Multidrop or point-to-point topologies supported.
- Specified bandwidth assignments for real-time applications

applicability and typical application for IEEE 1394 backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics
  - Alternate control path to the parallel backplane bus
  - Test, maintenance, and troubleshooting
  - Software debug and support interface
- System enhancement
  - Fault tolerance
  - Live insertion
  - CSR access
  - Auxiliary 2-bit bus with a 64-bit address space to the parallel backplane bus
- Peripheral monitoring
  - Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with another externally wired monitor bus, such as defined by the Intelligent Platform Management Interface (IPMI).

The 1394 backplane physical layer (PHY) and the SN74GTLP1394 provide a cost-effective way to add high-speed 1394 connections to every daughter card in almost any backplane. More information on the backplane physical layer devices and how to implement the 1394 standard in backplane and cable applications can be found at: *www.ti.com/sc/1394.*

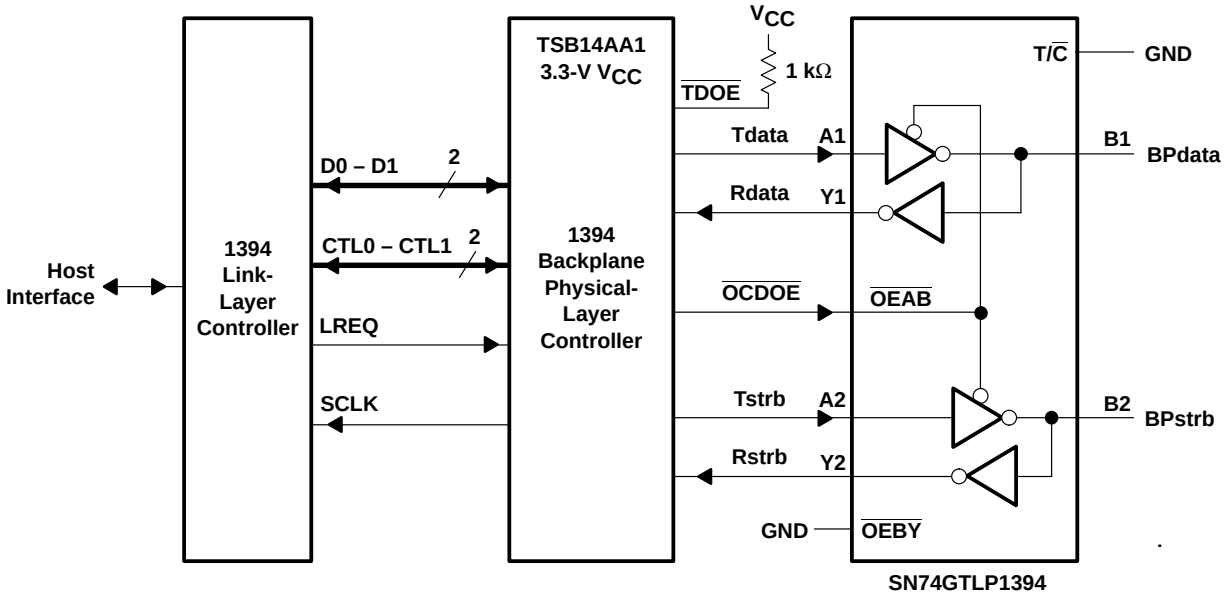
APPLICATION INFORMATION

SN74GTLP1394 interface with the TSB14AA1 1394 backplane PHY

- A1, B1, and Y1 are used for the PHY data signals.
- A2, B2, and Y2 are used for the PHY strobe signals.
- PHY N_OEB_D or $\overline{\text{OCDOE}}$ connects to $\overline{\text{OEAB}}$, which controls the PHY transmit signals.
- $\overline{\text{OEBY}}$ is connected to GND since the transceiver always must be able to receive signals from the backplane and relay them to the PHY.
- T/$\overline{\text{C}}$ is connected to GND for inverted signals.
- V_{CC} is nominal 3.3 V.
- BIAS V_{CC} is connected to nominal 3.3 V to support live insertion.
- V_{REF} normally is 2/3 of V_{TT}.
- $\overline{\text{ERC}}$ normally is connected to GND for slow edge-rate operation because frequencies of only 50 MHz (S100) and 25 MHz (S50) are required.

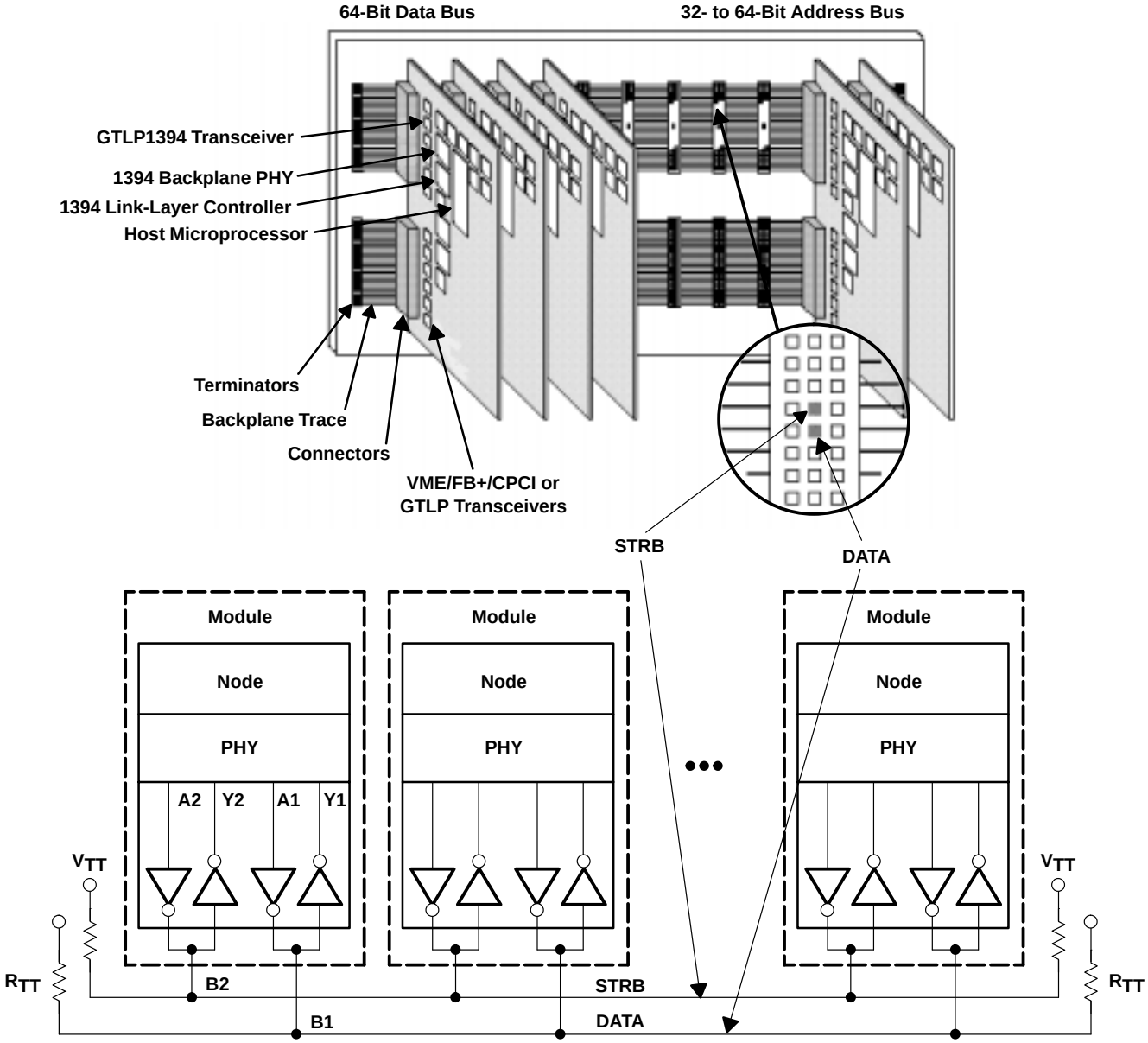
APPLICATION INFORMATION

logical representation



APPLICATION INFORMATION

physical representation

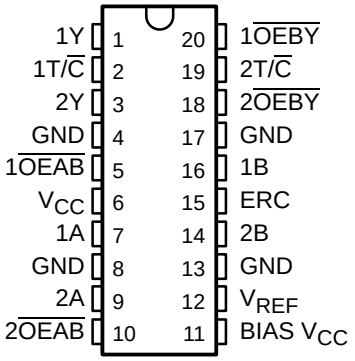


TWO 1-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE BUS TRANSCEIVERS WITH SPLIT LVTTL PORT, FEEDBACK PATH, AND SELECTABLE POLARITY

SCES349B – JUNE 2001 – REVISED AUGUST 2001

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Polarity Control Selects True or Complementary Outputs**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP1395 is two 1-bit, high-drive, 3-wire bus transceivers that provide LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation for applications, such as primary and secondary clocks, that require individual output-enable and true/complement controls. The device allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins, which provide a feedback path for control and diagnostics monitoring. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels and is designed especially to work with the Texas Instruments 3.3-V 1394 backplane physical-layer controller. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuitry minimizes bus settling time, and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes, with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP1395 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

PRODUCT PREVIEW

OEC and TI-OPC are trademarks of Texas Instruments.

PRODUCT PREVIEW

description (continued)

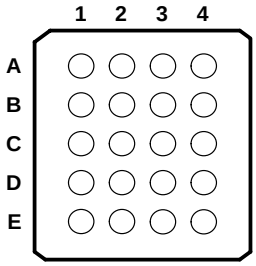
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1T/$\overline{C}$	1Y	1$\overline{OEBY}$	2T/$\overline{C}$
B	GND	GND	2Y	2$\overline{OEBY}$
C	V_{CC}	1$\overline{OEAB}$	ERC	1B
D	GNE	GND	1A	2B
E	2$\overline{OEAB}$	2A	BIAS V_{CC}	V_{REF}

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP1395DW	GTLP1395
		Tape and reel	SN74GTLP1395DWR	
	TSSOP – PW	Tape and reel	SN74GTLP1395PWR	GP395
	TVSOP – DGV	Tape and reel	SN74GTLP1395DGVR	GP395
	VFBGA – GQN	Tape and reel	SN74GTLP1395GQNR	GP395

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The output-enable (1$\overline{OEAB}$, 1$\overline{OEBY}$) and polarity-control (1T/$\overline{C}$) inputs control 1A, 1B, and 1Y. 2$\overline{OEAB}$, 2$\overline{OEBY}$, and 2T/$\overline{C}$ control 2A, 2B, and 2Y.

$\overline{OEAB}$ controls the activity of the B port. When $\overline{OEAB}$ is low, the B-port output is active. When $\overline{OEAB}$ is high, the B-port output is disabled.

A separate LVTTL A input and Y output provide a feedback path for control and diagnostics monitoring. $\overline{OEBY}$ controls the Y output. When $\overline{OEBY}$ is low, the Y output is active. When $\overline{OEBY}$ is high, the Y output is disabled.

T/$\overline{C}$ selects polarity of data transmission in both directions. When T/$\overline{C}$ is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/$\overline{C}$ is low, data transmission is complementary, and inverted A data goes to the B bus and inverted B data goes to the Y bus.

Function Tables

OUTPUT CONTROL

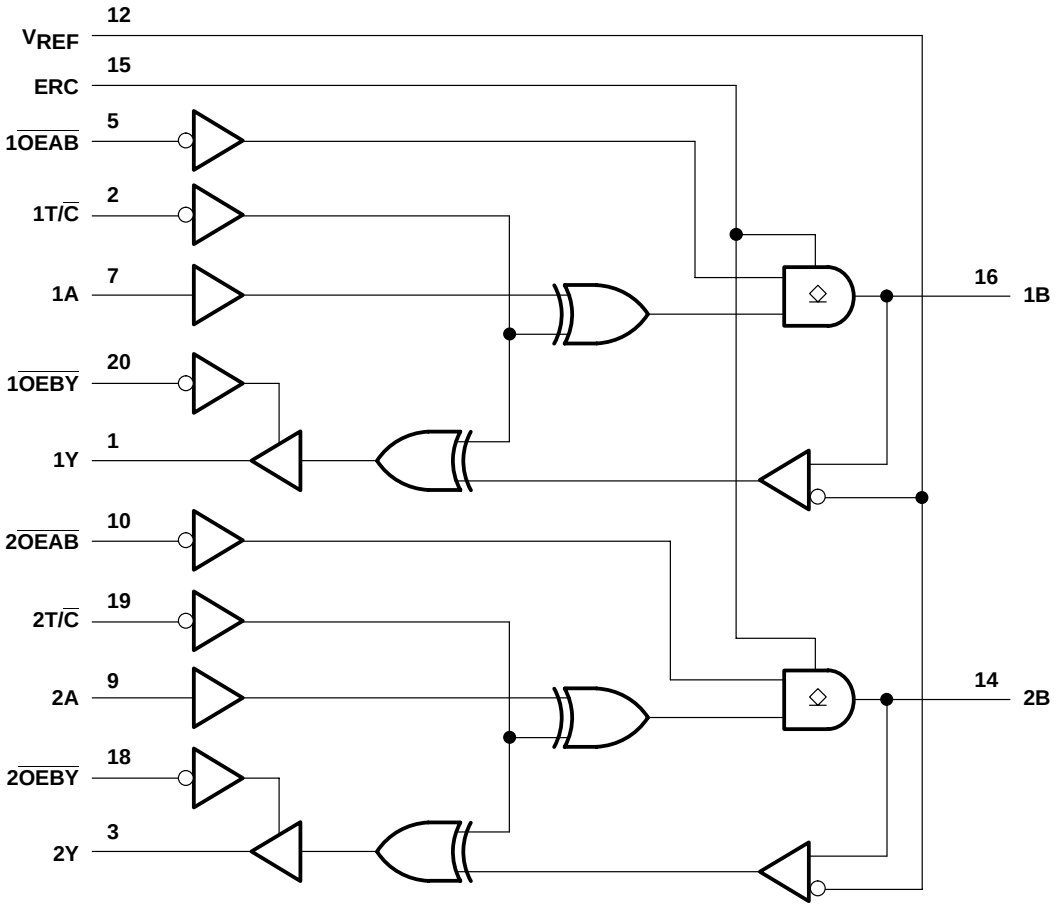
INPUTS			OUTPUT	MODE
T/$\overline{C}$	$\overline{OEAB}$	$\overline{OEBY}$		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True transparent
H	H	L	B data to Y bus	
H	L	L	A data to B bus, B data to Y bus	True transparent with feedback path
L	L	H	Inverted A data to B bus	Inverted transparent
L	H	L	Inverted B data to Y bus	
L	L	L	Inverted A data to B bus, Inverted B data to Y bus	Inverted transparent with feedback path

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC LOGIC LEVEL	OUTPUT B-PORT EDGE RATE
H	Slow
L	Fast

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for the DGV, DW, and PW packages.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A inputs, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): Y outputs	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: Y outputs	48 mA
B port	200 mA
Current into any output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	92°C/W
DW package	58°C/W
GQN package	28°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

PRODUCT PREVIEW

PRODUCT PREVIEW

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			V
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Y outputs			–24	mA
I_{OL}	Low-level output current	Y outputs			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally it is two-thirds V_{TT}. TI-OPC is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V,	V_I = 0 to 5.5 V			±10	µA
I_{OZ}‡	Y outputs	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	Y outputs or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}§		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	A-port inputs	V_I = 3.15 V or 0					pF
	Control inputs						
C_o	Y outputs	V_O = 3.15 V or 0					pF
C_{io}	B port	V_O = 1.5 V or 0					pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

hot-insertion specifications for A inputs and Y outputs over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS				MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V			5	mA
	V_{CC} = 3.15 V to 3.45 V					10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0		0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V		–1		µA

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	A	B	Slow				ns
t_{PHL}							
t_{PLH}	A	B	Fast				ns
t_{PHL}							
t_{PLH}	A	Y	Slow				ns
t_{PHL}							
t_{PLH}	A	Y	Fast				ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	B	Slow				ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	B	Fast				ns
t_{PHL}							
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (20% to 80%)		Slow				ns
			Fast				
t_f	Fall time, B outputs (80% to 20%)		Slow				ns
			Fast				
t_{PLH}	B	Y					ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	Y					ns
t_{PHL}							
t_{en}	$\overline{OEBY}$	Y					ns
t_{dis}							

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

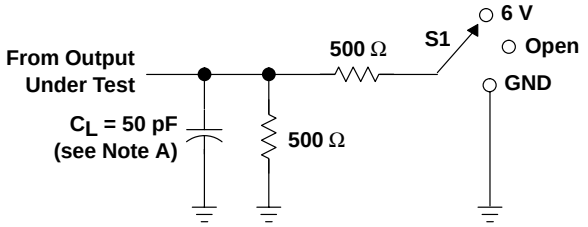
skew characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V, standard lumped loads (C_L = 30 pF for B port and C_L = 50 pF for Y port) (unless otherwise noted)(see Figure 1)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE‡	MIN	TYP§	MAX	UNIT
$t_{sk(LH)}$¶	A	B	Slow				ns
$t_{sk(HL)}$¶							
$t_{sk(LH)}$¶	A	B	Fast				ns
$t_{sk(HL)}$¶							
$t_{sk(LH)}$¶	B	Y					ns
$t_{sk(HL)}$¶							
$t_{sk(t)}$¶	A	B	Slow				ns
			Fast				ns
	B	Y					ns
$t_{sk(prLH)}$#	A	B	Slow				ns
$t_{sk(prHL)}$#							
$t_{sk(prLH)}$#	A	B	Fast				ns
$t_{sk(prHL)}$#							
$t_{sk(prLH)}$#	B	Y					ns
$t_{sk(prHL)}$#							

† Actual skew values between GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
‡ Slow (ERC = L) and Fast (ERC = H)
§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].
# $t_{sk(prLH)}$/$t_{sk(prHL)}$ – The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages and at the same temperature, and have identical package types, identical specified loads, and identical logic functions. Furthermore, these values are provided by SPICE simulations.

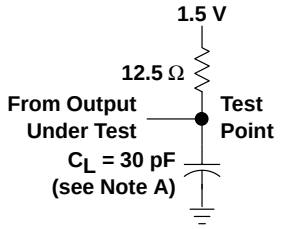
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

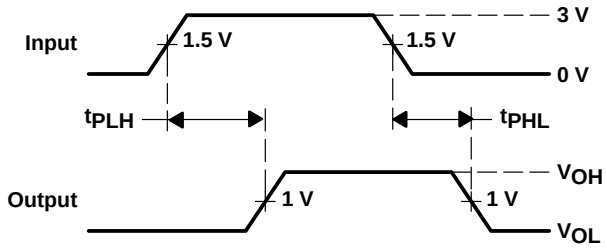


LOAD CIRCUIT FOR Y OUTPUTS

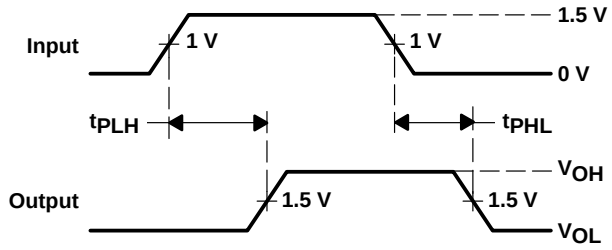
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



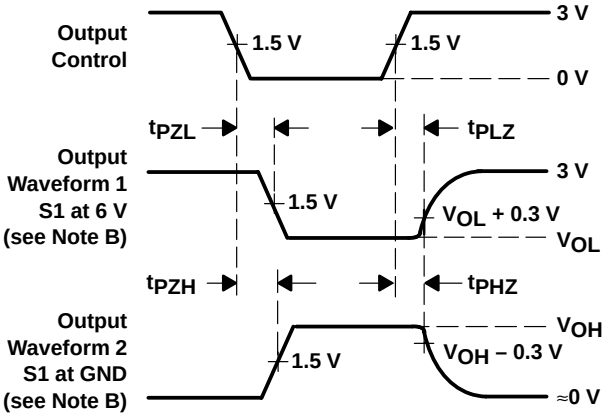
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A input to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to Y output)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A input)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in the backplane. See www.ti.com/sc/gtlp for more information.

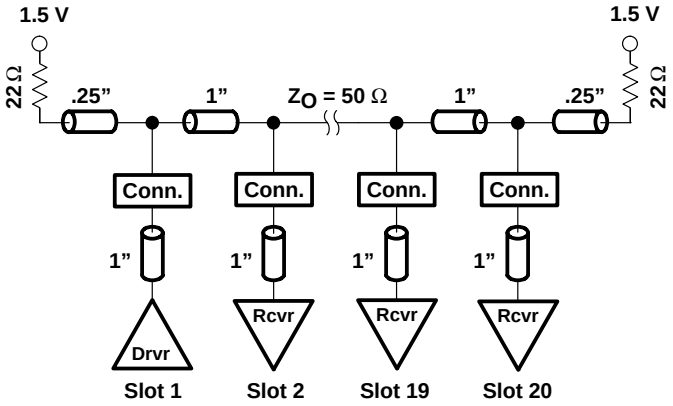


Figure 2. High-Drive Test Backplane

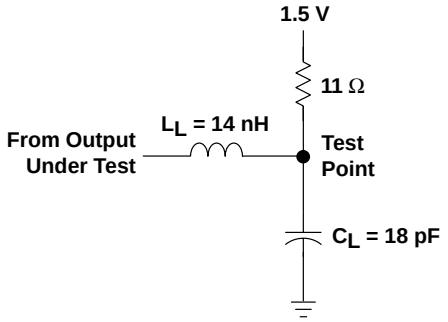


Figure 3. High-Drive RLC Network

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow		ns
t_{PHL}					
t_{PLH}	A	B	Fast		ns
t_{PHL}					
t_{PLH}	A	Y	Slow		ns
t_{PHL}					
t_{PLH}	A	Y	Fast		ns
t_{PHL}					
t_r	Rise time, B outputs (20% to 80%)		Slow		ns
			Fast		
t_f	Fall time, B outputs (80% to 20%)		Slow		ns
			Fast		

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.

PRODUCT PREVIEW

APPLICATION INFORMATION

operational description

The GTLP1395 is designed specifically for use with the TI 1394 backplane layer controller family to transmit the 1394 backplane serial bus across parallel backplanes. But, it is a versatile two 1-bit device that also can provide multiple 1-bit clocks or an ATM read and write clock in multislot parallel backplane applications.

The 1394–1995 is an IEEE designation for a high-performance serial bus. This serial bus defines both a backplane (e.g., GTLP, VME, FB+, CPCI, etc.) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 25, 50, or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol. The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The primary application of the backplane version is to provide a robust control interface to each daughter card. The 1394 standard also provides new services such as real-time I/O and live connect/disconnect capability for external devices.

electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, each having up to 63 nodes and each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes can reside physically in a single module, and multiple ports can reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. A maximum of 63 nodes can be connected to one network.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data bit period, essentially doubling the jitter tolerance with very little additional circuitry overhead in the hardware.

APPLICATION INFORMATION

protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 µs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus. The cable environment's tree topology is resolved during a sequence of events, triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all the information has been gathered on each node, the bus goes into an idle state, waiting for the beginning of the standard arbitration process.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus-state determination, bus-access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

backplane features

- 25-, 50-, and 100-Mbps data rates for backplane environments
- Live connection/disconnection possible without data loss or interruption
- Configuration ROM and status registers supporting plug and play
- Multidrop or point-to-point topologies supported.
- Specified bandwidth assignments for real-time applications

applicability and typical application for IEEE 1394 backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics
  - Alternate control path to the parallel backplane bus
  - Test, maintenance, and troubleshooting
  - Software debug and support interface
- System enhancement
  - Fault tolerance
  - Live insertion
  - CSR access
  - Auxiliary 2-bit bus with a 64-bit address space to the parallel backplane bus
- Peripheral monitoring
  - Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with another externally wired monitor bus, such as defined by the Intelligent Platform Management Interface (IPMI)

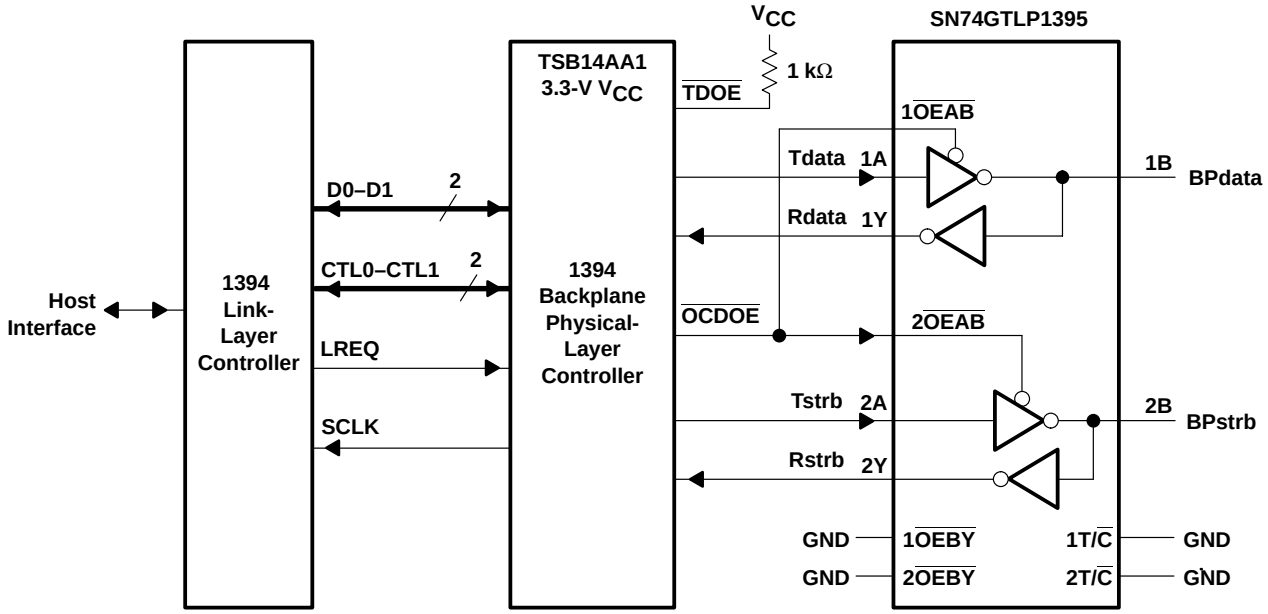
The 1394 backplane physical layer (PHY) and the SN74GTLP1395 provide a cost-effective way to add high-speed 1394 connections to every daughter card in almost any backplane. More information on the backplane PHY devices and how to implement the 1394 standard in backplane and cable applications can be found at www.ti.com/sc/1394.

APPLICATION INFORMATION

SN74GTLP1395 interface with the TSB14AA1 1394 backplane PHY

- 1A, 1B, and 1Y are used for the PHY data signals.
- 2A, 2B, and 2Y are used for the PHY strobe signals.
- PHY N_OEB_D or $\overline{\text{OCDOE}}$ connects to 1$\overline{\text{OEAB}}$ and 2$\overline{\text{OEAB}}$, which control the PHY transmit signals.
- 1$\overline{\text{OEBY}}$ and 2$\overline{\text{OEBY}}$ are connected to GND because the transceiver must always be able to receive signals from the backplane and relay them to the PHY.
- 1T/$\overline{\text{C}}$ and 2T/$\overline{\text{C}}$ are connected to GND for inverted signals.
- V_{CC} is nominal 3.3 V.
- BIAS V_{CC} is connected to nominal 3.3 V to support live insertion.
- V_{REF} is normally 2/3 of V_{TT}.
- ERC is normally connected to V_{CC} for slow edge-rate operation because frequencies of only 50 MHz (S100) and 25 MHz (S50) are required.

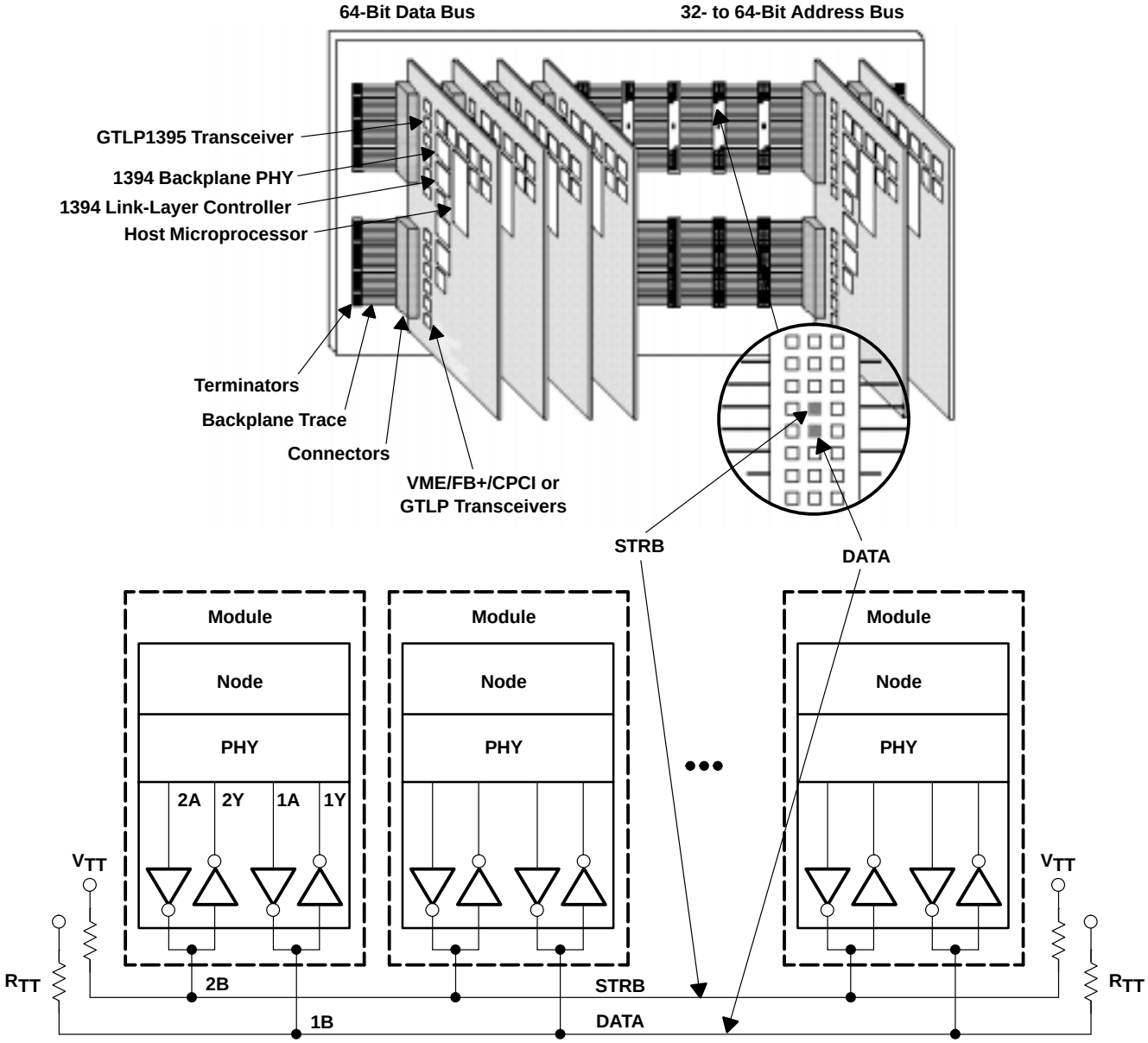
logical representation



PRODUCT PREVIEW

APPLICATION INFORMATION

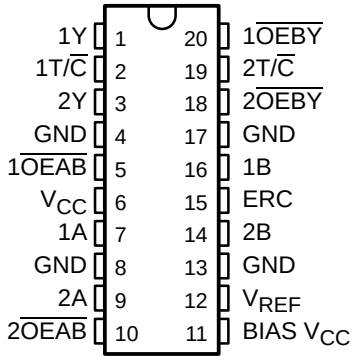
physical representation



PRODUCT PREVIEW

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **Y Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Polarity Control Selects True or Complementary Outputs**

DGV, DW, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP21395 is two 1-bit, high-drive, 3-wire bus transceivers that provide LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation for applications, such as primary and secondary clocks, that require individual output-enable and true/complement controls. The device allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins, which provide a feedback path for control and diagnostics monitoring. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels and is designed especially to work with the Texas Instruments 3.3-V 1394 backplane physical-layer controller. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuitry minimizes bus settling time, and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes, with equivalent load impedance down to 11 Ω.

The Y outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP21395 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

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PRODUCT PREVIEW

description (continued)

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

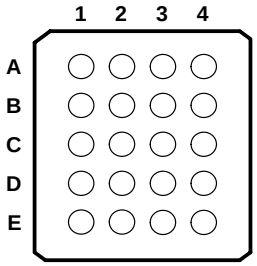
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1T/$\overline{C}$	1Y	1$\overline{OEBY}$	2T/$\overline{C}$
B	GND	GND	2Y	2$\overline{OEBY}$
C	V_{CC}	1$\overline{OEAB}$	ERC	1B
D	GND	GND	1A	2B
E	2$\overline{OEAB}$	2A	BIAS V_{CC}	V_{REF}

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLP21395DW	GTLP21395
		Tape and reel	SN74GTLP21395DWR	
	TSSOP – PW	Tape and reel	SN74GTLP21395PWR	
	TVSOP – DGV	Tape and reel	SN74GTLP21395DGVR	
	VFBGA – GQN	Tape and reel	SN74GTLP21395GQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The output-enable (1$\overline{OEAB}$, 1$\overline{OEBY}$) and polarity-control (1T/$\overline{C}$) inputs control 1A, 1B, and 1Y. 2$\overline{OEAB}$, 2$\overline{OEBY}$, and 2T/$\overline{C}$ control 2A, 2B, and 2Y.

$\overline{OEAB}$ controls the activity of the B port. When $\overline{OEAB}$ is low, the B-port output is active. When $\overline{OEAB}$ is high, the B-port output is disabled.

A separate LVTTL A input and Y output provide a feedback path for control and diagnostics monitoring. $\overline{OEBY}$ controls the Y output. When $\overline{OEBY}$ is low, the Y output is active. When $\overline{OEBY}$ is high, the Y output is disabled.

T/$\overline{C}$ selects polarity of data transmission in both directions. When T/$\overline{C}$ is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/$\overline{C}$ is low, data transmission is complementary, and inverted A data goes to the B bus and inverted B data goes to the Y bus.

Function Tables

OUTPUT CONTROL

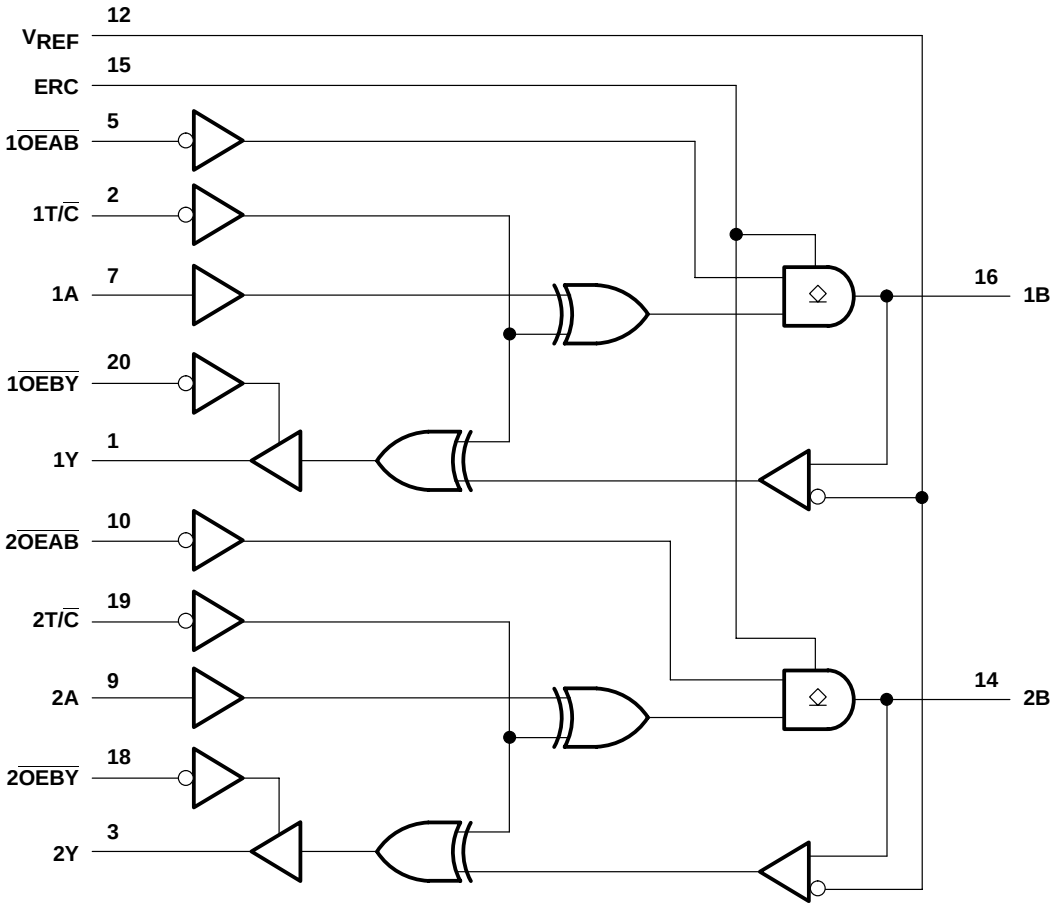
INPUTS			OUTPUT	MODE
T/$\overline{C}$	$\overline{OEAB}$	$\overline{OEBY}$		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True transparent
H	H	L	B data to Y bus	
H	L	L	A data to B bus, B data to Y bus	True transparent with feedback path
L	L	H	Inverted A data to B bus	Inverted transparent
L	H	L	Inverted B data to Y bus	
L	L	L	Inverted A data to B bus, Inverted B data to Y bus	Inverted transparent with feedback path

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC LOGIC LEVEL	OUTPUT B-PORT EDGE RATE
H	Slow
L	Fast

PRODUCT PREVIEW

logic diagram (positive logic)



Pin numbers shown are for DGV, DW, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A inputs, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): Y outputs	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: Y outputs	24 mA
B port	200 mA
Current into any output in the high state, I_O (see Note 2)	24 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGV package	92°C/W
DW package	58°C/W
GQN package	28°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			V
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Y outputs			–12	mA
I_{OL}	Low-level output current	Y outputs			12	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally it is two-thirds V_{TT}. TI-OPC is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2			
V_{OL}	Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA			0.8	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V,	V_I = 0 to 5.5 V			±10	µA
I_{OZ}‡	Y outputs	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	Y outputs or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}§		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	A-port inputs	V_I = 3.15 V or 0					pF
	Control inputs						
C_o	Y outputs	V_O = 3.15 V or 0					pF
C_{io}	B port	V_O = 1.5 V or 0					pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

hot-insertion specifications for A inputs and Y outputs over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OEBY}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS				MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V,	$\overline{OEAB}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V			5	mA
	V_{CC} = 3.15 V to 3.45 V					10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0		0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V		–1		µA

PRODUCT PREVIEW

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	A	B	Slow				ns
t_{PHL}							
t_{PLH}	A	B	Fast				ns
t_{PHL}							
t_{PLH}	A	Y	Slow				ns
t_{PHL}							
t_{PLH}	A	Y	Fast				ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	B	Slow				ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	B	Fast				ns
t_{PHL}							
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (20% to 80%)		Slow				ns
			Fast				
t_f	Fall time, B outputs (80% to 20%)		Slow				ns
			Fast				
t_{PLH}	B	Y					ns
t_{PHL}							
t_{PLH}	$T/\overline{C}$	Y					ns
t_{PHL}							
t_{en}	$\overline{OEBY}$	Y					ns
t_{dis}							

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

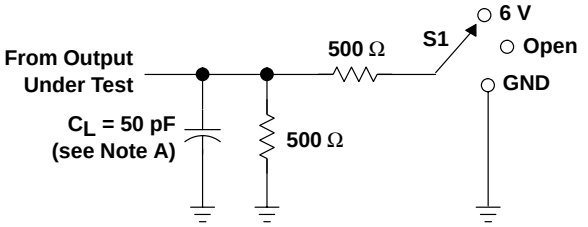
skew characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V, standard lumped loads (C_L = 30 pF for B port and C_L = 50 pF for Y port) (unless otherwise noted)(see Figure 1)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE‡	MIN	TYP§	MAX	UNIT
$t_{sk(LH)}$¶	A	B	Slow				ns
$t_{sk(HL)}$¶							
$t_{sk(LH)}$¶	A	B	Fast				ns
$t_{sk(HL)}$¶							
$t_{sk(LH)}$¶	B	Y					ns
$t_{sk(HL)}$¶							
$t_{sk(t)}$¶	A	B	Slow				ns
			Fast				ns
	B	Y					ns
$t_{sk(prLH)}$#	A	B	Slow				ns
$t_{sk(prHL)}$#							
$t_{sk(prLH)}$#	A	B	Fast				ns
$t_{sk(prHL)}$#							
$t_{sk(prLH)}$#	B	Y					ns
$t_{sk(prHL)}$#							

† Actual skew values between GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
‡ Slow (ERC = L) and Fast (ERC = H)
§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].
# $t_{sk(prLH)}$/$t_{sk(prHL)}$ – The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages and at the same temperature, and have identical package types, identical specified loads, and identical logic functions. Furthermore, these values are provided by SPICE simulations.

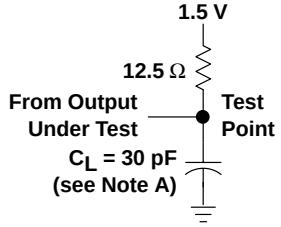
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

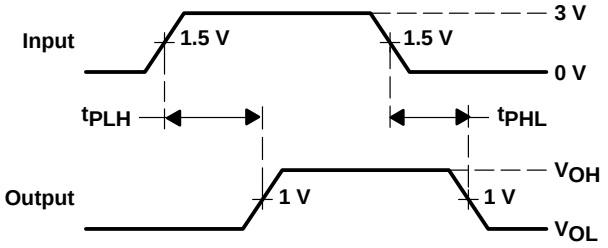


LOAD CIRCUIT FOR Y OUTPUTS

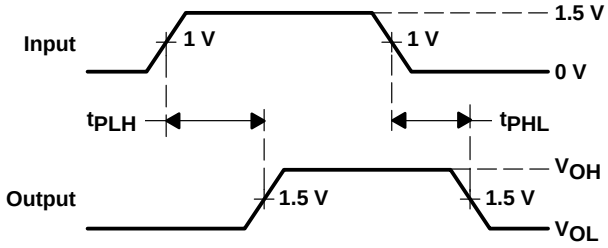
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



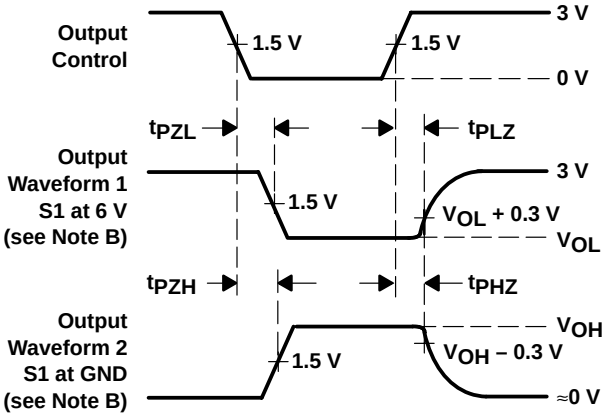
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A input to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to Y output)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A input)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in the backplane. See www.ti.com/sc/gtlp for more information.

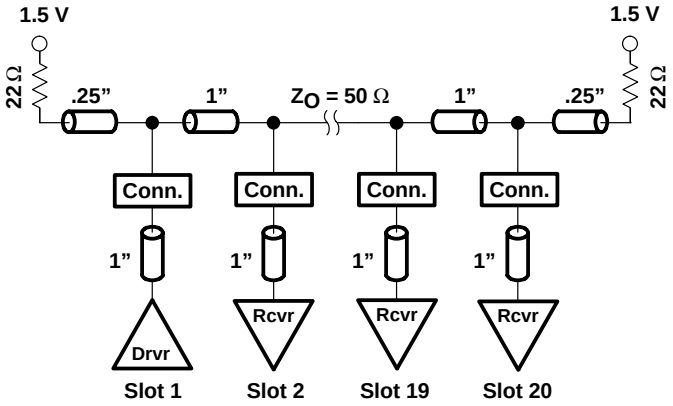


Figure 2. High-Drive Test Backplane

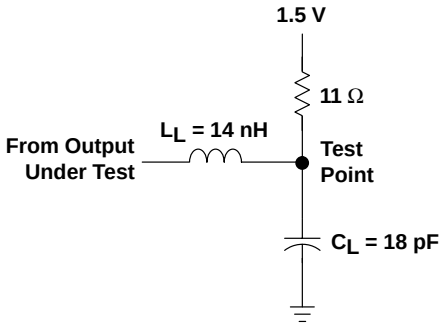


Figure 3. High-Drive RLC Network

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow		ns
t_{PHL}					
t_{PLH}	A	B	Fast		ns
t_{PHL}					
t_{PLH}	A	Y	Slow		ns
t_{PHL}					
t_{PLH}	A	Y	Fast		ns
t_{PHL}					
t_r	Rise time, B outputs (20% to 80%)		Slow		ns
			Fast		
t_f	Fall time, B outputs (80% to 20%)		Slow		ns
			Fast		

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

PRODUCT PREVIEW

APPLICATION INFORMATION

operational description

The GTLP21395 is designed specifically for use with the TI 1394 backplane layer controller family to transmit the 1394 backplane serial bus across parallel backplanes. But, it is a versatile two 1-bit device that also can provide multiple 1-bit clocks or an ATM read and write clock in multislot parallel backplane applications.

The 1394–1995 is an IEEE designation for a high-performance serial bus. This serial bus defines both a backplane (e.g., GTLP, VME, FB+, CPCI, etc.) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 25, 50, or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol. The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The primary application of the backplane version is to provide a robust control interface to each daughter card. The 1394 standard also provides new services such as real-time I/O and live connect/disconnect capability for external devices.

electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, each having up to 63 nodes and each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes can reside physically in a single module, and multiple ports can reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. A maximum of 63 nodes can be connected to one network.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data-bit period, essentially doubling the jitter tolerance with very little additional circuitry overhead in the hardware.

APPLICATION INFORMATION

protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 µs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus. The cable environment's tree topology is resolved during a sequence of events, triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all the information has been gathered on each node, the bus goes into an idle state, waiting for the beginning of the standard arbitration process.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus-state determination, bus-access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

backplane features

- 25-, 50-, and 100-Mbps data rates for backplane environments
- Live connection/disconnection possible without data loss or interruption
- Configuration ROM and status registers supporting plug and play
- Multidrop or point-to-point topologies supported.
- Specified bandwidth assignments for real-time applications

applicability and typical application for IEEE 1394 backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics
  - Alternate control path to the parallel backplane bus
  - Test, maintenance, and troubleshooting
  - Software debug and support interface
- System enhancement
  - Fault tolerance
  - Live insertion
  - CSR access
  - Auxiliary 2-bit bus with a 64-bit address space to the parallel backplane bus
- Peripheral monitoring
  - Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with another externally wired monitor bus, such as defined by the Intelligent Platform Management Interface (IPMI)

The 1394 backplane physical layer (PHY) and the SN74GTLP21395 provide a cost-effective way to add high-speed 1394 connections to every daughter card in almost any backplane. More information on the backplane PHY devices and how to implement the 1394 standard in backplane and cable applications can be found at www.ti.com/sc/1394.

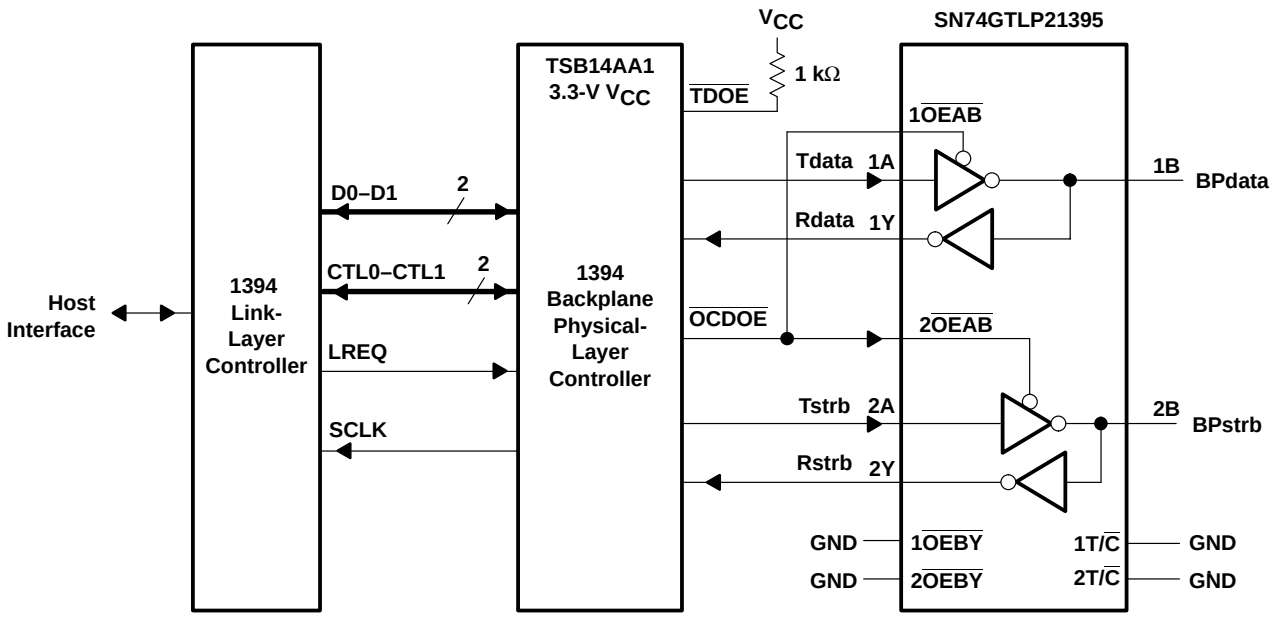
PRODUCT PREVIEW

APPLICATION INFORMATION

SN74GTLP21395 interface with the TSB14AA1 1394 backplane PHY

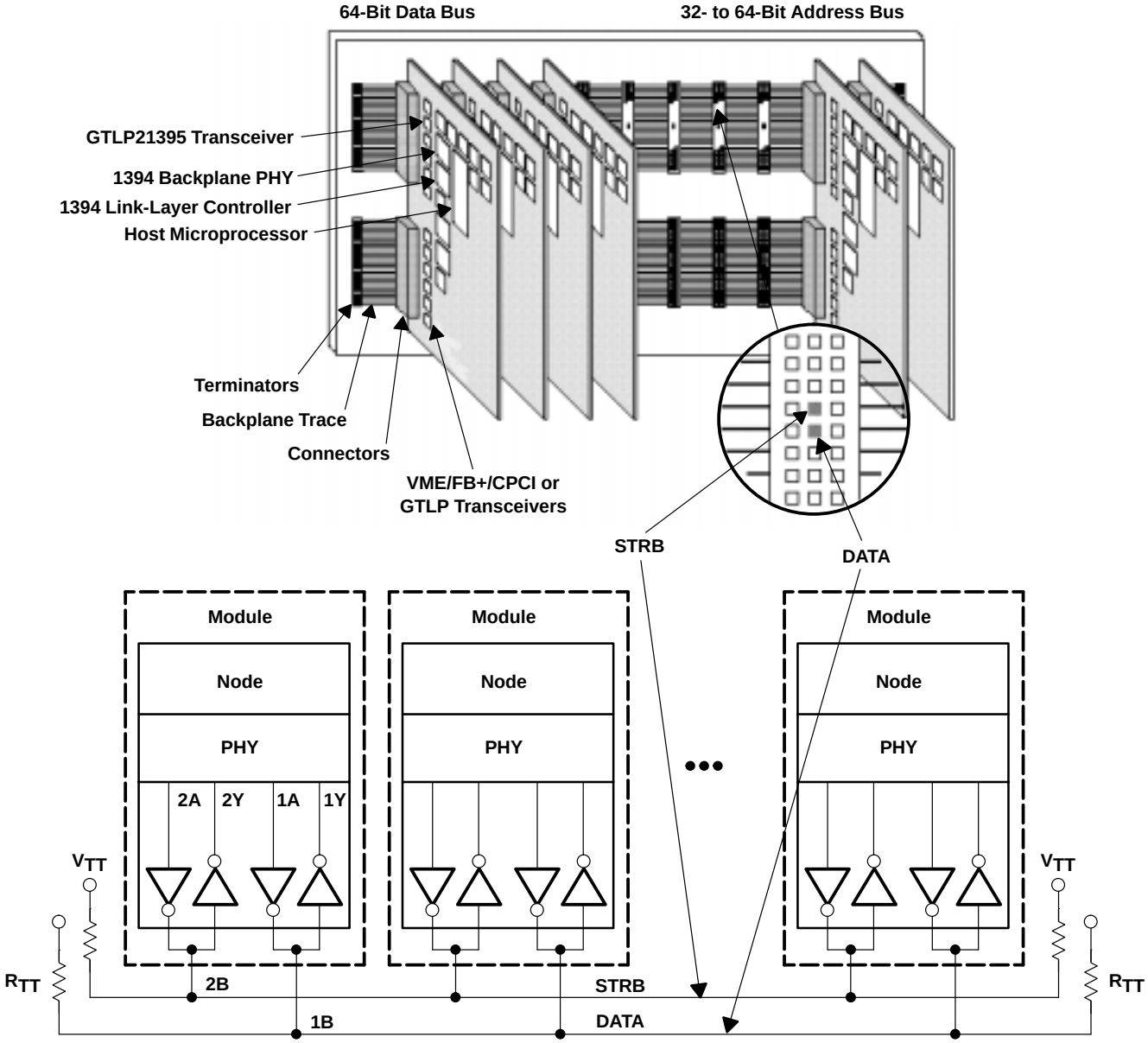
- 1A, 1B, and 1Y are used for the PHY data signals.
- 2A, 2B, and 2Y are used for the PHY strobe signals.
- PHY N_OEB_D or $\overline{\text{OCDOE}}$ connects to 1$\overline{\text{OEAB}}$ and 2$\overline{\text{OEAB}}$, which control the PHY transmit signals.
- 1$\overline{\text{OEBY}}$ and 2$\overline{\text{OEBY}}$ are connected to GND because the transceiver must always be able to receive signals from the backplane and relay them to the PHY.
- 1T/$\overline{\text{C}}$ and 2T/$\overline{\text{C}}$ are connected to GND for inverted signals.
- V_{CC} is nominal 3.3 V.
- BIAS V_{CC} is connected to nominal 3.3 V to support live insertion.
- V_{REF} is normally 2/3 of V_{TT}.
- ERC is normally connected to V_{CC} for slow edge-rate operation because frequencies of only 50 MHz (S100) and 25 MHz (S50) are required.

logical representation



APPLICATION INFORMATION

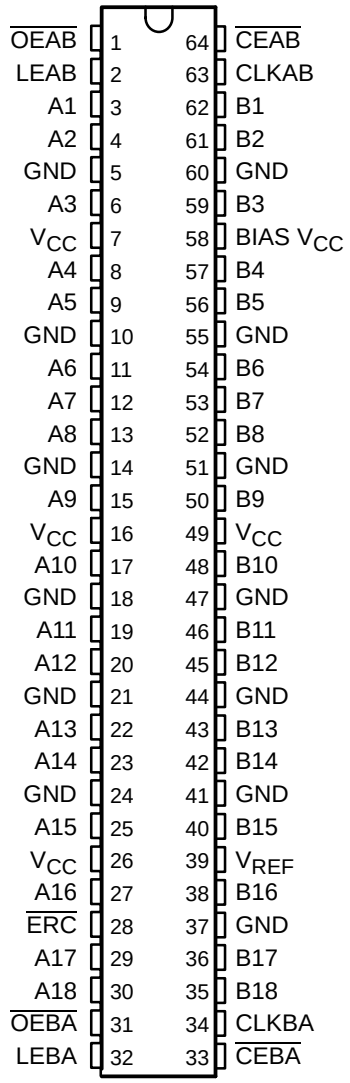
physical representation



PRODUCT PREVIEW

- **Member of the Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1612 is a high-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1612 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

OEC, TI, TI-OPC, UBT, and Widebus are trademarks of Texas Instruments.

description (continued)

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1612DGGR	GTLPH1612

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1612 is a high-drive (100 mA), 18-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1612 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH1612 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by the clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{OEAB}$ and OEBA). $\overline{CEAB}$ and $\overline{CEBA}$ and $\overline{OEAB}$ and $\overline{OEBA}$ control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{CEAB}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{CEAB}$ and LEAB are low. the A data is latched regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except that $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA are used.

Function Tables

OUTPUT ENABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

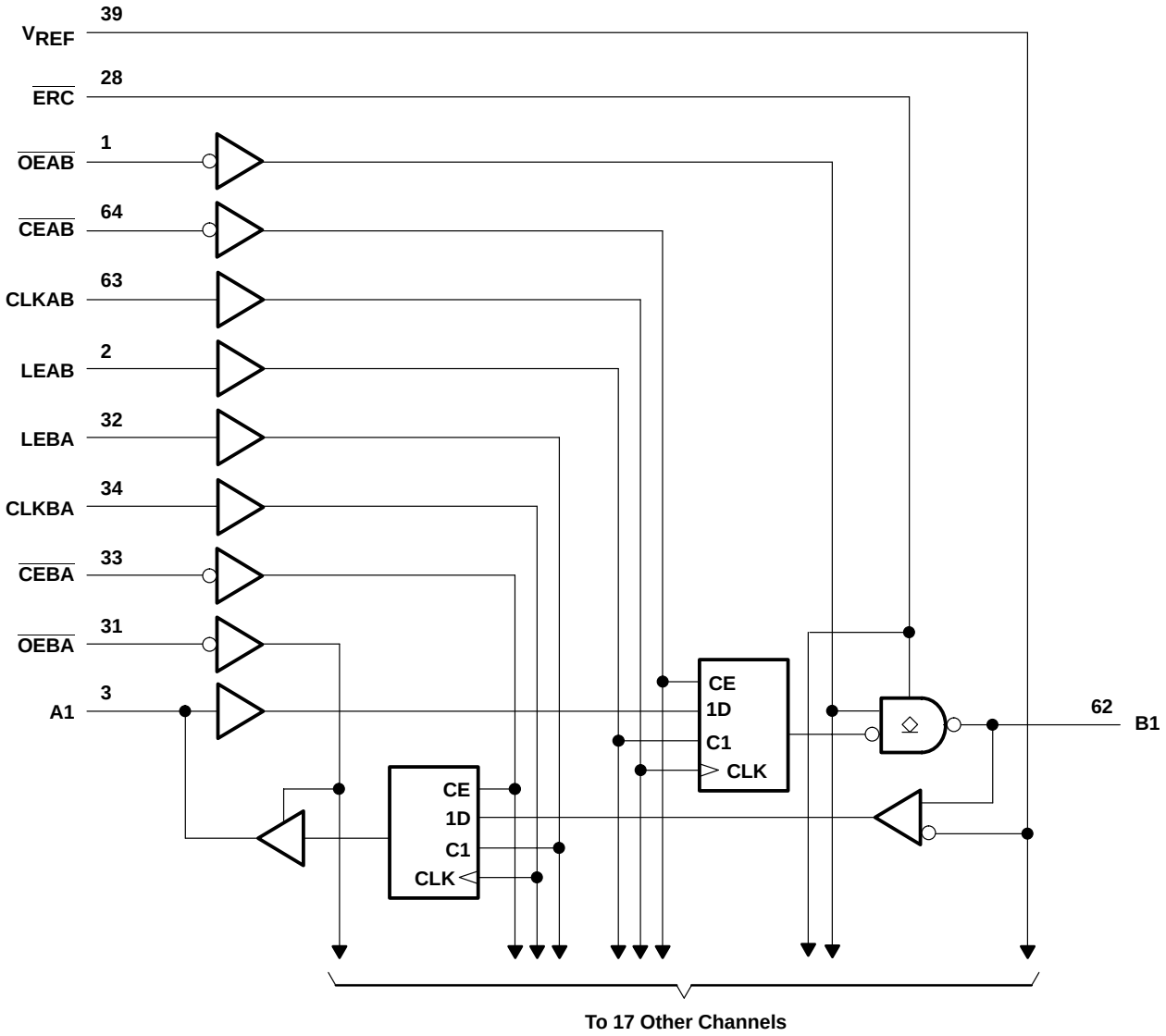
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port, $\overline{ERC}$, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	55°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	$V_O = V_{CC}$			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			45	mA
			Outputs low			45	
			Outputs disabled			45	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5.5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	8	pF
	B port	V_O = 1.5 V or 0			9.5	11.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (unless otherwise noted)

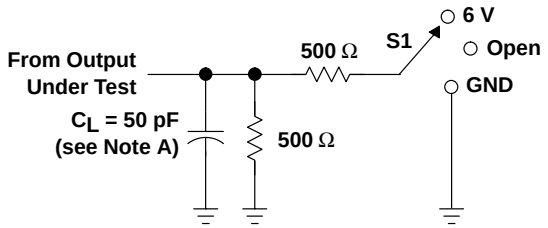
			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	3		ns
		CLKAB or CLKBA high or low	3		
t_{su}	Setup time	A before CLKAB↑	2.2		ns
		B before CLKBA↑	2.4		
		A before LEAB↓, CLK = Don't care	1.8		
		B before LEBA↓, CLK = Don't care	2.1		
		$\overline{CEAB}$ before CLKAB↑	1.5		
		$\overline{CEBA}$ before CLKBA↑	1.5		
t_h	Hold time	A after CLKAB↑	0.7		ns
		B after CLKBA↑	0.5		
		A after LEAB↓, CLK = Don't care	1.2		
		B after LEBA↓, CLK = Don't care	0.9		
		$\overline{CEAB}$ after CLKAB↑	1.5		
		$\overline{CEBA}$ after CLKBA↑	1.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (see Figure 1)

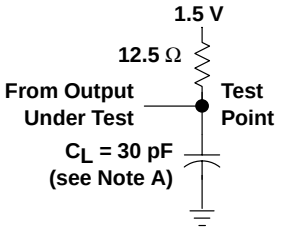
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	A	B	Slow	4.2	5.6	7.1	ns
t_{PHL}				3	4.4	6.3	
t_{PLH}	A	B	Fast	3	4.3	5.7	ns
t_{PHL}				2.6	3.8	5.3	
t_{PLH}	LEAB	B	Slow	4.6	6.1	7.7	ns
t_{PHL}				3.3	4.7	6.5	
t_{PLH}	LEAB	B	Fast	3.4	4.8	6.2	ns
t_{PHL}				3	4.2	5.7	
t_{PLH}	CLKAB	B	Slow	4.7	6.2	7.7	ns
t_{PHL}				3.2	4.7	6.4	
t_{PLH}	CLKAB	B	Fast	3.5	4.9	6.2	ns
t_{PHL}				2.9	4.2	5.6	
t_{en}	$\overline{OEAB}$	B	Slow	3	4.6	6.5	ns
t_{dis}				4.6	6	7.5	
t_{en}	$\overline{OEAB}$	B	Fast	2.7	4.1	5.6	ns
t_{dis}				3.4	4.8	6.2	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.3		
t_f	Fall time, B outputs (80% to 20%)		Slow		3.3		ns
			Fast		2.5		
t_{PLH}	B	A		1.3	2.9	4.6	ns
t_{PHL}				1.6	3	4.2	
t_{PLH}	LEBA	A		1.5	3.2	4.6	ns
t_{PHL}				1.5	3	3.9	
t_{PLH}	CLKBA	A		1.5	3.3	4.8	ns
t_{PHL}				1.5	3	4.2	
t_{en}	$\overline{OEBA}$	A		1.2	2.5	5	ns
t_{dis}				2.3	3.8	5.5	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

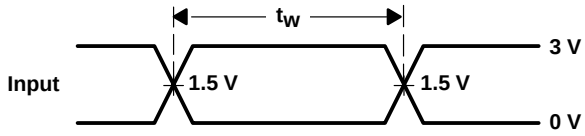


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

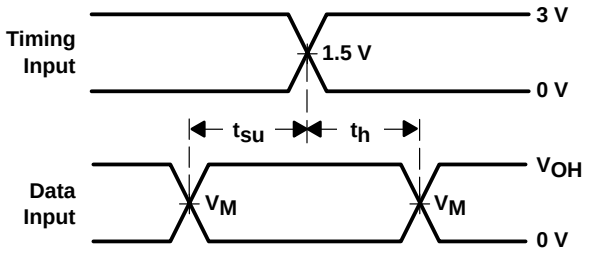


LOAD CIRCUIT FOR A OUTPUTS

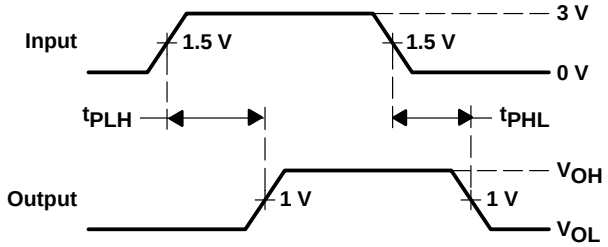
LOAD CIRCUIT FOR B OUTPUTS



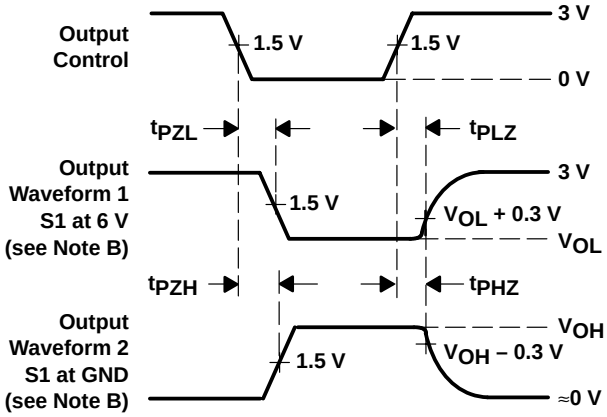
VOLTAGE WAVEFORMS
PULSE DURATION



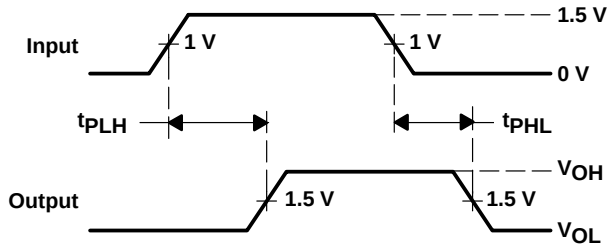
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

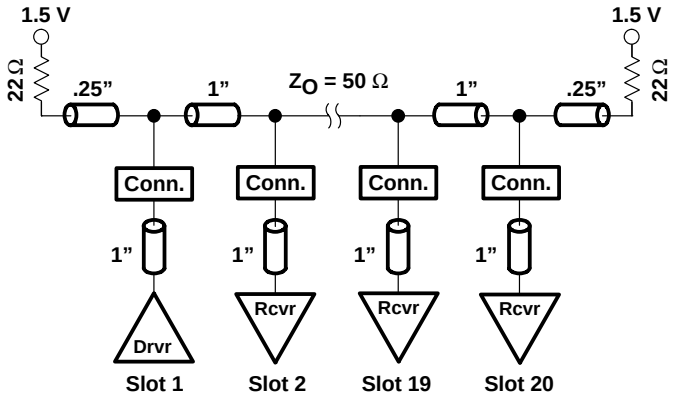


Figure 2. High-Drive Test Backplane

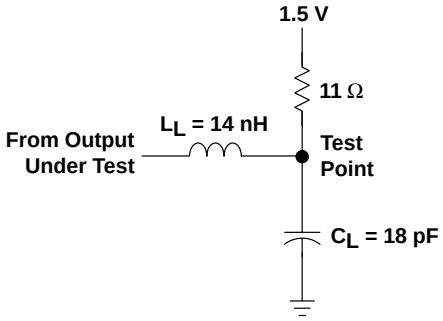


Figure 3. High-Drive RLC Network

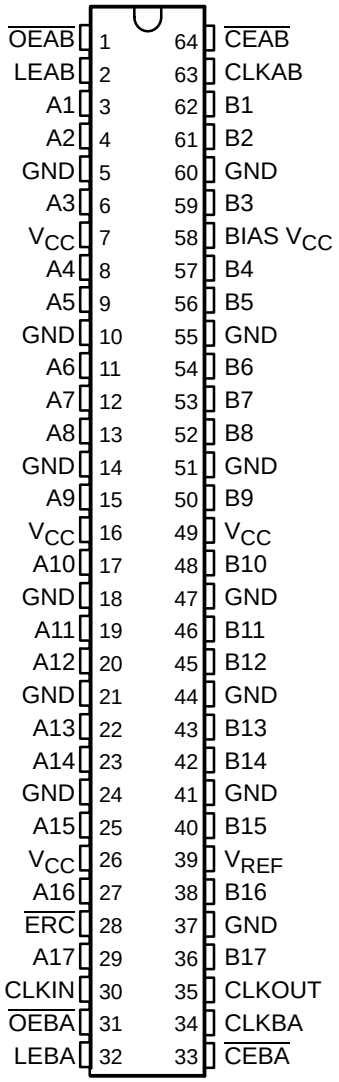
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	5.3	ns
t_{PHL}				5.3	
t_{PLH}	A	B	Fast	4	ns
t_{PHL}				4	
t_{PLH}	LEAB	B	Slow	5.2	ns
t_{PHL}				5.2	
t_{PLH}	LEAB	B	Fast	3.9	ns
t_{PHL}				3.9	
t_{PLH}	CLK	B	Slow	5.5	ns
t_{PHL}				5.5	
t_{PLH}	CLK	B	Fast	4.3	ns
t_{PHL}				4.3	
t_{en}	$\overline{OEAB}$	B	Slow	5.7	ns
t_{dis}				4.3	
t_{en}	$\overline{OEAB}$	B	Fast	4.3	ns
t_{dis}				3.8	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP Buffered CLKAB Signal (CLKOUT)**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1616 is a high-drive, 17-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. Additionally, it provides for a copy of CLKAB at GTLP signal levels (CLKOUT) and conversion of a GTLP clock to LVTTL logic levels (CLKIN). The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

OEC, TI, TI-OPC, UBT, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1616 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1616DGGR	GTLPH1616

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1616 is a high-drive (100 mA), 17-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1616 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH1616 UBT transceiver replaces all above functions					

Additionally, the device allows for transparent conversion of CLKAB-to-GTLP signal levels (CLKOUT) and CLKOUT-to-LVTTL logic levels (CLKIN).

Data flow in each direction is controlled by clock enables ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$). $\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$ enable all 17 bits, and $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ control the 17 bits of data and the CLKOUT/CLKIN buffered clock path for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{\text{CEAB}}$ and LEAB are low, the A data is latched regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, LEBA, and CLKBA are used.

Function Tables

OUTPUT ENABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

BUFFERED CLOCK

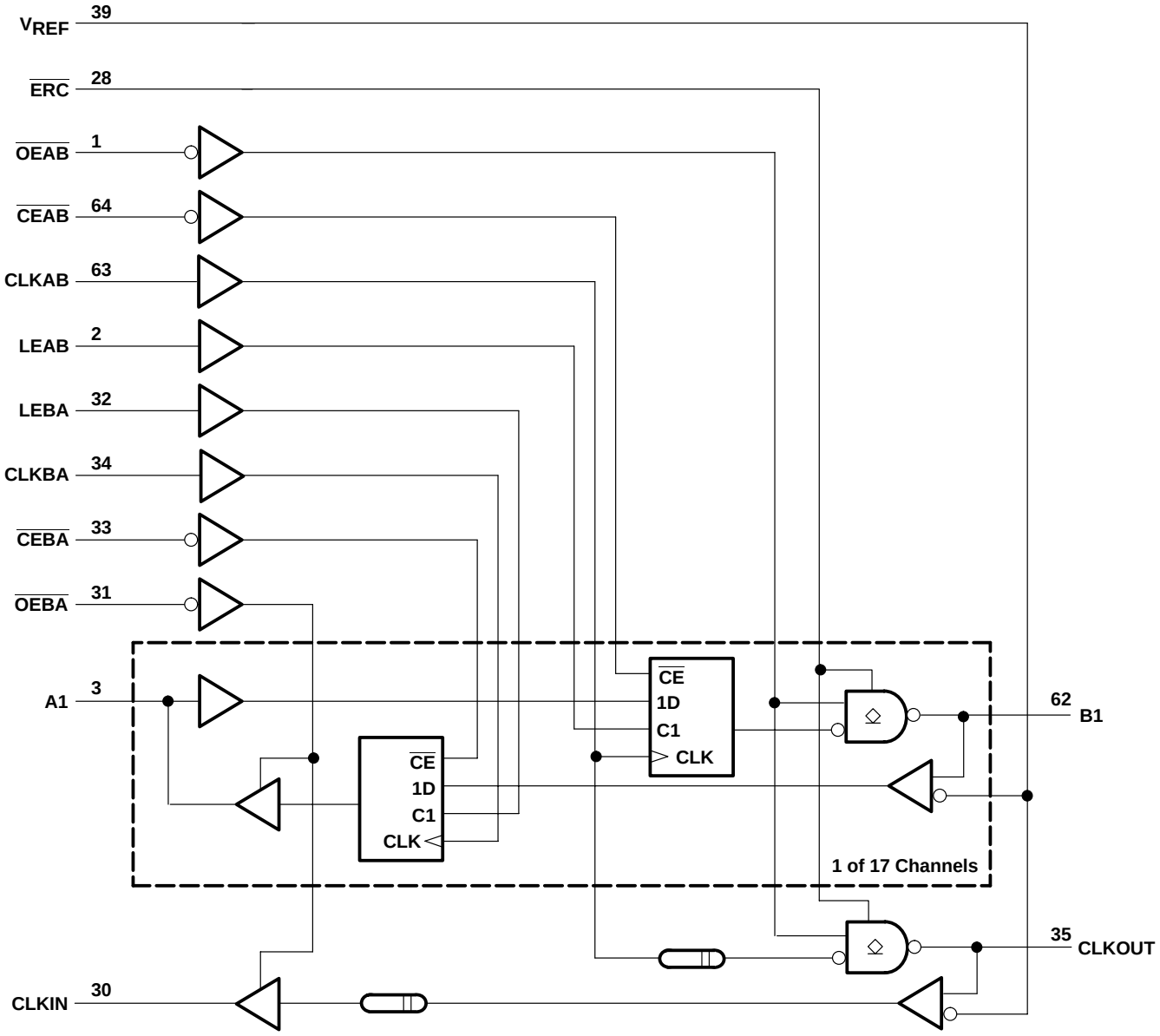
INPUTS				OPERATION OR FUNCTION	MODE
$\overline{CE}$	LE	$\overline{OEAB}$	$\overline{OEBA}$		
X	X	H	H	Z	Isolation
X	X	L	H	CLKAB to CLKOUT	True delayed clock signal
X	X	H	L	CLKOUT to CLKIN	
X	X	L	L	CLKAB to CLKOUT, CLKOUT to CLKIN	True delayed clock signal with feedback path¶

¶ This condition is not recommended.

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port, $\overline{ERC}$, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	55°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			45	mA
			Outputs low			45	
			Outputs disabled			45	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5.5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	8	pF
	B port or CLKOUT	V_O = 1.5 V or 0			9.5	11.5	
C_o	CLKIN	V_O = 3.15 V or 0			4.5	5.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (unless otherwise noted)

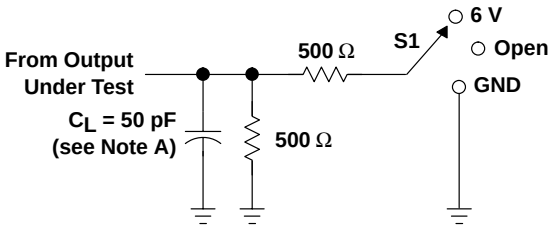
			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	3		ns
		CLKAB or CLKBA high or low	3		
t_{su}	Setup time	A before CLKAB↑	2.2		ns
		B before CLKBA↑	2.4		
		A before LEAB↓, CLK = Don't care	1.8		
		B before LEBA↓, CLK = Don't care	2.1		
		$\overline{CEAB}$ before CLKAB↑	1.5		
		$\overline{CEBA}$ before CLKBA↑	1.5		
t_h	Hold time	A after CLKAB↑	0.7		ns
		B after CLKBA↑	0.5		
		A after LEAB↓, CLK = Don't care	1.2		
		B after LEBA↓, CLK = Don't care	0.9		
		$\overline{CEAB}$ after CLKAB↑	1.5		
		$\overline{CEBA}$ after CLKBA↑	1.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (see Figure 1)

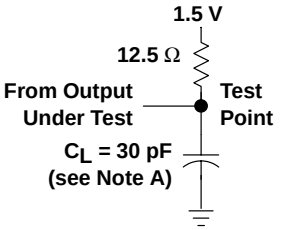
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	A	B	Slow	4.3	5.6	7.1	ns
t_{PHL}				3.2	4.6	6.4	
t_{PLH}	A	B	Fast	3.2	4.3	5.6	ns
t_{PHL}				2.7	3.9	5.3	
t_{PLH}	LEAB	B	Slow	4.8	6.2	7.8	ns
t_{PHL}				3.5	4.9	6.7	
t_{PLH}	LEAB	B	Fast	3.5	4.8	6.2	ns
t_{PHL}				3.1	4.3	5.8	
t_{PLH}	CLKAB	B	Slow	4.8	6.1	7.6	ns
t_{PHL}				3.5	4.8	6.6	
t_{PLH}	CLKAB	B	Fast	3.6	4.9	6.2	ns
t_{PHL}				3.1	4.3	5.7	
t_{PLH}	CLKAB	CLKOUT	Slow	5.5	6.9	8.5	ns
t_{PHL}				5.5	7	9.3	
t_{PLH}	CLKAB	CLKOUT	Fast	4	5.3	6.7	ns
t_{PHL}				4.4	5.8	7.6	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Slow	4.8	6.2	7.8	ns
t_{dis}				3.4	5.2	7.8	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Fast	3.6	4.8	6.2	ns
t_{dis}				3	4.4	6.1	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.4		
t_f	Fall time, B outputs (80% to 20%)		Slow		3.3		ns
			Fast		2.4		
t_{PLH}	B	A	—	1.1	2.8	4.3	ns
t_{PHL}				1.9	3.1	4.1	
t_{PLH}	LEBA	A	—	1.3	3.1	4.6	ns
t_{PHL}				1.4	2.6	3.8	
t_{PLH}	CLKBA	A	—	1.3	3.3	4.8	ns
t_{PHL}				1.8	2.9	4.1	
t_{PLH}	CLKOUT	CLKIN	—	2.2	3.7	5.3	ns
t_{PHL}				2.7	3.9	5.1	
t_{en}	$\overline{OEBA}$	A or CLKIN	—	1.2	2.9	4.8	ns
t_{dis}				2.3	4	5.5	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

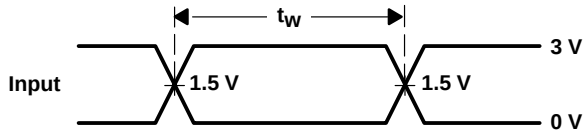


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

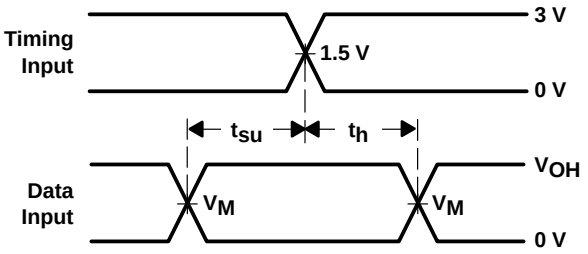


LOAD CIRCUIT FOR A OUTPUTS

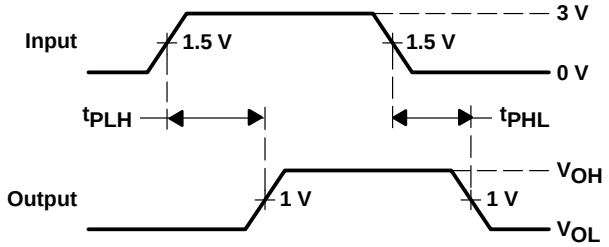
LOAD CIRCUIT FOR B OUTPUTS



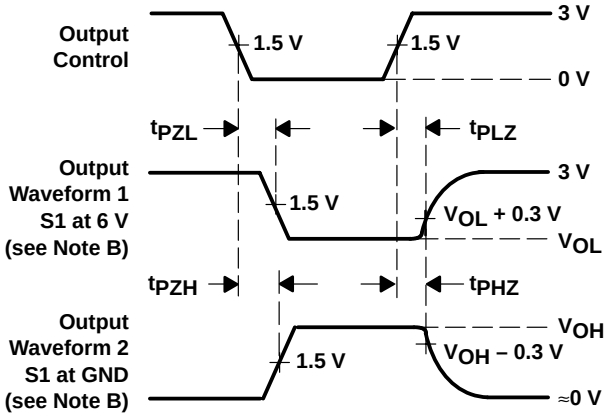
VOLTAGE WAVEFORMS
PULSE DURATION



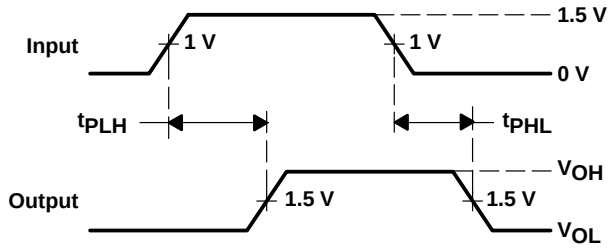
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (see Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

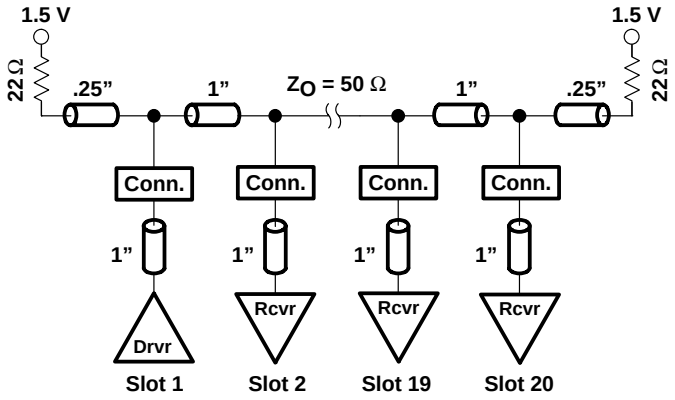


Figure 2. High-Drive Test Backplane

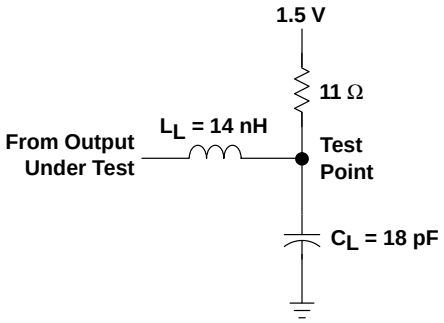


Figure 3. High-Drive RLC Network

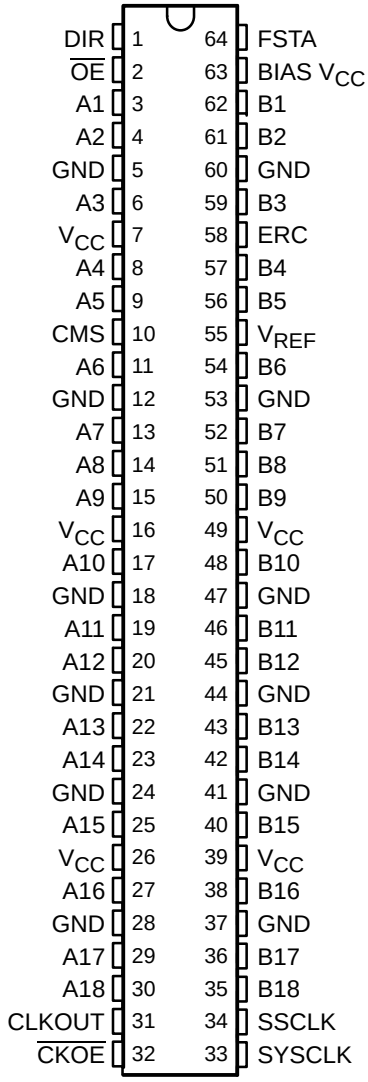
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	5.3	ns
t_{PHL}				5.3	
t_{PLH}	A	B	Fast	4	ns
t_{PHL}				4	
t_{PLH}	LEAB	B	Slow	5.2	ns
t_{PHL}				5.2	
t_{PLH}	LEAB	B	Fast	3.9	ns
t_{PHL}				3.9	
t_{PLH}	CLK	B	Slow	5.5	ns
t_{PHL}				5.5	
t_{PLH}	CLK	B	Fast	4.3	ns
t_{PHL}				4.3	
t_{PLH}	CLKAB	CLKOUT	Slow	5.9	ns
t_{PHL}				5.9	
t_{PLH}	CLKAB	CLKOUT	Fast	4.8	ns
t_{PHL}				4.8	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Slow	5.7	ns
t_{dis}				4.3	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Fast	4.3	ns
t_{dis}				3.8	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP Buffered SYSCLK Signal (SSCLK) for Source Synchronous Applications**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1627 is a high-drive, 18-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent and latched modes of data transfer. Additionally, with the use of the clock-mode select (CMS) input, the device can be used in source synchronous and clock synchronous applications. Source synchronous applications require the skew between the clock output and data output to be minimized for optimum maximum-frequency system performance. In order to reduce this skew, aflexible setup time adjustment (FSTA) feature is incorporated into the device that sets a predetermined delay between the clock and data. The CMS and direction (DIR) inputs control the mode of the device. The system clock (SYSCLK) and CLKOUT pins are LVTTL compatible, while the source synchronous I/O is GTLP compatible. The benefits include compensation for output-to-output skew coming from the driver itself, and compensation for process skew if more than one driver is used. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

PRODUCT PREVIEW

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PRODUCT PREVIEW

description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1627 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1627DGGR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1627 is a high-drive (100 mA), 18-bit bus transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent or latched modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1627 Bus Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
SN74GTLPH1627 bus transceiver replaces all above functions					

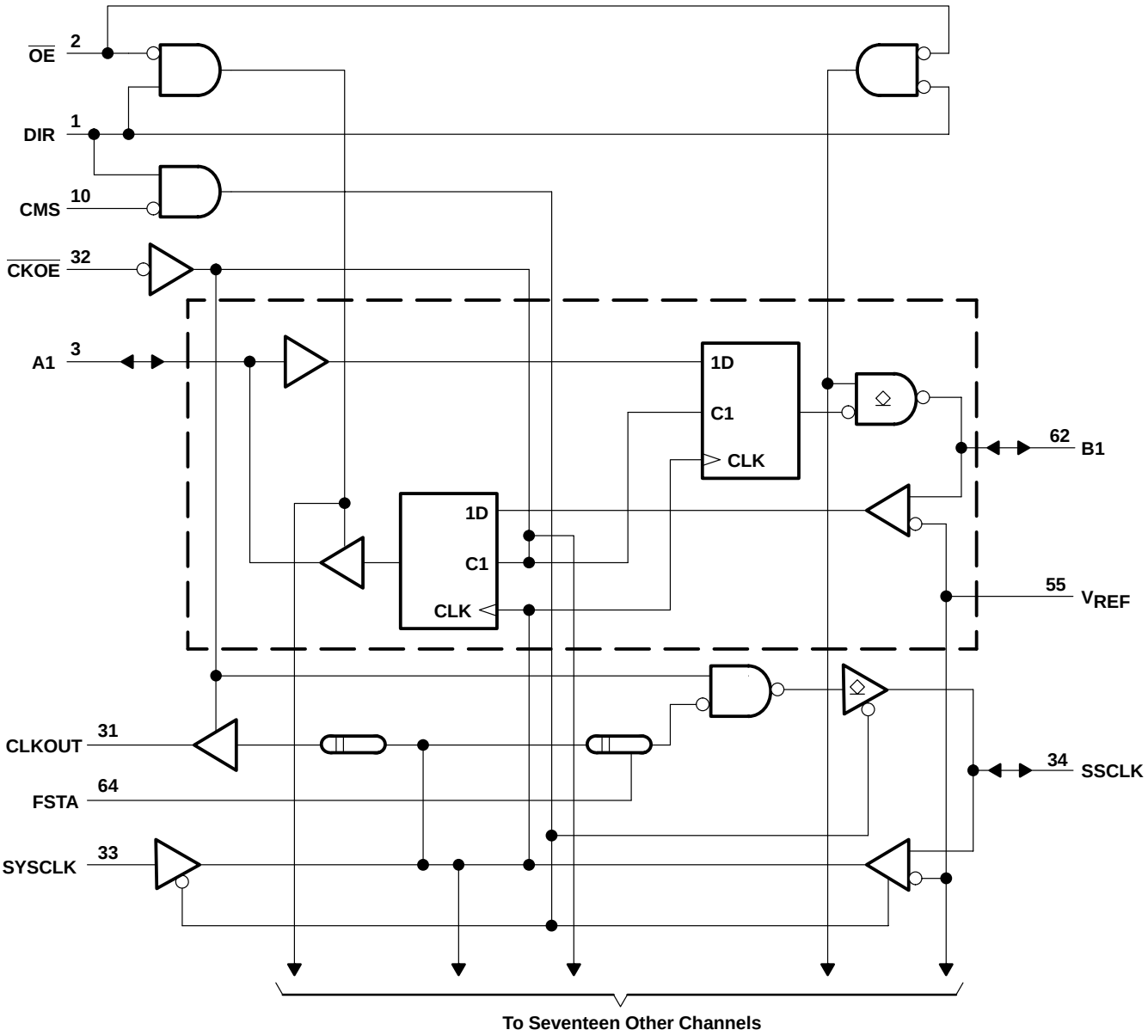
Additionally, the device allows for conversion of the system clock (SYSCLK) to GTLP signal levels (SSCLK) and LVTTL signal levels (CLKOUT). It also provides conversion of a GTLP source synchronous clock to LVTTL signal levels (CLKOUT).

The device allows for conversion of the LVTTL system clock (SYSCLK) to GTLP (SSCLK) and LVTTL (CLKOUT) signal levels when used as the transmitter and GTLP source synchronous clock (SSCLK) to LVTTL (CLKOUT) signal levels when used as the receiver in source synchronous applications. Source synchronous operation removes time-of-flight restrictions and allows for increased data throughput. CMS is used to switch between system synchronous mode and clock synchronous mode. The clock output-enable ($\overline{\text{CKOE}}$) input is used to switch between latched and transparent mode.

Data flow in each direction is controlled by $\overline{\text{CKOE}}$, clock (SYSCLK or SSCLK), direction (DIR), and $\overline{\text{OE}}$. $\overline{\text{OE}}$ controls the 18 bits of data. The CLKOUT/SSCLK buffered clock path for the A-to-B and B-to-A directions is controlled by $\overline{\text{CKOE}}$. In the data isolation mode ($\overline{\text{OE}}$ high, $\overline{\text{CKOE}}$ low), A data may be stored in one register and/or B data may be stored in the other register.

PRODUCT PREVIEW

logic diagram (positive logic)



Function Tables

A-TO-B DIRECTION

INPUTS						OUTPUTS			MODE	
$\overline{CKOE}$	$\overline{OE}$	CMS	DIR	SYSCLK	A	SSCLK	CLKOUT	B		
L	L	X	L	H or L	X	SYSCLK	SYSCLK	B_0	Latched storage of A	Source synchronous
L	L	X	L	↑	L	SYSCLK	SYSCLK	L	Clocked storage of A	
L	L	X	L	↑	H	SYSCLK	SYSCLK	H		
L	H	X	L	X	X	SYSCLK	SYSCLK	Z	Data isolation	
H	L	X	L	X	L	Z	Z	L	Transparent transmission of A	
H	L	X	L	X	H	Z	Z	H		
H	H	X	X	X	X	Z	Z	Z	Isolation	
L	H	H	X	↑	X	SYSCLK	SYSCLK	Z	Transmit SYSCLK	
L	H	H	X	H or L	X	SYSCLK	SYSCLK	Z		

B-TO-A DIRECTION

INPUTS							OUTPUTS			MODE	
$\overline{CKOE}$	$\overline{OE}$	CMS	DIR	SYSCLK	SSCLK	B	SSCLK	CLKOUT	A		
L	L	L	H	X	H or L	X	Input	SSCLK	A_0	Latched storage of B	Source synchronous
L	L	L	H	X	↑	L	Input	SSCLK	L	Clocked storage of B	
L	L	L	H	X	↑	H	Input	SSCLK	H		
L	H	L	H	X	X	X	Input	SSCLK	Z	Data isolation	
L	L	H	H	H or L	Output	X	SYSCLK	SYSCLK	A_0	Latched storage of B	Clock synchronous
L	L	H	H	↑	Output	L	SYSCLK	SYSCLK	L	Clocked storage of B	
L	L	H	H	↑	Output	H	SYSCLK	SYSCLK	H		
L	H	H	H	X	Output	X	SYSCLK	SYSCLK	Z	Data isolation	
H	L	X	H	X	Output	L	Z	Z	L	Transparent transmission of B	
H	L	X	H	X	Output	H	Z	Z	H		
H	H	X	X	X	Output	X	Z	Z	Z	Isolation	
L	H	L	X	X	↑	X	Input	SSCLK	Z	Receive SSCLK	
L	H	L	X	X	H or L	X	Input	SSCLK	Z		

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC LOGIC LEVEL	OUTPUT B-PORT EDGE RATE
H	Slow
L	Fast

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A-port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	55°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

PRODUCT PREVIEW

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port and SSCLK			V_{TT}	V
		Except B port and SSCLK		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port and SSCLK	V_{REF}+0.05			V
		Except B port and SSCLK	2			
V_{IL}	Low-level input voltage	B port and SSCLK			V_{REF}–0.05	V
		Except B port and SSCLK			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port and CLKOUT			–24	mA
I_{OL}	Low-level output current	A port and CLKOUT			24	mA
		B port and SSCLK			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

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electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port and CLKOUT	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port and CLKOUT	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port and SSCLK	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	SYSCLK and control inputs	V_{CC} = 3.45 V,	V_I = 0 to 5.5 V			±10	µA
I_{OZ}‡	B port and SSCLK	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	µA
	CLKOUT	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	
I_{OZH}‡	A port	V_{CC} = 3.45 V,	V_O = V_{CC}			10	µA
I_{OZL}‡	A port	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A port, B port, or SSCLK	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	SYSCLK inputs	V_I = 3.15 V or 0					pF
	Control inputs	V_I = 3.15 V or 0					
C_{io}	A port	V_O = 3.15 V or 0					pF
	B port or SSCLK	V_O = 1.5 V or 0					
C_o	CLKOUT	V_O = 3.15 V or 0					pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency				MHz
t_w	Pulse duration	$\overline{CKOE}$ high			ns
		SYSCLK or SSCLK high or low			
t_{su}	Setup time	A before SYSCLK↑			ns
		B before SYSCLK↑ or SSCLK↑			
		A before $\overline{CKOE}$↓			
		B before $\overline{CKOE}$↓			
t_h	Hold time	A after SYSCLK↑			ns
		B after SYSCLK↑ or SSCLK↑			
		A after $\overline{CKOE}$↓			
		B after $\overline{CKOE}$↓			

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	FSTA	MIN	TYP‡	MAX	UNIT
f_{max}								MHz
t_{PLH}	A	B	Slow	–				ns
t_{PHL}								
t_{PLH}	A	B	Fast	–				ns
t_{PHL}								
t_{PLH}	$\overline{CKOE}$	B	Slow	–				ns
t_{PHL}								
t_{PLH}	$\overline{CKOE}$	B	Fast	–				ns
t_{PHL}								
t_{PLH}	SYSCLK	B	Slow	–				ns
t_{PHL}								
t_{PLH}	SYSCLK	B	Fast	–				ns
t_{PHL}								
t_{en}	$\overline{OE}$	B	Slow	–				ns
t_{dis}								
t_{en}	$\overline{OE}$	B	Fast	–				ns
t_{dis}								
t_r	Rise time, B and SSCLK outputs (20% to 80%)		Slow	–				ns
			Fast					
t_f	Fall time, B and SSCLK outputs (80% to 20%)		Slow	–				ns
			Fast					
t_{PLH}	B	A	–	–				ns
t_{PHL}								
t_{PLH}	$\overline{CKOE}$	A	–	–				ns
t_{PHL}								
t_{PLH}	SYSCLK or SSCLK	A	–	–				ns
t_{PHL}								
t_{PLH}	SYSCLK or SSCLK	CLKOUT	–	GND				ns
t_{PHL}								
t_{PLH}	SYSCLK or SSCLK	CLKOUT	–	V_{CC}				ns
t_{PHL}								
t_{en}	$\overline{OE}$	A	–	–				ns
t_{dis}								
t_{en}	$\overline{CKOE}$	CLKOUT	–	–				ns
t_{dis}								

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V (unless otherwise noted); standard lumped loads, C_L = 30 pF for B port (see Figure 1)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE‡	FSTA	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$t_{sk(LH)}$¶	SYSCLK	B	Slow	–					ns
$t_{sk(HL)}$¶									
$t_{sk(LH)}$¶	SYSCLK	B	Fast	–					ns
$t_{sk(HL)}$¶									
$t_{sk(LH)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	GND	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(HL)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	GND	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(LH)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	GND	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(HL)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	GND	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(LH)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	V_{CC}	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(HL)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	V_{CC}	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(LH)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	V_{CC}	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				
$t_{sk(HL)}$¶	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	V_{CC}	V_{CC} = 3.15 V, T = 85°C				ns
					V_{CC} = 3.3 V, T = 25°C				
					V_{CC} = 3.45 V, T = –40°C				

† Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
‡ Slow (ERC = H) and Fast (ERC = L)
§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ $t_{sk(LH)}/t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature. The specifications apply to any outputs switching in the same direction, either high to low [$t_{sk(HL)}$], low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

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skew characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V (unless otherwise noted); standard lumped loads, C_L = 30 pF for B port (see Figure 1) (continued)†

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE‡	FSTA	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
$t_{sk(t)}$¶	SYSCLK	B	Slow	–					ns
			Fast	–					
$t_{sk(prLH)}$#	SYSCLK	B	Slow	–					ns
$t_{sk(prHL)}$#									
$t_{sk(prLH)}$#	SYSCLK	B	Fast	–					ns
$t_{sk(prHL)}$#									

† Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
‡ Slow (ERC = H) and Fast (ERC = L)
§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
¶ $t_{sk(LH)}/t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature. The specifications apply to any outputs switching in the same direction, either high to low [$t_{sk(HL)}$], low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].
# $t_{sk(prLH)}$ or $t_{sk(prHL)}$ – Part-to-part skew is designed as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst-case V_{CC} and temperature. Furthermore, these values are provided by SPICE simulations.

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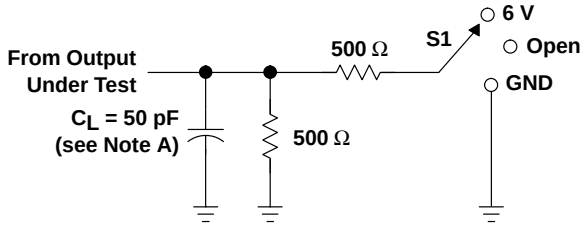
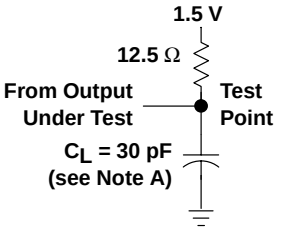
PARAMETER MEASUREMENT INFORMATION

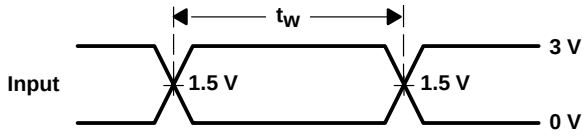


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

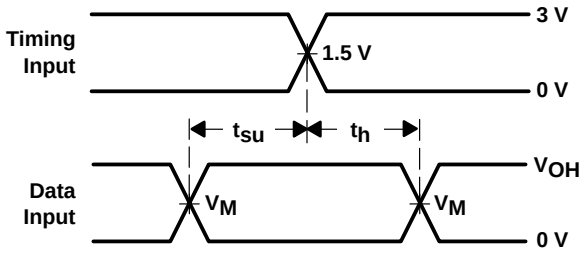


LOAD CIRCUIT FOR A OUTPUTS

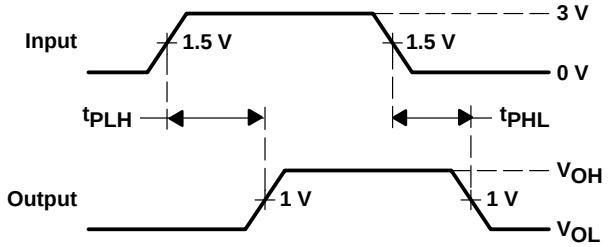
LOAD CIRCUIT FOR B OUTPUTS



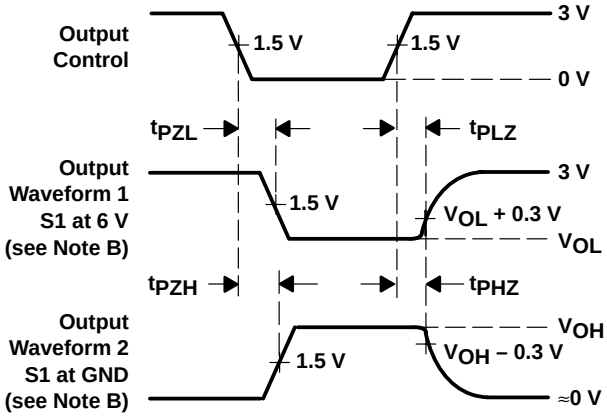
VOLTAGE WAVEFORMS
PULSE DURATION



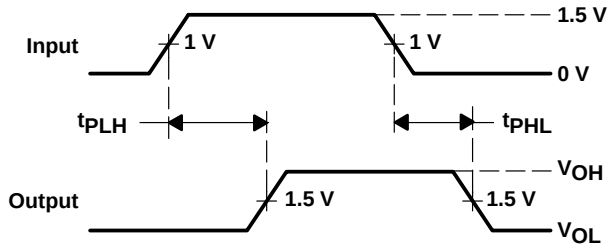
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. Load circuit for A outputs is also used for CLKOUT; load circuit for B outputs is also used for SSCLK.

Figure 1. Load Circuits and Voltage Waveforms

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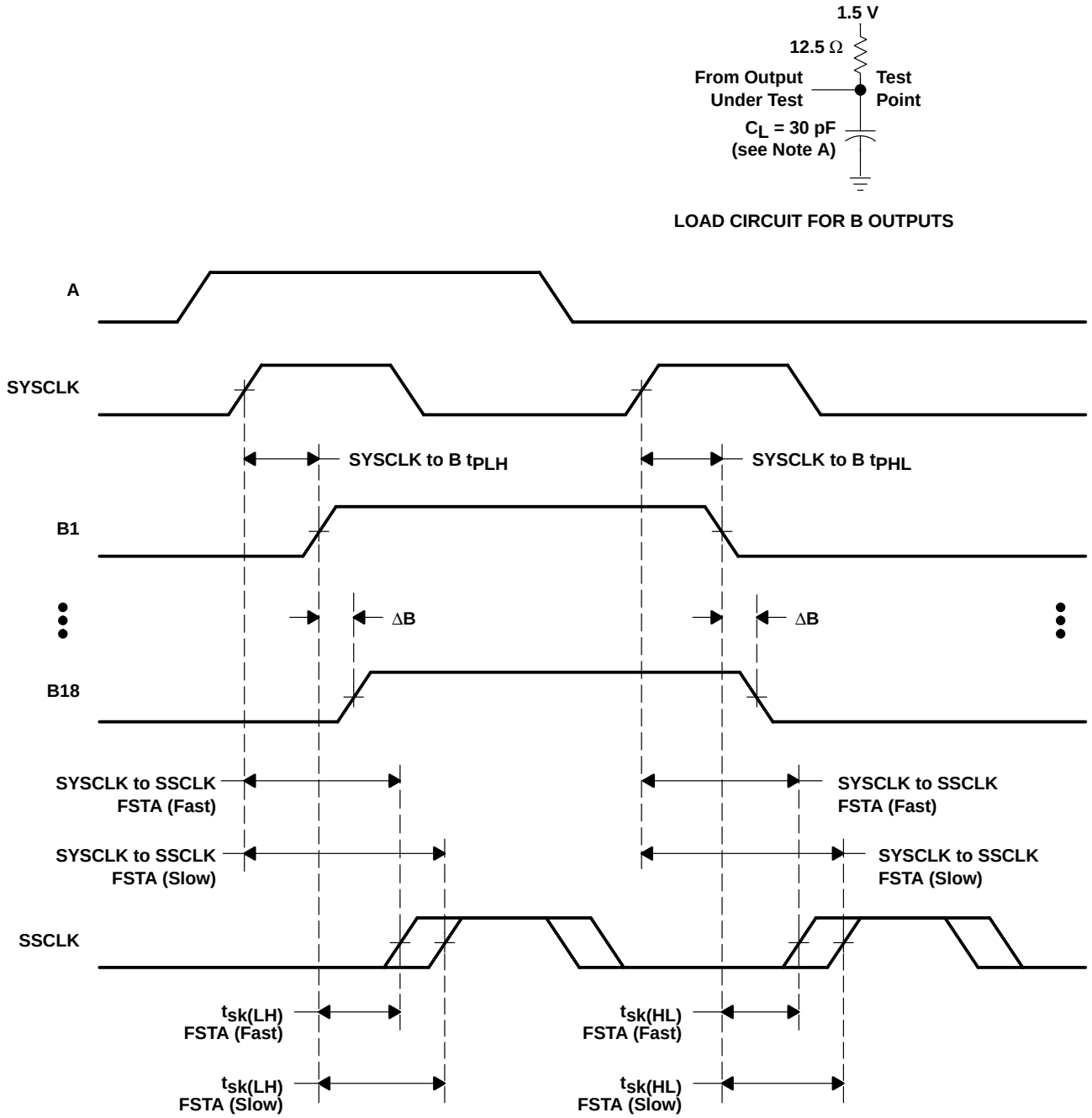

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. Load circuit for B outputs is also used for SSCLK.

Figure 2. Load Circuit and SYSCLK to SSCLK + ΔB Skew Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 3. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 4. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

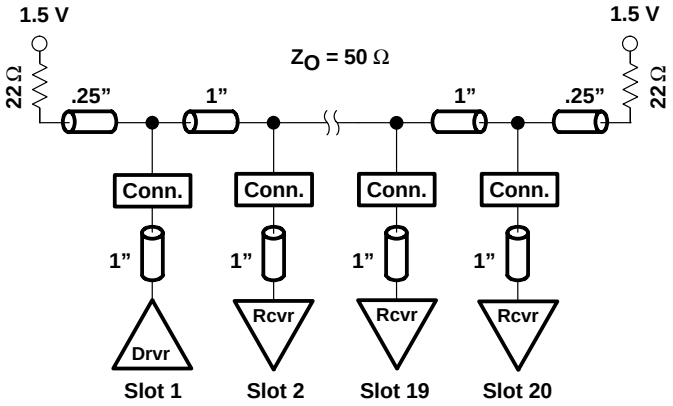

Figure 3. High-Drive Test Backplane

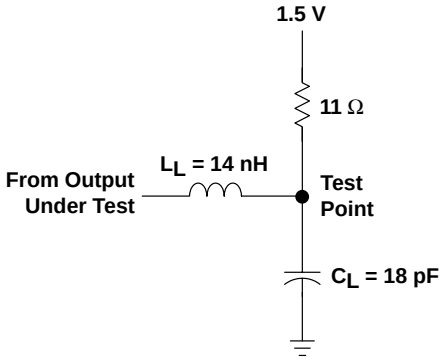

Figure 4. High-Drive RLC Network

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PRODUCT PREVIEW

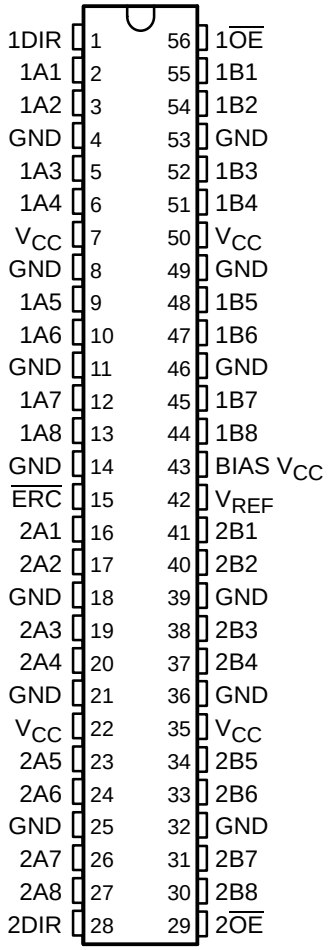
switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	FSTA	TYP‡	UNIT
t_{PLH}	A	B	Slow	–		ns
t_{PHL}						
t_{PLH}			Fast	–		
t_{PHL}						
t_{PLH}	SYSCLK	B	Slow	–		ns
t_{PHL}						
t_{PLH}			Fast	–		
t_{PHL}						
t_{PLH}	SYSCLK	SSCLK	Slow	GND		ns
t_{PHL}						
t_{PLH}			Fast			
t_{PHL}						
t_{PLH}			Slow	V_{CC}		
t_{PHL}						
t_{PLH}			Fast			
t_{PHL}						
t_r	Rise time, B and SSCLK outputs (20% to 80%)		Slow	–	1.6	ns
			Fast	–	1	
t_f	Fall time, B and SSCLK outputs (80% to 20%)		Slow	–	1.5	ns
			Fast	–	1.6	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLPH1645 is a high-drive, 16-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1645 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

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description (continued)

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

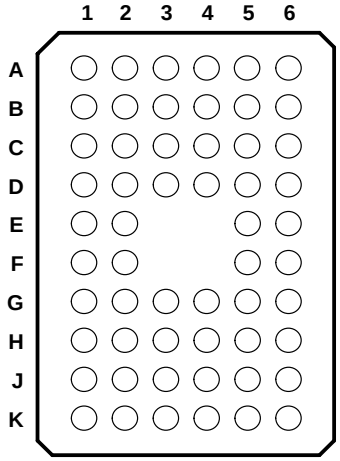
This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	1DIR	$1\overline{OE}$	1B1	1B2
B	1A4	1A3	GND	GND	1B3	1B4
C	1A5	GND	V_{CC}	V_{CC}	GND	1B5
D	1A7	1A6	GND	GND	1B6	1B7
E	GND	1A8			1B8	BIAS V_{CC}
F	$\overline{ERC}$	2A1			2B1	V_{REF}
G	2A2	2A3	GND	GND	2B3	2B2
H	2A4	GND	V_{CC}	V_{CC}	GND	2B4
J	2A5	2A6	GND	GND	2B6	2B5
K	2A7	2A8	2DIR	$2\overline{OE}$	2B8	2B7

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1645DGGR	GTLPH1645
	TVSOP – DGV	Tape and reel	SN74GTLPH1645DGVR	GL45
	VFBGA – GQL	Tape and reel	SN74GTLPH1645GQLR	GL45

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1645 is a high-drive (100 mA), 16-bit bus transceiver partitioned as two 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except $\overline{OE}$ and DIR are low.

Function Tables

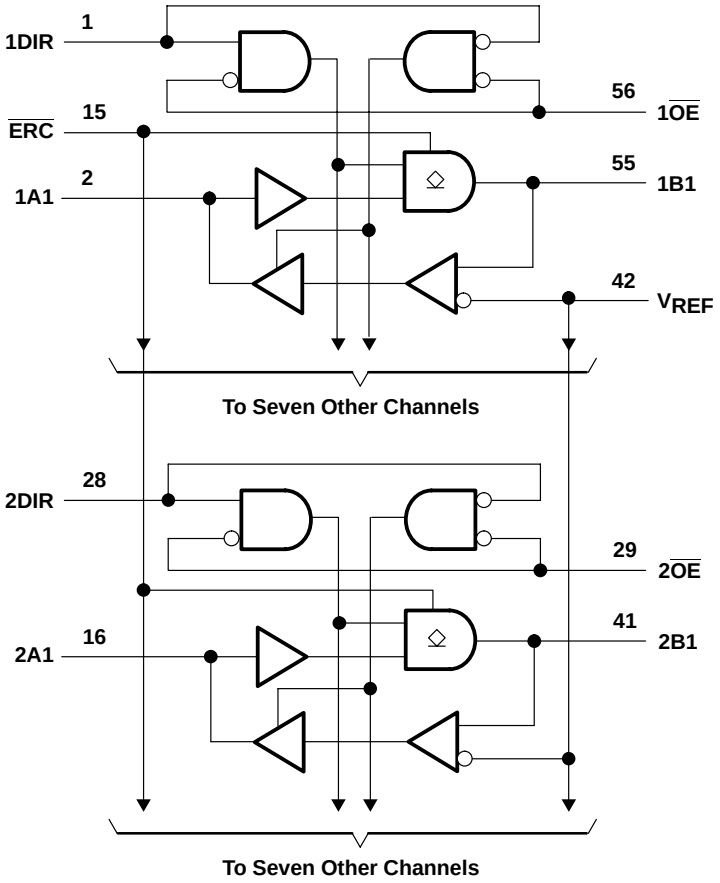
OUTPUT CONTROL

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port, $\overline{ERC}$, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DGV package	48°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	7.5	pF
	B port	V_O = 1.5 V or 0			9.5	11	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

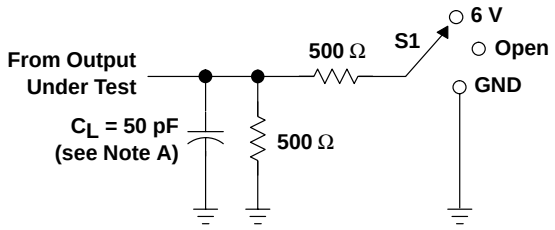
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	A	B	Slow	3.9		7.2	ns
t_{PHL}				3.1		8.4	
t_{PLH}	A	B	Fast	2.6		5.7	ns
t_{PHL}				2.1		5.8	
t_{en}	$\overline{OE}$	B	Slow	4.1		7.3	ns
t_{dis}				4		9.4	
t_{en}	$\overline{OE}$	B	Fast	2.9		5.9	ns
t_{dis}				4		6.9	
t_r	Rise time, B outputs (20% to 80%)		Slow		3		ns
			Fast		1.5		
t_f	Fall time, B outputs (80% to 20%)		Slow		4		ns
			Fast		2.5		
t_{PLH}	B	A	—	0.5		6.7	ns
t_{PHL}				1.2		4.5	
t_{en}	$\overline{OE}$	A	—	1.1		6.3	ns
t_{dis}				1.7		5.1	

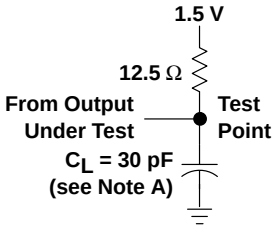
† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

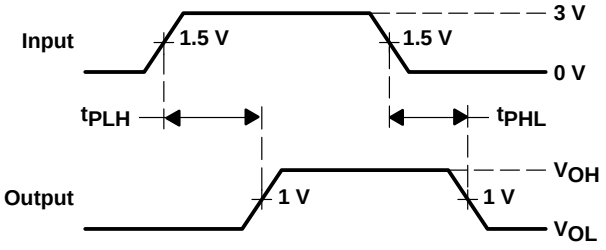


LOAD CIRCUIT FOR A OUTPUTS

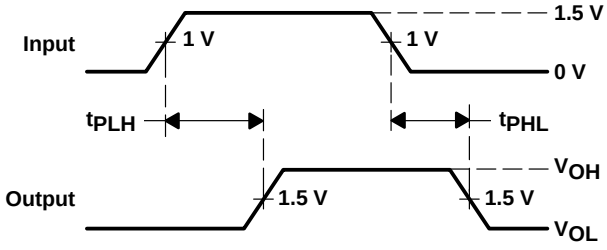
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



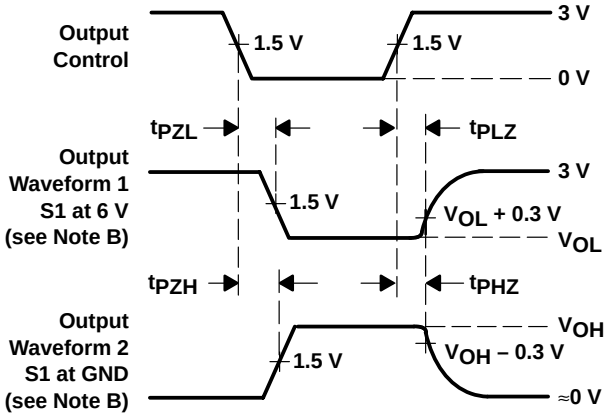
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

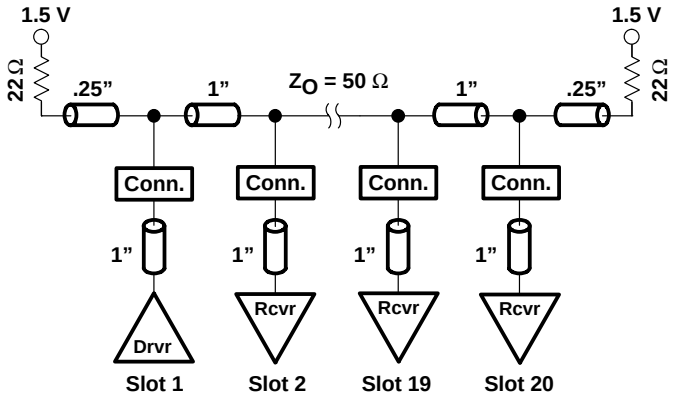


Figure 2. High-Drive Test Backplane

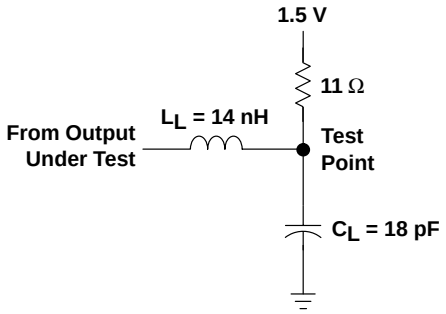


Figure 3. High-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	4.9	ns
t_{PHL}				4.9	
t_{PLH}	A	B	Fast	3.7	ns
t_{PHL}				3.7	
t_{en}	$\overline{OE}$	B	Slow	5.1	ns
t_{dis}				5.4	
t_{en}	$\overline{OE}$	B	Fast	4.1	ns
t_{dis}				4.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of Texas Instruments' Widebus+™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

description

The SN74GTLPH3245 is a high-drive, 32-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as four 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC circuitry, and TI-OPC circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH3245 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

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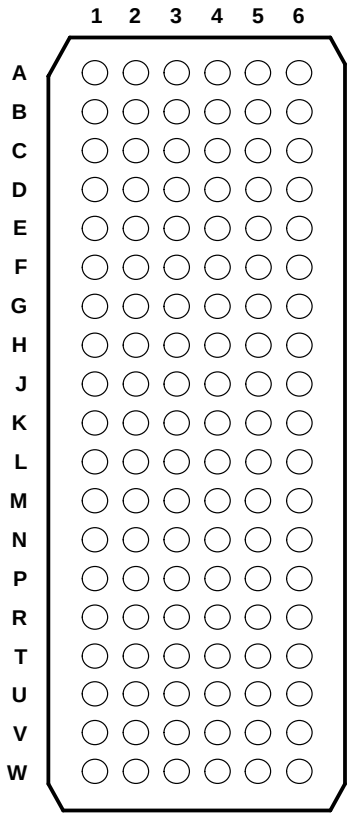
description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GKF PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1A3	1A2	1A1	1B1	1B2	1B3
B	GND	1A4	1DIR	1$\overline{OE}$	1B4	GND
C	1A6	1A5	GND	GND	1B5	1B6
D	1A8	1A7	1V_{CC}	1V_{CC}	1B7	1B8
E	1$\overline{ERC}$	GND	GND	GND	1BIAS V_{CC}	1V_{REF}
F	2A2	2A1	GND	GND	2B1	2B2
G	2A4	2A3	1V_{CC}	1V_{CC}	2B3	2B4
H	GND	2A5	GND	GND	2B5	GND
J	2A6	2A7	2A8	2B8	2B7	2B6
K	NC	3A1	2DIR	2$\overline{OE}$	3B1	NC
L	3A3	3A2	3DIR	3$\overline{OE}$	3B2	3B3
M	GND	3A4	GND	GND	3B4	GND
N	3A6	3A5	2V_{CC}	2V_{CC}	3B5	3B6
P	3A8	3A7	GND	GND	3B7	3B8
R	2$\overline{ERC}$	GND	GND	GND	2BIAS V_{CC}	2V_{REF}
T	4A2	4A1	2V_{CC}	2V_{CC}	4B1	4B2
U	4A4	4A3	GND	GND	4B3	4B4
V	GND	4A5	4A8	4B8	4B5	GND
W	4A6	4A7	4DIR	4$\overline{OE}$	4B7	4B6

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKF	Tape and reel	SN74GTLPH3245GKFR	GM45

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH3245 is a high-drive (100 mA), 32-bit bus transceiver partitioned in four 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{OE}$ and DIR are low.

Function Tables

OUTPUT CONTROL

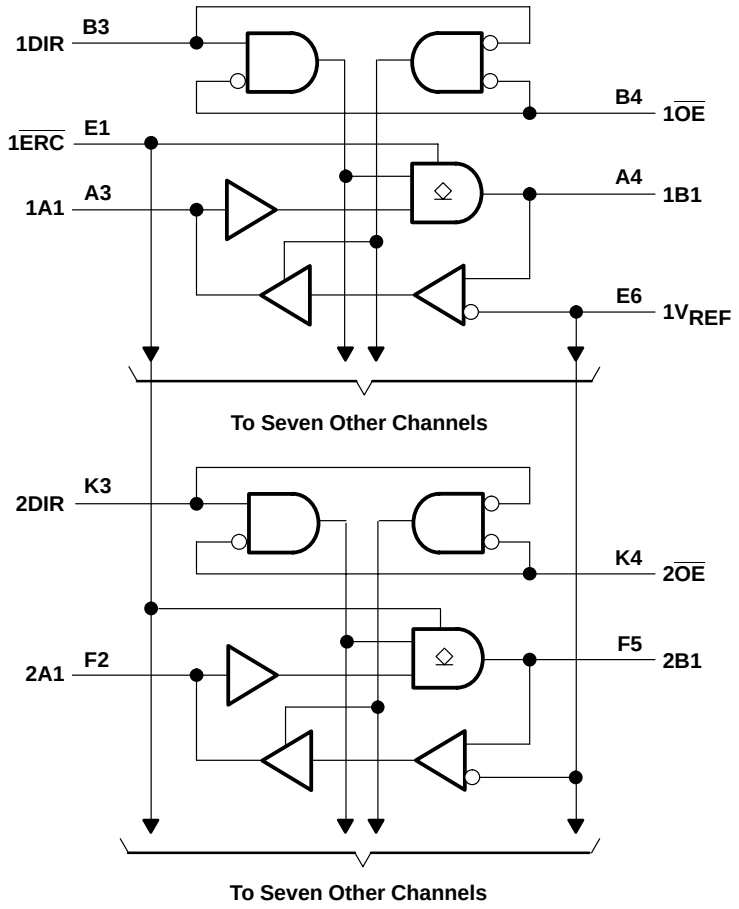
INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

PRODUCT PREVIEW

logic diagram (positive logic)†



† $1V_{CC}$ and 1BIAS V_{CC} are associated with these channels.

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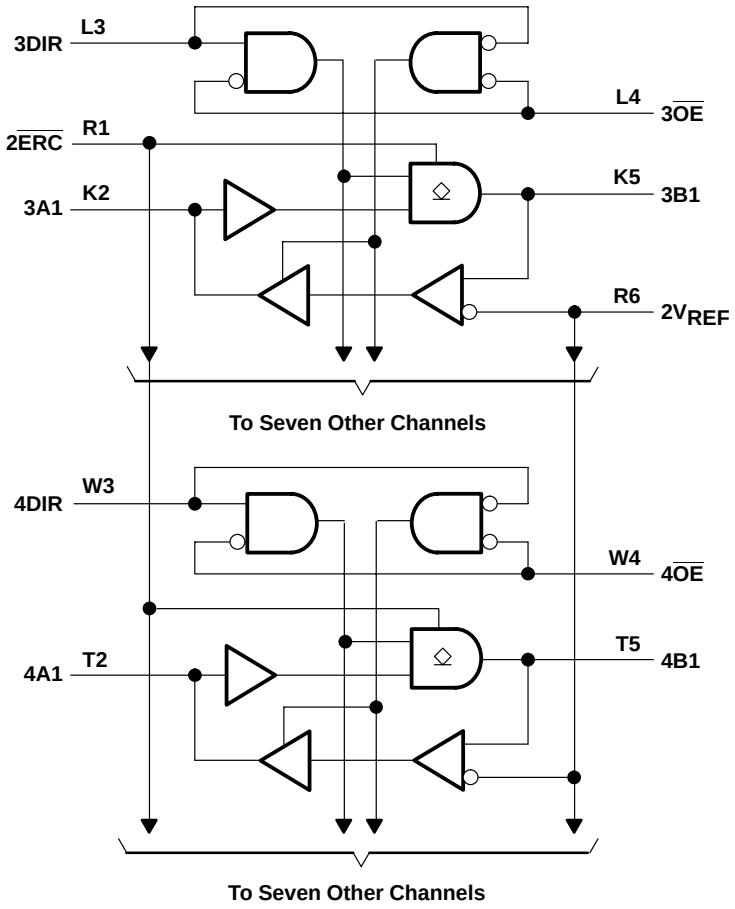
logic diagram (positive logic) (continued)†



† $2V_{CC}$ and 2BIAS V_{CC} are associated with these channels.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port, $\overline{ERC}$, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	36°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

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electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±10	µA
			V_I = 5.5 V			±20	
	B port		V_I = 0 to 1.5 V			±10	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
I_{CCD}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND, One data input switching at 50% duty cycle	Outputs enabled				mA/MHz
			Outputs disabled				
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0					pF
C_{io}	A port	V_O = 3.15 V or 0					pF
	B port	V_O = 1.5 V or 0					

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

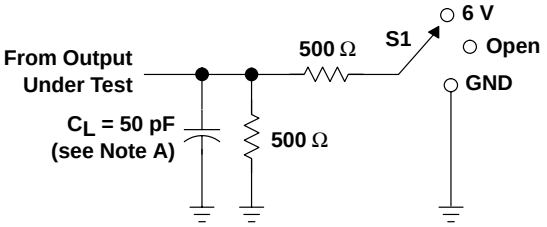
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	A	B	Slow				ns
t_{PHL}							
t_{PLH}	A	B	Fast				ns
t_{PHL}							
t_{en}	$\overline{OE}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OE}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (20% to 80%)		Slow				ns
			Fast				
t_f	Fall time, B outputs (80% to 20%)		Slow				ns
			Fast				
t_{PLH}	B	A	—				ns
t_{PHL}							
t_{en}	$\overline{OE}$	A	—				ns
t_{dis}							

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

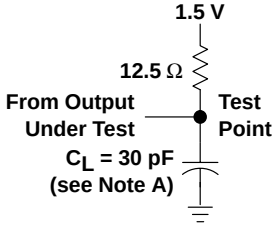
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

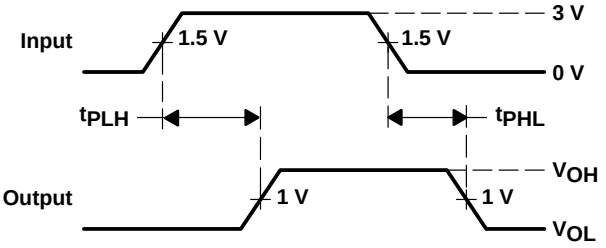


LOAD CIRCUIT FOR A OUTPUTS

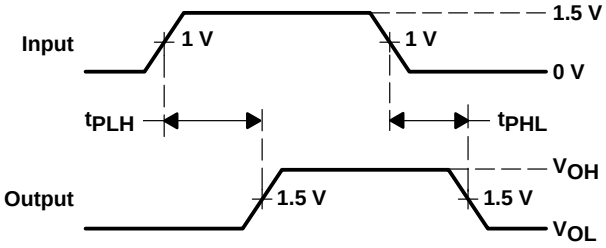
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



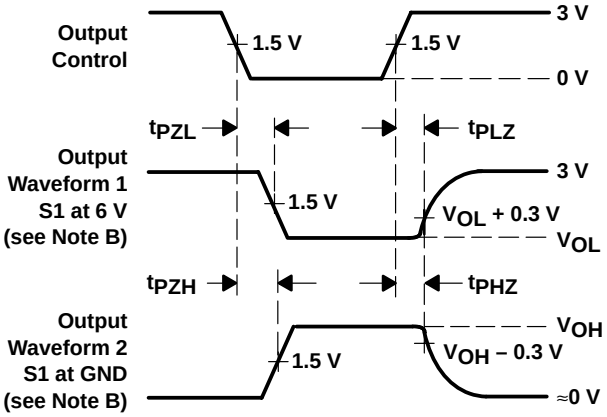
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PRODUCT PREVIEW

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

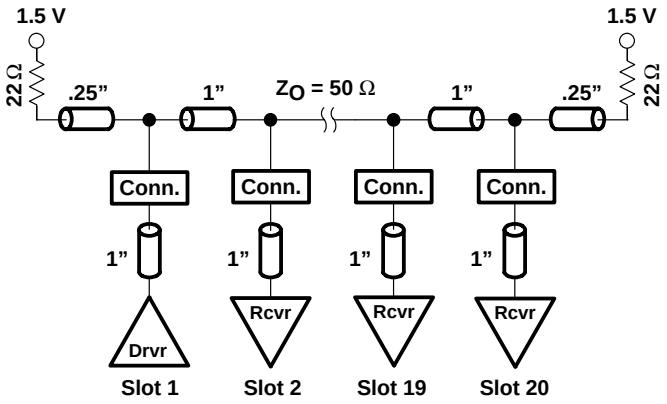


Figure 2. High-Drive Test Backplane

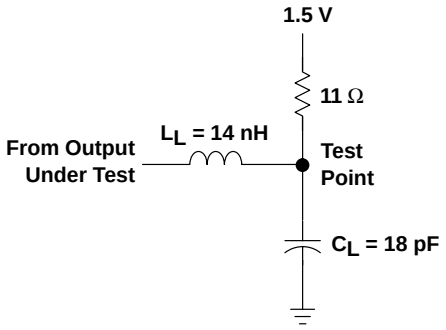


Figure 3. High-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

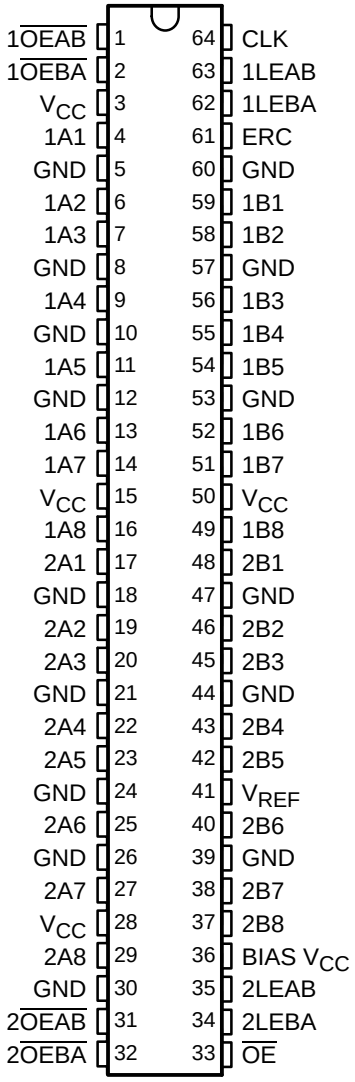
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	4.9	ns
t_{PHL}				4.9	
t_{PLH}	A	B	Fast	3.7	ns
t_{PHL}				3.7	
t_{en}	$\overline{OE}$	B	Slow	5.1	ns
t_{dis}				5.4	
t_{en}	$\overline{OE}$	B	Fast	4.1	ns
t_{dis}				4.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

PRODUCT PREVIEW

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Partitioned as Two 8-Bit Transceivers With Individual Latch Timing and Output Control, but With a Common Clock**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1655 is a high-drive, 16-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers and allows for transparent, latched, and clocked modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

OEC, TI, TI-OPC, UBT, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1655 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1655DGGR	GTLPH1655

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1655 is a high-drive (100 mA), 16-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or clocked modes. The device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output signals and a common clock for both transceiver words. It can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1655 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541
Latched transceiver	’543			’16543
Latch	’373, ’573	’843	’841	’16373
Registered transceiver	’646, ’652			’16646, ’16652
Flip-flop	’374, ’574		’821	’16374
SN74GTLPH1655 UBT transceiver replaces all above functions				

Data flow for each word is determined by the respective latch enables (xLEAB and xLEBA), output enables (x$\overline{\text{OEAB}}$ and x$\overline{\text{OEBA}}$), and clock (CLK). The output enables (1$\overline{\text{OEAB}}$, 1$\overline{\text{OEBA}}$, 2$\overline{\text{OEAB}}$, and 2$\overline{\text{OEBA}}$) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively. Note that CLK is common to both directions and both 8-bit words. $\overline{\text{OE}}$ also is common and disables all I/O ports simultaneously.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When $\overline{\text{OEAB}}$ is low, the outputs are active. With $\overline{\text{OEAB}}$ high, the outputs are in the high-impedance state.

The data flow for the B-to-A direction is identical, except $\overline{\text{OEBA}}$, LEBA, and CLK are used.

Function Tables

FUNCTION†

INPUTS				OUTPUT B	MODE
$\overline{\text{OEAB}}$	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	L	H	X	B_0‡	Latched storage of A data
L	L	L	X	B_0§	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

† A-to-B data flow is shown. B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and CLK. The condition when $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

Function Tables (Continued)

OUTPUT ENABLE

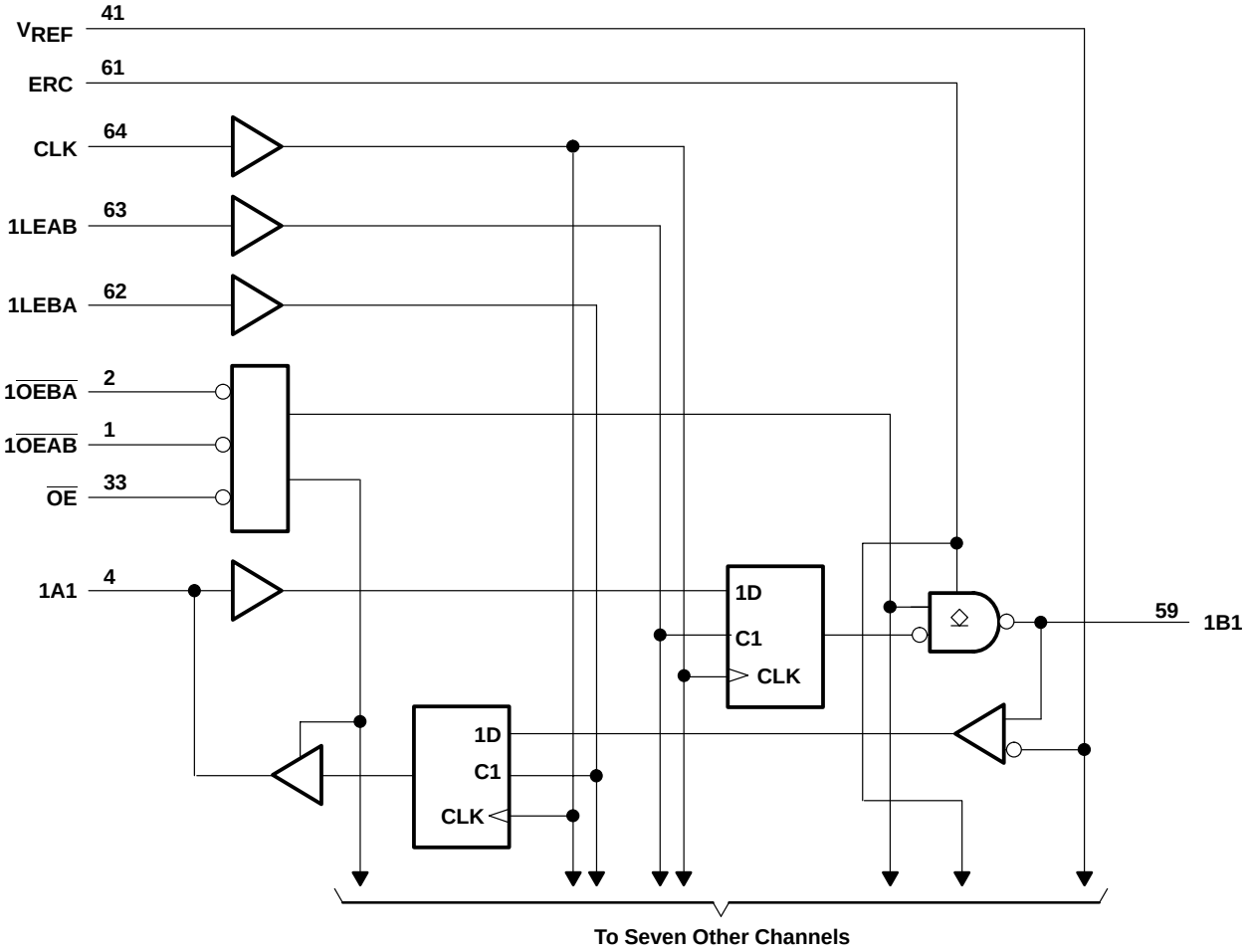
INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{OEAB}$	$\overline{OEBA}$	A PORT	B PORT
L	L	L	Active	Active†
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

† This condition is not recommended.

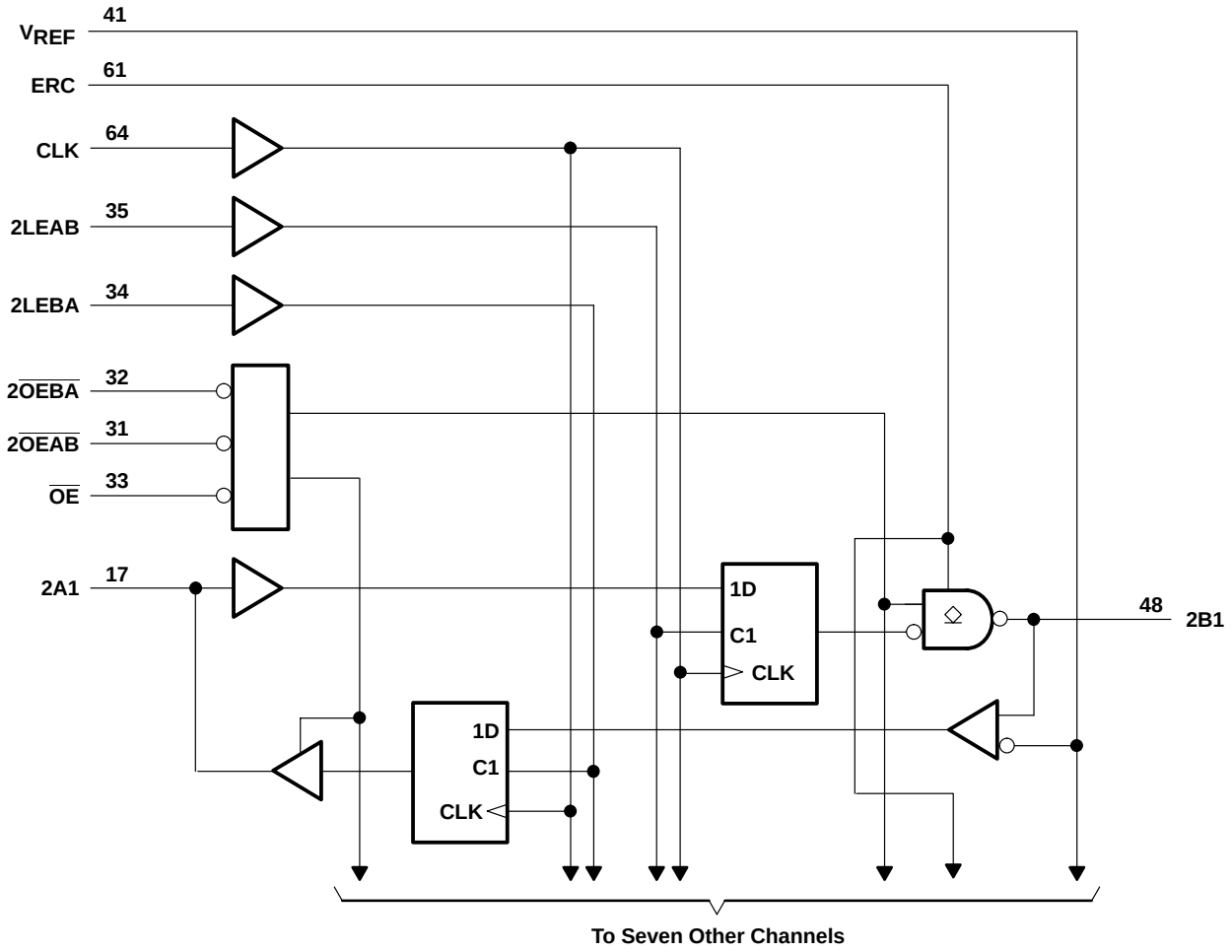
B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

logic diagram (positive logic)



logic diagram (positive logic) (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	200 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	55°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		ERC	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and ERC	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		ERC		GND	0.6	
		Except B port and ERC			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	$V_O = V_{CC}$			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4.5	6.5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	7.5	pF
	B port	V_O = 1.5 V or 0			8.5	10.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

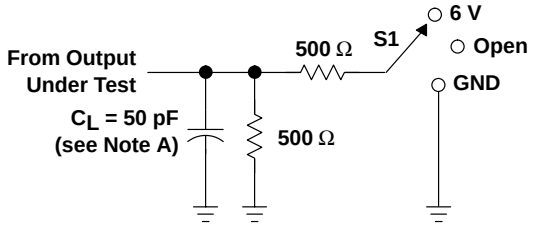
			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	3		ns
		CLK high or low	3		
t_{su}	Setup time	A before CLK	3		ns
		B before CLK	3		
		A before LEAB↓, CLK = don't care	2.5		
		B before LEBA↓, CLK = don't care	2.5		
t_h	Hold time	A after CLK	0.5		ns
		B after CLK	0.5		
		A after LEAB↓, CLK = don't care	0.5		
		B after LEBA↓, CLK = don't care	0.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

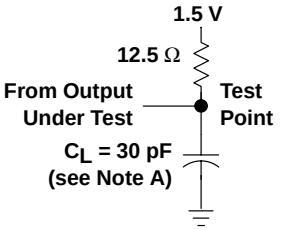
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	A	B	Slow	3.5		7.7	ns
t_{PHL}				2.4		6.3	
t_{PLH}	A	B	Fast	2		6.3	ns
t_{PHL}				2		5.9	
t_{PLH}	LEAB	B	Slow	3.5		7.8	ns
t_{PHL}				2.7		6.4	
t_{PLH}	LEAB	B	Fast	2		6.4	ns
t_{PHL}				2		6	
t_{PLH}	CLK	B	Slow	4.7		8	ns
t_{PHL}				2.7		6.4	
t_{PLH}	CLK	B	Fast	3.6		6.8	ns
t_{PHL}				2		6.1	
t_{en}	$\overline{OE}$	B	Slow	3.5		7.3	ns
t_{dis}				3.5		7	
t_{en}	$\overline{OE}$	B	Fast	2		6	ns
t_{dis}				2		6.6	
t_{en}	$\overline{OEAB}$	B	Slow	3.5		7.4	ns
t_{dis}				3.5		7	
t_{en}	$\overline{OEAB}$	B	Fast	2		6.1	ns
t_{dis}				2		6.3	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.6		ns
			Fast		1.5		
t_f	Fall time, B outputs (80% to 20%)		Slow		3		ns
			Fast		2.2		
t_{PLH}	B	A	–	1.5		5.5	ns
t_{PHL}				1.5		5.5	
t_{PLH}	LEBA	A	–	1.3		5.2	ns
t_{PHL}				1		5	
t_{PLH}	CLK	A	–	1.2		6.3	ns
t_{PHL}				1		5	
t_{en}	$\overline{OE}$	A	–	1.5		5.6	ns
t_{dis}				1.5		6.1	
t_{en}	$\overline{OEBA}$	A	–	1.2		5.4	ns
t_{dis}				2		6.1	

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

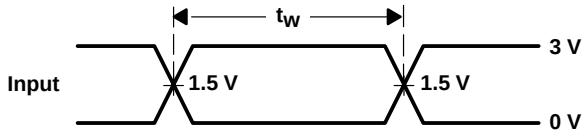


TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND

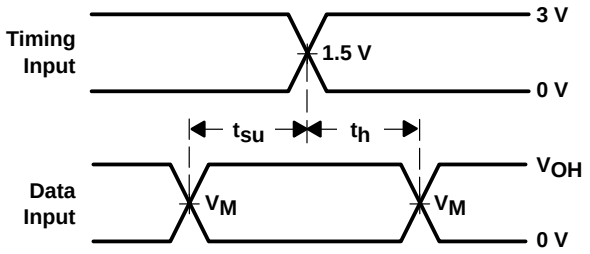


LOAD CIRCUIT FOR A OUTPUTS

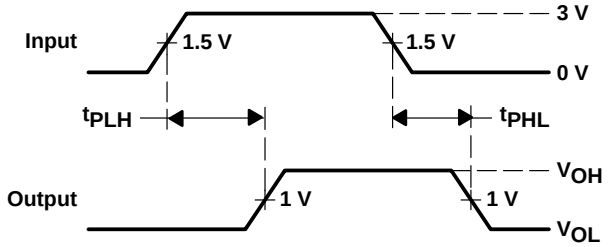
LOAD CIRCUIT FOR B OUTPUTS



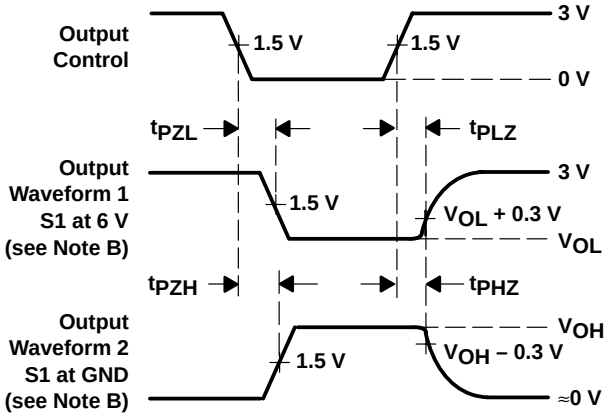
VOLTAGE WAVEFORMS
PULSE DURATION



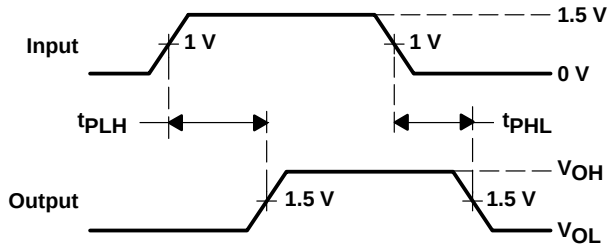
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

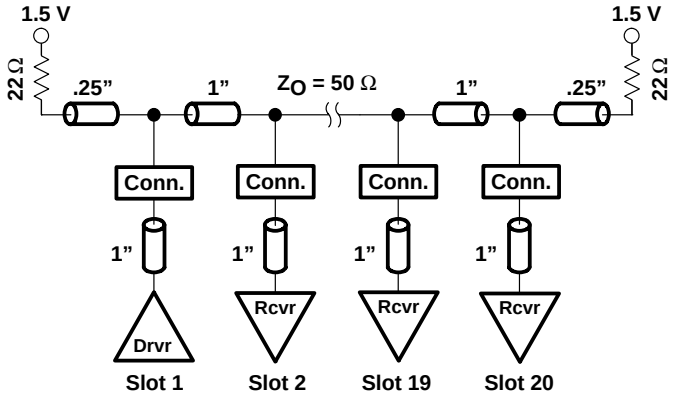


Figure 2. High-Drive Test Backplane

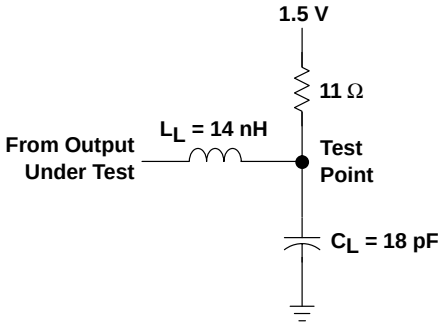


Figure 3. High-Drive RLC Network

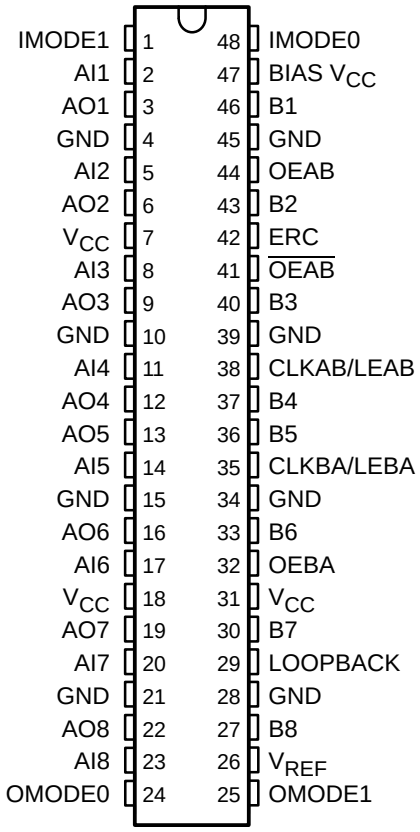
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	5	ns
t_{PHL}				5	
t_{PLH}	A	B	Fast	3.8	ns
t_{PHL}				3.8	
t_{PLH}	LEAB	B	Slow	4.9	ns
t_{PHL}				4.9	
t_{PLH}	LEAB	B	Fast	3.9	ns
t_{PHL}				3.9	
t_{PLH}	CLK	B	Slow	4.8	ns
t_{PHL}				4.8	
t_{PLH}	CLK	B	Fast	3.7	ns
t_{PHL}				3.7	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$	B	Slow	4.9	ns
t_{dis}				4.7	
t_{en}	$\overline{OEAB}$ or $\overline{OE}$	B	Fast	3.5	ns
t_{dis}				4.1	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow (ERC = V_{CC}) and Fast (ERC = GND)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Open-Drain Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLP2033 is a high-drive, 8-bit, three-wire registered transceiver that provides inverted LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent, latched, and flip-flop modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring, the same functionality as the SN74FB2033. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

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description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP2033 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and can be directly driven by TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

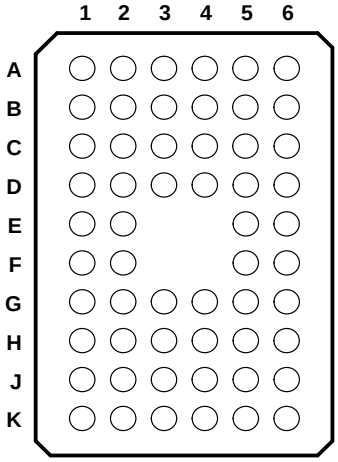
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OEAB}$ should be tied to V_{CC} through a pullup resistor and OEAB and OEBA should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	IMODE1	NC	NC	NC	NC	IMODE0
B	AO1	AI1	GND	GND	BIAS V_{CC}	B1
C	AO2	AI2	V_{CC}	ERC	OEAB	B2
D	AO3	AI3	GND	GND	$\overline{OEAB}$	B3
E	AO4	AI4			CLKAB/LEAB	B4
F	AO5	AI5			CLKBA/LEBA	B5
G	AO6	AI6	GND	GND	OEBA	B6
H	AO7	AI7	V_{CC}	V_{CC}	LOOPBACK	B7
J	AO8	AI8	GND	GND	V_{REF}	B8
K	OMODE0	NC	NC	NC	NC	OMODE1

NC = No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP2033DGGR	GTLP2033
	TVSOP – DGV	Tape and reel	SN74GTLP2033DGVR	GT2033
	VFBGA – GQL	Tape and reel	SN74GTLP2033GQLR	GR033

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP2033 is a high-drive (100 mA), 8-bit, three-wire registered transceiver containing D-type latches and D-type flip-flops for data-path operation in the transparent, latched, or flip-flop modes. Data transmission is complementary, with inverted AI data going to the B port and inverted B data going to AO. The split LVTTL AI and AO provides a feedback path for control and diagnostics monitoring.

The logic element for data flow in each direction is configured by two mode (IMODE1 and IMODE0 for B to A, OMODE1 and OMODE0 for A to B) inputs as a buffer, D-type flip-flop, or D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock (CLKAB/LEAB or CLKBA/LEBA) input. In the latch mode, the clock inputs serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO enable/disable control is provided by OEBA. When OEBA is low or when V_{CC} is less than 1.5 V, AO is in the high-impedance state. When OEBA is high, AO is active (high or low logic levels).

The B port is controlled by OEAB and $\overline{OEAB}$. If OEAB is low, $\overline{OEAB}$ is high, or V_{CC} is less than 1.5 V, the B port is inactive. If OEAB is high and $\overline{OEAB}$ is low, the B port is active.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO) or inactive (B port) states.

Function Tables

FUNCTION/MODE

INPUTS								OUTPUT	MODE
OEBA	OEAB	$\overline{OEAB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK		
L	L	X	X	X	X	X	X	Z	Isolation
L	X	H	X	X	X	X	X		
X	H	L	L	L	X	X	X	Inverted AI to B	Buffer
X	H	L	L	H	X	X	X		Flip-flop
X	H	L	H	X	X	X	X		Latch
H	L	X	X	X	L	L	L	Inverted B to AO	Buffer
H	X	H	X	X	L	L	L		
H	L	X	X	X	L	H	L	Inverted B to AO	Flip-flop
H	X	H	X	X	L	H	L		
H	L	X	X	X	H	X	L	Inverted B to AO	Latch
H	X	H	X	X	H	X	L		
H	L	X	X	X	L	L	H	AI to AO	Buffer
H	X	H	X	X	L	L	H		
H	L	X	X	X	L	H	H	AI to AO	Flip-flop
H	X	H	X	X	L	H	H		
H	L	X	X	X	H	X	H	AI to AO	Latch
H	X	H	X	X	H	X	H		
H	H	L	X	X	X	X	L	Inverted AI to B, Inverted B to AO	Transparent with feedback path

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEBA	OEAB	$\overline{OEAB}$	AO	B
L	X	X	Z	
H	X	X	Active	
X	L	L		Z
X	L	H		Z
X	H	L		Active
X	H	H		Z

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	B port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

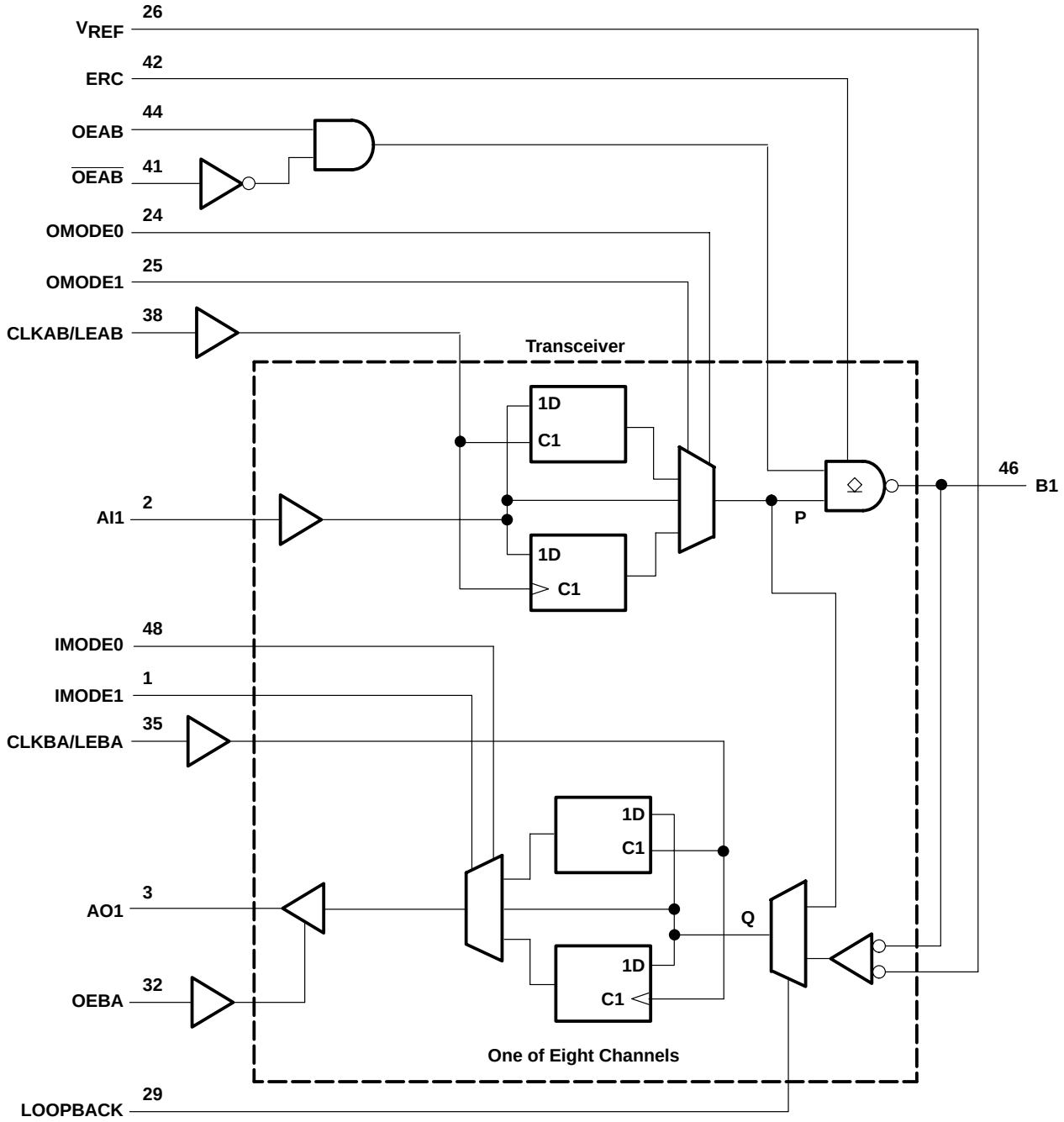
FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC	OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	
H	Slow
L	Fast

functional block diagram



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): AI port, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): AO port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port	48 mA
B port	200 mA
Current into any A-port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port and V_{REF}		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO			–24	mA
I_{OL}	Low-level output current	AO			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	AI and control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZ}‡	AO	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	AO or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}§		V_{CC} = 3.45 V, One AI or control input at V_{CC} – 0.6 V, Other AI or control inputs at V_{CC} or GND				1.5	mA
C_i	AI	V_I = 3.15 V or 0			3.5	4.5	pF
	Control inputs				3.5	5.5	
C_o	AO	V_O = 3.15 V or 0			5	6	pF
C_{io}	B port	V_O = 1.5 V or 0			8.5	10	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}				±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}				±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	2.8		ns
t_{su}	Setup time	AI before CLKAB↑	1.1		ns
		AI before CLKBA↑	1.4		
		B before CLKBA↑	1		
		AI before LEAB↓	1.6		
		AI before LEBA↓	2.1		
		B before LEBA↓	2.2		
t_h	Hold time	AI after CLKAB↑	0.3		ns
		AI after CLKBA↑	0.2		
		B after CLKBA↑	0.6		
		AI after LEAB↓	0.3		
		AI after LEBA↓	0		
		B after LEBA↓	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	AI (buffer)	B	Slow	3		7.4	ns
t_{PHL}				3		7.1	
t_{PLH}	AI (buffer)	B	Fast	2		5.9	ns
t_{PHL}				2		5.8	
t_{PLH}	B (buffer)	AO	–	1		5.7	ns
t_{PHL}				1		5	
t_{PLH}	LEAB (latch mode)	B	Slow	4.2		8.6	ns
t_{PHL}				3.2		7.7	
t_{PLH}	LEAB (latch mode)	B	Fast	3.2		7.6	ns
t_{PHL}				2.8		6.7	
t_{PLH}	LEAB (latch mode)	AO	–	2		7	ns
t_{PHL}				1.8		6.3	
t_{PLH}	LEBA (latch mode)	AO	–	1		5.7	ns
t_{PHL}				1		4.7	
t_{PLH}	OEAB	B	Slow	3.8		7.5	ns
t_{PHL}				3.1		7	
t_{PLH}	OEAB	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PLH}	$\overline{OEAB}$	B	Slow	3.5		7.5	ns
t_{PHL}				3		7.2	
t_{PLH}	$\overline{OEAB}$	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PZH}	OEBA	AO	–	1		4.7	ns
t_{PZL}				1		3.4	
t_{PHZ}	OEBA	AO	–	1		5.2	ns
t_{PLZ}				1		4.9	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	4.4		8.8	ns
t_{PHL}				3.6		8.1	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	3.2		7.2	ns
t_{PHL}				3.1		6.9	
t_{PLH}	CLKAB (flip-flop mode)	AO	–	2		6.9	ns
t_{PHL}				1.8		6.4	
t_{PLH}	CLKBA (flip-flop mode)	AO	–	1		5.6	ns
t_{PHL}				1		4.9	
t_{PLH}	OMODE	B	Slow	3.8		8.7	ns
t_{PHL}				3.2		8.2	
t_{PLH}	OMODE	B	Fast	2.7		7.2	ns
t_{PHL}				2.7		7.2	
t_{PLH}	IMODE	AO	–	1		5.6	ns
t_{PHL}				1		4.6	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	LOOPBACK	AO	–	2.5	6.2	6.2	ns
t_{PHL}				2	5	5	
t_{PLH}	AI (loopback high)	AO	–	1	5.6	5.6	ns
t_{PHL}				1	5	5	
t_r	Rise time, B-port outputs (20% to 80%)		Slow		2.8		ns
			Fast		1.5		
	Rise time, AO (10% to 90%)				3.5		
t_f	Fall time, B-port outputs (80% to 20%)		Slow		3		ns
			Fast		1.8		
	Fall time, AO (90% to 10%)				1.5		

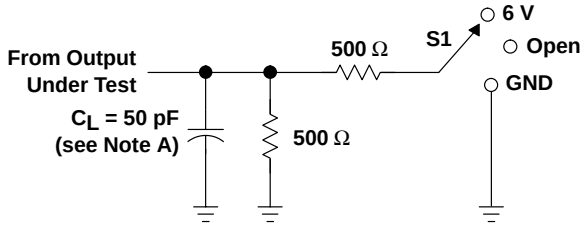
† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)§

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}$¶	AI	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	AI	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(t)}$¶	AI	B	Slow		1.4	2	ns
			Fast		0.6	1.4	
	CLKAB/LEAB	B	Slow		1.8	2.5	
			Fast		0.9	1.8	

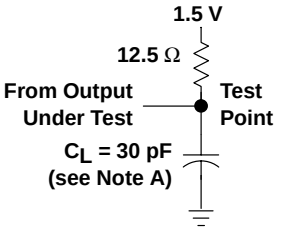
† Slow (ERC = L) and Fast (ERC = H)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION

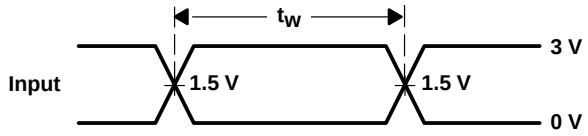


LOAD CIRCUIT FOR A OUTPUTS

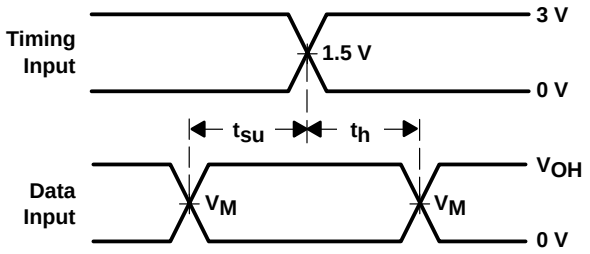
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



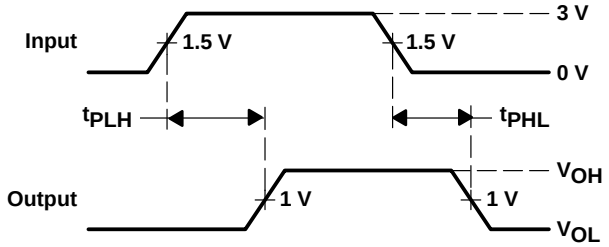
LOAD CIRCUIT FOR B OUTPUTS



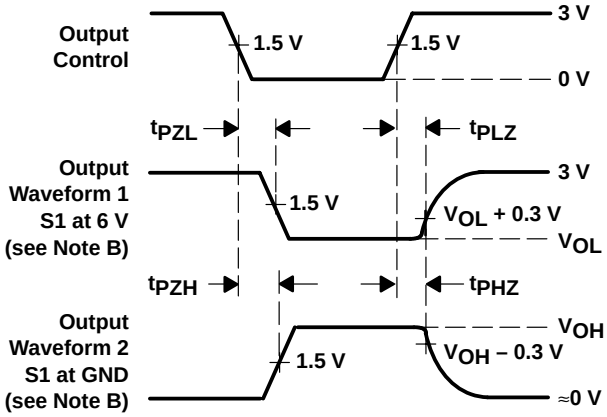
VOLTAGE WAVEFORMS
PULSE DURATION



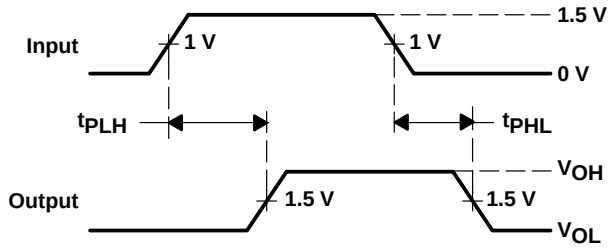
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to AO)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

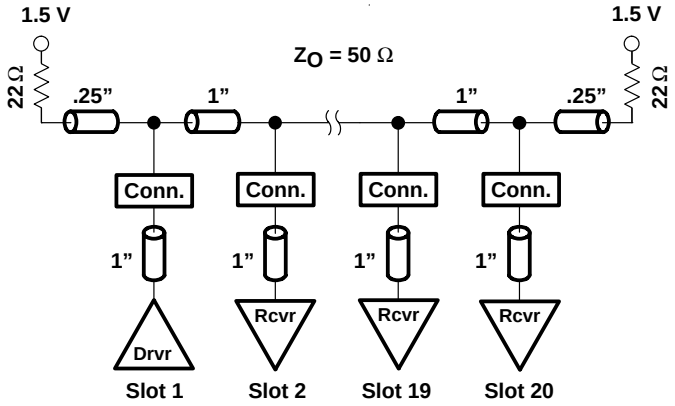


Figure 2. High-Drive Test Backplane

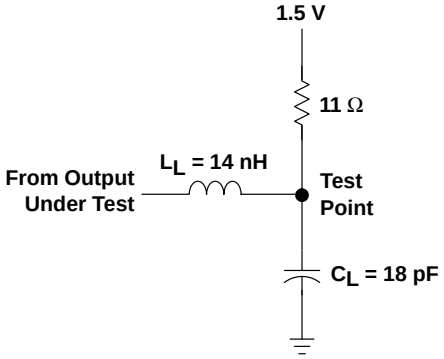


Figure 3. High-Drive RLC Network

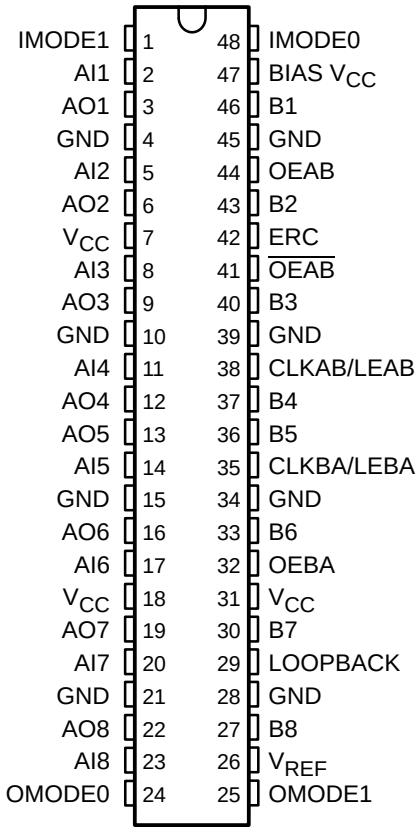
switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI (buffer)	B	Slow	4.7	ns
t_{PHL}				5	
t_{PLH}	AI (buffer)	B	Fast	3.7	ns
t_{PHL}				4	
t_{PLH}	LEAB (latch mode)	B	Slow	5.5	ns
t_{PHL}				5.8	
t_{PLH}	LEAB (latch mode)	B	Fast	4.6	ns
t_{PHL}				4.8	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	5.8	ns
t_{PHL}				6	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	4.9	ns
t_{PHL}				4.9	
t_{PLH}	OMODE	B	Slow	5.5	ns
t_{PHL}				5.7	
t_{PLH}	OMODE	B	Fast	4.5	ns
t_{PHL}				4.7	
t_r	Rise time, B-port outputs (20% to 80%)		Slow	1.8	ns
			Fast	1.1	
t_f	Fall time, B-port outputs (80% to 20%)		Slow	3.4	ns
			Fast	2.6	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **AO Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Open-Drain Outputs (100 mA)**
- **Reduced LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLP22033 is a high-drive, 8-bit, three-wire registered transceiver that provides inverted LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent, latched, and flip-flop modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring, the same functionality as the SN74FB2033. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

The AO outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

OEC, TI-OPC, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP22033 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and can be directly driven by TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

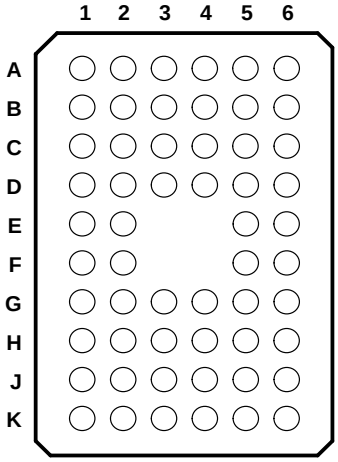
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OEAB}$ should be tied to V_{CC} through a pullup resistor and OEAB and OEBA should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	IMODE1	NC	NC	NC	NC	IMODE0
B	AO1	AI1	GND	GND	BIAS V_{CC}	B1
C	AO2	AI2	V_{CC}	ERC	OEAB	B2
D	AO3	AI3	GND	GND	$\overline{OEAB}$	B3
E	AO4	AI4			CLKAB/LEAB	B4
F	AO5	AI5			CLKBA/LEBA	B5
G	AO6	AI6	GND	GND	OEBA	B6
H	AO7	AI7	V_{CC}	V_{CC}	LOOPBACK	B7
J	AO8	AI8	GND	GND	V_{REF}	B8
K	OMODE0	NC	NC	NC	NC	OMODE1

NC = No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP22033DGGR	GTLP22033
	TVSOP – DGV	Tape and reel	SN74GTLP22033DGVR	GT22033
	VFBGA – GQL	Tape and reel	SN74GTLP22033GQLR	GS033

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP22033 is a high-drive (100 mA), 8-bit, three-wire registered transceiver containing D-type latches and D-type flip-flops for data-path operation in the transparent, latched, or flip-flop modes. Data transmission is complementary, with inverted AI data going to the B port and inverted B data going to AO. The split LVTTL AI and AO provides a feedback path for control and diagnostics monitoring.

The logic element for data flow in each direction is configured by two mode (IMODE1 and IMODE0 for B to A, OMODE1 and OMODE0 for A to B) inputs as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock (CLKAB/LEAB or CLKBA/LEBA) input. In the latch mode, the clock inputs serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO enable/disable control is provided by OEBA. When OEBA is low or when V_{CC} is less than 1.5 V, AO is in the high-impedance state. When OEBA is high, AO is active (high or low logic levels).

The B port is controlled by OEAB and $\overline{OEAB}$. If OEAB is low, $\overline{OEAB}$ is high, or V_{CC} is less than 1.5 V, the B port is inactive. If OEAB is high and $\overline{OEAB}$ is low, the B port is active.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO) or inactive (B port) states.

Function Tables

FUNCTION/MODE

INPUTS								OUTPUT	MODE
OEBA	OEAB	$\overline{OEAB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK		
L	L	X	X	X	X	X	X	Z	Isolation
L	X	H	X	X	X	X	X		
X	H	L	L	L	X	X	X	Inverted AI to B	Buffer
X	H	L	L	H	X	X	X		Flip-flop
X	H	L	H	X	X	X	X		Latch
H	L	X	X	X	L	L	L	Inverted B to AO	Buffer
H	X	H	X	X	L	L	L		
H	L	X	X	X	L	H	L	Inverted B to AO	Flip-flop
H	X	H	X	X	L	H	L		
H	L	X	X	X	H	X	L	Inverted B to AO	Latch
H	X	H	X	X	H	X	L		
H	L	X	X	X	L	L	H	AI to AO	Buffer
H	X	H	X	X	L	L	H		
H	L	X	X	X	L	H	H	AI to AO	Flip-flop
H	X	H	X	X	L	H	H		
H	L	X	X	X	H	X	H	AI to AO	Latch
H	X	H	X	X	H	X	H		
H	H	L	X	X	X	X	L	Inverted AI to B, Inverted B to AO	Transparent with feedback path

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEBA	OEAB	$\overline{OEAB}$	AO	B
L	X	X	Z	
H	X	X	Active	
X	L	L		Z
X	L	H		Z
X	H	L		Active
X	H	H		Z

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	B port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

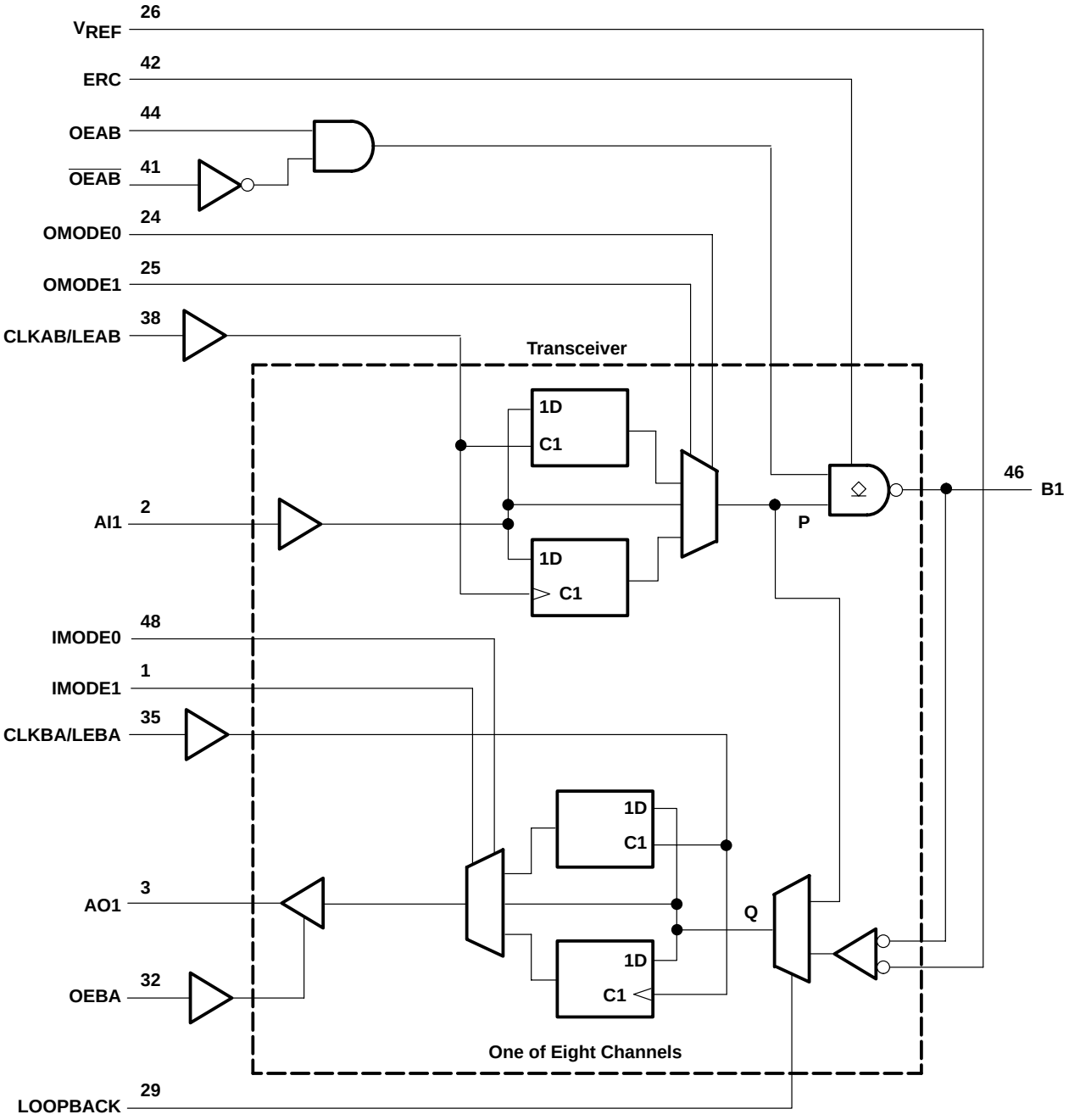
FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC	OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	
H	Slow
L	Fast

functional block diagram



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): AI port, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): AO port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port	24 mA
B port	200 mA
Current into any A-port output in the high state, I_O (see Note 2)	24 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port and V_{REF}		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO			–12	mA
I_{OL}	Low-level output current	AO			12	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2			
V_{OL}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA			0.8	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	AI and control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZ}‡	AO	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	AO or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}§		V_{CC} = 3.45 V, One AI or control input at V_{CC} – 0.6 V, Other AI or control inputs at V_{CC} or GND				1.5	mA
C_i	AI	V_I = 3.15 V or 0			3.5	4.5	pF
	Control inputs				3.5	5.5	
C_o	AO	V_O = 3.15 V or 0			5	6	pF
C_{io}	B port	V_O = 1.5 V or 0			8.5	10	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}				±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}				±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	2.8		ns
t_{su}	Setup time	AI before CLKAB↑	1.1		ns
		AI before CLKBA↑	1.4		
		B before CLKBA↑	1		
		AI before LEAB↓	1.6		
		AI before LEBA↓	2.1		
		B before LEBA↓	2.2		
t_h	Hold time	AI after CLKAB↑	0.3		ns
		AI after CLKBA↑	0.2		
		B after CLKBA↑	0.6		
		AI after LEAB↓	0.3		
		AI after LEBA↓	0		
		B after LEBA↓	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	AI (buffer)	B	Slow	3		7.4	ns
t_{PHL}				3		7.1	
t_{PLH}	AI (buffer)	B	Fast	2		5.9	ns
t_{PHL}				2		5.8	
t_{PLH}	B (buffer)	AO	–	1		6.1	ns
t_{PHL}				1		5.4	
t_{PLH}	LEAB (latch mode)	B	Slow	4.2		8.6	ns
t_{PHL}				3.2		7.7	
t_{PLH}	LEAB (latch mode)	B	Fast	3.2		7.6	ns
t_{PHL}				2.8		6.7	
t_{PLH}	LEAB (latch mode)	AO	–	2		7.3	ns
t_{PHL}				1.8		6.6	
t_{PLH}	LEBA (latch mode)	AO	–	1		6	ns
t_{PHL}				1		5.2	
t_{PLH}	OEAB	B	Slow	3.8		7.5	ns
t_{PHL}				3.1		7	
t_{PLH}	OEAB	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PLH}	$\overline{OEAB}$	B	Slow	3.5		7.5	ns
t_{PHL}				3		7.2	
t_{PLH}	$\overline{OEAB}$	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PZH}	OEBA	AO	–	1		5.3	ns
t_{PZL}				1		4.2	
t_{PHZ}	OEBA	AO	–	1		5.5	ns
t_{PLZ}				1		5.2	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	4.4		8.8	ns
t_{PHL}				3.6		8.1	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	3.2		7.2	ns
t_{PHL}				3.1		6.9	
t_{PLH}	CLKAB (flip-flop mode)	AO	–	2		7.5	ns
t_{PHL}				1.8		7	
t_{PLH}	CLKBA (flip-flop mode)	AO	–	1		6	ns
t_{PHL}				1		5.6	
t_{PLH}	OMODE	B	Slow	3.8		8.7	ns
t_{PHL}				3.2		8.2	
t_{PLH}	OMODE	B	Fast	2.7		7.2	ns
t_{PHL}				2.7		7.2	
t_{PLH}	IMODE	AO	–	1		6	ns
t_{PHL}				1		5.1	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	LOOPBACK	AO	–	2.5		6.8	ns
t_{PHL}				2		5.4	
t_{PLH}	AI (loopback high)	AO	–	1		6	ns
t_{PHL}				1		5.5	
t_r	Rise time, B-port outputs (20% to 80%)		Slow		2.8		ns
			Fast		1.5		
	Rise time, AO (10% to 90%)				5.5		
t_f	Fall time, B-port outputs (80% to 20%)		Slow		3		ns
			Fast		1.8		
	Fall time, AO (90% to 10%)				4.5		

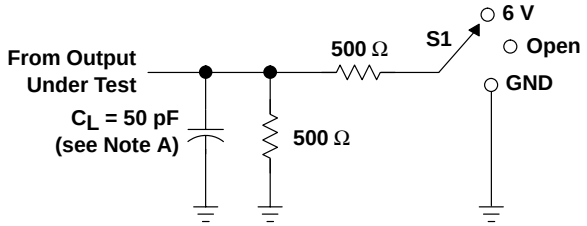
† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)§

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}$¶	AI	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	AI	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(t)}$¶	AI	B	Slow		1.4	2	ns
			Fast		0.6	1.4	
	CLKAB/LEAB	B	Slow		1.8	2.5	
			Fast		0.9	1.8	

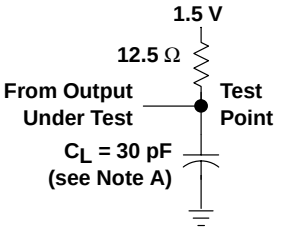
† Slow (ERC = L) and Fast (ERC = H)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION

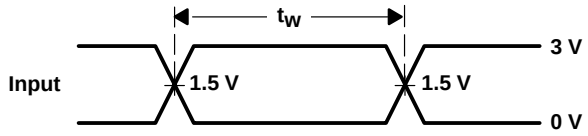


LOAD CIRCUIT FOR A OUTPUTS

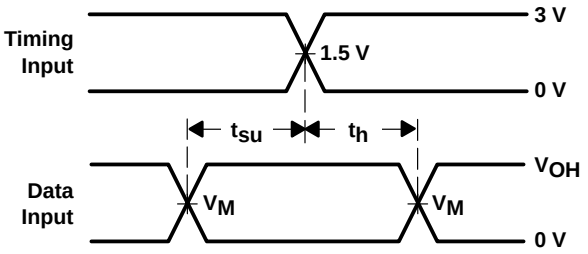
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



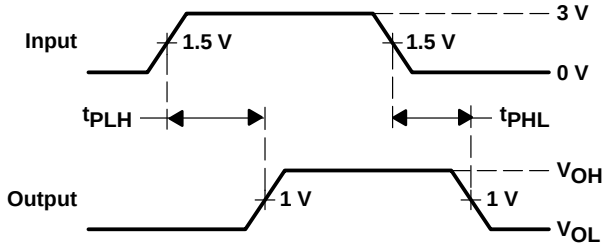
LOAD CIRCUIT FOR B OUTPUTS



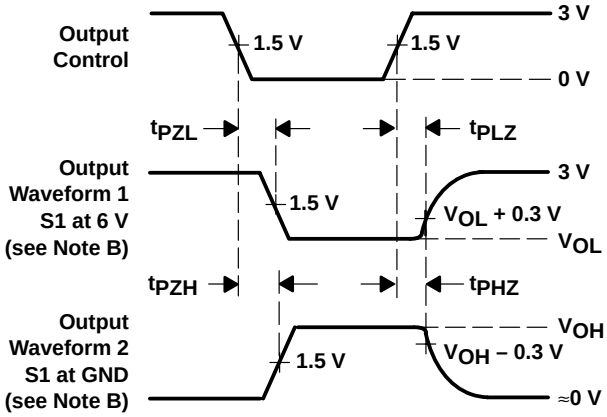
VOLTAGE WAVEFORMS
PULSE DURATION



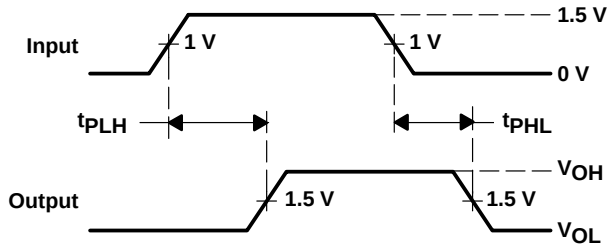
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to AO)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

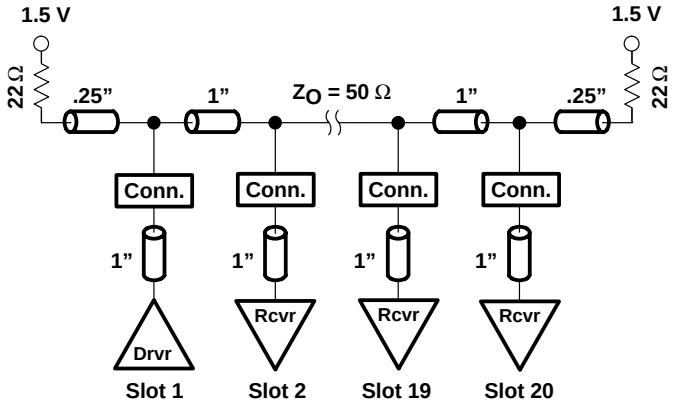


Figure 2. High-Drive Test Backplane

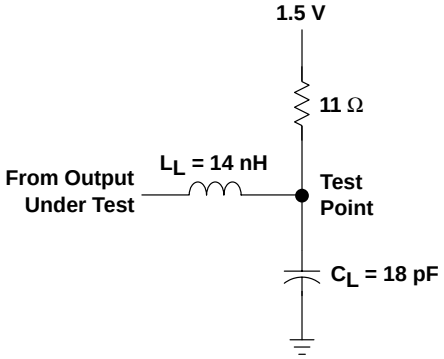


Figure 3. High-Drive RLC Network

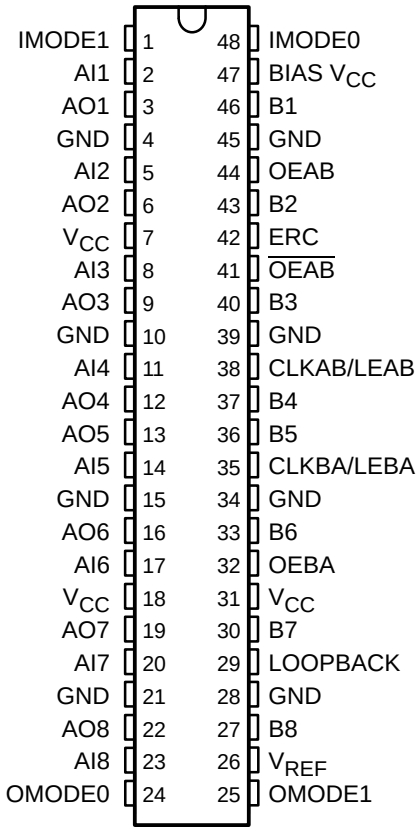
switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI (buffer)	B	Slow	4.7	ns
t_{PHL}				5	
t_{PLH}	AI (buffer)	B	Fast	3.7	ns
t_{PHL}				4	
t_{PLH}	LEAB (latch mode)	B	Slow	5.5	ns
t_{PHL}				5.8	
t_{PLH}	LEAB (latch mode)	B	Fast	4.6	ns
t_{PHL}				4.8	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	5.8	ns
t_{PHL}				6	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	4.9	ns
t_{PHL}				4.9	
t_{PLH}	OMODE	B	Slow	5.5	ns
t_{PHL}				5.7	
t_{PLH}	OMODE	B	Fast	4.5	ns
t_{PHL}				4.7	
t_r	Rise time, B-port outputs (20% to 80%)		Slow	1.8	ns
			Fast	1.1	
t_f	Fall time, B-port outputs (80% to 20%)		Slow	3.4	ns
			Fast	2.6	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Open-Drain Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLP2034 is a high-drive, 8-bit, three-wire registered transceiver that provides true LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent, latched, and flip-flop modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring, the same functionality as the SN74FB2033, but with true logic. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

OEC, TI-OPC, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP2034 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and can be directly driven by TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

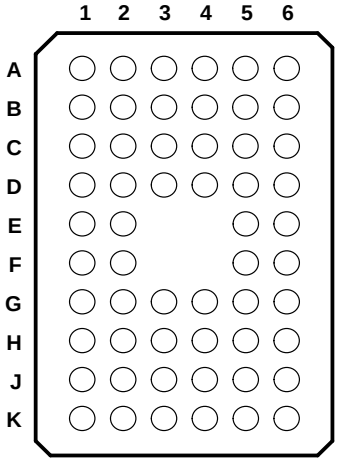
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OEAB}$ should be tied to V_{CC} through a pullup resistor and OEAB and OEBA should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	IMODE1	NC	NC	NC	NC	IMODE0
B	AO1	AI1	GND	GND	BIAS V_{CC}	B1
C	AO2	AI2	V_{CC}	ERC	OEAB	B2
D	AO3	AI3	GND	GND	$\overline{OEAB}$	B3
E	AO4	AI4			CLKAB/LEAB	B4
F	AO5	AI5			CLKBA/LEBA	B5
G	AO6	AI6	GND	GND	OEBA	B6
H	AO7	AI7	V_{CC}	V_{CC}	LOOPBACK	B7
J	AO8	AI8	GND	GND	V_{REF}	B8
K	OMODE0	NC	NC	NC	NC	OMODE1

NC = No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP2034DGGR	GTLP2034
	TVSOP – DGV	Tape and reel	SN74GTLP2034DGVR	GT2034
	VFBGA – GQL	Tape and reel	SN74GTLP2034GQLR	GR034

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP2034 is a high-drive (100 mA), 8-bit, three-wire registered transceiver containing D-type latches and D-type flip-flops for data-path operation in the transparent, latched, or flip-flop modes. Data transmission is true, with AI data going to the B port and B data going to AO. The split LVTTL AI and AO provides a feedback path for control and diagnostics monitoring.

The logic element for data flow in each direction is configured by two mode (IMODE1 and IMODE0 for B to A, OMODE1 and OMODE0 for A to B) inputs as a buffer, D-type flip-flop, or D-type latch. When configured in the buffer mode, the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock (CLKAB/LEAB or CLKBA/LEBA) input. In the latch mode, the clock inputs serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element is the B-to-A input.

The AO enable/disable control is provided by OEBA. When OEBA is low or when V_{CC} is less than 1.5 V, AO is in the high-impedance state. When OEBA is high, AO is active (high or low logic levels).

The B port is controlled by OEAB and $\overline{OEAB}$. If OEAB is low, $\overline{OEAB}$ is high, or V_{CC} is less than 1.5 V, the B port is inactive. If OEAB is high and $\overline{OEAB}$ is low, the B port is active.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO) or inactive (B port) states.

Function Tables

FUNCTION/MODE

INPUTS								OUTPUT	MODE
OEBA	OEAB	$\overline{OEAB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK		
L	L	X	X	X	X	X	X	Z	Isolation
L	X	H	X	X	X	X	X		
X	H	L	L	L	X	X	X	AI to B	Buffer
X	H	L	L	H	X	X	X		Flip-flop
X	H	L	H	X	X	X	X		Latch
H	L	X	X	X	L	L	L	B to AO	Buffer
H	X	H	X	X	L	L	L		
H	L	X	X	X	L	H	L	B to AO	Flip-flop
H	X	H	X	X	L	H	L		
H	L	X	X	X	H	X	L	B to AO	Latch
H	X	H	X	X	H	X	L		
H	L	X	X	X	L	L	H	AI to AO	Buffer
H	X	H	X	X	L	L	H		
H	L	X	X	X	L	H	H	AI to AO	Flip-flop
H	X	H	X	X	L	H	H		
H	L	X	X	X	H	X	H	AI to AO	Latch
H	X	H	X	X	H	X	H		
H	H	L	X	X	X	X	L	AI to B, B to AO	Transparent with feedback path

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEBA	OEAB	$\overline{OEAB}$	AO	B
L	X	X	Z	
H	X	X	Active	
X	L	L		Z
X	L	H		Z
X	H	L		Active
X	H	H		Z

BUFFER

INPUT	OUTPUT
L	L
H	H

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	L
H	H	H
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	B port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

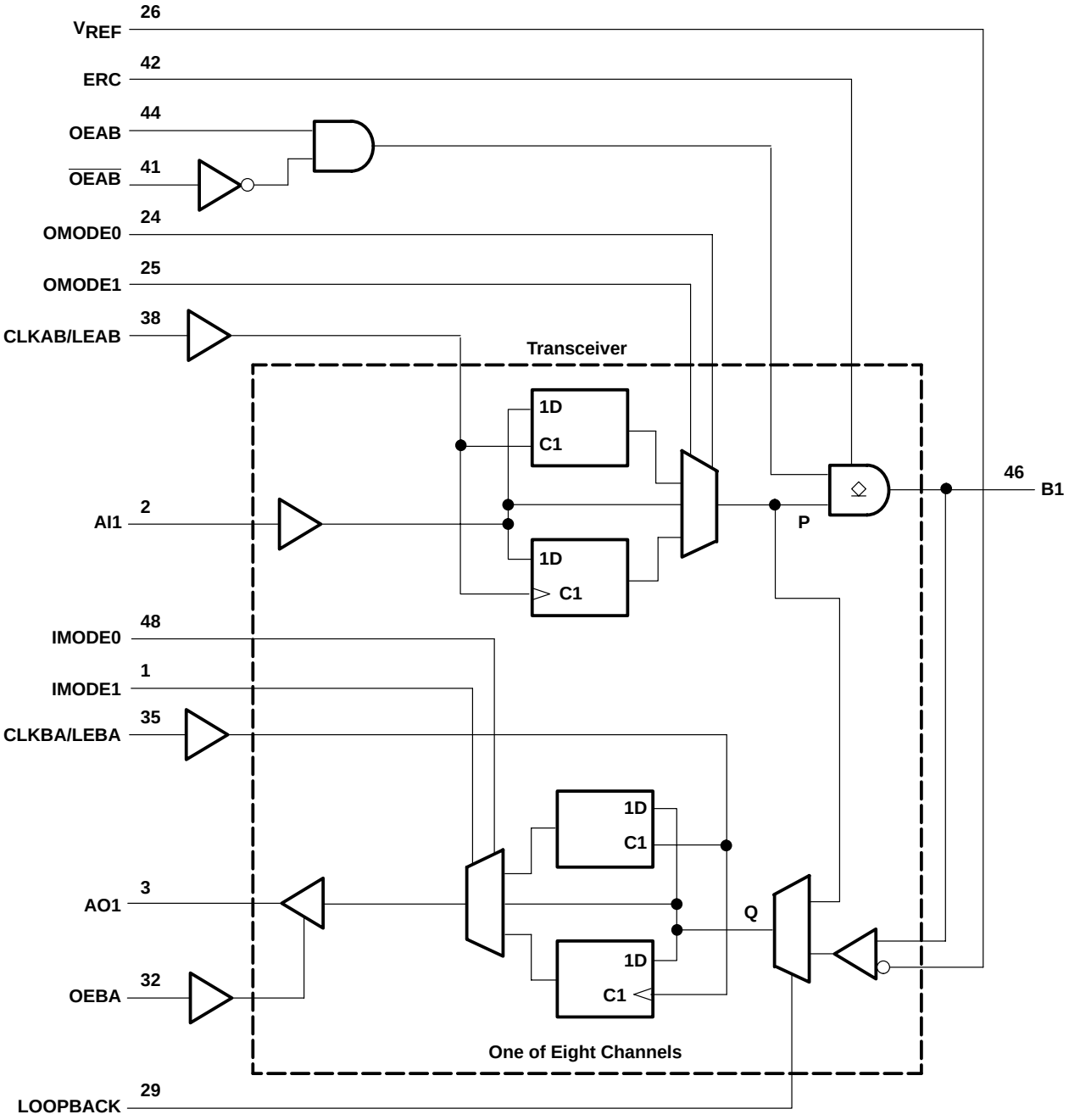
FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	L
↑	H	H

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC	OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	
H	Slow
L	Fast

functional block diagram



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): AI port, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): AO port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port	48 mA
B port	200 mA
Current into any A-port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port and V_{REF}		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO			–24	mA
I_{OL}	Low-level output current	AO			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	AI and control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZ}‡	AO	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	AO or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}§		V_{CC} = 3.45 V, One AI or control input at V_{CC} – 0.6 V, Other AI or control inputs at V_{CC} or GND				1.5	mA
C_i	AI	V_I = 3.15 V or 0			3.5	4.5	pF
	Control inputs				3.5	5.5	
C_o	AO	V_O = 3.15 V or 0			5	6	pF
C_{io}	B port	V_O = 1.5 V or 0			8.5	10	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}				±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0, BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}			±30	±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	2.8		ns
t_{su}	Setup time	AI before CLKAB↑	1.1		ns
		AI before CLKBA↑	1.4		
		B before CLKBA↑	1.3		
		AI before LEAB↓	1.3		
		AI before LEBA↓	2.1		
		B before LEBA↓	2.2		
t_h	Hold time	AI after CLKAB↑	0.3		ns
		AI after CLKBA↑	0.2		
		B after CLKBA↑	0.2		
		AI after LEAB↓	0.3		
		AI after LEBA↓	0		
		B after LEBA↓	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	AI (buffer)	B	Slow	3		7.1	ns
t_{PHL}				3		7	
t_{PLH}	AI (buffer)	B	Fast	2		5.6	ns
t_{PHL}				2		5.7	
t_{PLH}	B (buffer)	AO	–	1		5.4	ns
t_{PHL}				1		4.8	
t_{PLH}	LEAB (latch mode)	B	Slow	4.2		8.5	ns
t_{PHL}				3.2		7.3	
t_{PLH}	LEAB (latch mode)	B	Fast	3.2		7.1	ns
t_{PHL}				2.8		6.3	
t_{PLH}	LEAB (latch mode)	AO	–	2		6.6	ns
t_{PHL}				1.8		5.8	
t_{PLH}	LEBA (latch mode)	AO	–	1		5.3	ns
t_{PHL}				1		4.5	
t_{PLH}	OEAB	B	Slow	3.8		7.5	ns
t_{PHL}				3.1		7	
t_{PLH}	OEAB	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PLH}	$\overline{OEAB}$	B	Slow	3.5		7.5	ns
t_{PHL}				3		7.2	
t_{PLH}	$\overline{OEAB}$	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PZH}	OEBA	AO	–	1		4.7	ns
t_{PZL}				1		3.4	
t_{PHZ}	OEBA	AO	–	1		5.2	ns
t_{PLZ}				1		4.9	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	4.4		8.6	ns
t_{PHL}				3.6		8	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	3.2		7.1	ns
t_{PHL}				3.1		6.8	
t_{PLH}	CLKAB (flip-flop mode)	AO	–	2		6.9	ns
t_{PHL}				1.8		6.4	
t_{PLH}	CLKBA (flip-flop mode)	AO	–	1		5.6	ns
t_{PHL}				1		4.9	
t_{PLH}	OMODE	B	Slow	3.8		8.7	ns
t_{PHL}				3.2		8.2	
t_{PLH}	OMODE	B	Fast	2.7		7	ns
t_{PHL}				2.7		7	
t_{PLH}	IMODE	AO	–	1		5.6	ns
t_{PHL}				1		4.6	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	LOOPBACK	AO	–	2.5		5.5	ns
t_{PHL}				2		4.7	
t_{PLH}	AI (loopback high)	AO	–	1		5.3	ns
t_{PHL}				1		4.9	
t_r	Rise time, B-port outputs (20% to 80%)		Slow		2.8		ns
			Fast		1.5		
	Rise time, AO (10% to 90%)				3.5		
t_f	Fall time, B-port outputs (80% to 20%)		Slow		3		ns
			Fast		1.8		
	Fall time, AO (90% to 10%)				1.5		

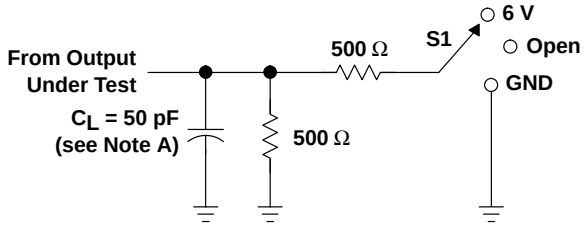
† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)§

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}$¶	AI	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	AI	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(t)}$¶	AI	B	Slow		1.4	2	ns
			Fast		0.6	1.4	
	CLKAB/LEAB	B	Slow		1.8	2.5	
			Fast		0.9	1.8	

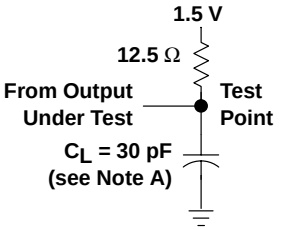
† Slow (ERC = L) and Fast (ERC = H)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION

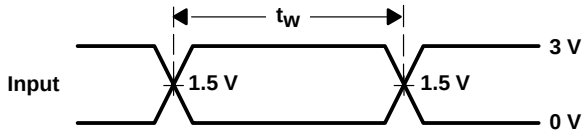


LOAD CIRCUIT FOR A OUTPUTS

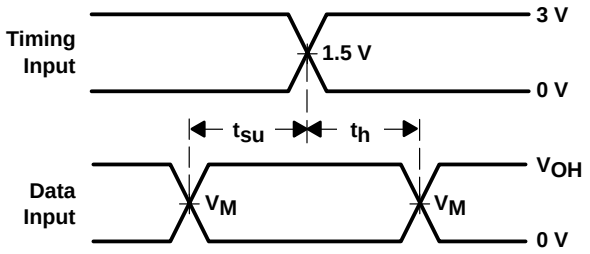
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



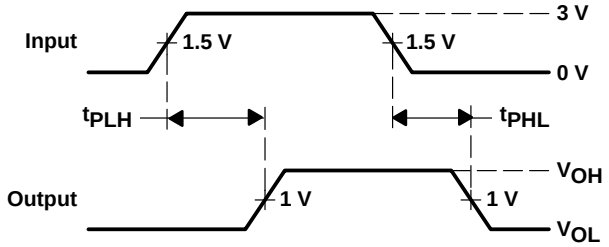
LOAD CIRCUIT FOR B OUTPUTS



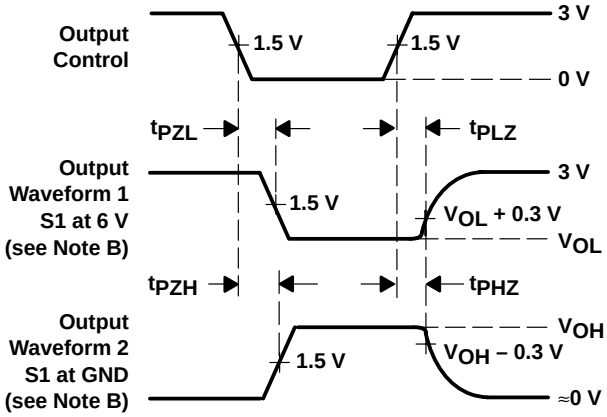
VOLTAGE WAVEFORMS
PULSE DURATION



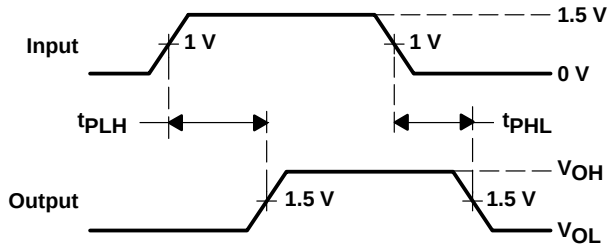
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to AO)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

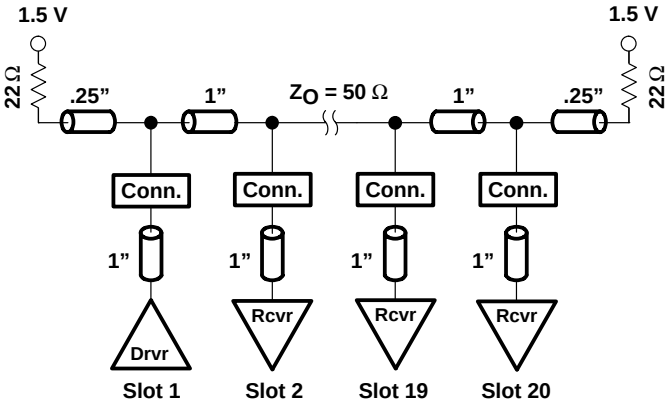


Figure 2. High-Drive Test Backplane

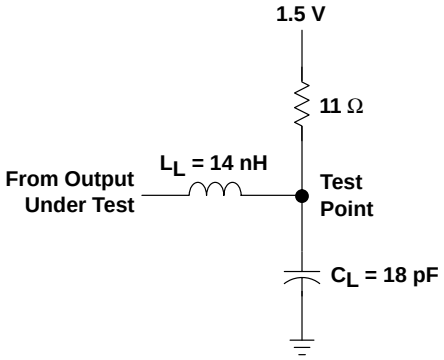


Figure 3. High-Drive RLC Network

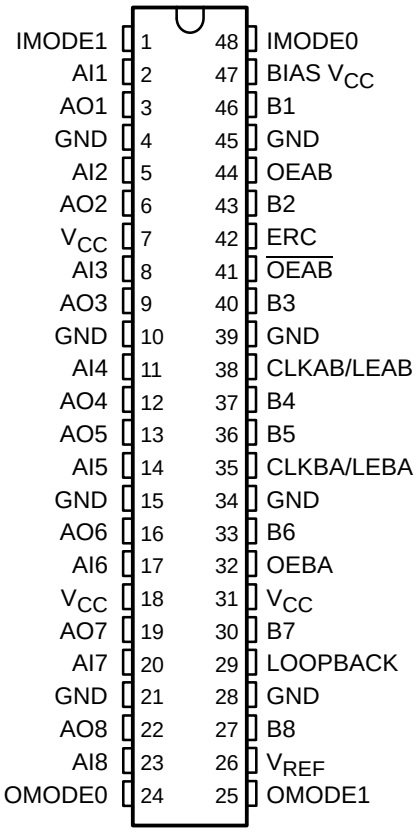
switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI (buffer)	B	Slow	5.7	ns
t_{PHL}				5.2	
t_{PLH}	AI (buffer)	B	Fast	3.7	ns
t_{PHL}				4.1	
t_{PLH}	LEAB (latch mode)	B	Slow	5.9	ns
t_{PHL}				5.7	
t_{PLH}	LEAB (latch mode)	B	Fast	4.8	ns
t_{PHL}				4.8	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	5.7	ns
t_{PHL}				6.4	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	4.7	ns
t_{PHL}				5.2	
t_{PLH}	OMODE	B	Slow	5.4	ns
t_{PHL}				6	
t_{PLH}	OMODE	B	Fast	4.5	ns
t_{PHL}				4.9	
t_r	Rise time, B-port outputs (20% to 80%)		Slow	2	ns
			Fast	1.1	
t_f	Fall time, B-port outputs (80% to 20%)		Slow	3.3	ns
			Fast	2.3	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **AO Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Open-Drain Outputs (100 mA)**
- **LVTTL Outputs (–12 mA/12 mA)**
- **Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLP22034 is a high-drive, 8-bit, three-wire registered transceiver that provides true LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent, latched, and flip-flop modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring, the same functionality as the SN74FB2033, but with true logic. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

The AO outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

OEC, TI-OPC, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP22034 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and can be directly driven by TTL or 5-V CMOS devices. V_{REF} is the B-port differential input reference voltage.

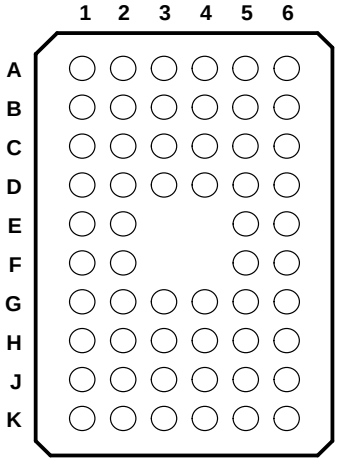
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OEAB}$ should be tied to V_{CC} through a pullup resistor and OEAB and OEBA should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	IMODE1	NC	NC	NC	NC	IMODE0
B	AO1	AI1	GND	GND	BIAS V_{CC}	B1
C	AO2	AI2	V_{CC}	ERC	OEAB	B2
D	AO3	AI3	GND	GND	$\overline{OEAB}$	B3
E	AO4	AI4			CLKAB/LEAB	B4
F	AO5	AI5			CLKBA/LEBA	B5
G	AO6	AI6	GND	GND	OEBA	B6
H	AO7	AI7	V_{CC}	V_{CC}	LOOPBACK	B7
J	AO8	AI8	GND	GND	V_{REF}	B8
K	OMODE0	NC	NC	NC	NC	OMODE1

NC = No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP22034DGGR	GTLP22034
	TVSOP – DGV	Tape and reel	SN74GTLP22034DGVR	GT22034
	VFBGA – GQL	Tape and reel	SN74GTLP22034GQLR	GS034

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLP22034 is a high-drive (100 mA), 8-bit, three-wire registered transceiver containing D-type latches and D-type flip-flops for data-path operation in the transparent, latched, or flip-flop modes. Data transmission is true, with AI data going to the B port and B data going to AO. The split LVTTL AI and AO provides a feedback path for control and diagnostics monitoring.

The logic element for data flow in each direction is configured by two mode (IMODE1 and IMODE0 for B to A, OMODE1 and OMODE0 for A to B) inputs as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock (CLKAB/LEAB or CLKBA/LEBA) input. In the latch mode, the clock inputs serve as active-high transparent latch enables.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, B-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element is the B-to-A input.

The AO enable/disable control is provided by OEBA. When OEBA is low or when V_{CC} is less than 1.5 V, AO is in the high-impedance state. When OEBA is high, AO is active (high or low logic levels).

The B port is controlled by OEAB and $\overline{OEAB}$. If OEAB is low, $\overline{OEAB}$ is high, or V_{CC} is less than 1.5 V, the B port is inactive. If OEAB is high and $\overline{OEAB}$ is low, the B port is active.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO) or inactive (B port) states.

Function Tables

FUNCTION/MODE

INPUTS								OUTPUT	MODE
OEBA	OEAB	$\overline{OEAB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK		
L	L	X	X	X	X	X	X	Z	Isolation
L	X	H	X	X	X	X	X		
X	H	L	L	L	X	X	X	AI to B	Buffer
X	H	L	L	H	X	X	X		Flip-flop
X	H	L	H	X	X	X	X		Latch
H	L	X	X	X	L	L	L	B to AO	Buffer
H	X	H	X	X	L	L	L		
H	L	X	X	X	L	H	L	B to AO	Flip-flop
H	X	H	X	X	L	H	L		
H	L	X	X	X	H	X	L	B to AO	Latch
H	X	H	X	X	H	X	L		
H	L	X	X	X	L	L	H	AI to AO	Buffer
H	X	H	X	X	L	L	H		
H	L	X	X	X	L	H	H	AI to AO	Flip-flop
H	X	H	X	X	L	H	H		
H	L	X	X	X	H	X	H	AI to AO	Latch
H	X	H	X	X	H	X	H		
H	H	L	X	X	X	X	L	AI to B, B to AO	Transparent with feedback path

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEBA	OEAB	$\overline{OEAB}$	AO	B
L	X	X	Z	
H	X	X	Active	
X	L	L		Z
X	L	H		Z
X	H	L		Active
X	H	H		Z

BUFFER

INPUT	OUTPUT
L	L
H	H

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	L
H	H	H
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	B port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

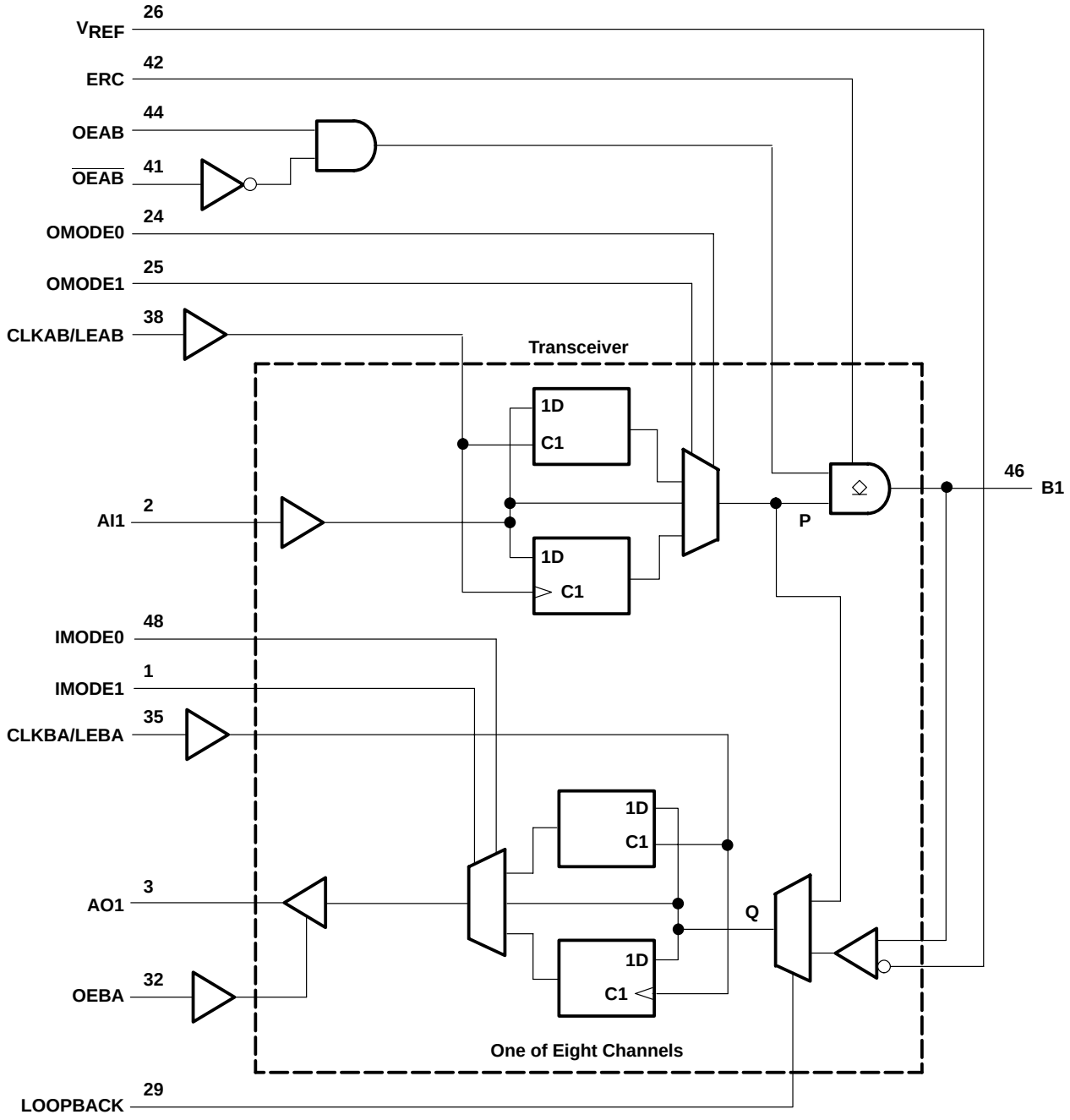
FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	L
↑	H	H

B-PORT EDGE-RATE CONTROL (ERC)

INPUT ERC	OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	
H	Slow
L	Fast

functional block diagram



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): AI port, ERC, and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): AO port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: AO port	24 mA
B port	200 mA
Current into any A-port output in the high state, I_O (see Note 2)	24 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port and V_{REF}		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO			–12	mA
I_{OL}	Low-level output current	AO			12	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused control and B-port inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2			
V_{OL}	AO	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA			0.8	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	AI and control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZ}‡	AO	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	µA
	B port	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	
I_{CC}	AO or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
ΔI_{CC}§		V_{CC} = 3.45 V, One AI or control input at V_{CC} – 0.6 V, Other AI or control inputs at V_{CC} or GND				1.5	mA
C_i	AI	V_I = 3.15 V or 0			3.5	4.5	pF
	Control inputs				3.5	5.5	
C_o	AO	V_O = 3.15 V or 0			5	6	pF
C_{io}	B port	V_O = 1.5 V or 0			8.5	10	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	OEBA = V_{CC}		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}			±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0, V_O = 0.5 V to 1.5 V, $\overline{OEAB}$ = 0 and OEAB = V_{CC}			±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	2.8		ns
t_{su}	Setup time	AI before CLKAB↑	1.1		ns
		AI before CLKBA↑	1.4		
		B before CLKBA↑	1.3		
		AI before LEAB↓	1.3		
		AI before LEBA↓	2.1		
		B before LEBA↓	2.2		
t_h	Hold time	AI after CLKAB↑	0.3		ns
		AI after CLKBA↑	0.2		
		B after CLKBA↑	0.2		
		AI after LEAB↓	0.3		
		AI after LEBA↓	0		
		B after LEBA↓	0		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	AI (buffer)	B	Slow	3		7.1	ns
t_{PHL}				3		7	
t_{PLH}	AI (buffer)	B	Fast	2		5.6	ns
t_{PHL}				2		5.7	
t_{PLH}	B (buffer)	AO	–	1		5.8	ns
t_{PHL}				1		5.2	
t_{PLH}	LEAB (latch mode)	B	Slow	4.2		8.5	ns
t_{PHL}				3.2		7.3	
t_{PLH}	LEAB (latch mode)	B	Fast	3.2		7.1	ns
t_{PHL}				2.8		6.3	
t_{PLH}	LEAB (latch mode)	AO	–	2		6.9	ns
t_{PHL}				1.8		6.1	
t_{PLH}	LEBA (latch mode)	AO	–	1		5.6	ns
t_{PHL}				1		5	
t_{PLH}	OEAB	B	Slow	3.8		7.5	ns
t_{PHL}				3.1		7	
t_{PLH}	OEAB	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PLH}	$\overline{OEAB}$	B	Slow	3.5		7.5	ns
t_{PHL}				3		7.2	
t_{PLH}	$\overline{OEAB}$	B	Fast	2.5		6	ns
t_{PHL}				2.5		6	
t_{PZH}	OEBA	AO	–	1		5.3	ns
t_{PZL}				1		4.2	
t_{PHZ}	OEBA	AO	–	1		5.5	ns
t_{PLZ}				1		5.2	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	4.4		8.6	ns
t_{PHL}				3.6		8	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	3.2		7.1	ns
t_{PHL}				3.1		6.8	
t_{PLH}	CLKAB (flip-flop mode)	AO	–	2		7.5	ns
t_{PHL}				1.8		7	
t_{PLH}	CLKBA (flip-flop mode)	AO	–	1		6	ns
t_{PHL}				1		5.6	
t_{PLH}	OMODE	B	Slow	3.8		8.7	ns
t_{PHL}				3.2		8.2	
t_{PLH}	OMODE	B	Fast	2.7		7	ns
t_{PHL}				2.7		7	
t_{PLH}	IMODE	AO	–	1		6	ns
t_{PHL}				1		5.1	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1) (continued)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{PLH}	LOOPBACK	AO	–	2.5		6.1	ns
t_{PHL}				2		5.1	
t_{PLH}	AI (loopback high)	AO	–	1		5.7	ns
t_{PHL}				1		5.4	
t_r	Rise time, B-port outputs (20% to 80%)		Slow		2.8		ns
			Fast		1.5		
	Rise time, AO (10% to 90%)				5.5		
t_f	Fall time, B-port outputs (80% to 20%)		Slow		3		ns
			Fast		1.8		
	Fall time, AO (90% to 10%)				4.5		

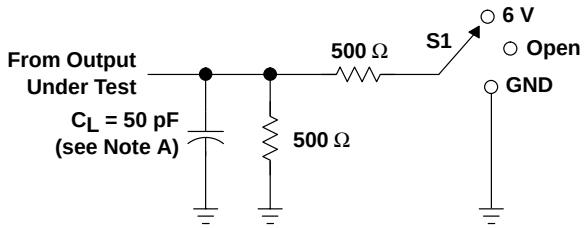
† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

skew characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)§

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
$t_{sk(LH)}$¶	AI	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	AI	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Slow		0.5	1	ns
$t_{sk(HL)}$¶					0.5	1	
$t_{sk(LH)}$¶	CLKAB/LEAB	B	Fast		0.4	0.9	ns
$t_{sk(HL)}$¶					0.4	0.9	
$t_{sk(t)}$¶	AI	B	Slow		1.4	2	ns
			Fast		0.6	1.4	
	CLKAB/LEAB	B	Slow		1.8	2.5	
			Fast		0.9	1.8	

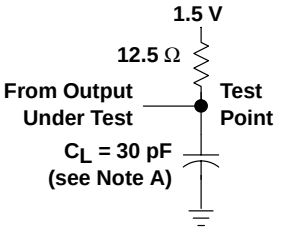
† Slow (ERC = L) and Fast (ERC = H)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
¶ $t_{sk(LH)}$/$t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in the same direction either high to low [$t_{sk(HL)}$] or low to high [$t_{sk(LH)}$] or in opposite directions, both low to high and high to low [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION

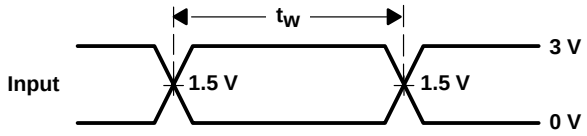


LOAD CIRCUIT FOR A OUTPUTS

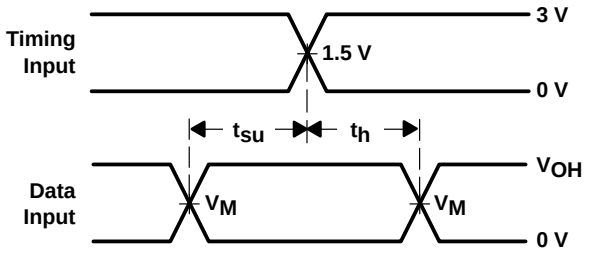
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



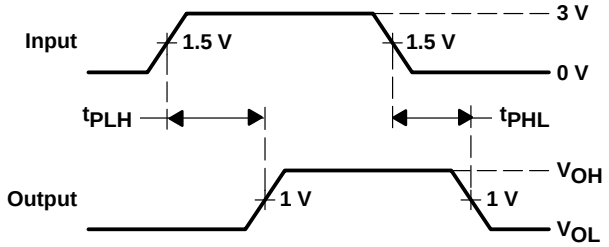
LOAD CIRCUIT FOR B OUTPUTS



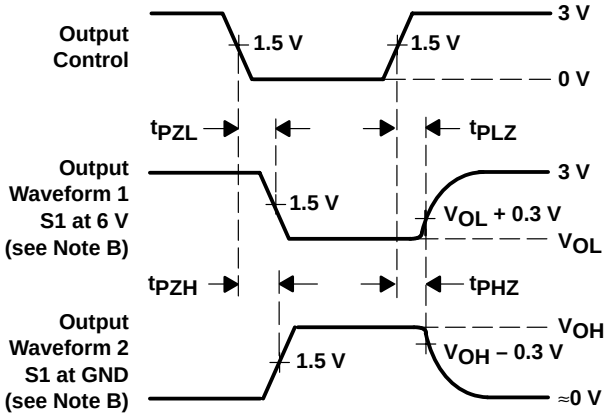
VOLTAGE WAVEFORMS
PULSE DURATION



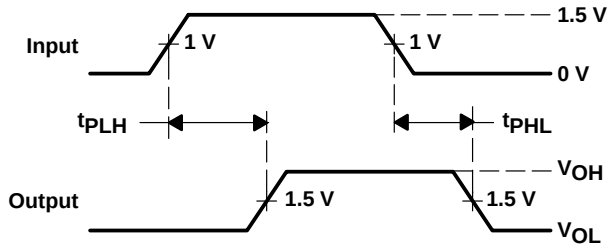
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(AI to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(AO)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to AO)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application is probably a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

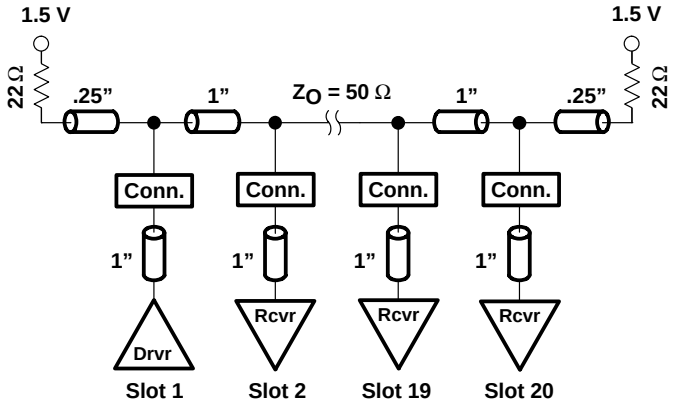


Figure 2. High-Drive Test Backplane

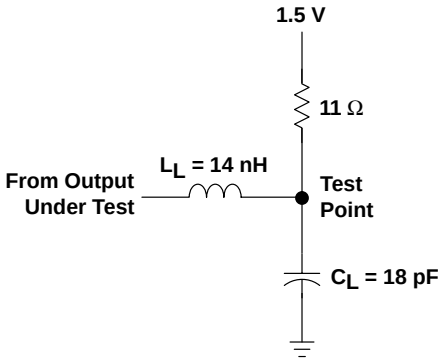


Figure 3. High-Drive RLC Network

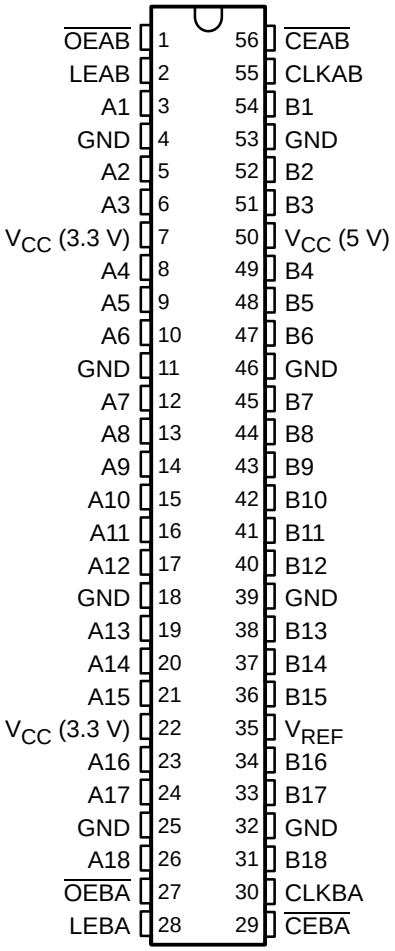
switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	AI (buffer)	B	Slow	5.7	ns
t_{PHL}				5.2	
t_{PLH}	AI (buffer)	B	Fast	3.7	ns
t_{PHL}				4.1	
t_{PLH}	LEAB (latch mode)	B	Slow	5.9	ns
t_{PHL}				5.7	
t_{PLH}	LEAB (latch mode)	B	Fast	4.8	ns
t_{PHL}				4.8	
t_{PLH}	CLKAB (flip-flop mode)	B	Slow	5.7	ns
t_{PHL}				6.4	
t_{PLH}	CLKAB (flip-flop mode)	B	Fast	4.7	ns
t_{PHL}				5.2	
t_{PLH}	OMODE	B	Slow	5.4	ns
t_{PHL}				6	
t_{PLH}	OMODE	B	Fast	4.5	ns
t_{PHL}				4.9	
t_r	Rise time, B-port outputs (20% to 80%)		Slow	2	ns
			Fast	1.1	
t_f	Fall time, B-port outputs (80% to 20%)		Slow	3.3	ns
			Fast	2.3	

† Slow (ERC = H) and Fast (ERC = L)
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (34 mA)**
- **LVTTL Outputs (–32 mA/64 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on A-Port Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTLPH16612 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. This device provides a high-speed interface between cards operating at LVTTL logic levels and backplanes operating at GTLP signal levels. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. These improvements minimize bus-settling time and have been designed and tested using several backplane models.

GTLP is a TI™ derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16612 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

The B port normally operates at GTLP levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

To improve signal integrity, the SN74GTLPH16612 B-port output transition time is optimized for distributed backplane loads.

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description (continued)

V_{CC} (5 V) supplies the internal and GTLP circuitry, while V_{CC} (3.3 V) supplies the LVTTL output buffers.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTLPH16612DL	GTLPH16612
		Tape and reel	SN74GTLPH16612DLR	
	TSSOP – DGG	Tape and reel	SN74GTLPH16612GR	GTLPH16612

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16612 is a medium-drive (34 mA), 18-bit UBT transceiver, containing D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16612 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH16612 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by the clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{OEAB}$ and $\overline{OEBA}$).

For A-to-B data flow, when $\overline{CEAB}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{CEAB}$ and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

The data flow for B-to-A is similar to that of A-to-B, except that $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA are used.

FUNCTION TABLE†

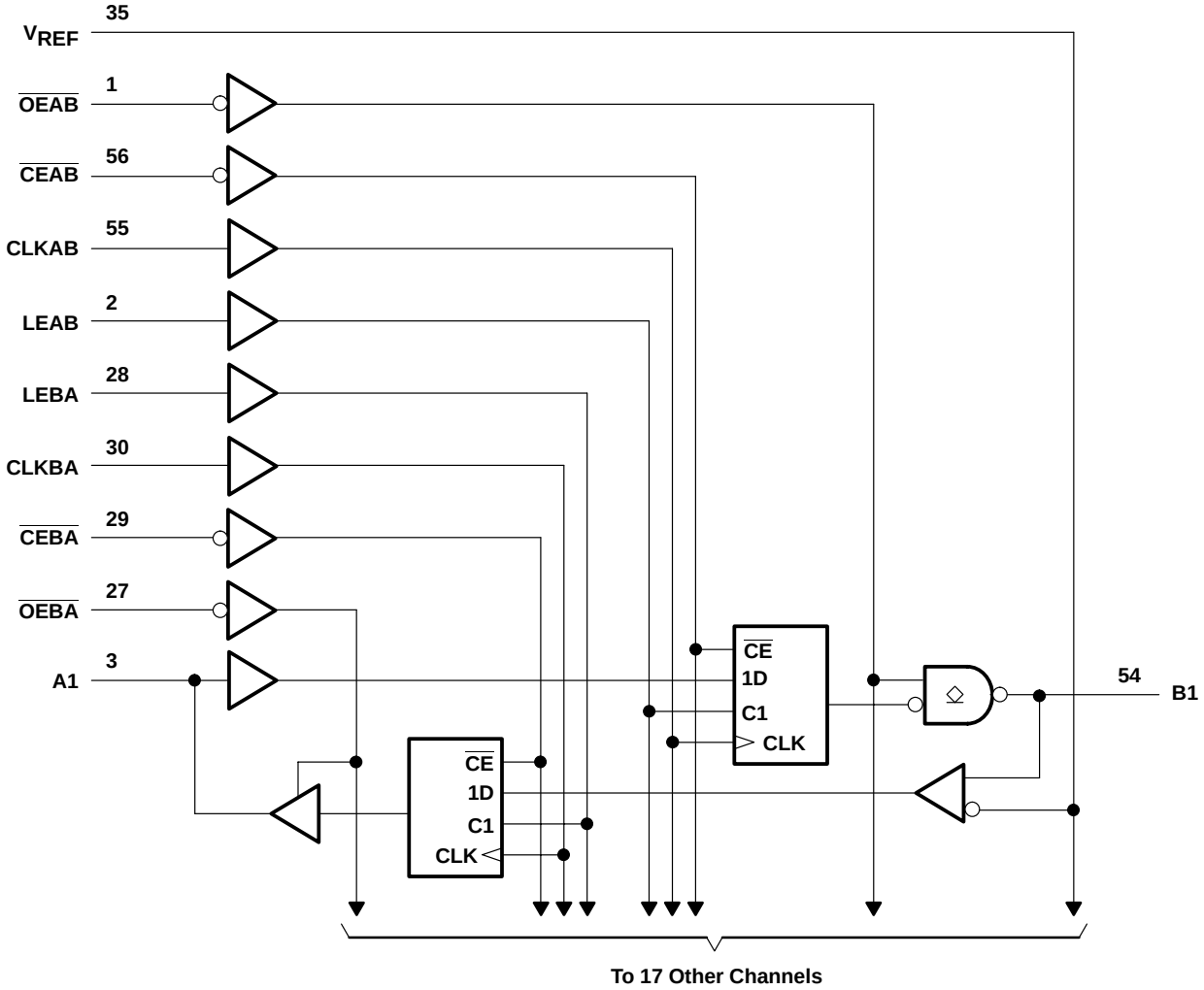
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . . –0.5 V to 4.6 V
5 V . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 128 mA
B port . . . . . 80 mA
Current into any A port output in the high state, I_O (see Note 2) . . . . . 64 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 64°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–32	mA
I_{OL}	Low-level output current	A port			64	mA
		B port			34	
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V		I_{OH} = –100 µA	V_{CC} (3.3 V) –0.2			V
		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			
				I_{OH} = –32 mA	2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OL} = 100 µA			0.2	V
				I_{OL} = 16 mA			0.4	
				I_{OL} = 32 mA			0.5	
				I_{OL} = 64 mA			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_{OL} = 34 mA			0.65	
I_I	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V,	V_{CC} (5 V) = 0 or 5.25 V,	V_I = 5.5 V			10	µA
	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20	
				V_I = V_{CC} (3.3 V)			1	
				V_I = 0			–30	
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5	
				V_I = 0			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				100	µA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			µA
				V_I = 2 V	–75			
				V_I = 0 to V_{CC} (3.3 V)‡			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = V_{CC} (3.3 V)			1	µA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 1.5 V			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0			–1	µA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0.65 V			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND§, V_I = V_{TT} or GND¶		Outputs high			1	mA
				Outputs low			5	
				Outputs disabled			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND§, V_I = V_{TT} or GND¶		Outputs high			120	mA
				Outputs low			120	
				Outputs disabled			120	
ΔI_{CC} (3.3 V)#		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, One A-port or control input at 2.7 V, Other A-port or control inputs at V_{CC} (3.3 V) or GND					1	mA
C_i	Control inputs	V_I = 3.15 V or 0				4		pF
C_{io}	A port	V_O = 3.15 V or 0				8.5		pF
	B port	V_O = 1.5 V or 0				8		

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the V_I for A-port or control inputs.
¶ This is the V_I for B port.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted) (see Figure 1)

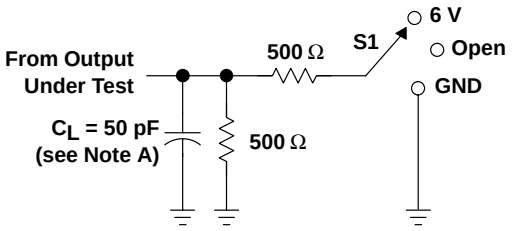
			MIN	MAX	UNIT
f_{clock}	Clock frequency			85	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.7		
t_{su}	Setup time	A before CLKAB↑	1		ns
		B before CLKBA↑	1.8		
		A before LEAB↓	0.5		
		B before LEBA↓	1.2		
		$\overline{CEAB}$ before CLKAB↑	1.2		
		$\overline{CEBA}$ before CLKBA↑	1.4		
t_h	Hold time	A after CLKAB↑	1.9		ns
		B after CLKBA↑	0.5		
		A after LEAB↓	2.7		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.2		
		$\overline{CEBA}$ after CLKBA↑	1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			85			MHz
t_{PLH}	A	B	2.5		6.9	ns
t_{PHL}			2.5		6.9	
t_{PLH}	LEAB	B	3.2		7.3	ns
t_{PHL}			3.2		7.3	
t_{PLH}	CLKAB	B	3.4		7.8	ns
t_{PHL}			3.4		7.8	
t_{en}	$\overline{OEAB}$	B	2.8		7	ns
t_{dis}			2.8		7	
t_r	Transition time, B outputs (20% to 80%)			2.6		ns
t_f	Transition time, B outputs (80% to 20%)			2.6		ns
t_{PLH}	B	A	1.5		5.7	ns
t_{PHL}			1.5		5.7	
t_{PLH}	LEBA	A	1.8		5.7	ns
t_{PHL}			1.8		5.7	
t_{PLH}	CLKBA	A	2.3		5.5	ns
t_{PHL}			2.3		5.5	
t_{en}	$\overline{OEBA}$	A	1.8		6.1	ns
t_{dis}			1.8		6.1	

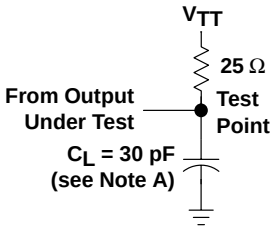
† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

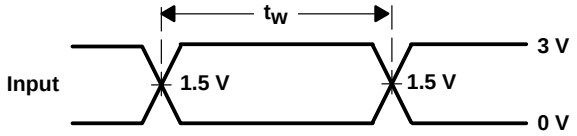


LOAD CIRCUIT FOR A OUTPUTS

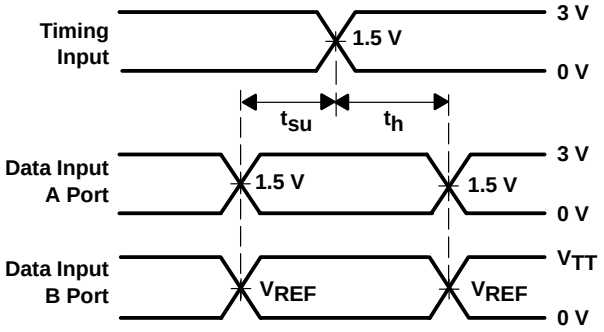
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



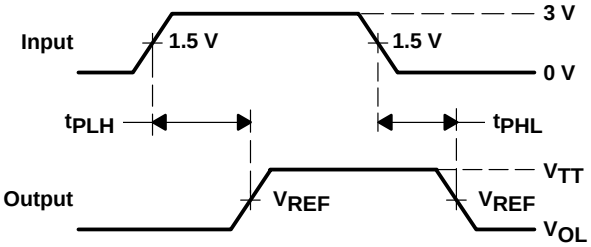
LOAD CIRCUIT FOR B OUTPUTS



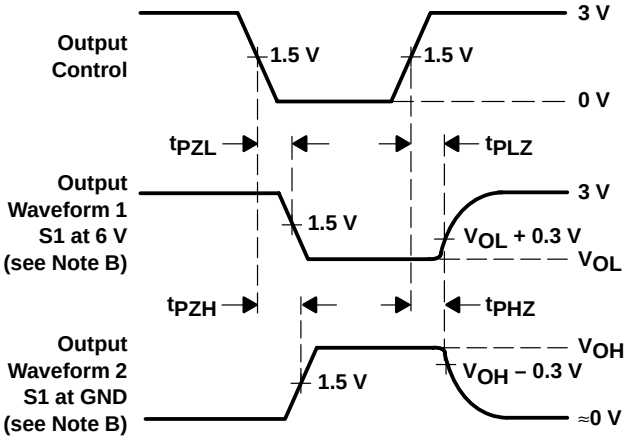
VOLTAGE WAVEFORMS
PULSE DURATION



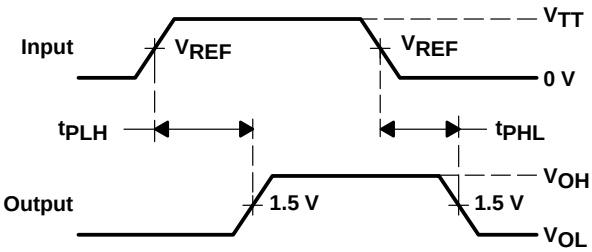
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The previous switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to an RLC circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

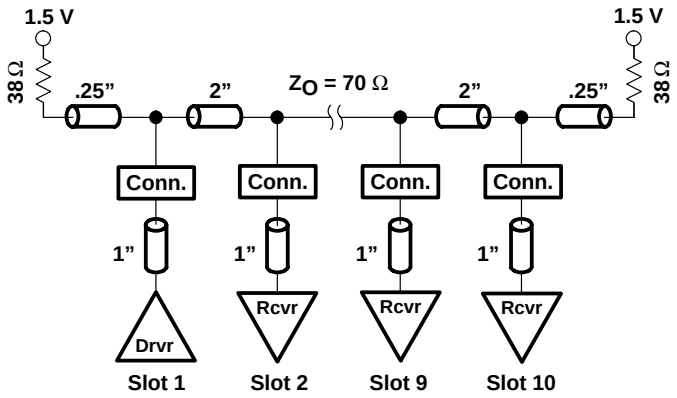


Figure 2. Medium-Drive Test Backplane

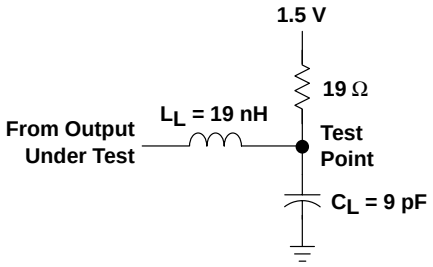


Figure 3. Medium-Drive RLC Network

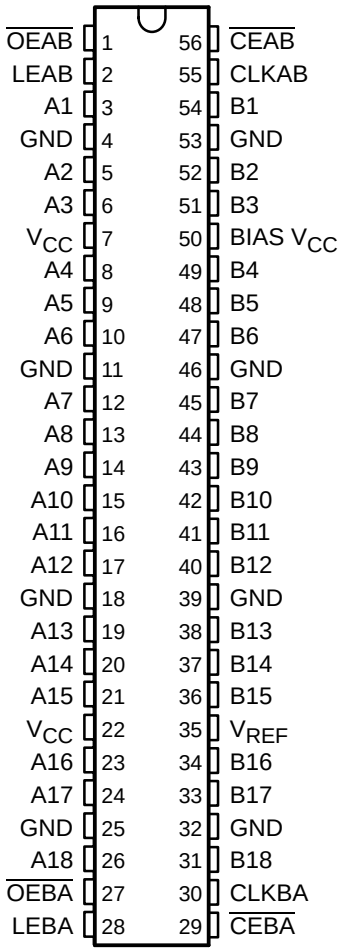
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	UNIT
f_{max}			85		MHz
t_{PLH}	A	B		3.6	ns
t_{PHL}				3.6	
t_{PLH}	LEAB	B		4.3	ns
t_{PHL}				4.3	
t_{PLH}	CLKAB	B		4.4	ns
t_{PHL}				4.4	
t_{en}	$\overline{OEAB}$	B		4.1	ns
t_{dis}				4.3	
t_r	Rise time, B outputs (20% to 80%)			1.4	ns
t_f	Fall time, B outputs (80% to 20%)			2.1	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and Clock-Enabled Modes**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLPH16912 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16912 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

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description (continued)

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16912GR	GTLPH16912
	TVSOP – DGV	Tape and reel	SN74GTLPH16912VR	GL912

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16912 is a medium-drive (50 mA), 18-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16912 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH16912 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{OEAB}$ and $\overline{OEBA}$). $\overline{CEAB}$ and $\overline{CEBA}$ and $\overline{OEAB}$ and $\overline{OEBA}$ control the 18 bits of data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{CEAB}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{CEAB}$ and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low). If LEAB is high, the device is in transparent mode. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA are used.

FUNCTION TABLE†

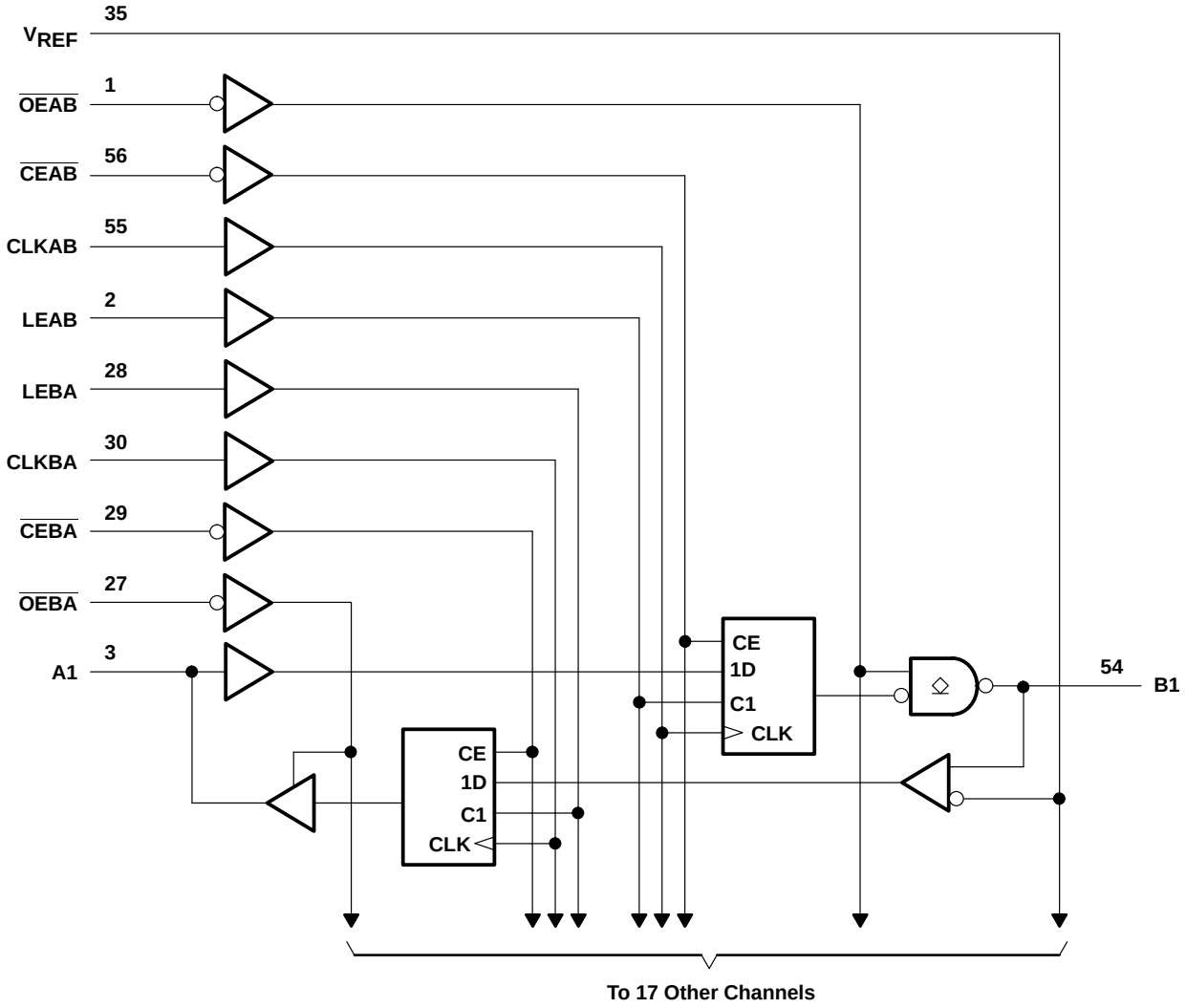
INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DGV package	48°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±10	µA
			V_I = 5.5 V			±20	
	B port		V_I = 0 to 1.5 V			±10	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5.5	pF
C_{io}	A port	V_O = 3.15 V or 0			7	8.5	pF
	B port	V_O = 1.5 V or 0			8.5	9.5	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

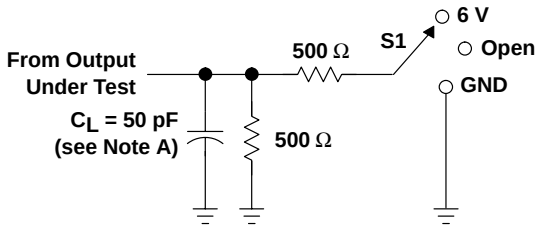
			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	2.8		ns
		CLKAB or CLKBA high or low	2.8		
t_{su}	Setup time	A before CLKAB↑	1.8		ns
		B before CLKBA↑	1.5		
		A before LEAB↓	1		
		B before LEBA↓	2		
		$\overline{CEAB}$ before CLKAB↑	1.5		
		$\overline{CEBA}$ before CLKBA↑	1.4		
t_h	Hold time	A after CLKAB↑	0.3		ns
		B after CLKBA↑	0.4		
		A after LEAB↓	1.1		
		B after LEBA↓	0.4		
		$\overline{CEAB}$ after CLKAB↑	1		
		$\overline{CEBA}$ after CLKBA↑	1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			175			MHz
t_{PLH}	A	B	2.1		6	ns
t_{PHL}			2.1		6	
t_{PLH}	LEAB	B	2.2		6.3	ns
t_{PHL}			2.2		6.3	
t_{PLH}	CLKAB	B	2.2		6.5	ns
t_{PHL}			2.2		6.5	
t_{en}	$\overline{OEAB}$	B	2		6.5	ns
t_{dis}			2		6.1	
t_r	Rise time, B outputs (20% to 80%)			2.4		ns
t_f	Fall time, B outputs (80% to 20%)			2		ns
t_{PLH}	B	A	1.8		5.8	ns
t_{PHL}			1.8		5.8	
t_{PLH}	LEBA	A	0.4		5.3	ns
t_{PHL}			0.4		5.3	
t_{PLH}	CLKBA	A	.6		5.6	ns
t_{PHL}			.6		5.7	
t_{en}	$\overline{OEBA}$	A	0.3		6.2	ns
t_{dis}			0.3		5.9	

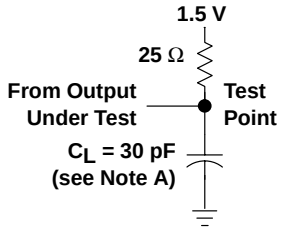
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

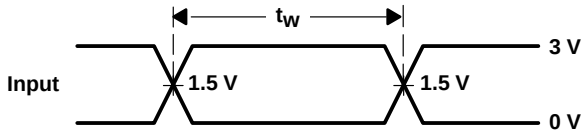


LOAD CIRCUIT FOR A OUTPUTS

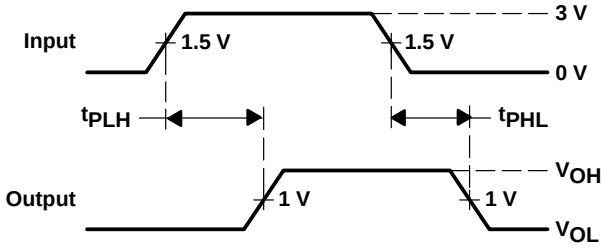
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



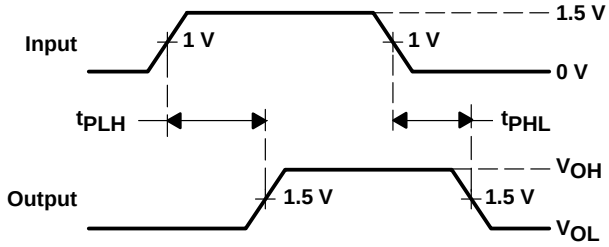
LOAD CIRCUIT FOR B OUTPUTS



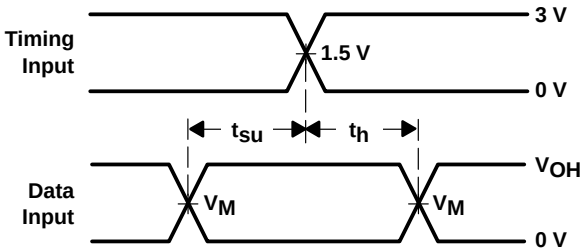
VOLTAGE WAVEFORMS
PULSE DURATION



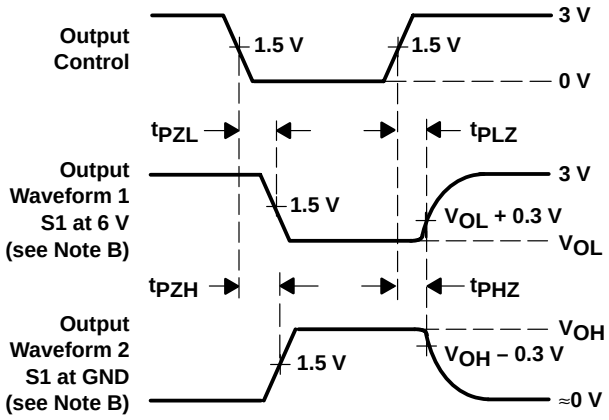
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

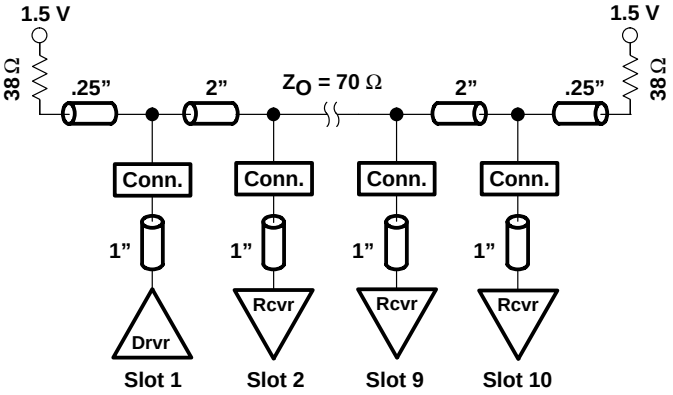


Figure 2. Medium-Drive Test Backplane

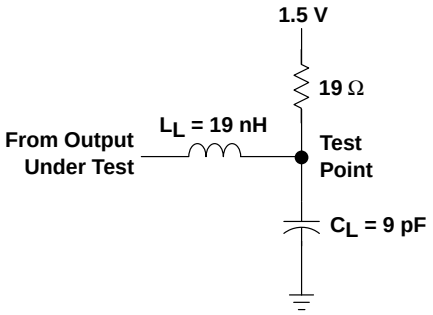


Figure 3. Medium-Drive RLC Network

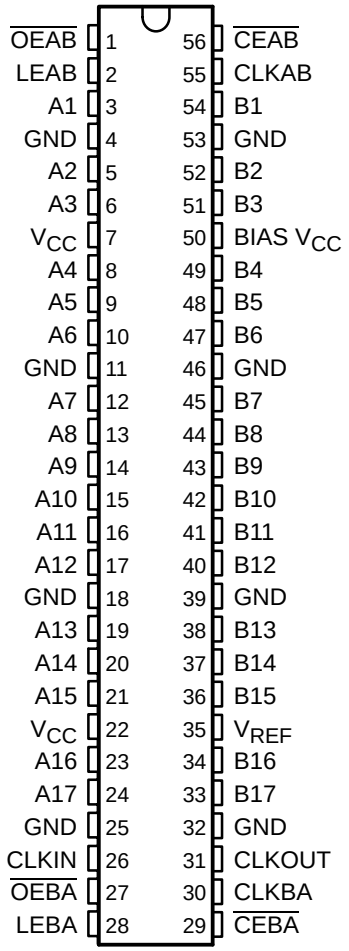
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	4.5	ns
t_{PHL}			4.5	
t_{PLH}	LEAB	B	4.7	ns
t_{PHL}			4.7	
t_{PLH}	CLKAB	B	4.7	ns
t_{PHL}			4.7	
t_{en}	$\overline{OEAB}$	B	4.8	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1.2	ns
t_f	Fall time, B outputs (80% to 20%)		2.5	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, and Clock-Enabled Mode**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP Buffered CLKAB Signal (CLKOUT)**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description

The SN74GTLPH16916 is a medium-drive, 17-bit UBT transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, and clock-enabled modes of data transfer. Additionally, it provides for a copy of CLKAB at GTLP signal levels (CLKOUT) and conversion of a GTLP clock to LVTTL logic levels (CLKIN). The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC circuitry, and TI-OPC circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

OEC, TI, TI-OPC, UBT, and Widebus are trademarks of Texas Instruments.

description (continued)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16916 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH16916GR	GTLPH16916
	TVSOP – DGV	Tape and reel	SN74GTLPH16916VR	GL916

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16916 is a medium-drive (50 mA), 17-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16916 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH16916 UBT transceiver replaces all above functions					

Additionally, it allows for transparent conversion of CLKAB-to-GTLP signal levels (CLKOUT) and CLKOUT-to-LVTTL logic levels (CLKIN).

Data flow in each direction is controlled by clock enables ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$). $\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$ enable all 17 bits, and $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ control the 17 bits of data and the CLKOUT/CLKIN buffered clock path for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{\text{CEAB}}$ and LEAB are low, the A data is latched regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, LEBA, and CLKBA are used.

Function Tables

OUTPUT ENABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

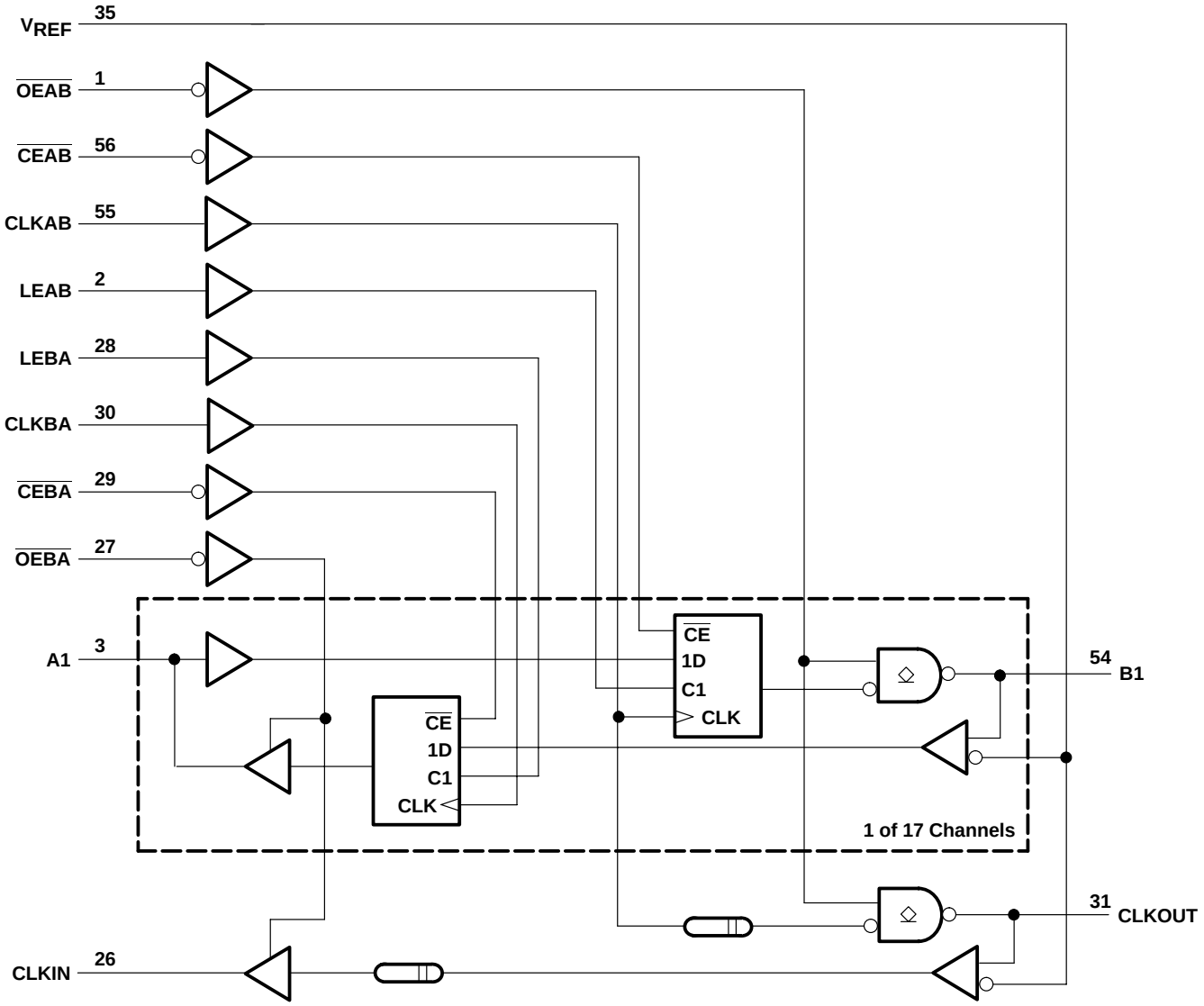
§ Output level before the indicated steady-state input conditions were established

BUFFERED CLOCK

INPUTS				OPERATION OR FUNCTION	MODE
$\overline{CE}$	LE	$\overline{OEAB}$	$\overline{OEBA}$		
X	X	H	H	Z	Isolation
X	X	L	H	CLKAB to CLKOUT	True delayed clock signal
X	X	H	L	CLKOUT to CLKIN	
X	X	L	L	CLKAB to CLKOUT, CLKOUT to CLKIN	True delayed clock signal with feedback path¶

¶ This condition is not recommended.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DGV package	48°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±10	µA
			V_I = 5.5 V			±20	
	B port		V_I = 0 to 1.5 V			±10	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5.5	pF
C_{io}	A port	V_O = 3.15 V or 0			7	8.5	pF
	B port or CLKOUT	V_O = 1.5 V or 0			8.5	9.5	
C_o	CLKIN	V_O = 3.15 V or 0			6	6.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

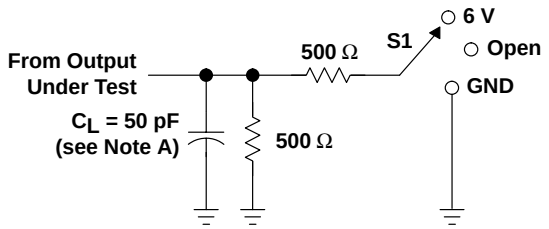
				MIN	MAX	UNIT
f_{clock}	Clock frequency	CLKAB to B or CLKBA to A			175	MHz
t_w	Pulse duration	LEAB or LEBA high		2.8		ns
		CLKAB to B or CLKBA to A	High or low	2.8		
t_{su}	Setup time	A before CLKAB↑		1.8		ns
		B before CLKBA↑		1.5		
		A before LEAB↓		1		
		B before LEBA↓		2		
		$\overline{CEAB}$ before CLKAB↑		1.5		
		$\overline{CEBA}$ before CLKBA↑		1.4		
t_h	Hold time	A after CLKAB↑		0.3		ns
		B after CLKBA↑		0.4		
		A after LEAB↓		1.1		
		B after LEBA↓		0.4		
		$\overline{CEAB}$ after CLKAB↑		1		
		$\overline{CEBA}$ after CLKBA↑		1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}	CLKAB or CLKBA	B or A	175			MHz
t_{PLH}	A	B	2.1		6	ns
t_{PHL}			2.1		6	
t_{PLH}	LEAB	B	2.2		6.3	ns
t_{PHL}			2.2		6.3	
t_{PLH}	CLKAB	B	2.2		6.3	ns
t_{PHL}			2.2		6.3	
t_{PLH}	CLKAB	CLKOUT	3.2		8	ns
t_{PHL}			3.2		8	
t_{en}	$\overline{OEAB}$	B or CLKOUT	2.6		6.5	ns
t_{dis}			2.6		6.1	
t_r	Rise time, B outputs (20% to 80%)			2.4		ns
t_f	Fall time, B outputs (80% to 20%)			2		ns
t_{PLH}	B	A	1.8		5.8	ns
t_{PHL}			1.8		5.8	
t_{PLH}	LEBA	A	1.7		5.3	ns
t_{PHL}			1.7		5.3	
t_{PLH}	CLKBA	A	1.8		5.7	ns
t_{PHL}			1.8		5.7	
t_{PLH}	CLKOUT	CLKIN	2.5		6.5	ns
t_{PHL}			2.5		6.5	
t_{en}	$\overline{OEBA}$	A or CLKIN	1.5		6.2	ns
t_{dis}			1.5		5.9	

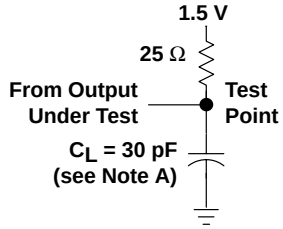
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

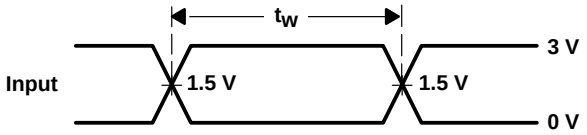


LOAD CIRCUIT FOR A OUTPUTS

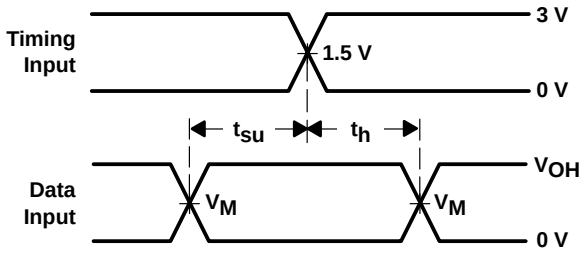
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



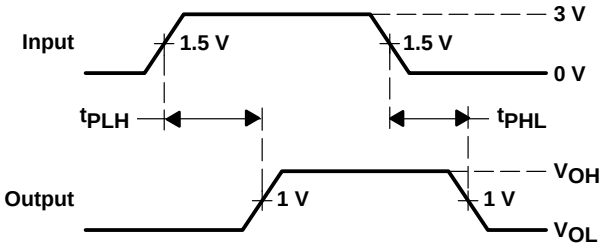
LOAD CIRCUIT FOR B OUTPUTS



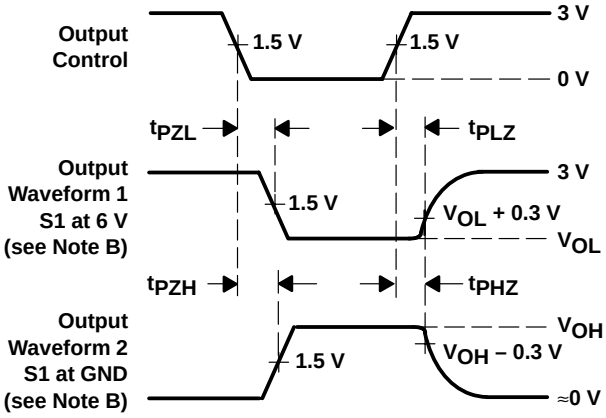
VOLTAGE WAVEFORMS
PULSE DURATION



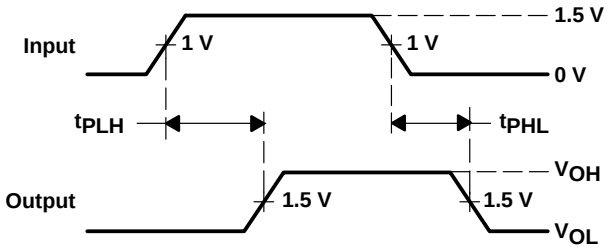
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

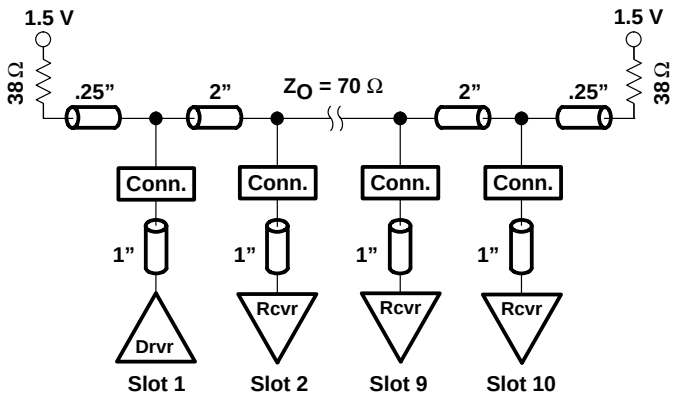


Figure 2. Medium-Drive Test Backplane

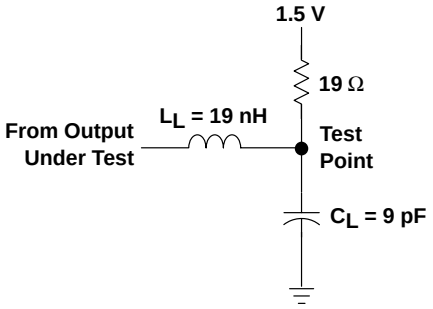


Figure 3. Medium-Drive RLC Network

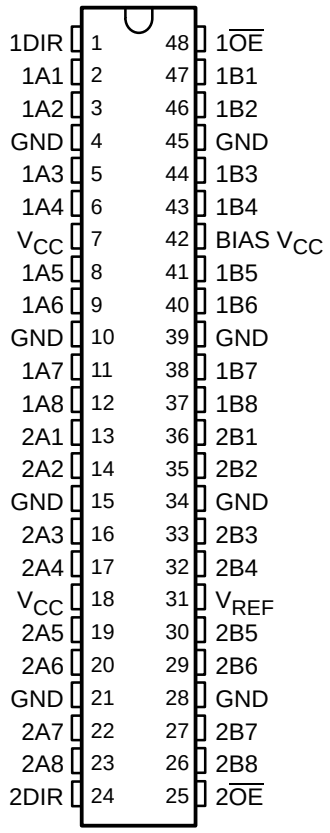
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	4.5	ns
t_{PHL}			4.5	
t_{PLH}	LEAB	B	4.7	ns
t_{PHL}			4.7	
t_{PLH}	CLKAB	B	4.7	ns
t_{PHL}			4.7	
t_{PLH}	CLKAB	CLKOUT	6	ns
t_{PHL}			6	
t_{en}	$\overline{OEAB}$	B or CLKOUT	4.8	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1.2	ns
t_f	Fall time, B outputs (80% to 20%)		2.5	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The SN74GTLPH16945 is a medium-drive, 16-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16945 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

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description (continued)

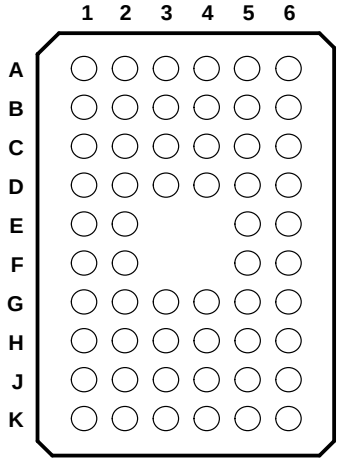
This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1A2	1A1	GND	GND	1B1	1B2
C	1A4	1A3	V_{CC}	BIAS V_{CC}	1B3	1B4
D	1A6	1A5	GND	GND	1B5	1B6
E	2A8	1A7			1B7	1B8
F	2A1	2A2			2B2	2B1
G	2A3	2A4	GND	GND	2B4	2B3
H	2A5	2A6	V_{CC}	V_{REF}	2B6	2B5
J	2A7	2A8	GND	GND	2B8	2B7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tape and reel	SN74GTLPH16945DLR	
	TSSOP – DGG	Tape and reel	SN74GTLPH16945GR	GTLPH16945
	TVSOP – DGV	Tape and reel	SN74GTLPH16945VR	GL945
	VFBGA – GQL	Tape and reel	SN74GTLPH16945KR	GL945

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16945 is a medium-drive (50 mA), 16-bit bus transceiver partitioned as two 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

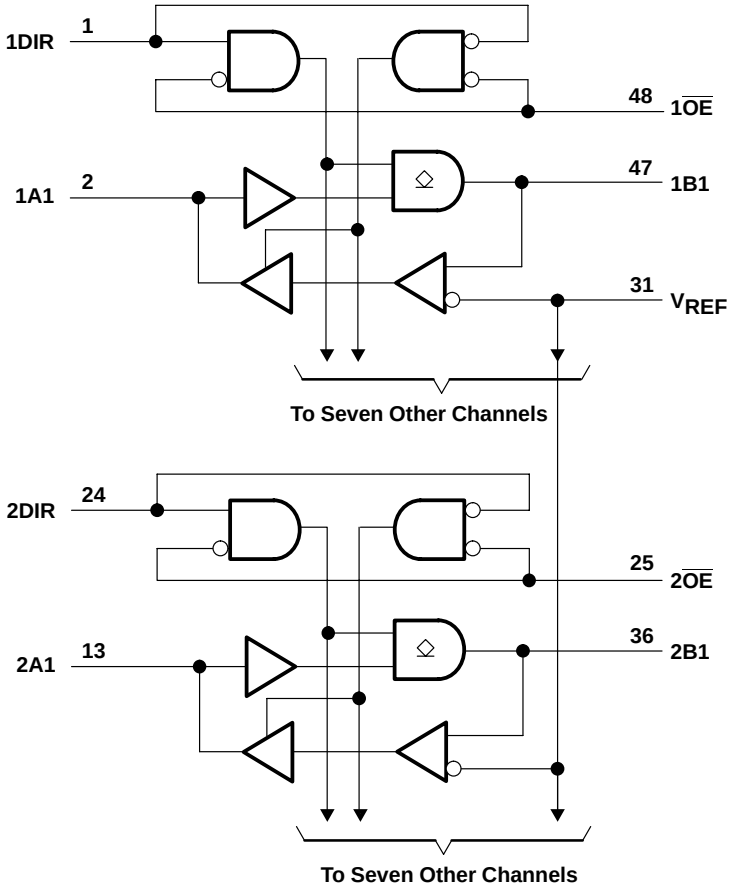
For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{OE}$ and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
GQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	µA
I_{OZH}‡	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	µA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	Control inputs	V_I = 3.15 V or 0			4.5	5	pF
C_{io}	A port	V_O = 3.15 V or 0			7.5	9	pF
	B port	V_O = 1.5 V or 0			7.5	9	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

live-insertion specifications for B port over recommended operating free-air temperature range

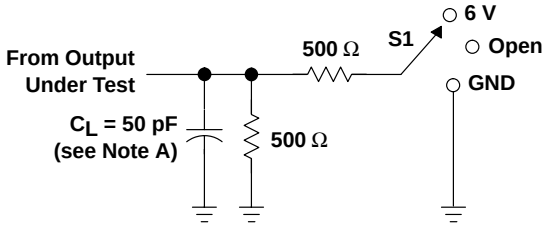
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	B	2.1		6.3	ns
t_{PHL}			2.1		6.3	
t_{en}	$\overline{OE}$	B	2		6.9	ns
t_{dis}			2		6.9	
t_r	Rise time, B outputs (20% to 80%)			2.5		ns
t_f	Fall time, B outputs (80% to 20%)			2.1		ns
t_{PLH}	B	A	2.1		5.3	ns
t_{PHL}			2.1		5.3	
t_{en}	$\overline{OE}$	A	0.3		5.7	ns
t_{dis}			0.3		5.7	

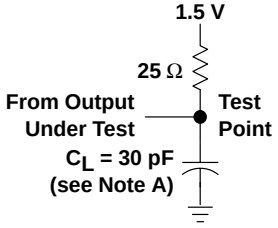
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

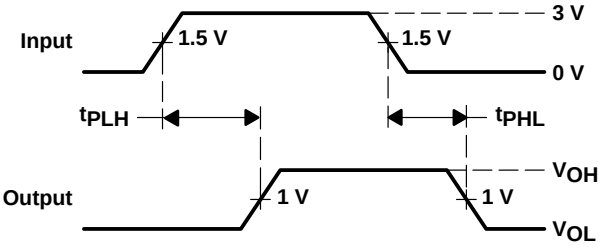


LOAD CIRCUIT FOR A OUTPUTS

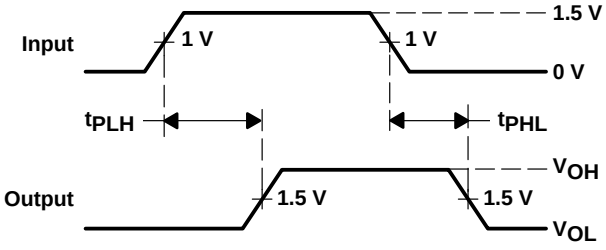
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



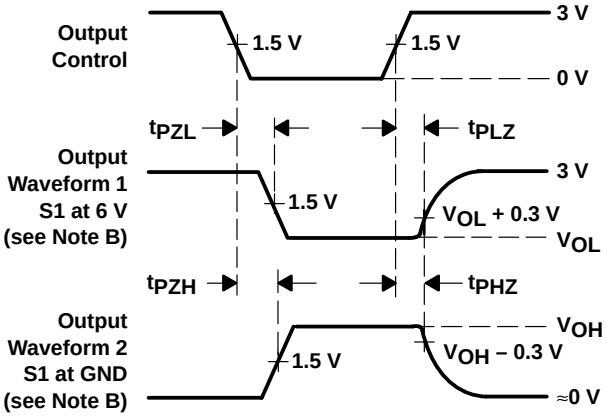
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

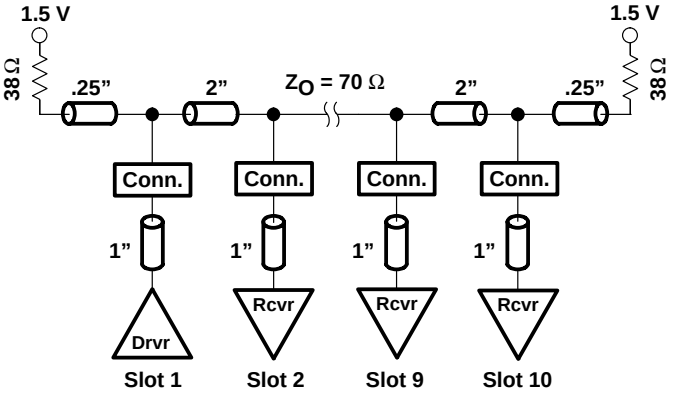


Figure 2. Medium-Drive Test Backplane

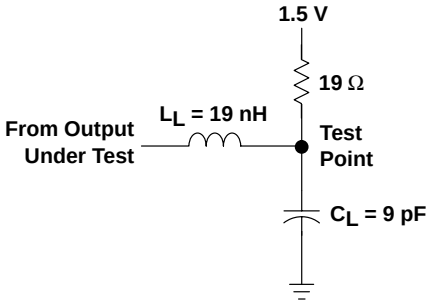


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	4.3	ns
t_{PHL}			4.3	
t_{en}	$\overline{OE}$	B	5	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1	ns
t_f	Fall time, B outputs (80% to 20%)		2	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

- **Member of Texas Instruments' Widebus+™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

description

The SN74GTLPH32945 is a medium-drive, 32-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as four 8-bit transceivers. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC circuitry, and TI-OPC circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 19 Ω.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH32945 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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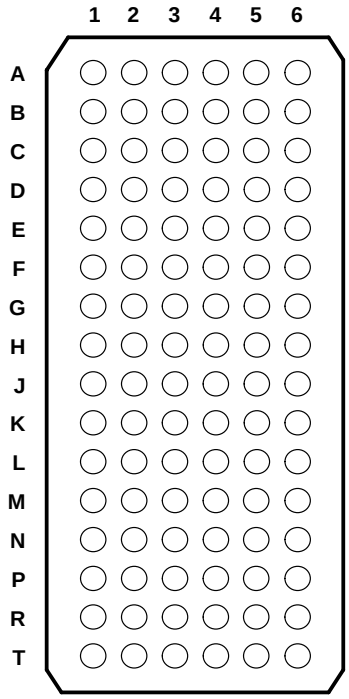
GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1A2	1A1	1DIR	1$\overline{OE}$	1B1	1B2
B	1A4	1A3	GND	GND	1B3	1B4
C	1A6	1A5	1V_{CC}	1BIAS V_{CC}	1B5	1B6
D	1A8	1A7	GND	GND	1B7	1B8
E	2A2	2A1	GND	GND	2B1	2B2
F	2A4	2A3	1V_{CC}	1V_{REF}	2B3	2B4
G	2A6	2A5	GND	GND	2B5	2B6
H	2A7	2A8	2DIR	2$\overline{OE}$	2B8	2B7
J	3A2	3A1	3DIR	3$\overline{OE}$	3B1	3B2
K	3A4	3A3	GND	GND	3B3	3B4
L	3A6	3A5	2V_{CC}	2BIAS V_{CC}	3B5	3B6
M	3A8	3A7	GND	GND	3B7	3B8
N	4A2	4A1	GND	GND	4B1	4B2
P	4A4	4A3	2V_{CC}	2V_{REF}	4B3	4B4
R	4A6	4A5	GND	GND	4B5	4B6
T	4A7	4A8	4DIR	4$\overline{OE}$	4B8	4B7

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	SN74GTLPH32945KR	GM45

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH32945 is a medium-drive (50 mA), 32-bit bus transceiver partitioned as four 8-bit segments and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. $\overline{OE}$ can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

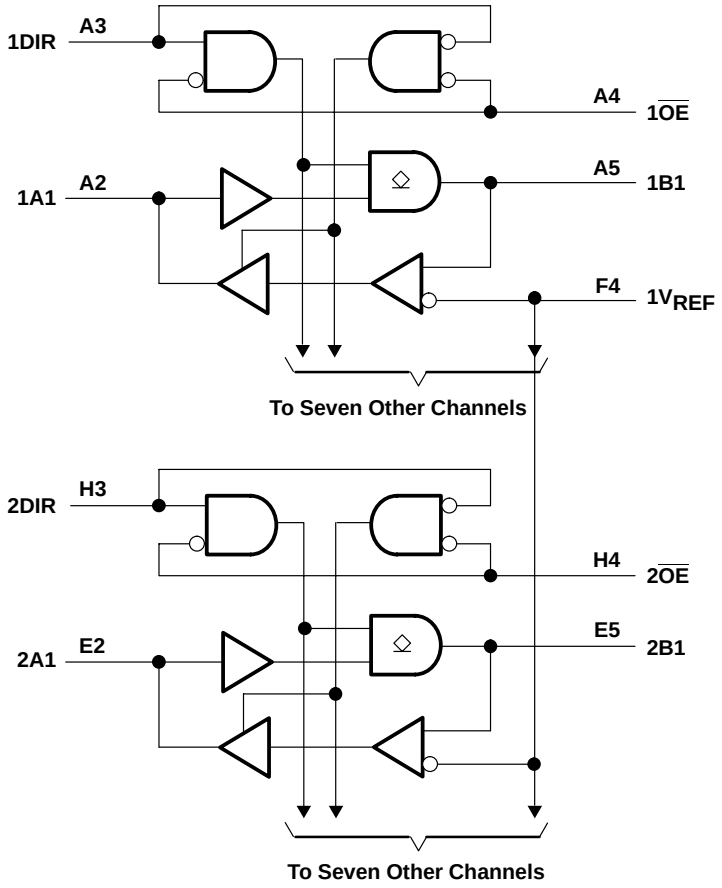
For A-to-B data flow, when $\overline{OE}$ is low and DIR is high, the B outputs take on the logic value of the A inputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to that of A to B, except $\overline{OE}$ and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{OE}$	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

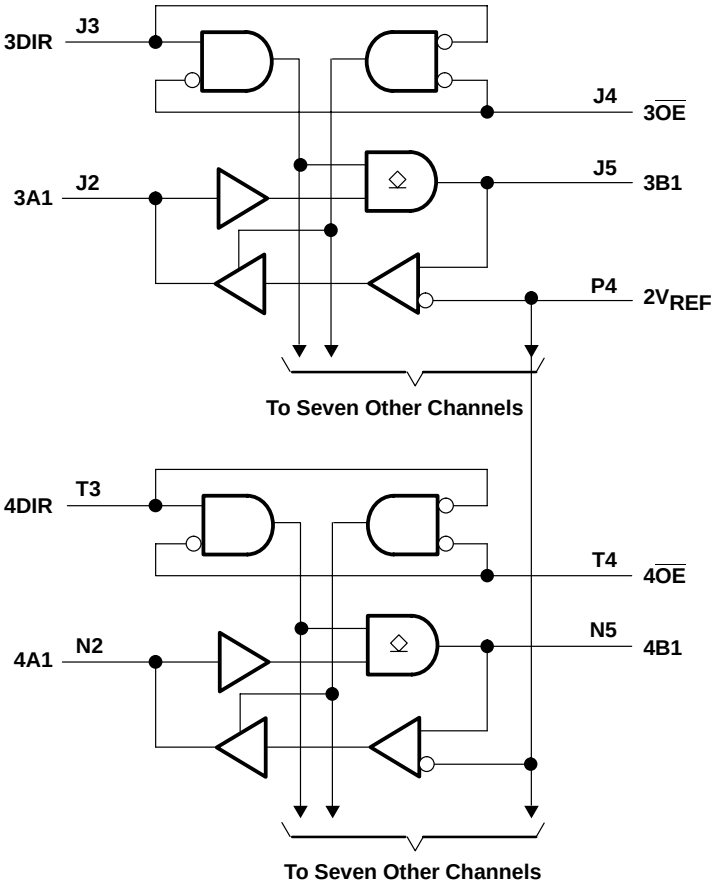
logic diagram (positive logic)†



† $1V_{CC}$ and 1BIAS V_{CC} are associated with these channels.

PRODUCT PREVIEW

logic diagram (positive logic) (continued)†



† $2V_{CC}$ and 2BIAS V_{CC} are associated with these channels.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port and control inputs	–0.5 V to 7 V
B port and V_{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O: A port	48 mA
B port	100 mA
Current into any A port output in the high state, I_O (see Note 2)	48 mA
Continuous current through each V_{CC} or GND	±100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3)	40°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES:
4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 40 mA			0.4	
			I_{OL} = 50 mA			0.55	
I_I‡	A-port and control inputs	V_{CC} = 3.45 V	V_I = 0 or V_{CC}			±10	µA
			V_I = 5.5 V			±20	
	B port		V_I = 0 to 1.5 V			±10	
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
I_{CCD}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND, One data input switching at 50% duty cycle	Outputs enabled				mA/MHz
			Outputs disabled				
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1	mA
C_i	Control inputs	V_I = 3.15 V or 0					pF
C_{io}	A port	V_O = 3.15 V or 0					pF
	B port	V_O = 1.5 V or 0					

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	µA

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live-insertion specifications for B port over recommended operating free-air temperature range

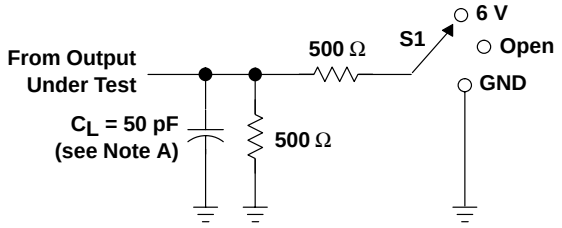
PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	A	B				ns
t_{PHL}						
t_{en}	$\overline{OE}$	B				ns
t_{dis}						
t_r	Rise time, B outputs (20% to 80%)					ns
t_f	Fall time, B outputs (80% to 20%)					ns
t_{PLH}	B	A				ns
t_{PHL}						
t_{en}	$\overline{OE}$	A				ns
t_{dis}						

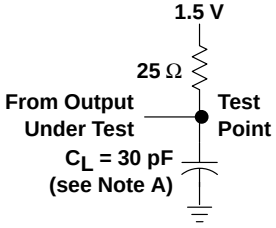
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

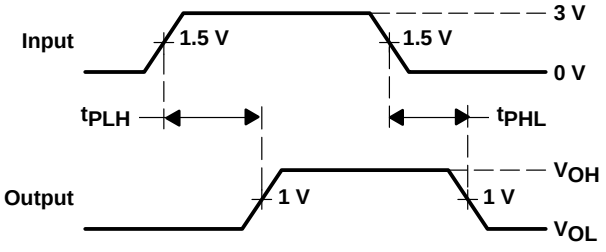


LOAD CIRCUIT FOR A OUTPUTS

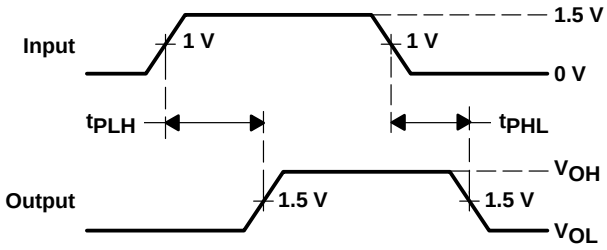
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



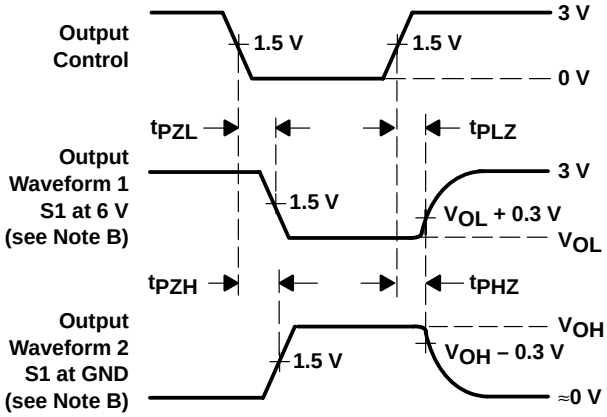
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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PRODUCT PREVIEW

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

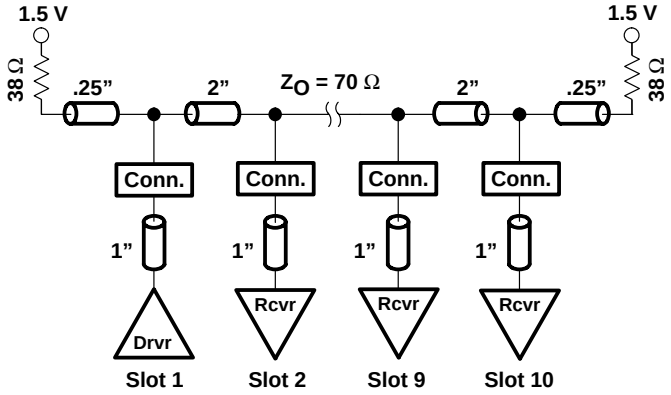


Figure 2. Medium-Drive Test Backplane

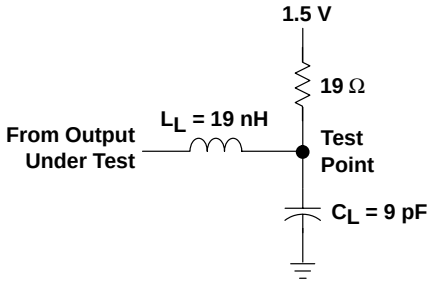


Figure 3. Medium-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

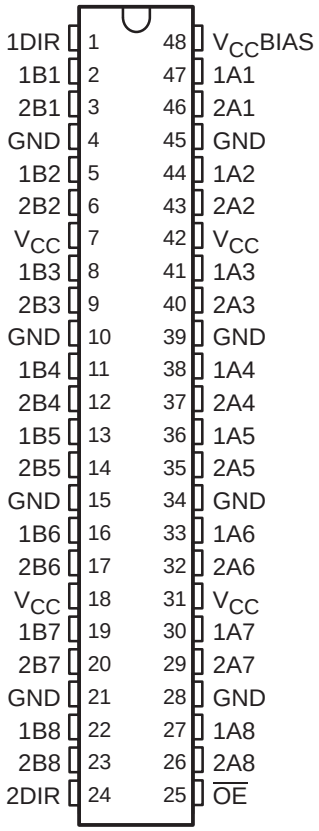
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP†	UNIT
t_{PLH}	A	B	4.3	ns
t_{PHL}			4.3	
t_{en}	$\overline{OE}$	B	5	ns
t_{dis}			4.4	
t_r	Rise time, B outputs (20% to 80%)		1	ns
t_f	Fall time, B outputs (80% to 20%)		2	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

Contents

- **Member of Texas Instruments' Widebus™ Family**
- **Supports the VME64 ETL Specification**
- **Reduced, TTL-Compatible, Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Equivalent 25-Ω Series Damping Resistor on B Port**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ABTE16245 is a 16-bit (dual-octal) noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. This device can be used as two 8-bit transceivers or one 16-bit transceiver. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has an equivalent 25-Ω series output resistor to reduce ringing. Active bus-hold inputs are also on the B port to hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Widebus is a trademark of Texas Instruments.

ORDERING INFORMATION

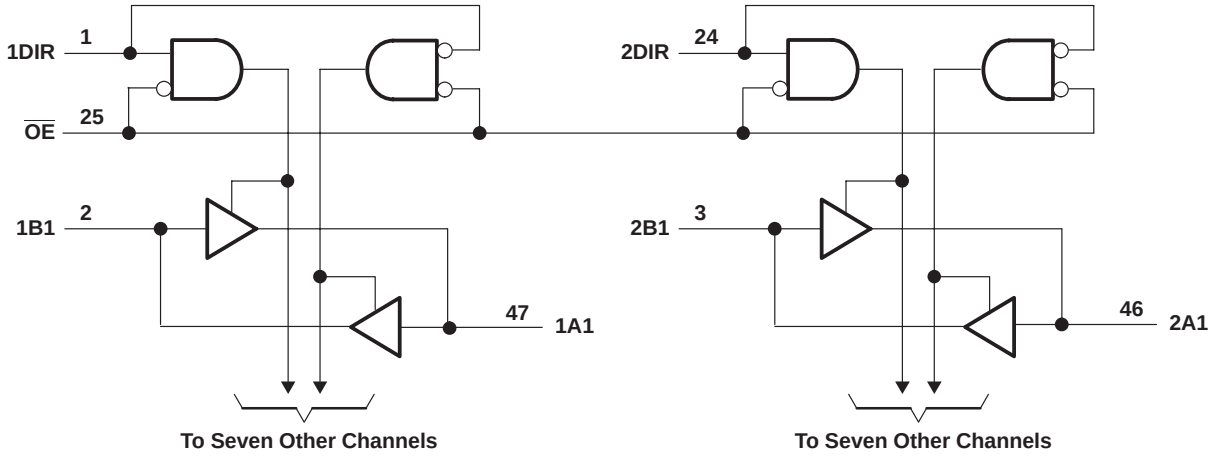
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ABTE16245DL	ABTE16245
		Tape and reel	SN74ABTE16245DLR	
	TSSOP – DGG	Tape and reel	SN74ABTE16245DGGR	ABTE16245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	A data to B bus
L	H	B data to A bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			V
		Except $\overline{OE}$	1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8	V
		Except $\overline{OE}$			1.4	
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	B bus			–12	mA
		A bus			–60	
I_{OL}	Low-level output current	B bus			12	mA
		A bus			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = –100 µA			V_{CC}–0.2	V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4			
			I_{OH} = –12 mA	2			
	A port	V_{CC} = 5.5 V,	I_{OH} = –1 mA			4.5	
		V_{CC} = 4.5 V	I_{OH} = –32 mA	2.4			
			I_{OH} = –64 mA	2			
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA			0.4	V
			I_{OL} = 12 mA			0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.55	
			I_{OL} = 90 mA			0.9	
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V	100			µA
			V_I = 2 V	–100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1	µA
	A or B ports	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±20	
I_{OZH}‡	A port	V_{CC} = 5.5 V,	V_O = 2.7 V			10	µA
I_{OZL}‡	A port	V_{CC} = 5.5 V,	V_O = 0.5 V			–10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50		–180	mA
	B port			–25		–90	
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V,	V_{CC}BIAS = 0			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		28	36	mA
			Outputs low		38	48	
			Outputs disabled		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V, C_L = 50 pF	$\overline{OE}$ high		0.02		mA/MHz
			$\overline{OE}$ low		0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V			2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V			4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0		250	700	µA
		V_{CC} = 4.5 V to 5.5 V‡,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0			20	
V_O	A port	V_{CC} = 0	V_{CC}BIAS = 4.5 V to 5.5 V		1.1	1.5	1.9	V
			V_{CC}BIAS = 4.75 V to 5.25 V		1.3	1.5	1.7	
I_O	A port	V_{CC} = 0,	V_{CC}BIAS = 4.5 V	V_O = 0	–20		–100	µA
				V_O = 3 V	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	B	1.5	3.3	4.2	1.5	5.2	ns
t_{PHL}			1.5	3.8	4.6	1.5	5.2	
t_{PLH}	B	A	1.5	3	3.8	1.5	4.5	ns
t_{PHL}			1.5	3.1	4	1.5	4.5	
t_{PZH}	$\overline{OE}$	A	2	3.9	5.3	2	6.2	ns
t_{PZL}			2	4.4	5.9	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.5	6	2	7.1	ns
t_{PZL}			2	5	6.4	2	7.3	
t_{PHZ}	$\overline{OE}$	A	2	4.9	5.9	2	6.7	ns
t_{PLZ}			2	3.7	4.6	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2	5.2	6.2	2	7	ns
t_{PLZ}			2	4	5	2	5.5	

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

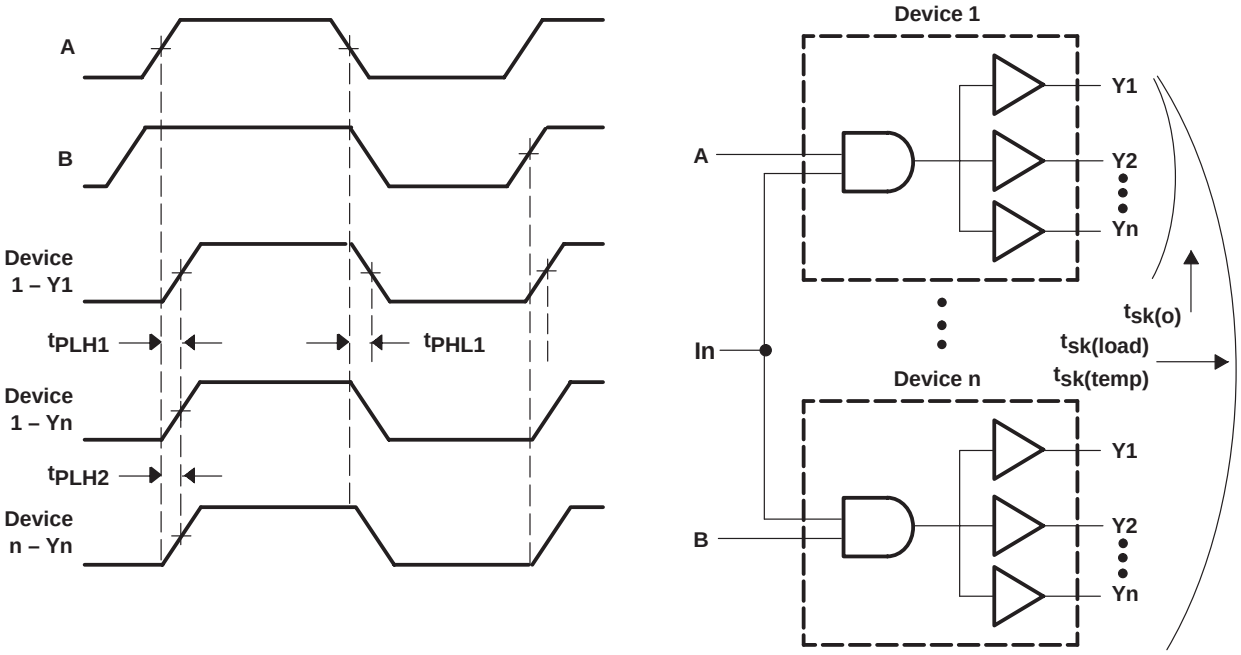
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	B	A	R_X = 13 Ω	1.5	3.2	4	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.6	
t_{PLH}	B	A	R_X = 26 Ω	1.5	3.1	4	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	4.9	
t_{PLH}	B	A	R_X = 56 Ω	1.5	3	3.8	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	4.7	
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2	ns
	A	B			0.4	0.8		2	
	B	A	R_X = 26 Ω		0.3	0.8		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3	ns
	A	B			0.7	1.1		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	7.9	ns

† t_t is measured between 1 V and 2 V of the output waveform.
‡ t_t is measured between 10% and 90% of the output waveform.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	MIN	MAX	UNIT
$t_{sk(temp)}$	A	B	V_{CC} = constant, ΔT_A = 20°C			2.5	ns
	B	A		R_X = 56 Ω		4	
$t_{sk(load)}$	B	B	V_{CC} = constant, Temperature = constant	R_X = 13, 26, or 56 Ω		4	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation-delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

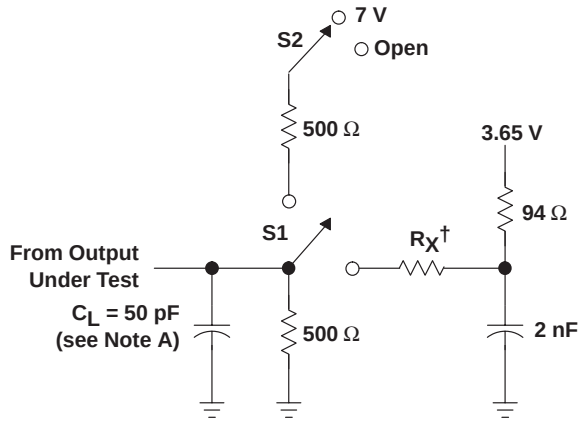
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of any two outputs of the same device switching in the same direction (e.g., $|t_{PLH1} - t_{PLH2}|$).

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

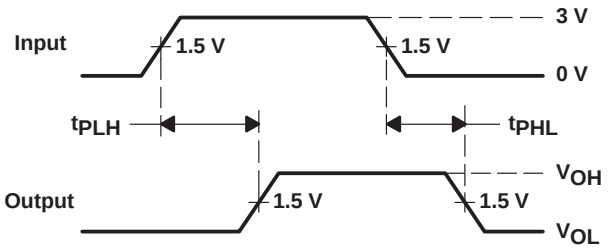


† R_X = 13, 26, or 56 Ω

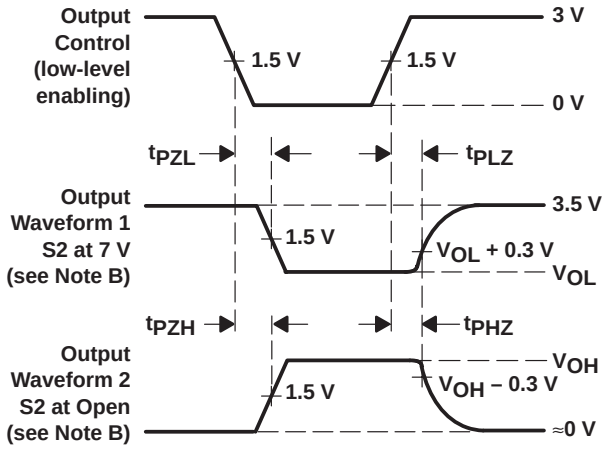
LOAD CIRCUIT FOR OUTPUTS

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (A and B port)	Up	Open
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH}	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured between 1 V and 2 V of the output waveform.
F. t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of Texas Instruments' Widebus™ Family**
- **Supports the VME64 ETL Specification**
- **Reduced TTL-Compatible Input Threshold Range**
- **High-Drive Outputs (I_{OH} = –60 mA, I_{OL} = 90 mA) Support Equivalent 25-Ω Incident-Wave Switching**
- **V_{CC}BIAS Pin Minimizes Signal Distortion During Live Insertion**
- **Internal Pullup Resistor on $\overline{OE}$ Keeps Outputs in High-Impedance State During Power Up or Power Down**
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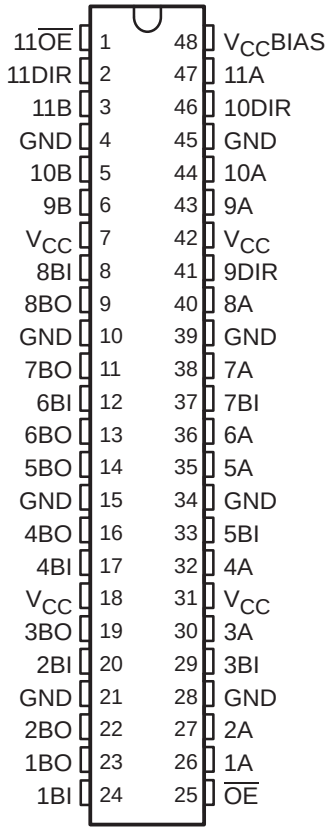
- **Equivalent 25-Ω Series Damping Resistor on B Port**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ABTE16246 is an 11-bit noninverting transceiver designed for asynchronous two-way communication between buses. This device has open-collector and 3-state outputs. The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated. When $\overline{OE}$ is low, the device is active.

The B port has an equivalent 25-Ω series output resistor to reduce ringing. Active bus-hold inputs on the B port hold unused or floating inputs at a valid logic level.

The A port provides for the precharging of the outputs via V_{CC}BIAS, which establishes a voltage between 1.3 V and 1.7 V when V_{CC} is not connected.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ABTE16246DL	ABTE16246
		Tape and reel	SN74ABTE16246DLR	
	TSSOP – DGG	Tape and reel	SN74ABTE16246DGGR	ABTE16246

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

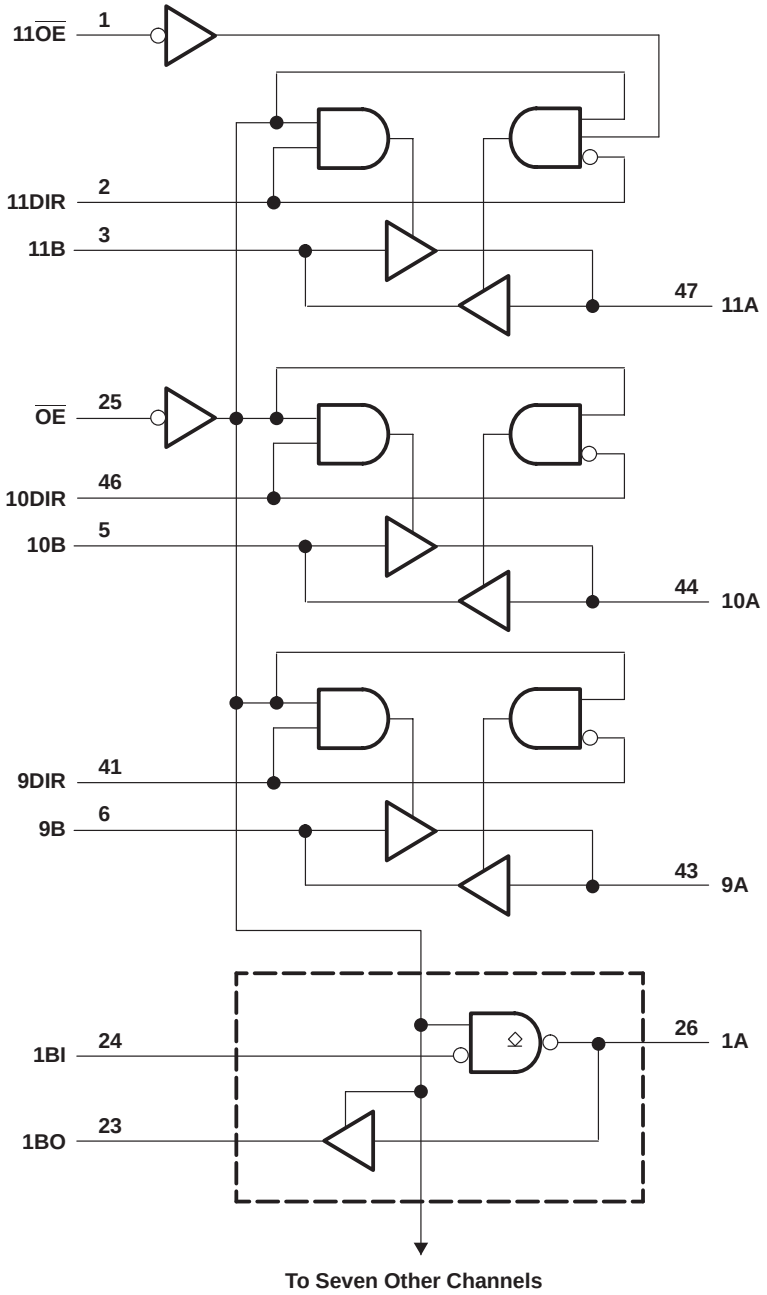
Widebus is a trademark of Texas Instruments.

FUNCTION TABLE

INPUTS					OPERATION
$\overline{OE}$	9DIR	10DIR	11DIR	11$\overline{OE}$	
H	X	X	X	X	Isolation
L	X	X	X	X	1BI–8BI data to 1A–8A bus (OC†), 1A–8A data to 1BO–8BO bus
L	L	X	X	X	9A data to 9B bus
L	H	X	X	X	9B data to 9A bus
L	X	L	X	X	10A data to 10B bus
L	X	H	X	X	10B data to 10A bus
L	X	X	L	L	11A data to 11B bus
L	X	X	L	H	11A, 11B isolation
L	X	X	H	X	11B data to 11A bus

† OC = Open-collector outputs

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{OE}$	2			V
		Except $\overline{OE}$	1.6			
V_{IL}	Low-level input voltage	$\overline{OE}$			0.8	V
		Except $\overline{OE}$			1.4	
V_{OH}	High-level output voltage	1A–8A	0		5.5	V
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	B bus			–12	mA
		9A–11A			–64	
I_{OL}	Low-level output current	B bus			12	mA
		A bus			90	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature		–40		85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	B port	V_{CC} = 5.5 V,	I_{OH} = –100 µA			V_{CC}–0.2	V
		V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4			
			I_{OH} = –12 mA	2			
	9A–11A	V_{CC} = 5.5 V,	I_{OH} = –1 mA			4.5	
		V_{CC} = 4.5 V	I_{OH} = –32 mA	2.4			
			I_{OH} = –64 mA	2			
I_{OH}	1A–8A	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			20	µA
V_{OL}	B port	V_{CC} = 4.5 V	I_{OL} = 1 mA			0.4	V
			I_{OL} = 12 mA			0.8	
	A port	V_{CC} = 4.5 V	I_{OL} = 64 mA			0.55	
			I_{OL} = 90 mA			0.9	
V_{hys}					100		mV
$I_{I(hold)}$	B port	V_{CC} = 4.5 V	V_I = 0.8 V	100			µA
			V_I = 2 V	–100			
		V_{CC} = 5.5 V,	V_I = 0 to 5.5 V			±500	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1	µA
	A or B ports					±20	
I_{OZH}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 2.7 V			10	µA
I_{OZL}‡	9A–11A	V_{CC} = 5.5 V,	V_O = 0.5 V			–10	µA
I_O	A port	V_{CC} = 5.5 V,	V_O = 2.5 V	–50		–180	mA
	B port			–25		–90	
I_{off}		V_{CC} = 0, V_I or V_O ≤ 4.5 V,	V_{CC}BIAS = 0			±100	µA
I_{CC}	A or B ports	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		28	36	mA
			Outputs low		38	48	
			Outputs disabled		20	32	
I_{CCD}	A or B ports	V_{CC} = 5 V, C_L = 50 pF	$\overline{OE}$ high		0.02		mA/MHz
			$\overline{OE}$ low		0.33		
C_i	Control inputs	V_I = 2.5 V or 0.5 V			2.5	4	pF
C_{io}	I/O ports	V_O = 2.5 V or 0.5 V			4.5	8	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CC} (V_{CC}BIAS)		V_{CC} = 0 to 4.5 V,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0		250	700	µA
		V_{CC} = 4.5 V to 5.5 V‡,	V_{CC}BIAS = 4.5 V to 5.5 V,	$I_{O(DC)}$ = 0			20	
V_O	A port	V_{CC} = 0	V_{CC}BIAS = 4.5 V to 5.5 V		1.1	1.5	1.9	V
			V_{CC}BIAS = 4.75 V to 5.25 V		1.3	1.5	1.7	
I_O	A port	V_{CC} = 0,	V_{CC}BIAS = 4.5 V	V_O = 0	–20		–100	µA
				V_O = 3 V	20		100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < V_{CC}BIAS

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	B	1.5	3.1	4.2	1.5	5.2	ns
t_{PHL}			1.5	3.5	4.6	1.5	5.2	
t_{PLH}	9B–11B	9A–11A	1.5	3	3.8	1.5	4.5	ns
t_{PHL}			1.5	3.2	4	1.5	4.5	
t_{PLH}§	1B–8B	1A–8A	1.5	3.2	4	1.5	4.5	ns
t_{PLH}¶			7.5	8.9	9.7	7.5	10.3	
t_{PHL}			1.5	3.2	4	1.5	4.5	
t_{PZH}	$\overline{OE}$	9A–11A	2	4.3	5.3	2	6.2	ns
t_{PZL}		1A–11A	2	4.4	5.4	2	6.8	
t_{PZH}	$\overline{OE}$	B	2	4.3	6	2	7.1	ns
t_{PZL}			2	4.5	6.4	2	7.3	
t_{PHZ}	$\overline{OE}$	9A–11A	2	4.2	5.9	2	6.7	ns
t_{PLZ}		1A–11A	2	3.5	4.6	2	5.1	
t_{PHZ}	$\overline{OE}$	B	2.5	4.3	6.2	2.5	7	ns
t_{PLZ}			2	3.6	5	2	5.5	

§ Measurement point is V_{OL} + 0.3 V.
¶ Measurement point is V_{OL} + 1.5 V.

extended switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

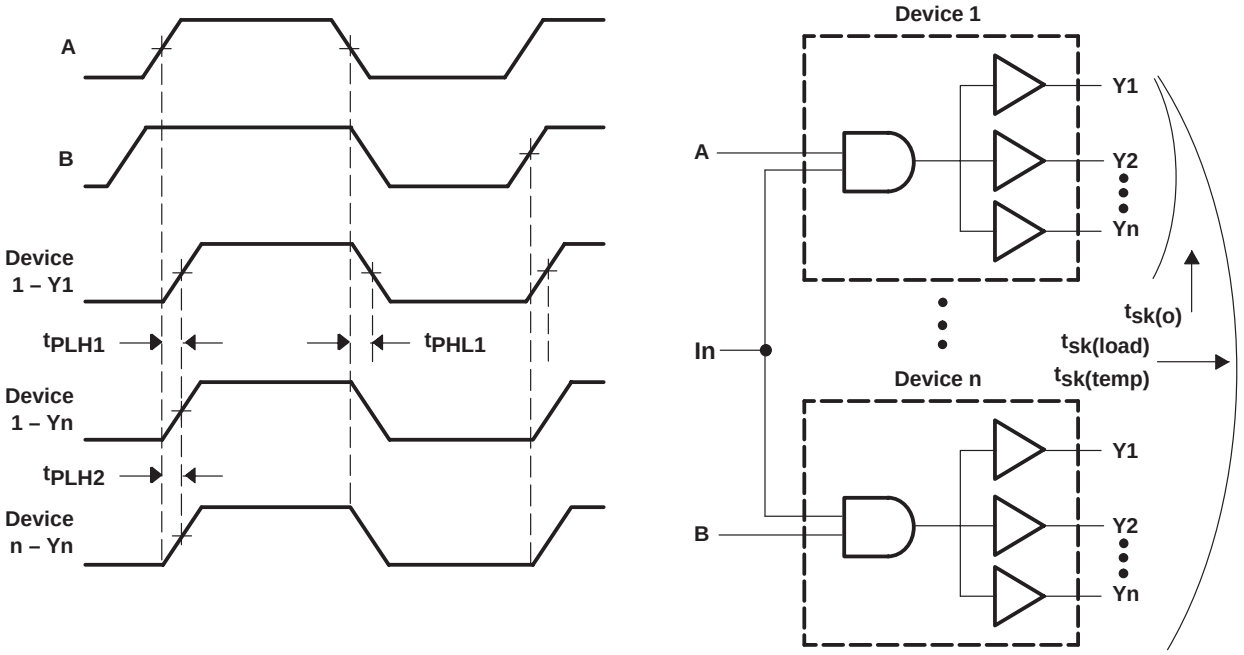
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	9B–11B	9A–11A	R_X = 13 Ω	1.5	3.2	4	1.5	4.8	ns
t_{PHL}				1.5	3.8	4.7	1.5	5.6	
t_{PHL}	1B–8B	1A–8A	R_X = 13 Ω	1.5	3.3	4.2	1.5	4.8	ns
t_{PLH}	9B–11B	9A–11A	R_X = 26 Ω	1.5	3.1	4	1.5	4.6	ns
t_{PHL}				1.5	3.5	4.4	1.5	4.9	
t_{PHL}	1B–8B	1A–8A	R_X = 26 Ω	1.5	3.1	4	1.5	4.4	ns
t_{PLH}	9B–11B	1A–8A	R_X = 56 Ω	1.5	3	3.8	1.5	4.5	ns
t_{PHL}				1.5	3.3	4.2	1.5	4.7	
t_{PHL}	1B–8B	1A–8A	R_X = 56 Ω	1.5	3	4	1.5	4.4	ns
$t_{sk(p)}$	B	A	R_X = Open		0.1	0.6		2	ns
	A	B			0.4	0.8		2	
	B	A	R_X = 26 Ω		0.3	0.8		2	
$t_{sk(o)}$	B	A	R_X = Open		0.3	0.7		1.3	ns
	A	B			0.7	1.1		1.3	
	B	A	R_X = 26 Ω		0.5	1		1.3	
t_t†	B	A	R_X = 26 Ω	0.5	0.8	1.5	0.5	1.5	ns
t_t‡	A	B	Rise or fall time 10%–90%	3.5	5.5	7.3	3.5	7.9	ns

† t_t is measured between 1 V and 2 V of the output waveform.
‡ t_t is measured between 10% and 90% of the output waveform.

extended output characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LOAD	MIN	MAX	UNIT
$t_{sk(temp)}$	A	B	V_{CC} = constant, ΔT_A = 20°C			2.5	ns
	B	A		R_X = 56 Ω		4	
$t_{sk(load)}$	B	A	V_{CC} = constant, Temperature = constant	R_X = 13, 26, or 56 Ω		4	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Pulse skew, $t_{sk(p)}$, is defined as the difference in propagation-delay times t_{PLH1} and t_{PHL1} on the same terminal at identical operating conditions.

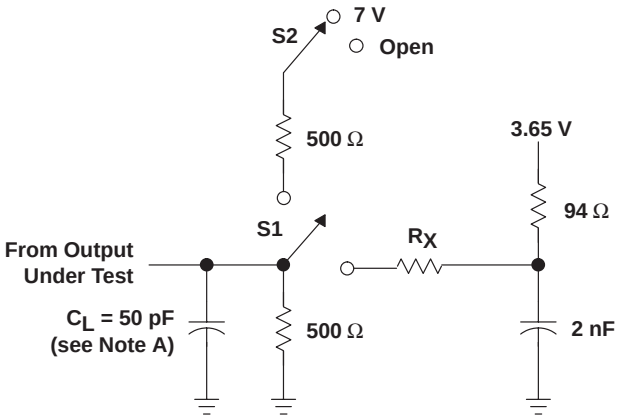
B. Output skew, $t_{sk(o)}$, is defined as the difference in propagation delay of any two outputs of the same device switching in the same direction (e.g., $|t_{PLH1} - t_{PLH2}|$) .

C. Temperature skew, $t_{sk(temp)}$, is the output skew of two devices, both having the same value of $V_{CC} \pm 1\%$ and with package temperature differences of 20°C.

D. Load skew, $t_{sk(load)}$, is measured with R_X in Figure 2 at 13 Ω for one unit and 56 Ω for the other unit.

Figure 1. Voltage Waveforms for Extended Characteristics

PARAMETER MEASUREMENT INFORMATION

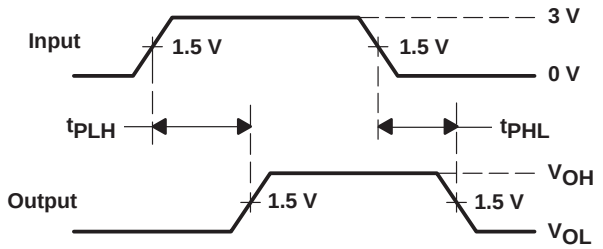


R_X = 13, 26, or 56 Ω

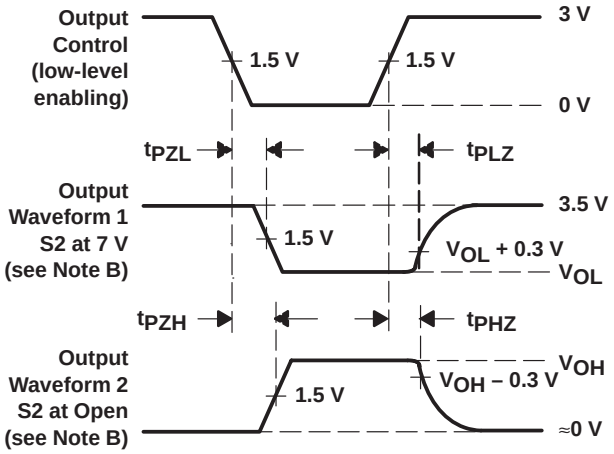
LOAD CIRCUIT

SWITCHING TABLE LOADS	S1	S2
t_{PLH}/t_{PHL} (9A–11A and B port)	Up	Open
t_{PLH}/t_{PHL} (1A–8A)	Up	7 V
t_{PLZ}/t_{PZL}	Up	7 V
t_{PHZ}/t_{PZH} (except 1A–8A)	Up	Open

EXTENDED SWITCHING TABLE LOADS	S1	S2
$t_{PLH}/t_{PHL}/t_{sk}$ (A port)	Down	X
$t_{PLH}/t_{PHL}/t_{sk}$ (B port)	Up	Open
t_t (A port) (see Note E)	Down	X
t_t (B port) (see Note F)	Up	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

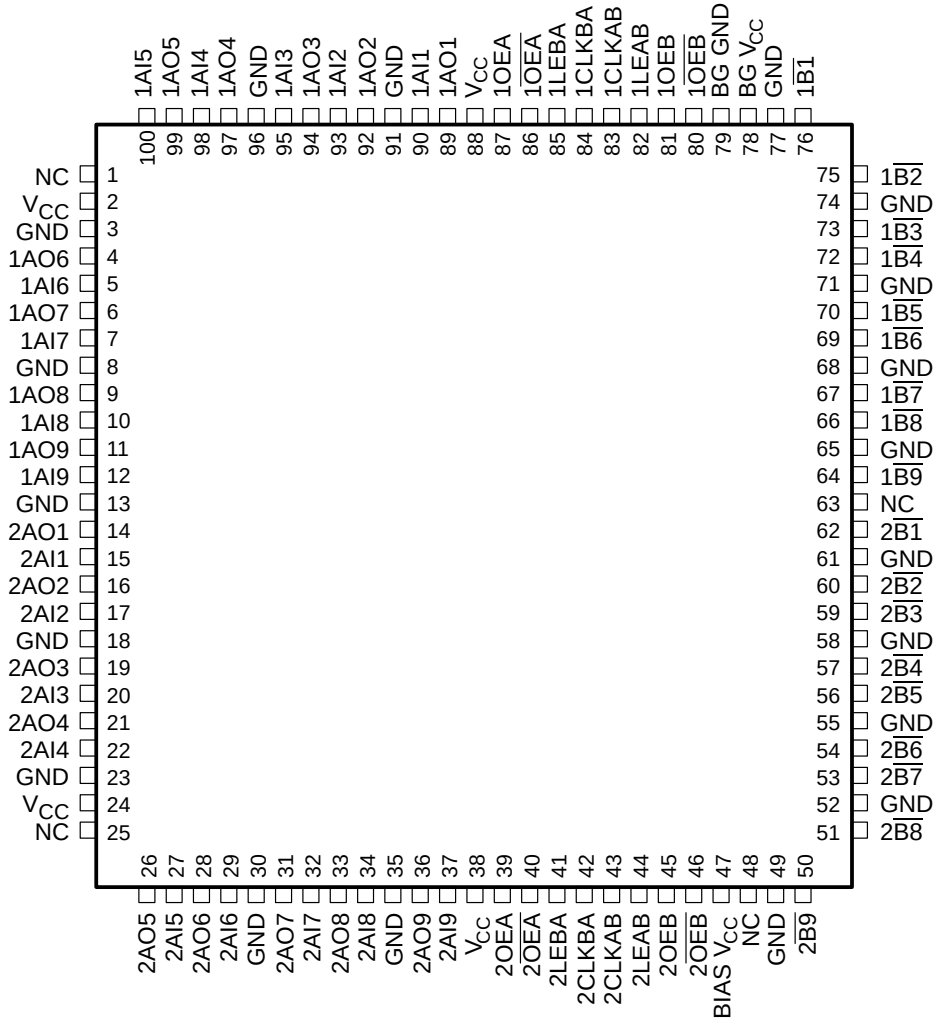
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_t is measured between 1 V and 2 V of the output waveform.
F. t_t is measured between 10% and 90% of the output waveform.

Figure 2. Load Circuit and Voltage Waveforms

Contents

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

PCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74FB1650 contains two 9-bit transceivers designed to translate signals between TTL and backplane transceiver-logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PCA	Tube	SN74FB1650PCA	FB1650

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

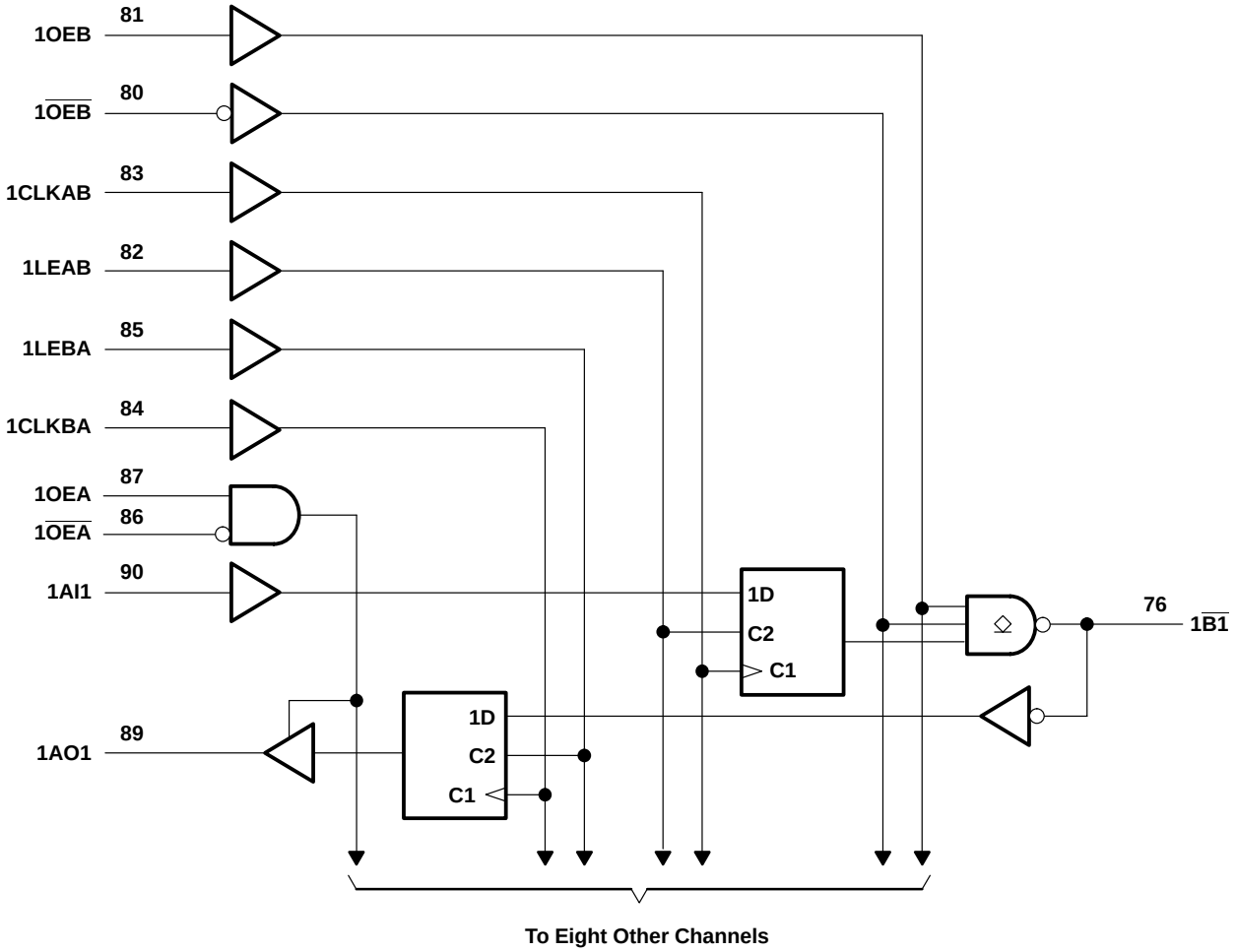
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–3	mA
I_{OL}	Low-level output current	A port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			100	mA
	$\overline{B}$ port to A port					120	
C_i	AI port	V_I = V_{CC} or GND			5.5		pF
	Control inputs				5.5		
C_o	AO ports	V_O = V_{CC} or GND			5.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 5.5 V				5.5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

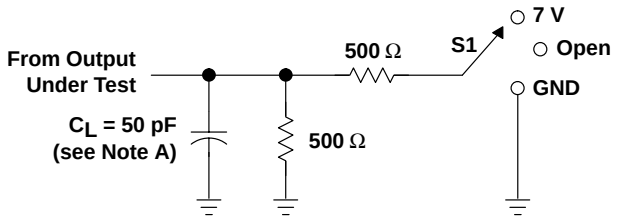
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	CLK or LE	3.3		3.3		ns
t_{su}	Setup time	Data before LE	4.8		4.8		ns
		Data before CLK↑	4.9		4.9		
t_h	Hold time	Data after LE	1.8		1.8		ns
		Data after CLK↑	1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

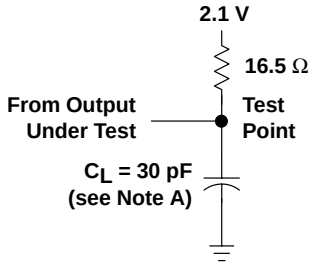
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI	$\overline{B}$	1.8	3.7	5.3	1.8	6.2	ns
t_{PHL}			2.9	4.4	6	2.9	7.2	
t_{PLH}	LEAB	$\overline{B}$	2.7	4.2	5.8	2.7	6.4	ns
t_{PHL}			3.5	5	6.5	3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	3.9	5.5	2.3	6	ns
t_{PHL}			2.9	4.5	6.1	2.9	6.7	
t_{PLH}	$\overline{B}$	AO	3.5	5.9	7.9	3.5	8.6	ns
t_{PHL}			2.2	3.7	5.3	2.2	5.7	
t_{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.1	ns
t_{PHL}			1.7	3	4.4	1.7	4.7	
t_{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.1	ns
t_{PHL}			1.7	3.1	4.6	1.7	4.9	
t_{PLH}	OEB	$\overline{B}$	2.7	4.6	6.4	2.7	6.7	ns
t_{PHL}			2.9	4.1	5.9	2.9	6.6	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.6	4.3	6.2	2.6	6.6	ns
t_{PHL}			3.4	4.6	6.4	3.4	7	
t_{PZH}	OEA	AO	1.4	2.9	4.4	1.4	4.9	ns
t_{PZL}			1.4	2.6	4	1.4	4.6	
t_{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.8	ns
t_{PLZ}			2.2	3.6	5	2.2	5.5	
t_{PZH}	$\overline{OEA}$	AO	1.7	3.3	4.7	1.7	5.5	ns
t_{PZL}			1.7	3.1	4.4	1.7	5.1	
t_{PHZ}	$\overline{OEA}$	AO	1.5	2.9	4.5	1.5	5.1	ns
t_{PLZ}			2	3.1	4.6	2	4.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1				ns
$t_{sk(o)}$†	Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.5				ns
t_t Transition time	$\overline{B}$ outputs (1.3 V to 1.8 V)		0.9	1.7	3.1	0.5	4.6	ns
	AO outputs (10% to 90%)		0.5	2	3.6	0.4	4.2	
$t_{(pr)}$	$\overline{B}$-port input pulse rejection		1			1		ns

† Skew values are applicable for through mode only.

PARAMETER MEASUREMENT INFORMATION

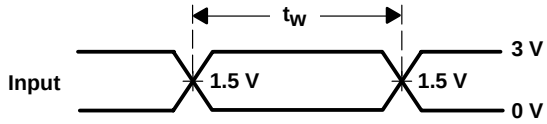


LOAD CIRCUIT FOR A OUTPUTS

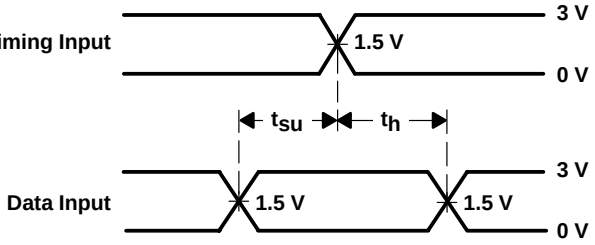


LOAD CIRCUIT FOR B OUTPUTS

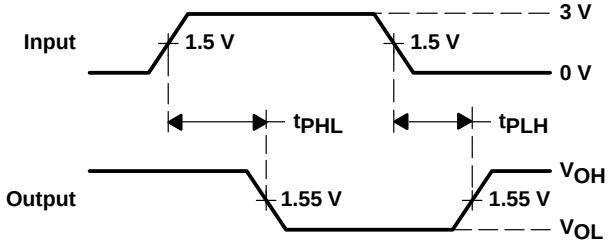
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



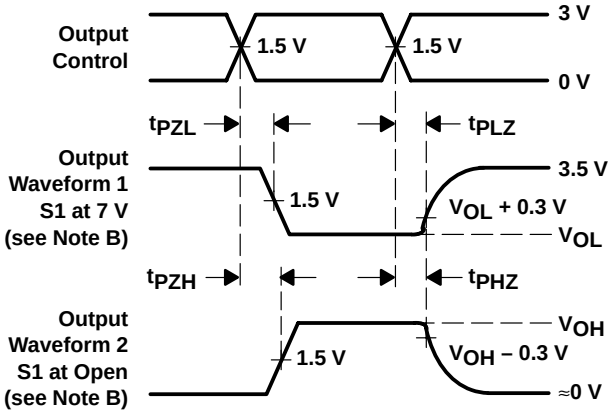
VOLTAGE WAVEFORMS
PULSE DURATION



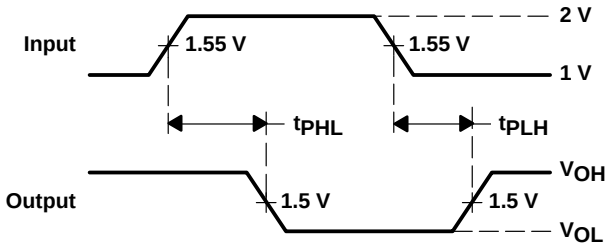
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



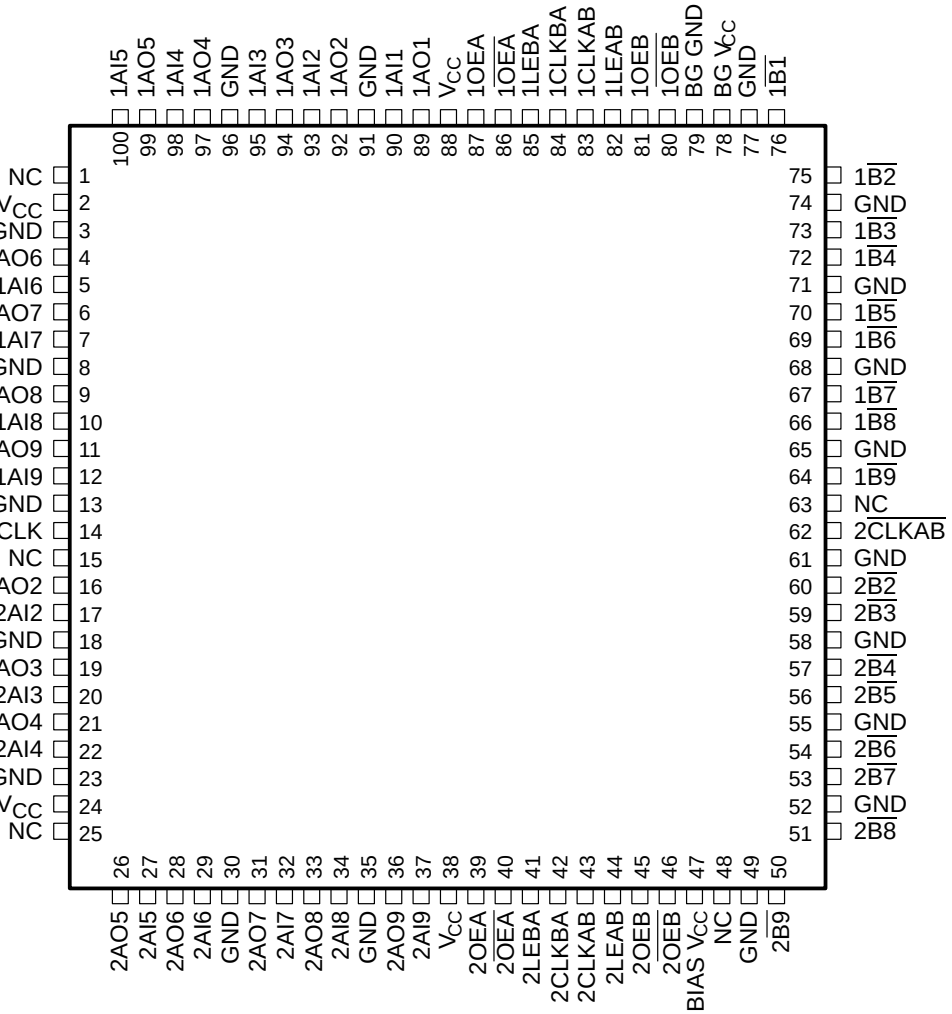
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

PCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74FB1651 contains an 8-bit and 9-bit transceiver with a buffered clock. The clock and the transceivers are designed to translate signals between TTL and backplane transceiver-logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PCA	Tube	SN74FB1651PCA	FB1651

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

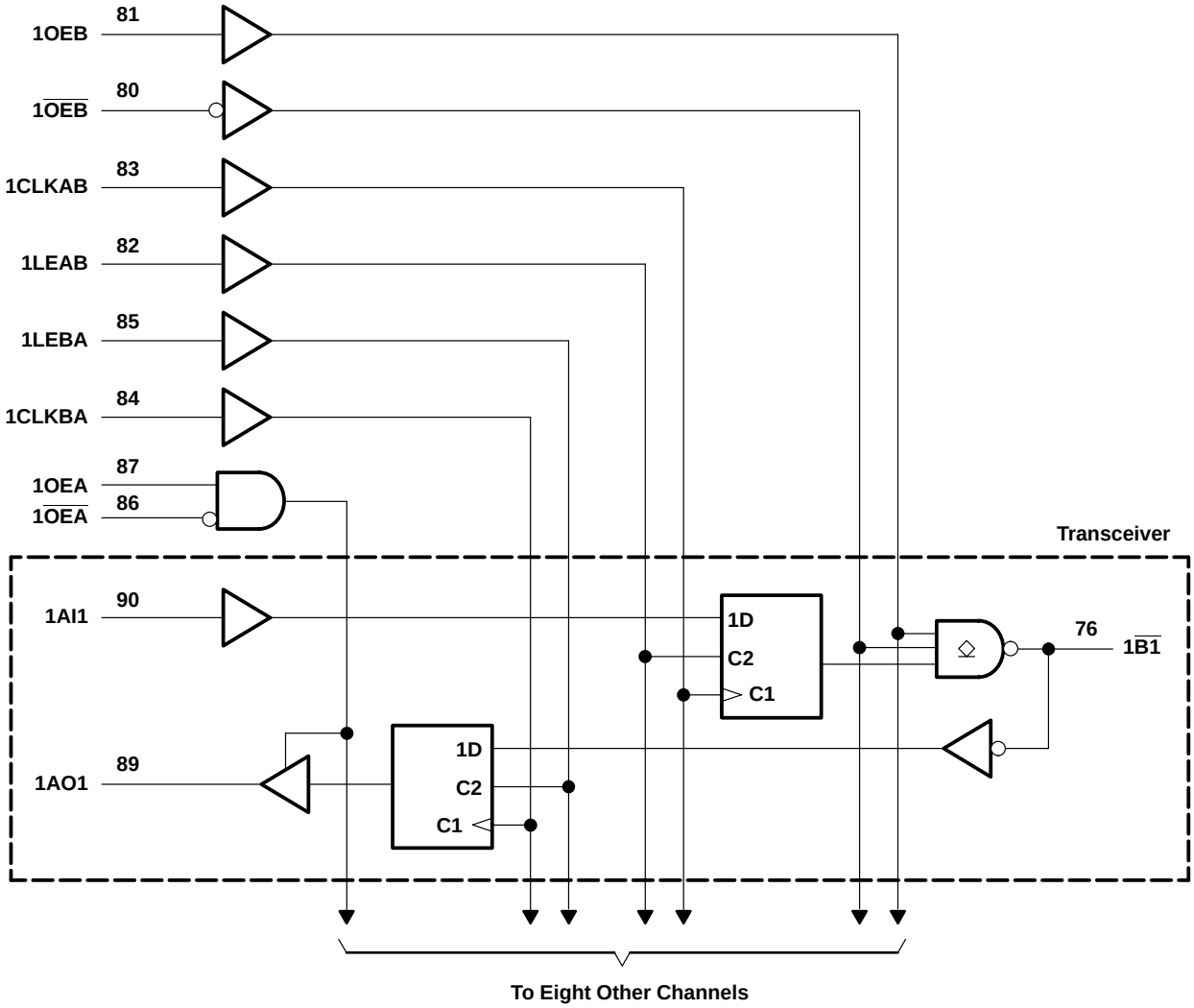
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

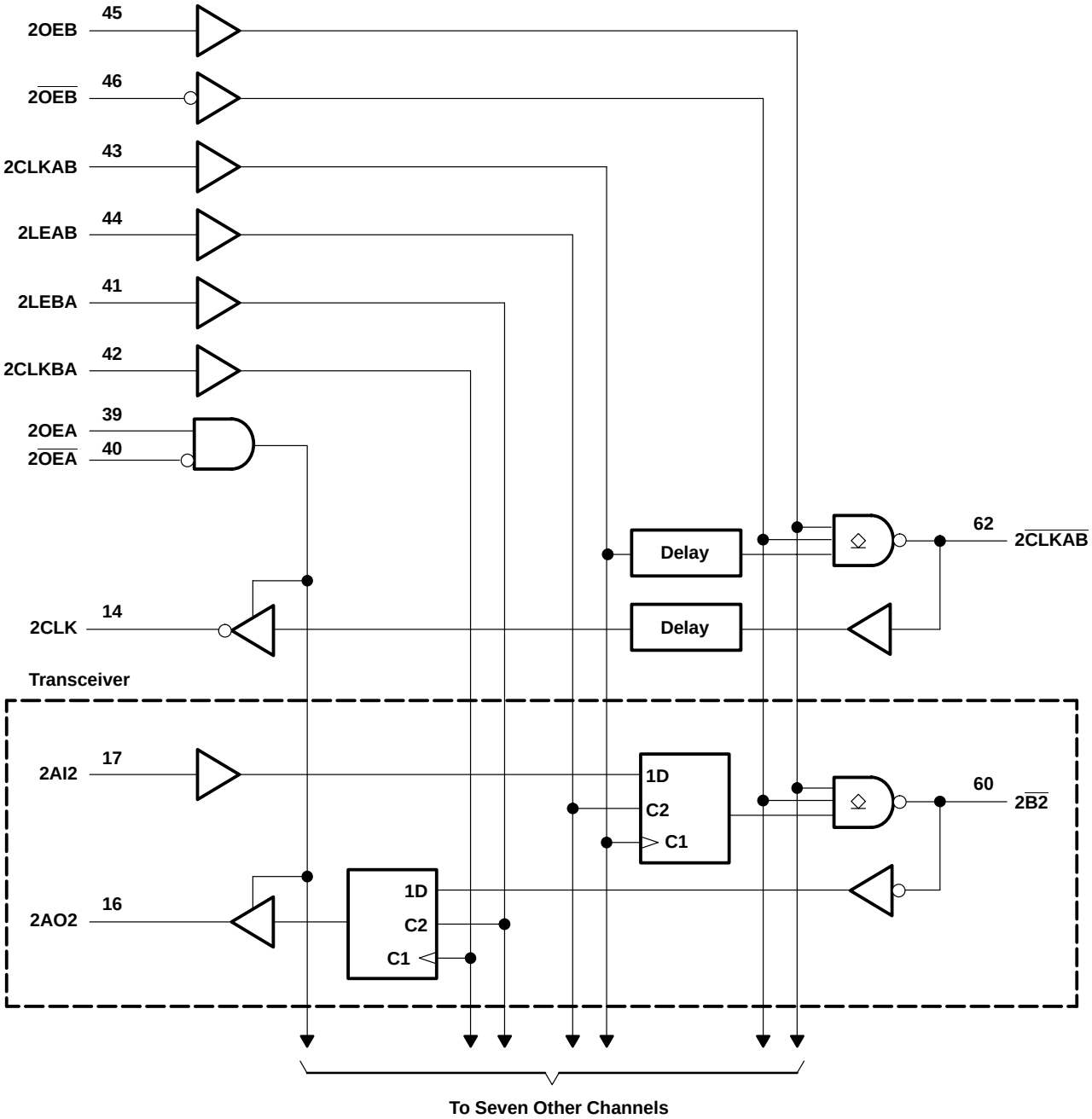
STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



functional block diagram (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}, BIAS V_{CC}, BG V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–3	mA
I_{OL}	Low-level output current	A port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			100	mA
	$\overline{B}$ port to A port					120	
C_i	AI port	V_I = 0.5 V or 2.5 V			5.5		pF
	Control inputs				5.5		
C_o	AO ports	V_O = 0.5 V or 2.5 V			5.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 5.5 V				5.5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0 ,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

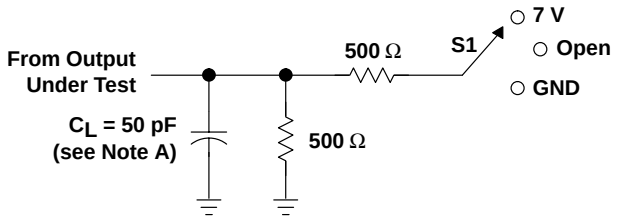
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	CLK or LE	3.3		3.3		ns
t_{su}	Setup time	Data before LE	4.8		4.8		ns
		Data before CLK↑	4.9		4.6		
t_h	Hold time	Data after LE	1.8		1.8		ns
		Data after CLK↑	1.1		1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

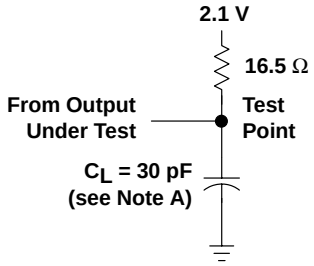
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI	$\overline{B}$	1.8	3.7	5.3	1.8	6.2	ns
t_{PHL}			2.9	4.4	6	2.9	6.6	
t_{PLH}	LEAB	$\overline{B}$	2.7	4.2	5.8	2.7	6.4	ns
t_{PHL}			3.5	5	6.5	3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	3.9	5.5	2.3	6	ns
t_{PHL}			2.9	4.5	6.1	2.9	6.7	
t_{PLH}	2CLKAB	$2\overline{CLKAB}$	4.6	6.9	8.8	4.6	9.9	ns
t_{PHL}			4.9	6.5	8.1	4.9	8.8	
t_{PLH}	$\overline{B}$	AO	3.5	5.9	7.9	3.5	8	ns
t_{PHL}			2.2	3.7	5.3	2.2	5.7	
t_{PLH}	LEBA	AO	1.8	3.2	4.6	1.8	5.1	ns
t_{PHL}			1.7	3	4.4	1.7	4.7	
t_{PLH}	CLKBA	AO	1.8	3.1	4.6	1.8	5.1	ns
t_{PHL}			1.7	3.1	4.6	1.7	4.9	
t_{PLH}	$2\overline{CLKAB}$	2CLK	6.4	9.7	11.8	6.4	13.4	ns
t_{PHL}			4.1	6.9	8.9	4.1	10.3	
t_{PLH}	OEB	$\overline{B}$	2.7	4.6	6.4	2.7	6.7	ns
t_{PHL}			2.9	4.1	5.9	2.9	6.6	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.6	4.3	6.2	2.6	6.6	ns
t_{PHL}			3.4	4.6	6.4	3.4	7	
t_{PZH}	OEA	AO	1.4	2.9	4.4	1.4	4.9	ns
t_{PZL}			1.4	2.6	4	1.4	4.6	
t_{PHZ}	OEA	AO	1.7	3.4	5.1	1.7	5.8	ns
t_{PLZ}			2.2	3.6	5	2.2	5.5	
t_{PZH}	$\overline{OEA}$	AO	1.7	3.3	4.7	1.7	5.5	ns
t_{PZL}			1.7	3.1	4.4	1.7	5.1	
t_{PHZ}	$\overline{OEA}$	AO	1.5	2.9	4.5	1.5	5.1	ns
t_{PLZ}			2	3.1	4.6	2	4.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1				ns
$t_{sk(o)}$†	Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.5				ns
t_t Transition time	$\overline{B}$ outputs (1.3 V to 1.8 V)		0.9	1.7		0.5	4.6	ns
	AO outputs (10% to 90%)		0.5	2		0.4	4.2	
$\overline{B}$-port input pulse rejection			1			1		ns

† Skew values are applicable for through mode only.

PARAMETER MEASUREMENT INFORMATION

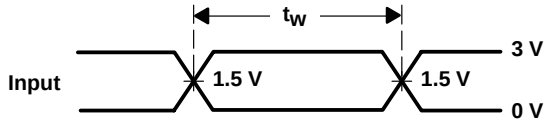


LOAD CIRCUIT FOR A OUTPUTS

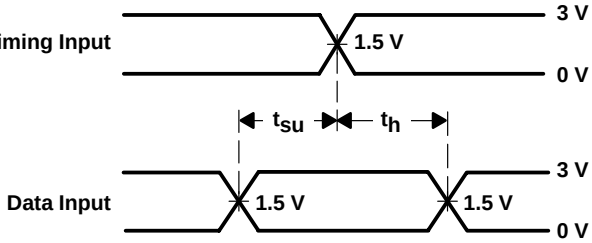


LOAD CIRCUIT FOR B OUTPUTS

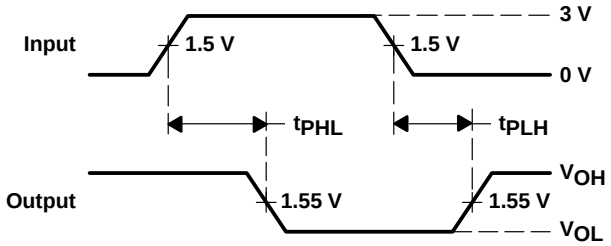
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



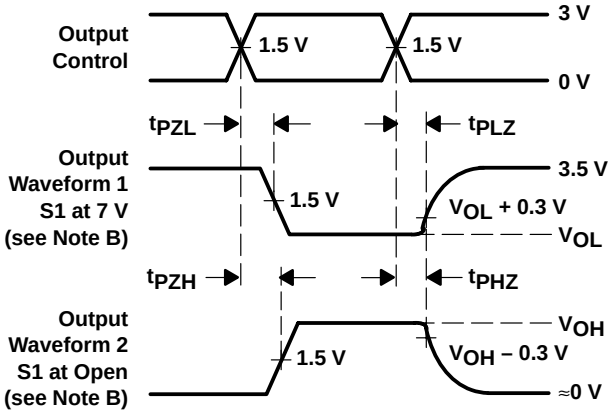
VOLTAGE WAVEFORMS
PULSE DURATION



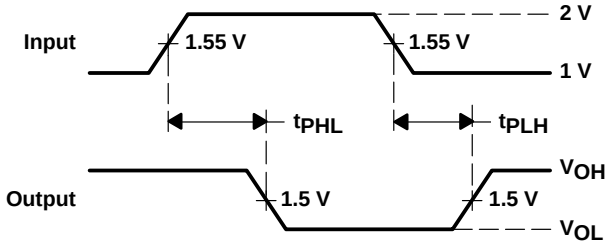
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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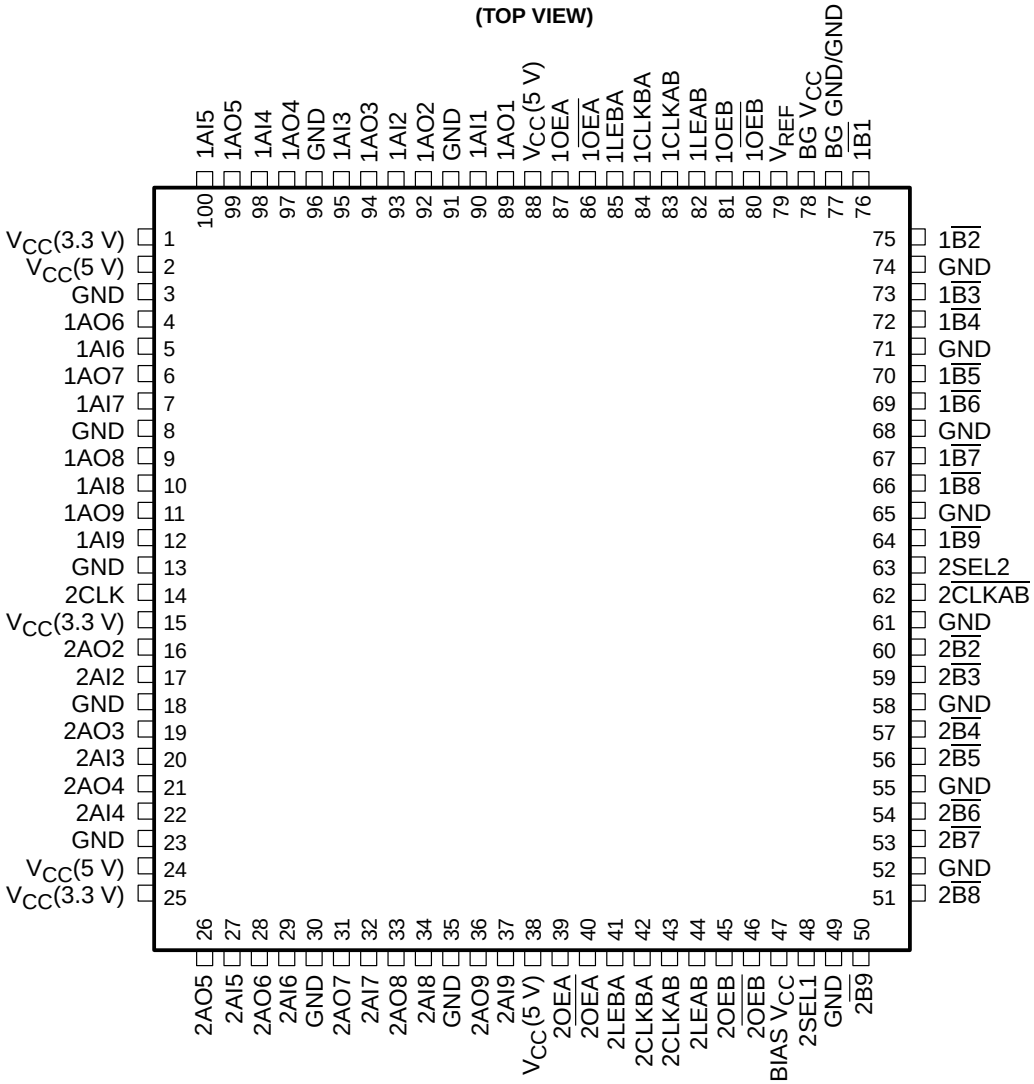
- **LVTTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **High-Impedance State During Power Up and Power Down**
- **Selectable Clock Delay**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion/Withdrawal**

PCA PACKAGE
(TOP VIEW)



description

The SN74FB1653 contains an 8-bit and a 9-bit transceiver with a buffered clock. The clock and transceivers are designed to translate signals between LVTTL and BTL environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991 (BTL).

The A port operates at LVTTL signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC}(5 V) typically is less than 2.5 V, the A outputs are in the high-impedance state.

The $\overline{B}$ port operates at BTL signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC}(5 V) typically is less than 2.5 V, the $\overline{B}$ port is turned off.

The clock-select (2SEL1 and 2SEL2) inputs are used to configure the TTL-to-BTL clock paths and delays (refer to the *Mux-Mode Delay* table).

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC}(5 V) is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

V_{REF} is used to bypass the internal threshold reference voltage of the device. It is recommended that this terminal be decoupled with a 0.1-µF capacitor.

Enhanced heat-dissipation techniques should be used when operating this device from AI to A0 at frequencies greater than 50 MHz, or from AI to $\overline{B}$ or $\overline{B}$ to A0 at frequencies greater than 100 MHz.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TQFP – PCA	Tube	SN74FB1653PCA	FB1653

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

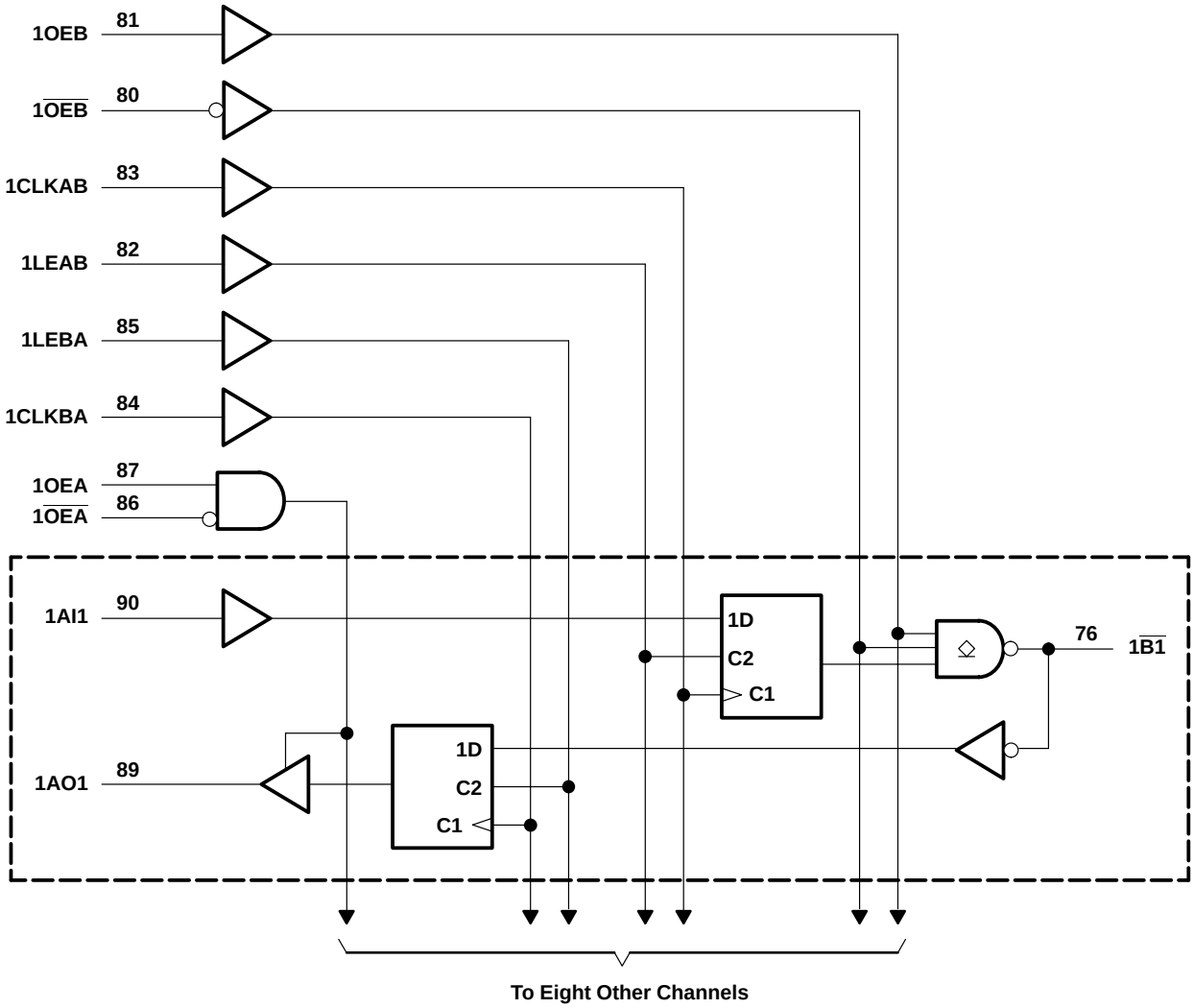
TRANSCEIVER

INPUTS				FUNCTION
$\overline{OEA}$	OEA	OEB	$\overline{OEB}$	
X	X	H	L	$\overline{A}$ data to B bus
L	H	X	X	$\overline{B}$ data to A bus
L	H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
X	X	L	X	B-bus isolation
X	X	X	H	
H	X	X	X	A-bus isolation
X	L	X	X	

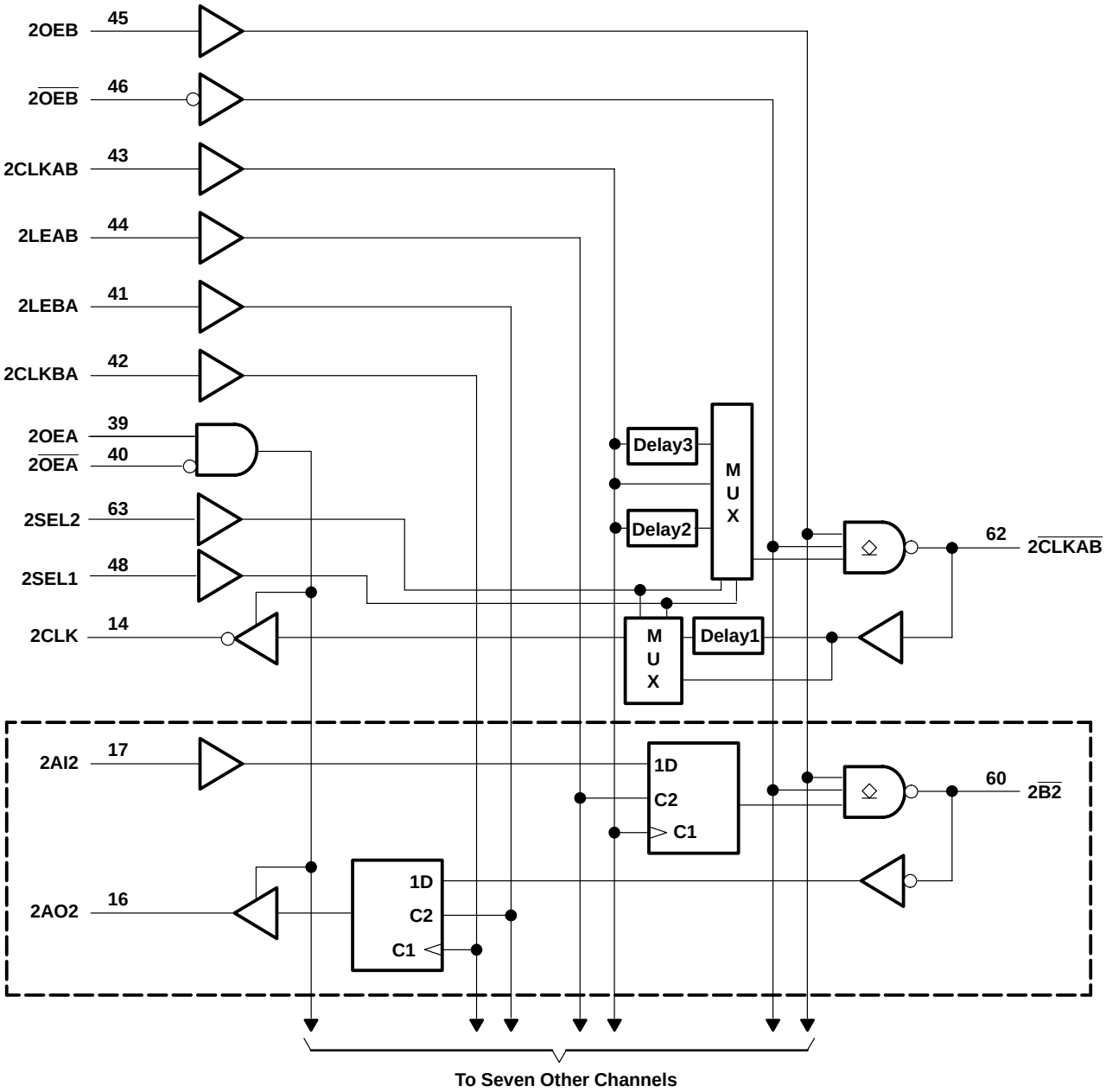
STORAGE MODE

INPUTS		FUNCTION
LE	CLK	
H	X	Transparent
L	↑	Store data
L	L	Storage

functional block diagram



functional block diagram (continued)



MUX-MODE DELAY

INPUTS		DELAY PATH†	
2SEL1	2SEL2	2CLKAB TO 2CLKAB	2CLKAB TO 2CLK
L	L	No delay	No delay
L	H	No delay	Delay1
H	L	Delay2	Delay1
H	H	Delay3	Delay1

† Refer to delay1 through delay3 in the functional block diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: V_{CC}(5 V), BIAS V_{CC}, BG V_{CC} . . . . . –0.5 V to 7 V
V_{CC}(3.3 V) . . . . . –0.5 V to 4.6 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current applied to any single output in the low state: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 22°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}, BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{CC}(3.3 V)	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3.3 V	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port		I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OH} = –3 mA	2.5			V
V_{OL}	AO port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC}(5 V) = 4.5 V, V_{CC}(3.3 V) = 3 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC}(5 V) = 0 to 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.6 V	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{CC}(5 V)	AI port to $\overline{B}$ port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.3 V	I_O = 0			145	mA
	$\overline{B}$ port to AO port					130	
	Outputs disabled					120	
I_{CC}(3.3 V)	$\overline{B}$ port to AO port	V_{CC}(5 V) = 5.5 V, V_{CC}(3.3 V) = 3.3 V	I_O = 0			1	mA
C_i	Control and AI inputs	V_I = 0.5 V or 2.5 V			6.5		pF
C_o	AO port	V_O = 0.5 V or 2.5 V			3.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC}(5 V) = 0 to 5.5 V,	V_{CC}(3.3 V) = 3.3 V			6.5	pF

† All typical values are at V_{CC}(5 V) = 5 V and V_{CC}(3.3 V) = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC}(5 V) = 0 to 4.5 V, V_{CC}(3.3 V) = 3.3 V	V_B = 0 to 2 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC}(5 V) = 4.5 V to 5.5 V, V_{CC}(3.3 V) = 3.3 V			10	
V_O	$\overline{B}$ port	V_{CC}(5 V) = 0, V_{CC}(3.3 V)= 0 V	V_I (BIAS V_{CC}) = 5 V	1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC}(5 V) = 0, V_{CC}(3.3 V) = 0 V	V_B = 1 V, V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC}(5 V) = 0 to 5.5 V, V_{CC}(3.3 V) = 3.3 V	OEB = 0 to 0.8 V		100	
		V_{CC}(5 V) = 0 to 2.2 V, V_{CC}(3.3 V) = 3.3 V	OEB = 0 to 5 V		100	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

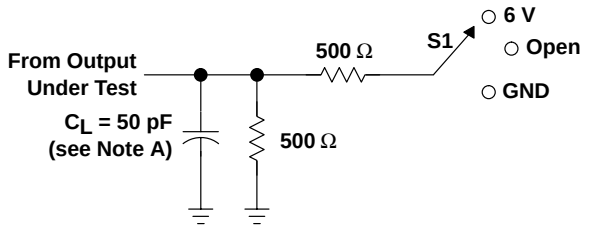
			MIN	MAX	UNIT
f_{clock}	Clock frequency			90	MHz
t_w	Pulse duration	LE high	3		ns
		CLK high or low	3		
t_{su}	Setup time	AI or $\overline{B}$ before LE↓	3.5		ns
		AI or $\overline{B}$ before CLK↑	3.5		
t_h	Hold time	AI or $\overline{B}$ after LE↓	1		ns
		AI or $\overline{B}$ after CLK↑	0.7		

switching characteristics over recommended operating free-air temperature range, V_{CC}(5 V) = 5 V ± 0.5 V and V_{CC}(3.3 V) = 3.3 V (see Figure 1)

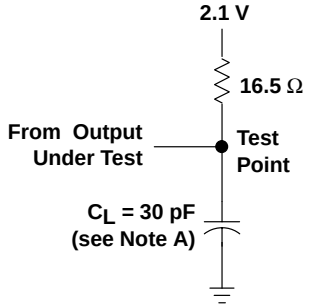
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			90		MHz
t_{PLH}	AI	$\overline{B}$	1.8	6.2	ns
t_{PHL}			2.9	6.6	
t_{PLH}	LEAB	$\overline{B}$	2.7	6.9	ns
t_{PHL}			3.5	7.3	
t_{PLH}	CLKAB	$\overline{B}$	2.3	6.4	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (no delay)	$2\overline{CLKAB}$	2.3	6	ns
t_{PHL}			2.9	6.7	
t_{PLH}	2CLKAB (delay2)	$2\overline{CLKAB}$	4.5	9.5	ns
t_{PHL}			4.5	9.5	
t_{PLH}	2CLKAB (delay3)	$2\overline{CLKAB}$	9.3	15.4	ns
t_{PHL}			9.3	15.4	
t_{PLH}	$\overline{B}$	AO	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	LEBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	CLKBA	AO	1.8	6.3	ns
t_{PHL}			1.8	6.3	
t_{PLH}	$2\overline{CLKAB}$ (delay1)	2CLK	5.7	12.3	ns
t_{PHL}			5.7	12.3	
t_{PLH}	$2\overline{CLKAB}$ (no delay)	2CLK	2	6.5	ns
t_{PHL}			2	6.5	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$	2.6	7	ns
t_{PHL}			2.6	7	
t_{PZH}	OEA or $\overline{OEA}$	AO	1.4	5.5	ns
t_{PZL}			1.4	5.5	
t_{PHZ}	OEA or $\overline{OEA}$	AO	1.4	6.5	ns
t_{PLZ}			1.4	5.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1.6	ns
	Pulse skew, $2\overline{CLKAB}$ to 2CLK			1.8	
$t_{sk(p)}$	Pulse skew, CLKAB to $\overline{B}$ or CLKBA to AO			1.5	ns
	Pulse skew, CLKAB to $2\overline{CLKAB}$			1.4	
$t_{sk(HL)}$, $t_{sk(LH)}$†	Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO			1	ns
$t_{sk(o)}$‡	Output skew, nondelayed mode for $2\overline{CLKAB}$, CLKAB to AO			1	ns
	Output skew, nondelayed mode for $2\overline{CLKAB}$, CLKAB to $\overline{B}$ and $2\overline{CLKAB}$			1	
$t_{sk(o)}$‡	Output skew, nondelayed mode for $2\overline{CLKAB}$, CLKAB to $\overline{B}$ and $2\overline{CLKAB}$			1.5	ns
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.5	4.6	ns
	Transition time, AO outputs (10% to 90%)		0.4	4.2	
t_{PR}	$\overline{B}$-port input pulse rejection		1		ns

† Skew values are applicable for through mode only, with single-output switching.
‡ Skew values are applicable for CLK mode only, with all outputs simultaneously switching high-to-low or low-to-high.

PARAMETER MEASUREMENT INFORMATION

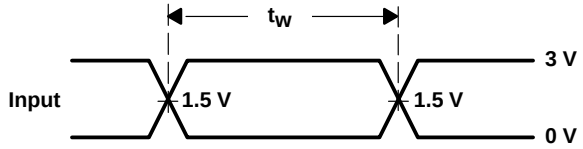


LOAD CIRCUIT FOR A OUTPUTS

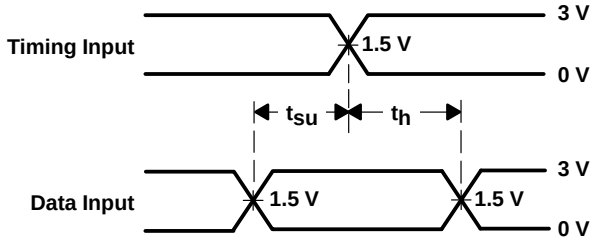


LOAD CIRCUIT FOR B OUTPUTS

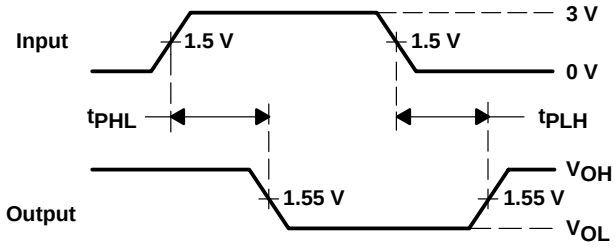
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



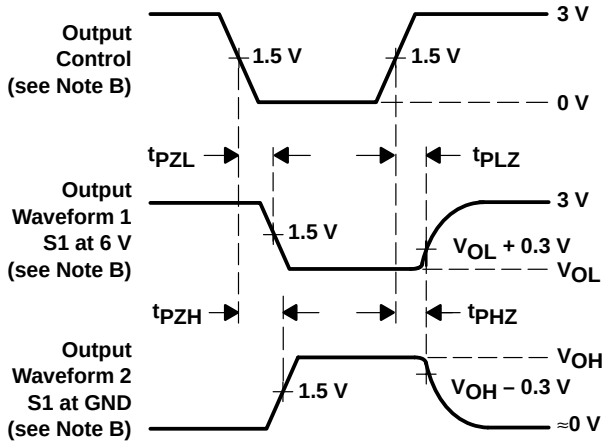
VOLTAGE WAVEFORMS
PULSE DURATION



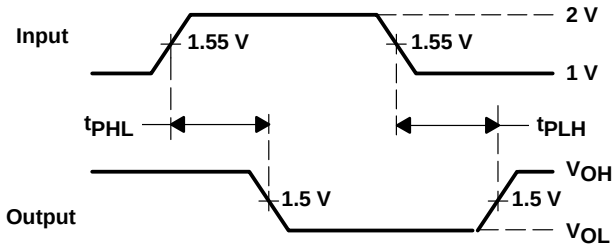
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A to B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A port)



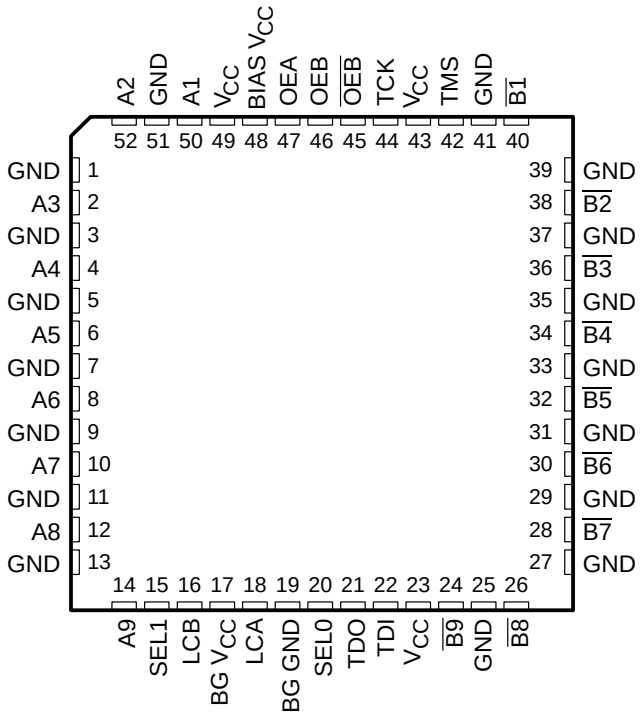
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **High-Impedance State During Power Up and Power Down**
- **BIAS V_{CC} Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2031 is a 9-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL signal levels. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus, although currently there are no plans to release a JTAG-featured version. TMS and TCK are not connected and TDI is shorted to TDO.

description (continued)

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

BG V_{CC} and BG GND are the supply inputs for the bias generator.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2031RC	FB2031

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

TRANSCEIVER

INPUTS			FUNCTION
OEA	OEB	$\overline{OEB}$	
L	H	L	$\overline{A}$ data to B bus
H	L	X	$\overline{B}$ data to A bus
H	X	H	
H	H	L	$\overline{A}$ data to B bus, $\overline{B}$ data to A bus
L	L	X	Isolation
L	X	H	

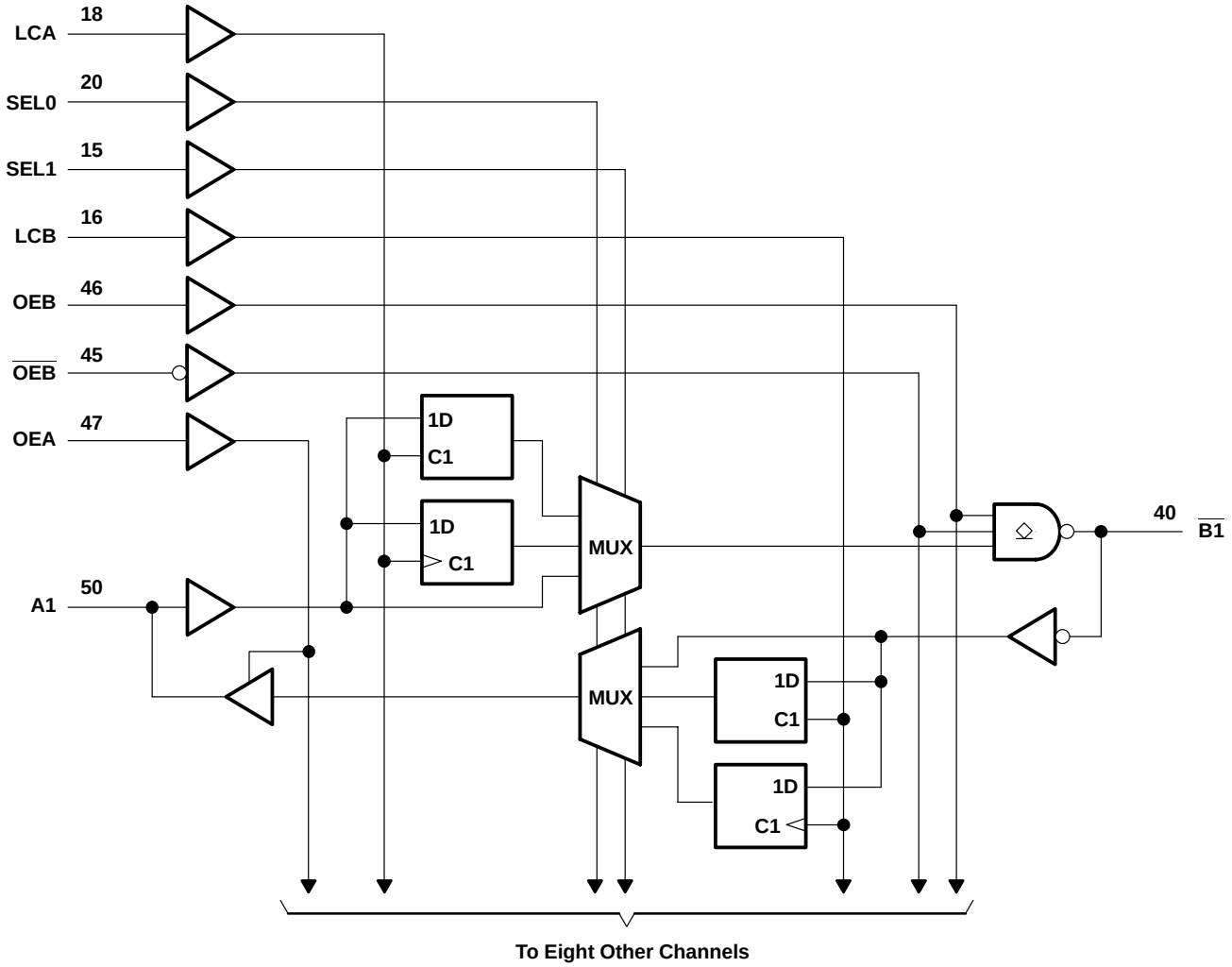
STORAGE MODE

LCA, LCB	RESULT
0	Transparent
1	Latches latched
↑	Flip-flops triggered

SELECT

SEL1	SEL0	MUX A B	MUX B A
0	0	Latch	Latch
0	1	Through	Through
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	A port			–3	mA
I_{OL}	Low-level output current	A port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	A port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	A port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OZH}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	A port	V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	A port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	A port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–30		–150	mA
I_{CC}	A port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			78	mA
	$\overline{B}$ port to A port					78	
C_i		V_I = 0.5 V or 2.5 V			4.5		pF
C_{io}	A port	V_O = 0.5 V or 2.5 V			8.5		pF
	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 5.5 V				6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

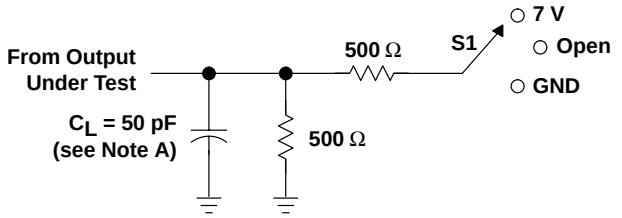
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				150	MHz
t_w	Pulse duration	LCA or LCB		3.3		ns
t_{su}	Setup time	Clock mode	Data before LCA↑	1.4		ns
			Data before LCB↑	2.8		
		Latch mode	Data before LCA↑	1.1		
			Data before LCB↑	2.4		
t_h	Hold time	Clock mode	Data after LCA↑	0.6		ns
			Data after LCB↑	0		
		Latch mode	Data after LCA↑	0.9		
			Data after LCB↑	0		

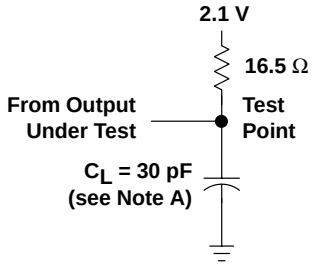
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	A (through mode)	$\overline{B}$	3.7	4.5	5.9	3.2	6.6	ns
t_{PHL}			2.9	4	5.7	2.6	5.9	
t_{PLH}	A (transparent)	$\overline{B}$	4.1	5	6.5	3.6	7.3	ns
t_{PHL}			3.3	4.5	6.1	3	6.5	
t_{PLH}	LCA	$\overline{B}$	4.5	5.4	7	3.9	7.8	ns
t_{PHL}			4	5.1	6.7	3.4	7.4	
t_{PLH}	LCB	A	2.8	3.7	4.7	1.9	6	ns
t_{PHL}			2.5	3.4	4.9	1.8	5.5	
t_{PLH}	SEL1 or SEL0	A	2.5	3.8	5.3	1.9	6.3	ns
t_{PHL}			2.2	3.5	5.1	1.6	5.6	
t_{PLH}	SEL1 or SEL0	$\overline{B}$	4.1	5.3	6.9	3.7	7.8	ns
t_{PHL}			3.7	5.2	6.9	3.3	7.7	
t_{PLH}	$\overline{B}$ (through mode)	A	3.1	4	5.6	2.2	7.1	ns
t_{PHL}			2.6	3.4	4.9	1.4	5.7	
t_{PLH}	$\overline{B}$ (transparent)	A	3.3	4.2	5.9	2.4	7.6	ns
t_{PHL}			2.8	3.9	5.5	1.8	6.3	
t_{PLH}	OEB or $\overline{OEB}$	$\overline{B}$	3.7	4.6	6.1	3.2	6.7	ns
t_{PHL}			2.9	4.3	5.8	2.5	6.4	
t_{PZH}	OEA	A	2.3	3.1	4.5	1.6	5	ns
t_{PZL}			1.9	2.7	4.1	1.6	4.4	
t_{PHZ}	OEA	A	2.2	3.1	4.5	1.5	5.2	ns
t_{PLZ}			2.5	3.3	4.9	2	5.2	
$t_{sk(p)}$ Pulse skew	A	$\overline{B}$		0.5				ns
	$\overline{B}$	A		0.3				
$t_{sk(o)}$ Output skew	A	$\overline{B}$		0.2				ns
	$\overline{B}$	A		0.3				
t_t	Transition time, $\overline{B}$ outputs (1.3 V to 1.8 V)		0.6	2	2.8	0.4	2.9	ns
	Transition time, $\overline{A}$ outputs (10% to 90%)		0.5	3.5	4.7	0	5.4	
$t_{(pr)}$	$\overline{B}$-port input pulse rejection		1			1		ns

PARAMETER MEASUREMENT INFORMATION

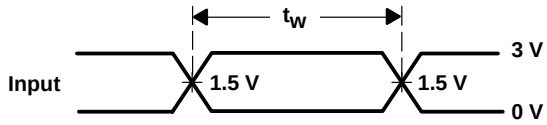


LOAD CIRCUIT FOR A OUTPUTS

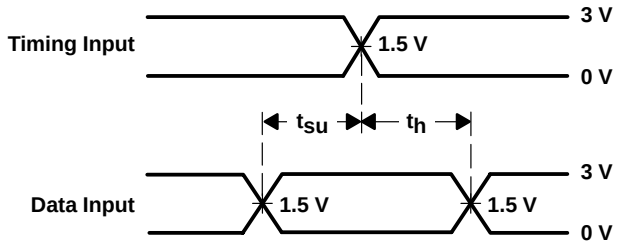


LOAD CIRCUIT FOR B OUTPUTS

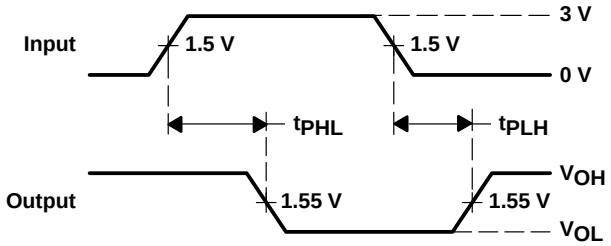
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



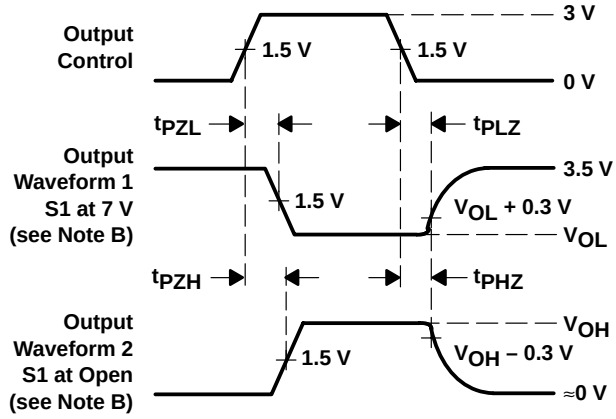
VOLTAGE WAVEFORMS
PULSE DURATION



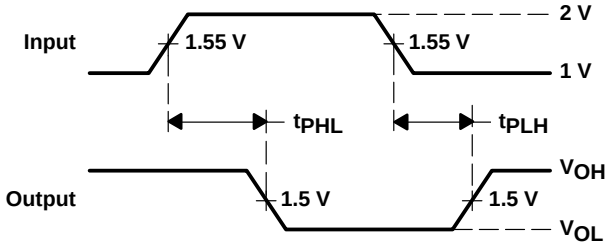
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



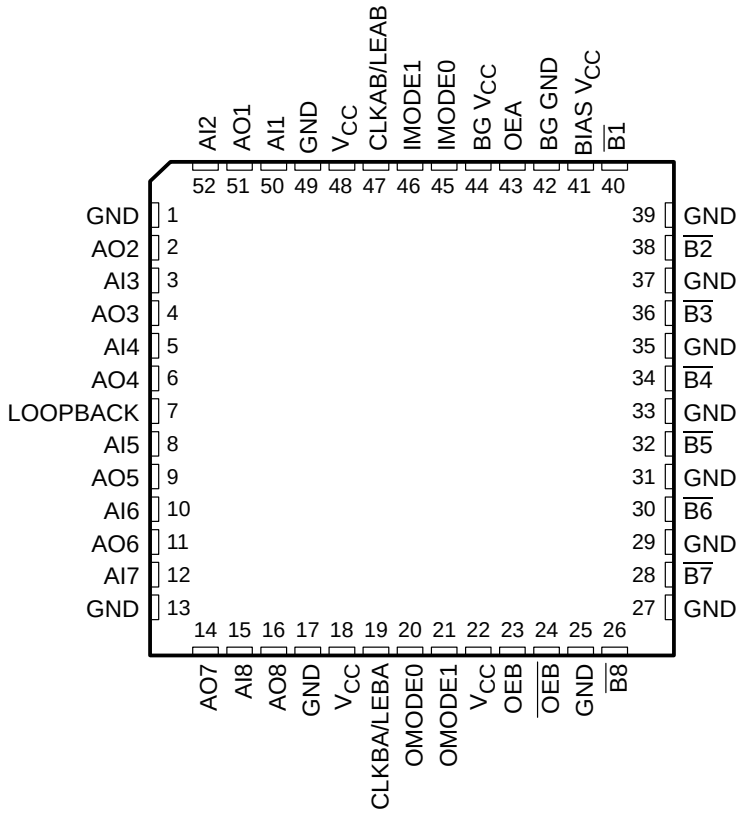
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2033A is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.

description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2033ARC	FB2033A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

FUNCTION/MODE

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	$\overline{B}$
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

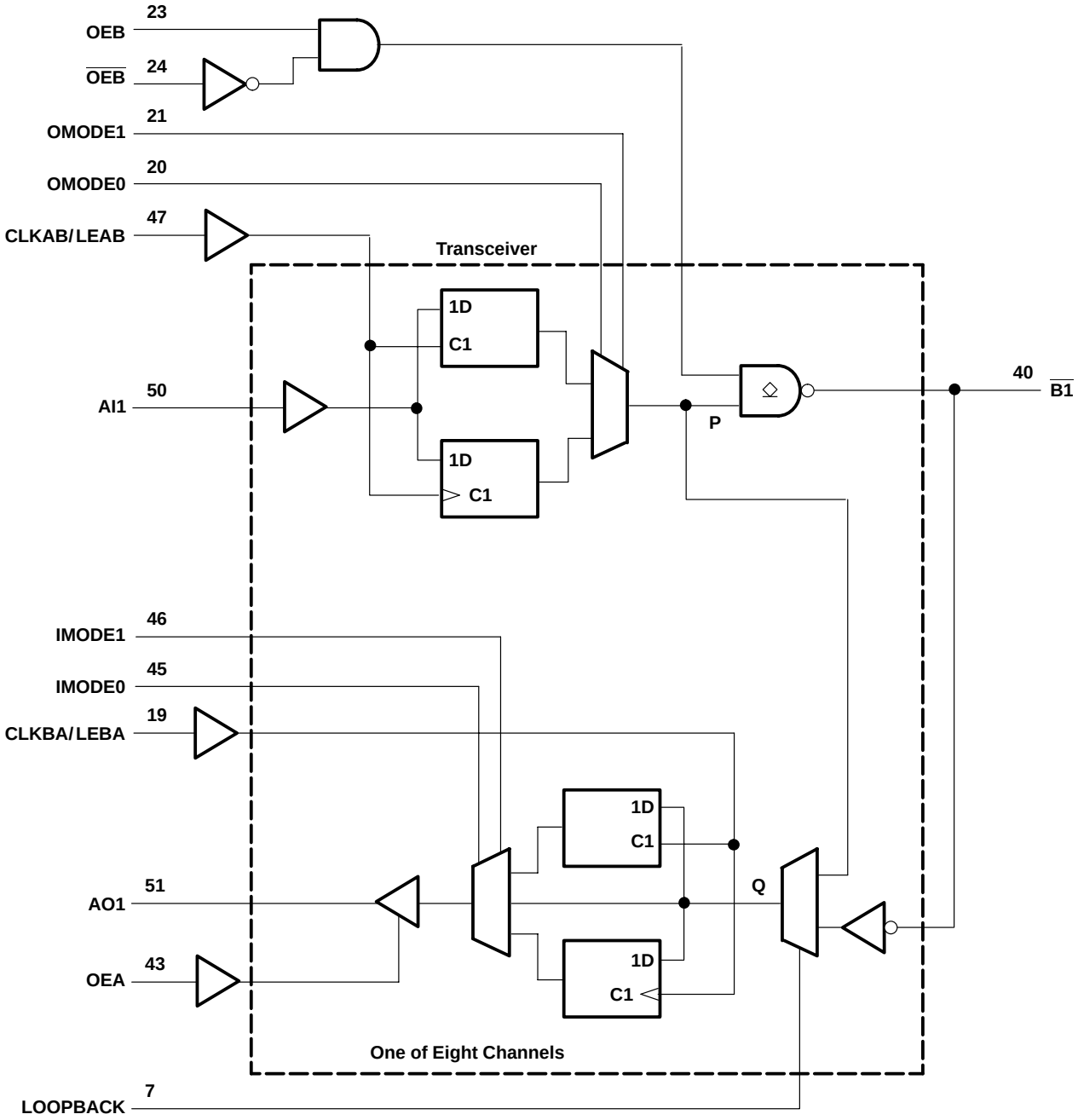
SELECT

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = –10 µA			V_{CC}–1.1	V
		V_{CC} = 4.75 V	I_{OH} = –3 mA	2.5	2.85	3.4	
			I_{OH} = –32 mA	2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5	V
			I_{OL} = 55 mA			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	
			I_{OL} = 4 mA	0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100	µA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	µA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V	V_I = 0.5 V			–50	µA
	$\overline{B}$ port‡		V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	µA
I_{OZPU}		V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}		V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OZH}	AO port	V_{CC} = 5.25 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.25 V,	V_O = 0.5 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	–40	–80	–150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	70	mA
C_i	AI port and control inputs	V_I = 0.5 V or 2.5 V			5		pF
C_o	AO port	V_O = 0.5 V or 2.5 V			5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				6	

† All typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		10	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

NOTE 3: The power-up sequence is GND, BIAS V_{CC}, V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t_{su}	Setup time	Data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t_h	Hold time	Data after CLKAB/LEAB or CLKBA/LEBA↑	0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			150			150		MHz
t_{PLH}	AI (through mode)	$\overline{B}$	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.9	3	4.2	1.9	4.5	
t_{PLH}	$\overline{B}$ (through mode)	AO	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			3	4.2	5.6	3	5.7	
t_{PLH}	AI (transparent)	$\overline{B}$	2.3	3.6	4.6	2.3	5.6	ns
t_{PHL}			1.9	3	4.1	1.9	4.5	
t_{PLH}	$\overline{B}$ (transparent)	AO	2.5	4.2	5.5	2.5	6.1	ns
t_{PHL}			3	4.2	5.6	3	5.7	
t_{PLH}	OEB	$\overline{B}$	2.4	3.7	4.7	2.4	5.8	ns
t_{PHL}			1.8	3	4.1	1.8	4.4	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2	3.4	4.3	2	5.2	ns
t_{PHL}			2	3.3	4.4	2	4.8	
t_{PZH}	OEA	AO	2	3.5	4.6	2	5.1	ns
t_{PZL}			2.7	4.2	5.1	2.7	5.4	
t_{PHZ}	OEA	AO	2.1	4	5	2.1	5.5	ns
t_{PLZ}			1.6	2.8	3.9	1.6	4.3	
t_{PLH}	CLKAB/LEAB	$\overline{B}$	3	4.7	5.8	3	6.9	ns
t_{PHL}			2.8	4.3	5.6	2.8	6.1	
t_{PLH}	CLKBA/LEBA	AO	2	3.6	4.9	2	5.4	ns
t_{PHL}			2.2	3.5	4.7	2.2	5.1	
t_{PLH}	OMODE	$\overline{B}$	2.4	5	6.1	2.4	7.2	ns
t_{PHL}			2.4	4.5	6	2.4	6.7	
t_{PLH}	IMODE	AO	1.8	4	5.3	1.8	5.9	ns
t_{PHL}			2.3	4.1	5.2	2.3	5.4	
t_{PLH}	LOOPBACK	AO	2.4	5	7	2.4	8	ns
t_{PHL}			3.1	4.6	5.7	3.1	5.9	
t_{PLH}	AI	AO	1.9	3.7	5.5	1.9	6.1	ns
t_{PHL}			2.6	4.2	5.6	2.6	5.8	
t_r	Rise time,1.3 V to 1.8 V, $\overline{B}$ port		0.5	1.2	2.1	0.5	3	ns
t_f	Fall time, 1.8 V to 1.3 V, $\overline{B}$ port		0.5	1.4	2.3	0.5	3	
t_r	Rise time, 10% to 90%, AO		2	3.3	4.2	2	5	ns
t_f	Fall time, 90% to 10%, AO		1	2.5	3.4	1	5	
$\overline{B}$-port input pulse rejection						1		ns

output-voltage characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OHP}	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		4.5	V
V_{OHV}	Minimum output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1	1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch	$\overline{B}$ port	I_{OL} = –50 mA	0.3		V

PARAMETER MEASUREMENT INFORMATION

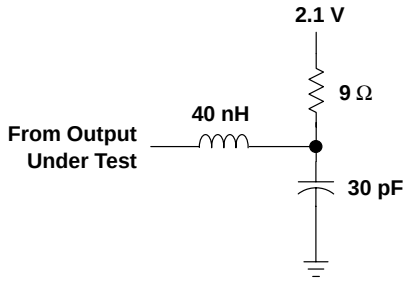
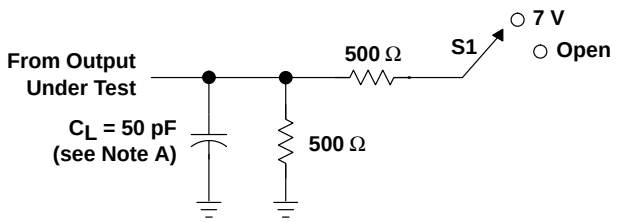
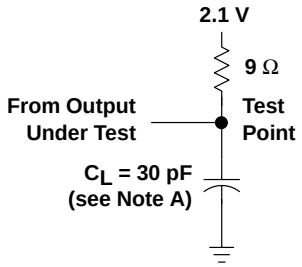


Figure 1. Load Circuit for V_{OHP} and V_{OHV}

PARAMETER MEASUREMENT INFORMATION

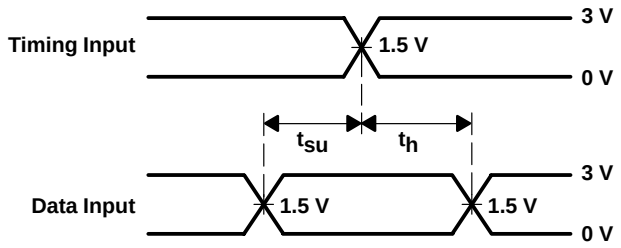


LOAD CIRCUIT FOR A OUTPUTS

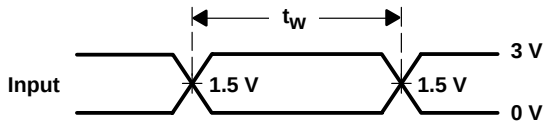


LOAD CIRCUIT FOR B OUTPUTS

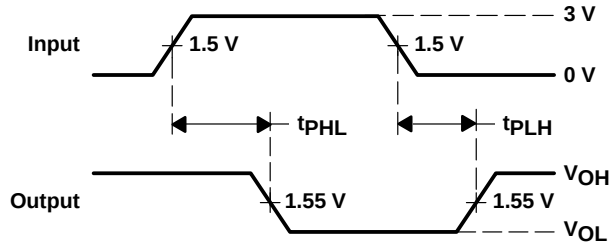
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



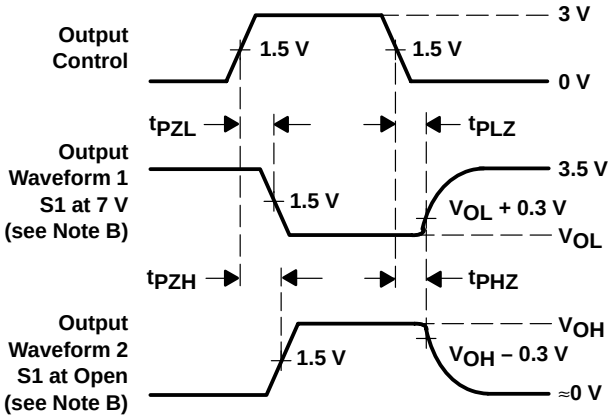
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



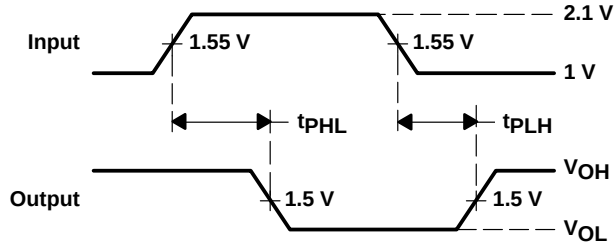
VOLTAGE WAVEFORMS
PULSE DURATION



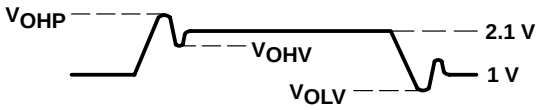
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



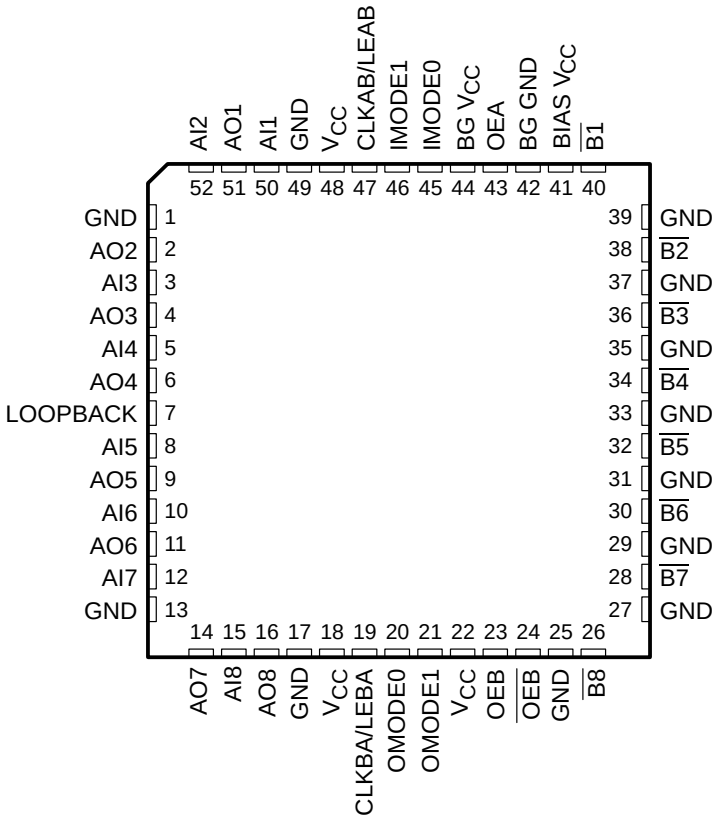
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2033K is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector $\overline{B}$ port operates at backplane transceiver logic (BTL) signal levels. The SN74FB2033K is specifically designed to be compatible with IEEE Std 1194.1-1991.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.

description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, $\overline{B}$-port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (before inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The $\overline{B}$ port is controlled by OEB and $\overline{OEB}$. If OEB is low, or $\overline{OEB}$ is high, or when V_{CC} is less than 2.5 V, the $\overline{B}$ port is inactive. If OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ($\overline{B}$ port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both of these clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2033KRC	FB2033K

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

FUNCTION

INPUTS								FUNCTION/MODE
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$, buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$, flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$, latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$, $\overline{B}$ to AO

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{OEB}$	AO	B
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q_0

Function Tables (Continued)

LOOPBACK

LOOPBACK	Q†
L	$\overline{B}$ port
H	Point P‡

† Q is the input to the B-to-A logic element.
‡ P is the output of the A-to-B logic element (see functional block diagram).

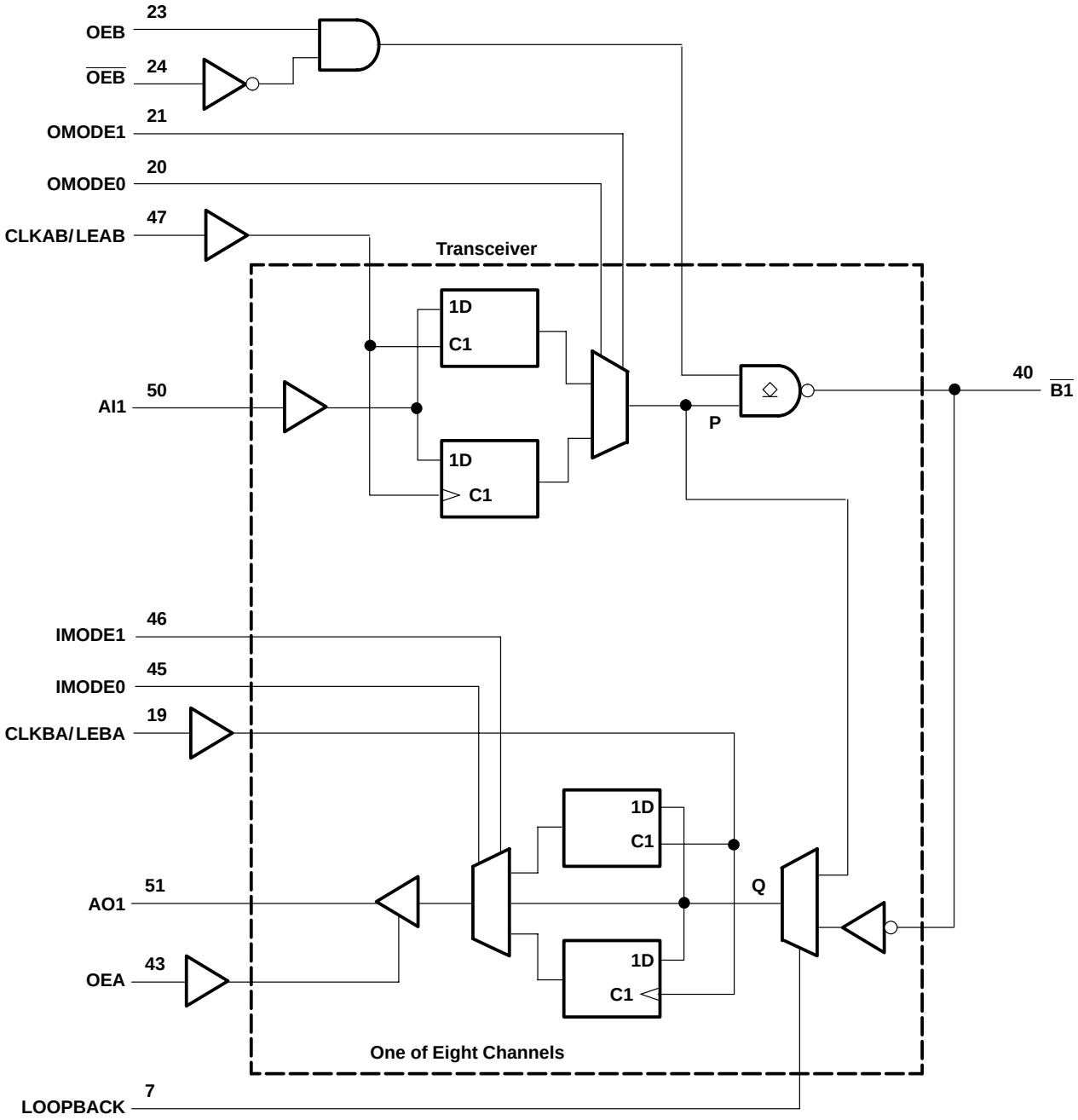
SELECT

INPUTS		SELECTED-LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q_0
↑	L	H
↑	H	L

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Voltage range applied to any B output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BG V_{CC}	Supply voltage		4.75	5	5.25	V
BIAS V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.75 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.75 V to 5.25 V,	I_{OH} = –10 µA			V_{CC}–1.1	V
		V_{CC} = 4.75 V	I_{OH} = –3 mA	2.5	2.85	3.4	
			I_{OH} = –32 mA	2			
V_{OL}	AO port	V_{CC} = 4.75 V	I_{OL} = 20 mA		0.33	0.5	V
			I_{OL} = 55 mA			0.8	
	$\overline{B}$ port	V_{CC} = 4.75 V	I_{OL} = 100 mA	0.75		1.1	
			I_{OL} = 4 mA	0.5			
I_I	Except $\overline{B}$ port	V_{CC} = 0,	V_I = 5.25 V			100	µA
I_{IH}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 2.7 V			50	µA
	$\overline{B}$ port‡	V_{CC} = 0 to 5.25 V,	V_I = 2.1 V			100	
I_{IL}	Except $\overline{B}$ port	V_{CC} = 5.25 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port‡	V_{CC} = 5.25 V,	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.25 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 2.1 V to 5.25 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 2.1 V to 5.25 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	A port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	A port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.25 V,	V_O = 0	–40	–80	–150	mA
I_{CC}	All outputs on	V_{CC} = 5.25 V,	I_O = 0		45	70	mA
C_i	AI port and control inputs	V_I = 0.5 V or 2.5 V			5		pF
C_o	AO port	V_O = 0.5 V or 2.5 V			5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.75 V				6	pF
		V_{CC} = 4.75 V to 5.25 V				6	

† All typical values are at V_{CC} = 5 V, TA = 25°C
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.75 V,	V_B = 0 to 2 V,	BIAS V_{CC} = 4.5 V to 5.5 V		1.2	mA
		V_{CC} = 4.75 V to 5.25 V,	V_B = 0 to 2 V,	BIAS V_{CC} = 4.5 V to 5.5 V		10	µA
V_O	$\overline{B}$ port	V_{CC} = 0,	BIAS V_{CC} = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.75 V to 5.25 V	–1		µA
		V_{CC} = 0 to 5.25 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

NOTE 3: Power-up sequence is GND, BIAS V_{CC}, V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA↑	0.7		0.7		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}				150			150		MHz
t_{PLH}		AI (through mode)	$\overline{B}$	2.8	5.1	6.8	2.8	8.1	ns
t_{PHL}				2.5	4.2	5.7	2.5	6.1	
t_{PLH}		$\overline{B}$ (through mode)	AO	3.1	4.3	5.1	2.2	6.6	ns
t_{PHL}				3.1	4.2	5.1	2.6	6	
t_{PLH}		AI (transparent)	$\overline{B}$	2.8	5.1	6.8	2.8	8.1	ns
t_{PHL}				2.6	4.2	5.7	2.6	6.1	
t_{PLH}		$\overline{B}$ (transparent)	AO	2.2	4.3	6	2.2	6.6	ns
t_{PHL}				2.5	4.2	5.6	2.5	6	
t_{PLH}		OEB	$\overline{B}$	2.7	5.1	6.8	2.7	8.3	ns
t_{PHL}				2.4	4.2	5.7	2.4	6.1	
t_{PLH}		$\overline{OEB}$	$\overline{B}$	2.5	4.8	6.4	2.5	7.7	ns
t_{PHL}				2.5	4.3	5.9	2.5	6.4	
t_{PZH}		OEA	AO	1.6	3.6	5.1	1.6	5.6	ns
t_{PZL}				2.3	4.3	5.7	2.3	6	
t_{PHZ}		OEA	AO	1.7	4	5.5	1.7	5.9	ns
t_{PLZ}				1.2	2.9	4.4	1.2	4.7	
t_{PLH}		CLKAB/LEAB	$\overline{B}$	5.2	6.5	7.8	3.7	9.9	ns
t_{PHL}				3.8	5.4	7.1	3.4	7.7	
t_{PLH}		CLKBA/LEBA	AO	1.7	3.8	5.5	1.7	5.9	ns
t_{PHL}				1.8	3.6	5.1	1.8	5.5	
t_{PLH}		OMODE	$\overline{B}$	2.9	6.6	8.4	2.9	10	ns
t_{PHL}				3	5.7	7.5	3	8.3	
t_{PLH}		IMODE	AO	1.4	4.1	5.8	1.4	6.4	ns
t_{PHL}				1.9	4.2	5.7	1.9	5.9	
t_{PLH}		LOOPBACK	AO	2	5.2	7.3	2	8.2	ns
t_{PHL}				2.6	4.8	6.3	2.6	6.4	
t_{PLH}		AI	AO	1.7	3.9	5.6	1.7	6.1	ns
t_{PHL}				2.2	4.3	5.7	2.2	5.9	
t_r	Rise time, 1.3 V to 1.8 V, $\overline{B}$ port			1.8	2.5	3.8	1.7	4	ns
t_f	Fall time, 1.8 V to 1.3 V, $\overline{B}$ port			1.7	2.5	3.8	1.5	4	
t_r	Rise time, 10% to 90%, AO			2.5	3.4	4.8	2	5	ns
t_f	Fall time, 90% to 10%, AO			1.5	2.5	3.8	1	5	
$\overline{B}$-port input pulse rejection							1		ns

output-voltage characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OHP}	Peak output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1		3	V
V_{OHV}	Minimum output voltage during turnoff of 100 mA into 40 nH	$\overline{B}$ port	See Figure 1	1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch	$\overline{B}$ port	I_{OL} = –50 mA	0.3		V

PARAMETER MEASUREMENT INFORMATION

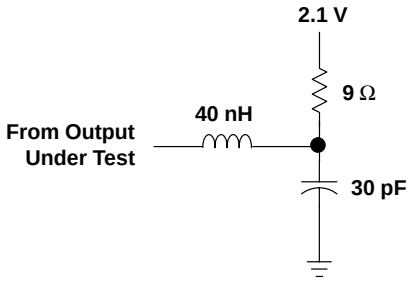
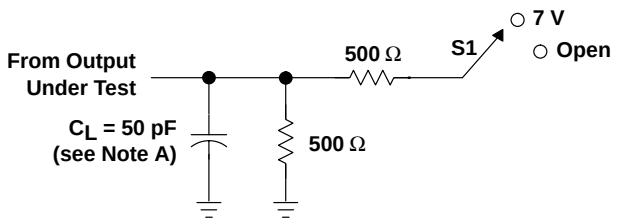
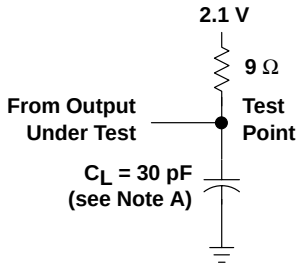


Figure 1. Load Circuit for V_{OHP} and V_{OHV}

PARAMETER MEASUREMENT INFORMATION

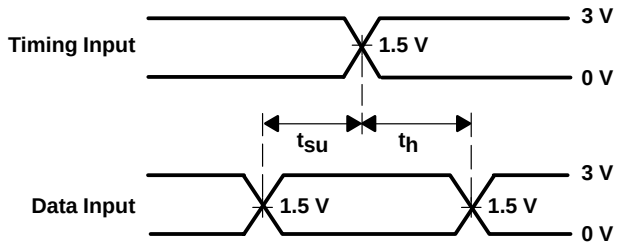


LOAD CIRCUIT FOR A OUTPUTS

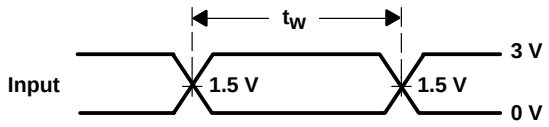


LOAD CIRCUIT FOR B OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



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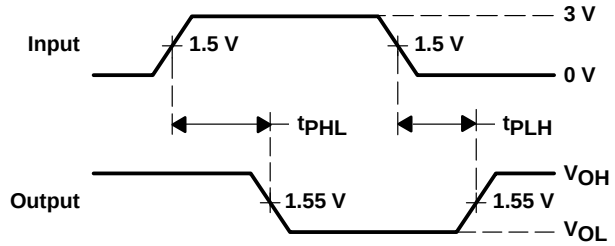
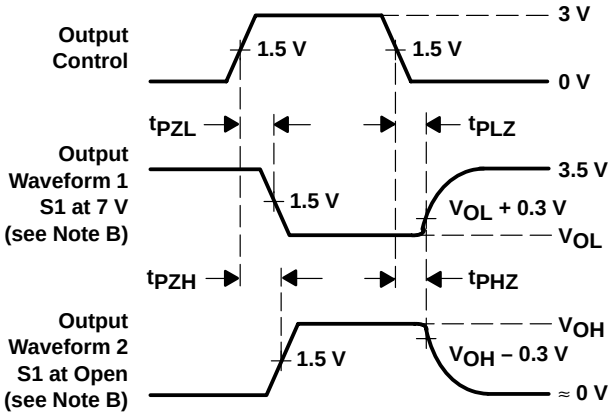
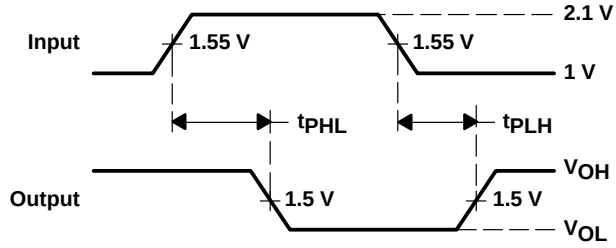
PULSE DURATION



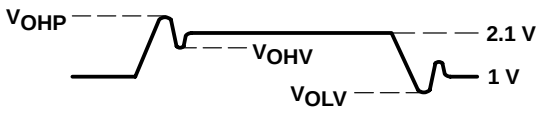
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



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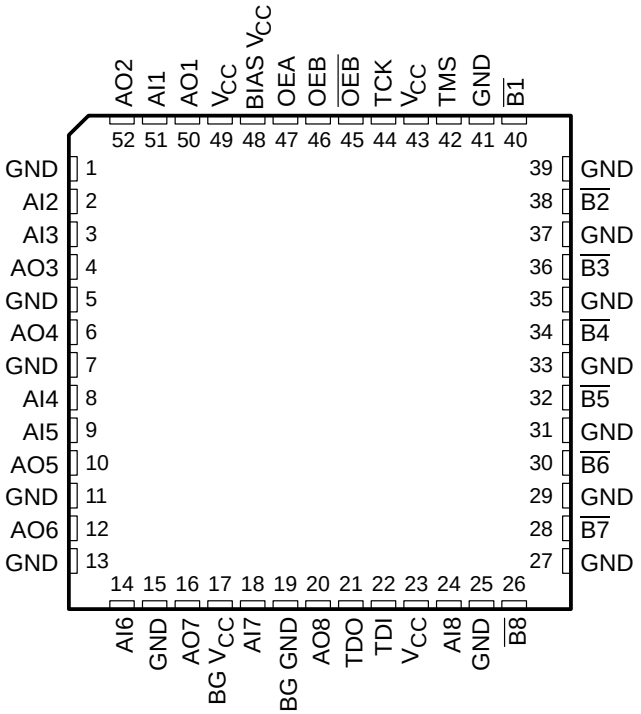
- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **High-Impedance State During Power Up and Power Down**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2040 is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The $\overline{B}$ port operates at BTL-signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off.

The A port operates at TTL-signal levels and has separate input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus, although currently there are no plans to release a JTAG-featured version. TMS and TCK are not connected, and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

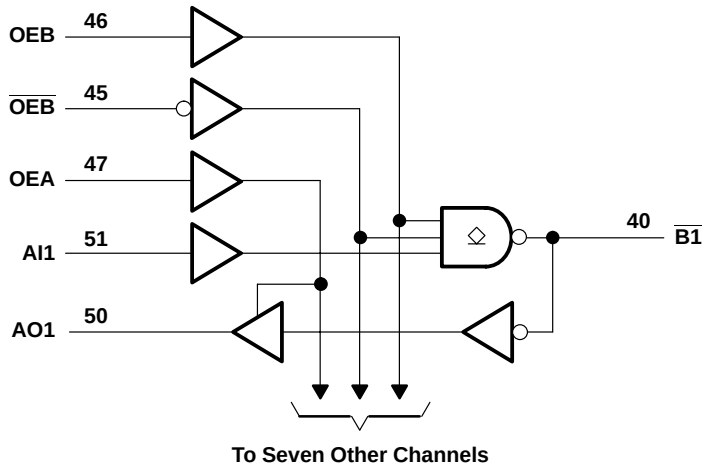
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2040RC	FB2040

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	A port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	A port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	–30		–180	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0		40		mA
	$\overline{B}$ port to AO port				70		
C_i	AI port	V_I = V_{CC} or GND			3.5		pF
	Control inputs				3		
C_o	AO port	V_O = V_{CC} or GND			6		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.5 V				5	pF
		V_{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

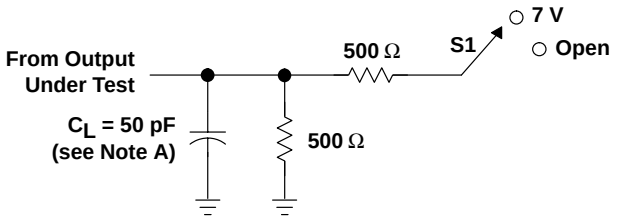
live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 to 5.5 V,	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

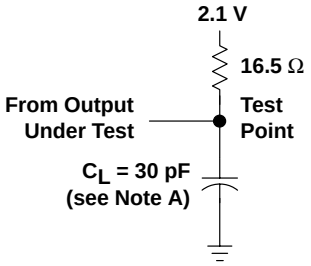
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	$\overline{B}$	3.2	4.5	6	2.4	6.5	ns
t_{PHL}			2.8	4.2	5.6	2.7	5.8	
t_{PLH}	$\overline{B}$	AO	2.3	3.8	5.7	1.9	6.2	ns
t_{PHL}			2.3	4.2	5.9	2	8.2	
t_{PLH}	OEB	$\overline{B}$	3.7	5.1	6.7	3	7	ns
t_{PHL}			3.1	4.6	5.9	3	6.1	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	3.6	5.2	6.8	3.3	7	ns
t_{PHL}			2.9	4.4	5.9	2.6	6.1	
t_{PZH}	OEA	AO	2.5	4	5.5	2.1	5.8	ns
t_{PZL}			2.1	3.6	4.8	2	5	
t_{PHZ}	OEA	AO	2.3	4.1	5.9	1.9	6.5	ns
t_{PLZ}			1.6	3.1	4.5	1.4	4.7	
$t_{sk(p)}$	Skew for any single channel $\lvert t_{PHL} - t_{PLH} \rvert$, AI to $\overline{B}$ or $\overline{B}$ to AO			0.5				ns
$t_{sk(o)}$	Skew between drivers in the same package, AI to $\overline{B}$ or $\overline{B}$ to AO			0.4				ns
t_r	Rise time, 1.3 V to 1.8 V, $\overline{B}$ port		2	2.8	3.8	1.7		ns
t_f	Fall time, 1.8 V to 1.3 V, $\overline{B}$ port		1	1.9	3	1	4.2	ns
$t_{(pr)}$	$\overline{B}$-port input pulse rejection					1	3.4	ns

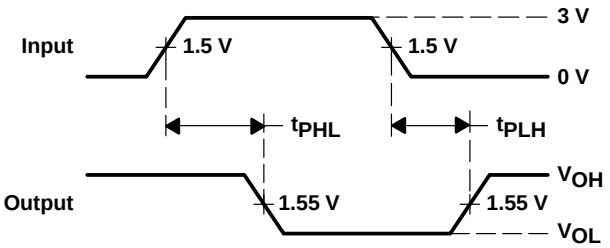
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR A OUTPUTS

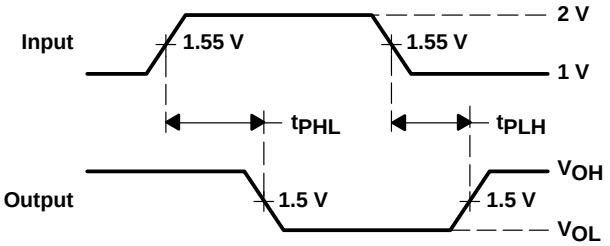


LOAD CIRCUIT FOR B OUTPUTS

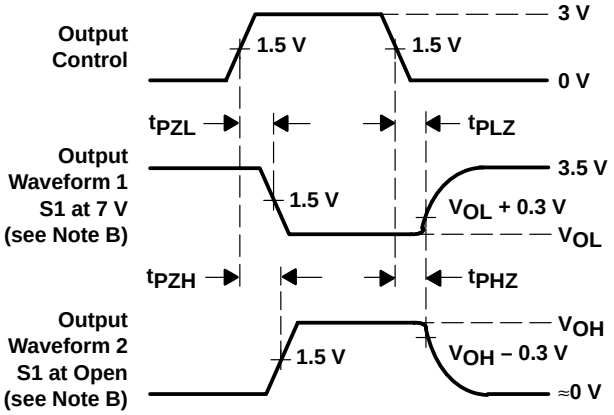


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



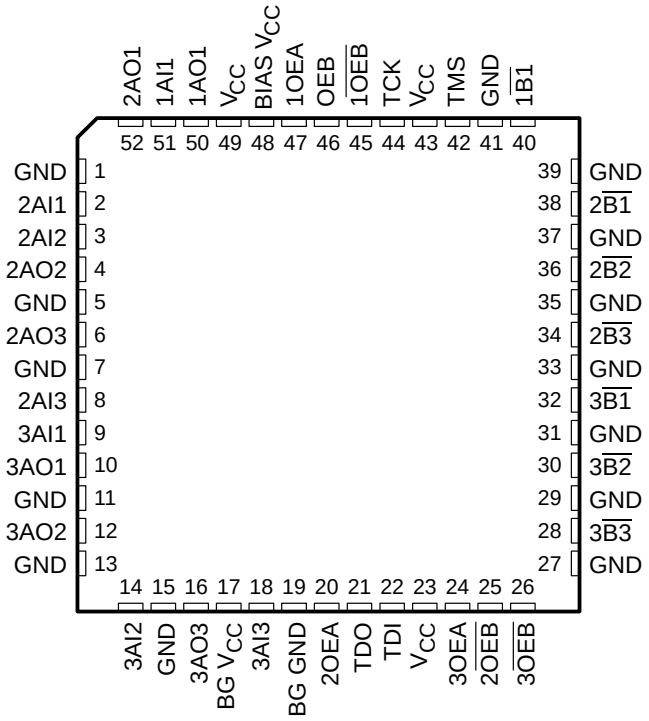
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) $\overline{B}$ Port**
- **Open-Collector $\overline{B}$-Port Outputs Sink 100 mA**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\overline{B}$-Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping to Aid in Line Termination**

RC PACKAGE
(TOP VIEW)



description

The SN74FB2041A is a 7-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments. The device is specifically designed to be compatible with IEEE Std 1194.1-1991.

The $\overline{B}$ port operates at BTL signal levels. The open-collector $\overline{B}$ ports are specified to sink 100 mA. Two output enables (OEB and $\overline{OEB}$) are provided for the $\overline{B}$ outputs. When OEB is high and $\overline{OEB}$ is low, the $\overline{B}$ port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, $\overline{OEB}$ is high, or V_{CC} is less than 2.1 V, the $\overline{B}$ port is turned off. The enable/disable logic partitions the device as two 3-bit sections and one 1-bit section.

The A port operates at TTL signal levels and has split input and output pins. The A outputs reflect the inverse of the data at the $\overline{B}$ port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

description (continued)

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus, although currently there are no plans to release a JTAG-featured version. TMS and TCK are not connected and TDI is shorted to TDO.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

ORDERING INFORMATION

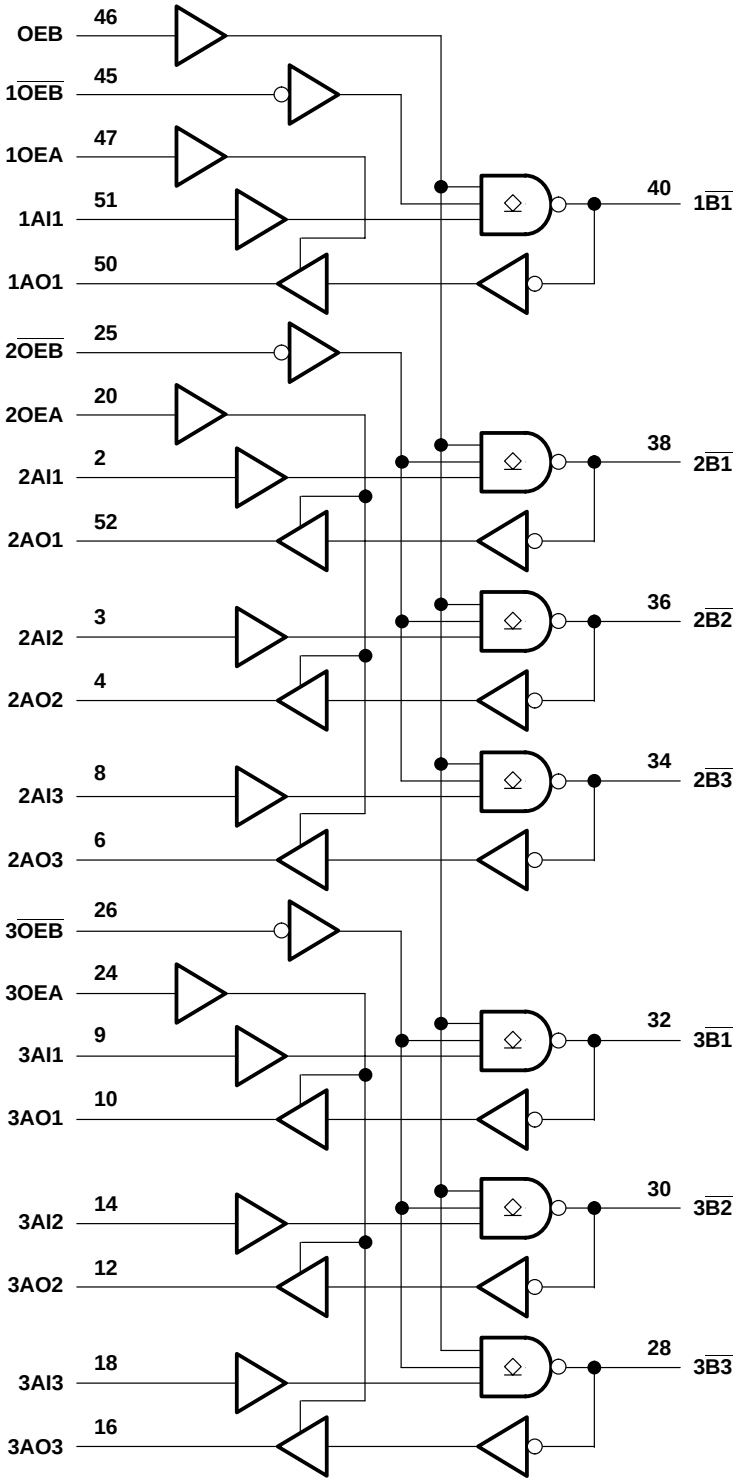
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFP – RC	Tube	SN74FB2041ARC	FB2041A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			FUNCTION
OEB	$\overline{OEB}$	OEA	
L	X	L	Isolation
X	H	L	
L	X	H	$\overline{B}$ data to AO bus
X	H	H	
H	L	L	$\overline{AI}$ data to B bus
H	L	H	$\overline{AI}$ data to B bus, $\overline{B}$ data to AO bus

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except $\overline{B}$ port . . . . . –1.2 V to 7 V
$\overline{B}$ port . . . . . –1.2 V to 3.5 V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, V_O . . . . . –0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O: A port . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK}: Except $\overline{B}$ port . . . . . –40 mA
$\overline{B}$ port . . . . . –18 mA
Current applied to any single output in the low state, I_O: A port . . . . . 48 mA
$\overline{B}$ port . . . . . 200 mA
Package thermal impedance, θ_{JA} (see Note 1) . . . . . 44°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}, BG V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{B}$ port	1.62		2.3	V
		Except $\overline{B}$ port	2			
V_{IL}	Low-level input voltage	$\overline{B}$ port	0.75		1.47	V
		Except $\overline{B}$ port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	AO port			–3	mA
I_{OL}	Low-level output current	AO port			24	mA
		$\overline{B}$ port			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to V_{CC}(5 V) or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
	Except $\overline{B}$ port	V_{CC} = 4.5 V,	I_I = –40 mA			–0.5	
V_{OH}	AO port	V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5	3.3		V
V_{OL}	AO port	V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
	$\overline{B}$ port	V_{CC} = 4.5 V	I_{OL} = 80 mA	0.75		1.1	
			I_{OL} = 100 mA			1.15	
I_I	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 5.5 V			50	µA
I_{IH}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 2.7 V			50	µA
I_{IL}‡	Except $\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.5 V			–50	µA
	$\overline{B}$ port	V_{CC} = 5.5 V,	V_I = 0.75 V			–100	
I_{OH}	$\overline{B}$ port	V_{CC} = 0 to 5.5 V,	V_O = 2.1 V			100	µA
I_{OZH}	AO port	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	AO port	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OZPU}	AO port	V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V			50	µA
I_{OZPD}	AO port	V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V			–50	µA
I_{OS}§	AO port	V_{CC} = 5.5 V,	V_O = 0	–30		–180	mA
I_{CC}	AI port to $\overline{B}$ port	V_{CC} = 5.5 V,	I_O = 0			45	mA
	$\overline{B}$ port to AO port					65	
C_i	AI port	V_I = 0.5 V or 2.5 V			3		pF
	Control inputs				3		
C_o	AO port	V_O = 0.5 V or 2.5 V			5.5		pF
C_{io}	$\overline{B}$ port per IEEE Std 1194.1-1991	V_{CC} = 0 to 4.5 V				5	pF
		V_{CC} = 4.5 V to 5.5 V				5	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

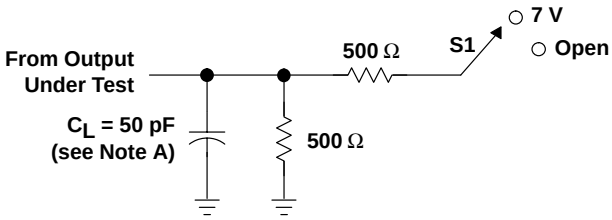
PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 4.5 V	V_B = 0 to 2 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V		450	µA
		V_{CC} = 4.5 V to 5.5 V				10	
V_O	$\overline{B}$ port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 5 V		1.62	2.1	V
I_O	$\overline{B}$ port	V_{CC} = 0,	V_B = 1 V,	V_I (BIAS V_{CC}) = 4.5 V to 5.5 V	–1		µA
		V_{CC} = 0 to 5.5 V,	OEB = 0 to 0.8 V			100	
		V_{CC} = 0 to 2.2 V,	OEB = 0 to 5 V			100	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

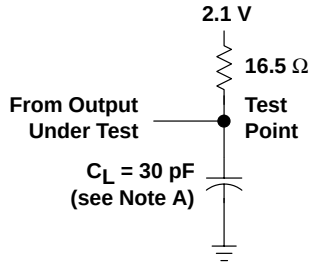
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	AI	$\overline{B}$	2.3	3.9	5.1	2	5.6	ns
t_{PHL}			2.6	4.1	5	2.5	5.3	
t_{PLH}	$\overline{B}$	AO	2	3.6	4.8	1.7	5.3	ns
t_{PHL}			2.3	3.8	4.9	2	6.4	
t_{PLH}	OEB	$\overline{B}$	3	4.6	5.8	2.6	6.3	ns
t_{PHL}			3.1	4.7	6	3.1	6.2	
t_{PLH}	$\overline{OEB}$	$\overline{B}$	2.7	4.3	5.6	2.6	5.8	ns
t_{PHL}			2.7	4.2	5.3	2.5	6.4	
t_{PZH}	OEA	AO	1.5	3.2	5.2	1.5	5.2	ns
t_{PZL}			1.1	2.8	5	1	5	
t_{PHZ}	OEA	AO	1	2.4	3.9	1	4.2	ns
t_{PLZ}			2.2	3.8	5.6	1.7	5.8	
$t_{sk(p)}$†	Pulse skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.5				ns
$t_{sk(o)}$†	Output skew, AI to $\overline{B}$ or $\overline{B}$ to AO			0.4				ns
t_t	Rise time, 1.3 V to 1.8 V, $\overline{B}$ outputs		1	1.6	2.4	1	2.5	ns
	Fall time, 1.8 V to 1.3 V, $\overline{B}$ outputs		1	1.4	2.3	1	2.4	
$t_{(pr)}$	$\overline{B}$-port input pulse rejection		1			1		ns

† Skew values are applicable for through mode only.

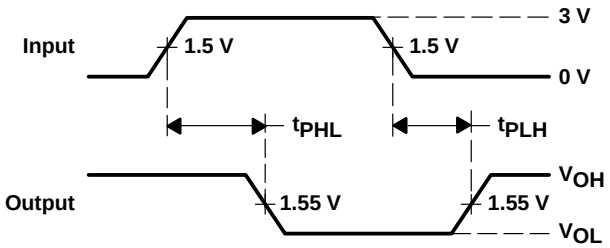
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR A OUTPUTS

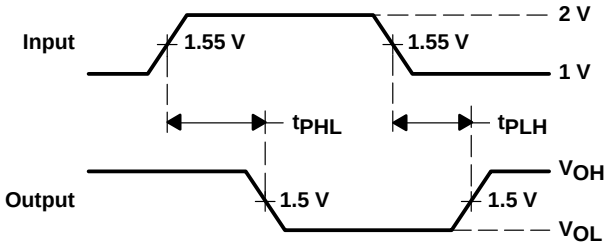


LOAD CIRCUIT FOR B OUTPUTS

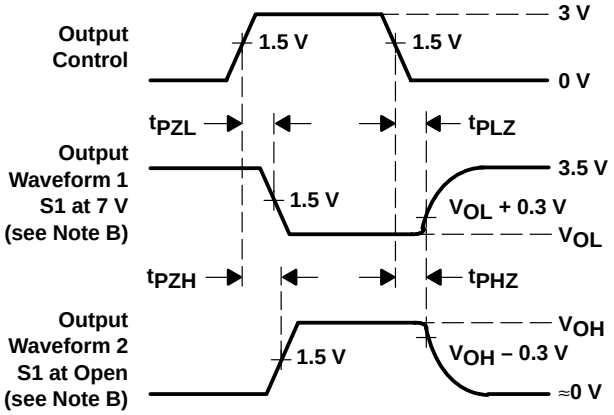


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)

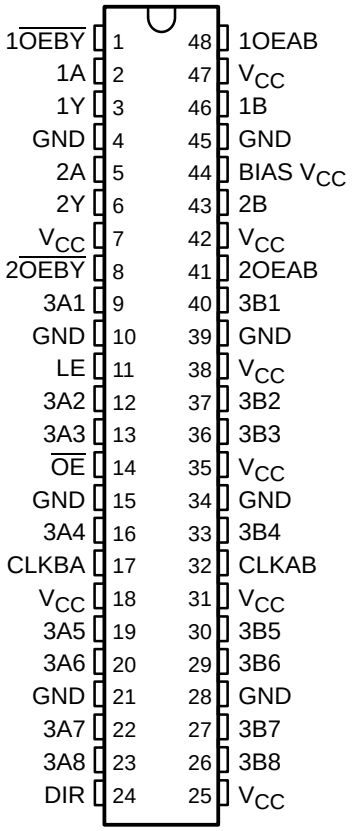
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: TTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns; BTL inputs: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Contents

- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference (EMI)**
- **Compliant With 2eVME and 2eSST Protocol**
- **Bidirectional Interface Between ETL and LVTTL Logic Levels**
- **Bus Transceiver Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring**
- **ETL and LVTTL Interfaces Are 5-V Tolerant**
- **Very Low Ground Bounce**
- **ETL Outputs (–48 mA/48 mA)**
- **LVTTL Outputs (–12 mA/12 mA)**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on 3A-Port Data Inputs**
- **26-Ω Equivalent Series Resistor on 3A Ports and Y Outputs**
- **Flow-Through Architecture Facilitates Printed Circuit Board Layout**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

DGG OR DGV PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

This 8-bit universal bus transceiver has two integral 1-bit three-wire bus transceivers and is designed for 3.3-V V_{CC} operation with 5-V tolerant inputs. The SN74VMEH22501 provides true LVTTL-to-ETL and ETL-to-LVTTL signal-level translation. The UBT™ transceiver allows transparent, latched, and flip-flop modes of data transfer, and the separate LVTTL input and outputs on the bus transceivers provide a feedback path for control and diagnostics monitoring. This device provides a high-speed interface between cards operating at LVTTL logic levels and VME64x or VME320† backplanes operating at ETL signal levels.

High-speed backplane operation is a direct result of the improved OEC™ circuitry and high drive that has been designed and tested into the VME64x backplane model. The ETL outputs are optimized for driving large capacitive loads and include modified input level (V_{IH}/V_{IL}) for increased noise immunity and reduced input skew. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and possibly 1-Gbyte transfer rates on the VME320 backplane.

† VME320 is a patented backplane construction by Arizona Digital, Inc.

PRODUCT PREVIEW

description (continued)

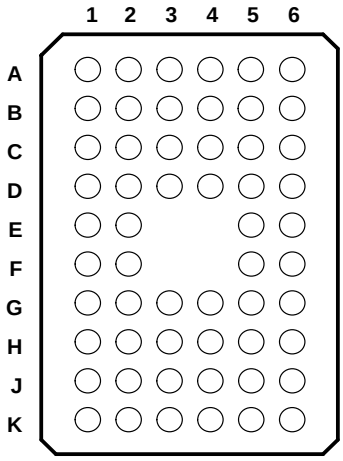
The B port operates at ETL levels, while the 1A and 2A inputs, 1Y and 2Y outputs, 3A port, and control inputs operate at LVTTL logic levels. All are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry prevents damaging current to backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the ETL B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable ($\overline{OE}$ and $\overline{OEBY}$) inputs should be tied to V_{CC} through a pullup resistor and output-enable (OEAB) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

GQL PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1$\overline{OEBY}$	NC	NC	NC	NC	1OEAB
B	1Y	1A	GND	GND	V_{CC}	1B
C	2Y	2A	V_{CC}	V_{CC}	BIAS V_{CC}	2B
D	3A1	2$\overline{OEBY}$	GND	GND	2OEAB	3B1
E	3A2	LE			V_{CC}	3B2
F	3A3	$\overline{OE}$			V_{CC}	3B3
G	3A4	CLKBA	GND	GND	CLKAB	3B4
H	3A5	3A6	V_{CC}	V_{CC}	3B6	3B5
J	3A7	3A8	GND	GND	3B8	3B7
K	DIR	NC	NC	NC	NC	V_{CC}

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	TSSOP – DGG	Tape and reel	SN74VMEH22501DGGR	
	TVSOP – DGV	Tape and reel	SN74VMEH22501DGVR	
	VFBGA – GQL	Tape and reel	SN74VMEH22501GQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74VMEH22501 is a high-drive (±48 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true. The device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

functional description for two 1-bit bus transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The $\overline{\text{OEBY}}$ input controls the 1Y or 2Y outputs. When $\overline{\text{OEBY}}$ is low, the Y outputs are active. When $\overline{\text{OEBY}}$ is high, the Y outputs are disabled.

The $\overline{\text{OEBY}}$ and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

1-BIT BUS TRANSCEIVER FUNCTION TABLE

INPUTS		OUTPUT	MODE
OEAB	$\overline{\text{OEBY}}$		
L	H	Z	Isolation
H	H	A data to B bus	True driver
L	L	B data to Y bus	
H	L	A data to B bus, B data to Y bus	True driver with feedback path

PRODUCT PREVIEW

functional description for 8-bit UBT transceiver

The 3A and 3B data flow in each direction is controlled by the $\overline{OE}$ and direction-control (DIR) inputs. When $\overline{OE}$ is low, all 3A- or 3B-port outputs are active. When $\overline{OE}$ is high, all 3A- or 3B-port outputs are in the high-impedance state.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	DIR	
H	X	Z
L	H	3A data to 3B bus
L	L	3B data to 3A bus

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.

UBT TRANSCEIVER FUNCTION TABLE†

INPUTS				OUTPUT 3B	MODE
$\overline{OE}$	LE	CLKAB	3A		
H	X	X	X	Z	Isolation
L	L	H	X	B_0‡	Latched storage of 3A data
L	L	L	X	B_0§	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of 3A data
L	L	↑	H	H	

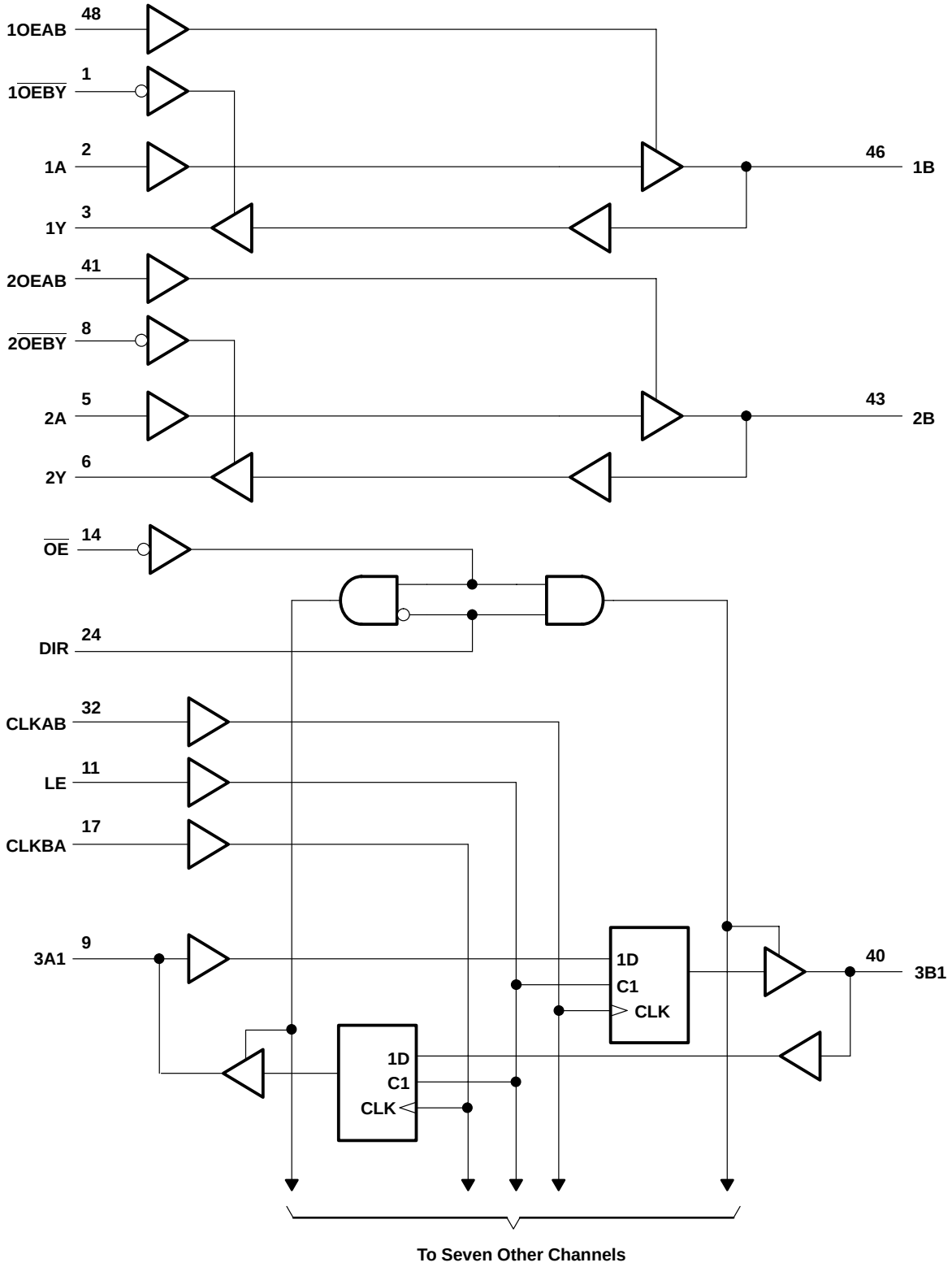
† 3A-to-3B data flow is shown; 3B-to-3A flow is similar, but uses CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low
§ Output level before the indicated steady-state input conditions were established

The UBT transceiver can replace any of the functions shown in Table 1.

Table 1. SN74VMEH22501 UBT Transceiver Replacement Functions

FUNCTION	8 BIT
Transceiver	’245, ’623, ’645
Buffer/driver	’241, ’244, ’541
Latched transceiver	’543
Latch	’373, ’573
Registered transceiver	’646, ’652
Flip-flop	’374, ’574
SN74VMEH22501 UBT transceiver replaces all above functions	

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1): 3A port or Y output . . . . . –0.5 V to V_{CC} + 0.5 V
B port . . . . . –0.5 V to 4.6 V
Output current in the low state, I_O: 3A port or Y output . . . . . 50 mA
B port . . . . . 100 mA
Output current in the high state, I_O: 3A port or Y output . . . . . –50 mA
B port . . . . . –100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}): B port . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
GQL package . . . . . 42°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 3 and 4)

			MIN	TYP	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_I	Input voltage	Control inputs or A port		V_{CC}	5.5	V
		B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	Control inputs or A port	2			V
		B port	0.5 V_{CC} + 50 mV			
V_{IL}	Low-level input voltage	Control inputs or A port			0.8	V
		B port			0.5 V_{CC} – 50 mV	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	3A port and Y output			–12	mA
		B port			–48	
I_{OL}	Low-level output current	3A port and Y output			12	mA
		B port			48	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		0		85	°C

NOTES: 3. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.

electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
	3A port and Y outputs	V_{CC} = 3.15 V	I_{OH} = –6 mA	2.4			
			I_{OH} = –12 mA	2			
	Any B port	V_{CC} = 3.15 V	I_{OH} = –24 mA	2.4			
			I_{OH} = –48 mA	2			
V_{OL}	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
	3A port, any B ports, and Y outputs	V_{CC} = 3.15 V	I_{OL} = 6 mA			0.55	
			I_{OL} = 12 mA			0.8	
	Any B port	V_{CC} = 3.15 V	I_{OL} = 24 mA			0.4	
			I_{OL} = 48 mA			0.55	
I_I	Control inputs, 1A and 2A	V_{CC} = 3.45 V,	V_I = V_{CC} or GND			±1	µA
		V_{CC} = 0 or 3.45 V,	V_I = 5.5 V			10	
	3A port and any B port	V_{CC} = 0 to 3.45 V,	V_I = 5.5 V			10	
		V_{CC} = 3.45 V	V_I = V_{CC}			1	
			V_I = 0			–5	
I_{OZH}‡	A port	V_{CC} = 3.45 V,	V_O = V_{CC}			10	µA
	B port	V_{CC} = 3.45 V,	V_O = V_{CC}			5	
I_{OZL}‡	A port	V_{CC} = 3.45 V,	V_O = GND			–10	µA
	B port	V_{CC} = 3.45 V,	V_O = GND			–5	
I_{OZ}	3A port and any B port§	V_{CC} = 3.45 V	V_I = 0 to V_{CC}			10	µA
			V_I = 5.5 V			5	
	Y output		V_I = 0 to V_{CC}			–10	
			V_I = 5.5 V			–5	
I_{off}		V_{CC} = 0, BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V			±100	µA
I_{BHL}¶	3A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}#	3A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}‖	3A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}☆	3A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
$I_{OZ(PU/PD)}$□		V_{CC} ≤ 1.5 V, V_O = 0.5 V to V_{CC}, V_I = GND or V_{CC}, $\overline{OE}$ = don't care				±100	µA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This parameter includes input leakage current.
¶ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.
# The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC}, then lowering it to V_{IH} min.
‖ An external driver must source at least I_{BHLO} to switch this node from low to high.
☆ An external driver must sink at least I_{BHHO} to switch this node from high to low.
□ High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range for A and B ports (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{CC}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			30	mA
			Outputs low			30	
			Outputs disabled			30	
I_{CCD}		V_{CC} = 3.45 V, I_O = 0, V_I = V_{CC} or GND, One data input switching at half clock frequency, 50% duty cycle	Outputs enabled				mA
			Outputs disabled				
ΔI_{CC}◊		V_{CC} = 3.15 V to 3.45 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				750	µA
C_i	1A and 2A inputs	V_I = 3.15 V or 0					pF
	Control inputs						
C_o	1Y or 2Y outputs	V_O = 3.15 V or 0					pF
C_{io}	3A port	V_{CC} = 3.3 V,	V_O = 3.3 V or 0				pF
	Any B port						

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
◊ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

live-insertion specifications over recommended operating free-air temperature range for B port

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V,	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			5	mA
	V_{CC} = 3.15 V to 3.45 V‡,	BIAS V_{CC} = 3.15 V to 3.45 V,	$I_{O(DC)}$ = 0			10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V		1.3	1.5	1.7	V
I_O	V_{CC} = 0	V_O = 0,	BIAS V_{CC} = 3.15 V	–20		–100	µA
		V_O = 3 V,	BIAS V_{CC} = 3.15 V	20		100	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ V_{CC} – 0.5 V < BIAS V_{CC}

timing requirements over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

				MIN	MAX	UNIT
f_{clock}	Clock frequency					MHz
t_w	Pulse duration	LE high				ns
		CLK high or low				
t_{su}	Setup time	3A before CLK↑	Data high			ns
			Data low			
		3A before LE↓	CLK high			
			CLK low			
		3B before CLK↑	Data high			
			Data low			
		3B before LE↓	CLK high			
			CLK low			
t_h	Hold time	3A after CLK↑	Data high			ns
			Data low			
		3A after LE↓	CLK high			
			CLK low			
		3B after CLK↑	Data high			
			Data low			
		3B after LE↓	CLK high			
			CLK low			

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B				ns
t_{PHL}						
t_{PLH}	1A or 2A	1Y or 2Y				ns
t_{PHL}						
t_{PZH}	OEAB	1B or 2B				ns
t_{PZL}						
t_{PHZ}	OEAB	1B or 2B				ns
t_{PLZ}						
t_r	Transition time, B port (10%–90%)					ns
t_f	Transition time, B port (90%–10%)					ns
t_{PLH}	1B of 2B	1Y or 2Y				ns
t_{PHL}						
t_{PZH}	$\overline{OEBY}$	1Y or 2Y				ns
t_{PZL}						
t_{PHZ}	$\overline{OEBY}$	1Y or 2Y				ns
t_{PLZ}						

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switching characteristics over recommended operating conditions for UBT transceiver (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}						MHz
t_{PLH}	3A	3B				ns
t_{PHL}						
t_{PLH}	LE	3B				ns
t_{PHL}						
t_{PLH}	CLKAB	3B				ns
t_{PHL}						
t_{PZH}	$\overline{OE}$	3B				ns
t_{PZL}						
t_{PHZ}	$\overline{OE}$	3B				ns
t_{PLZ}						
t_r	Transition time, B port (10%–90%)					ns
t_f	Transition time, B port (90%–10%)					ns
t_{PLH}	3B	3A				ns
t_{PHL}						
t_{PLH}	LE	3A				ns
t_{PHL}						
t_{PLH}	CLKBA	3A				ns
t_{PHL}						
t_{PZH}	$\overline{OE}$	3A				ns
t_{PZL}						
t_{PHZ}	$\overline{OE}$	3A				ns
t_{PLZ}						

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B				ns
$t_{sk(HL)}$						
$t_{sk(LH)}$	1B or 2B	1Y or 2Y				ns
$t_{sk(HL)}$						
$t_{sk(t)}$‡	1A or 2A	1B or 2B				ns
	1B or 2B	1Y or 2Y				
$t_{sk(pp)}$	1A or 2A	1B or 2B				ns
	1B or 2B	1Y or 2Y				

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

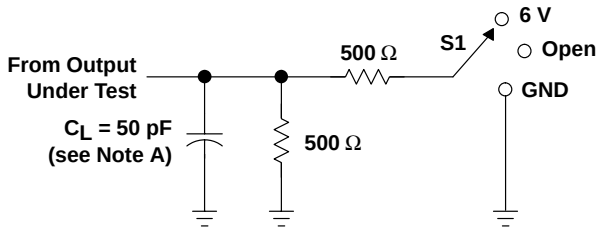
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	3A	3B				ns
$t_{sk(HL)}$						
$t_{sk(LH)}$	CLKAB	3B				ns
$t_{sk(HL)}$						
$t_{sk(LH)}$	3B	3A				ns
$t_{sk(HL)}$						
$t_{sk(LH)}$	CLKBA	3A				ns
$t_{sk(HL)}$						
$t_{sk(t)}$‡	3A	3B				ns
	CLKAB	3B				
	3B	3A				
	CLKBA	3A				
$t_{sk(pp)}$	3A	3B				ns
	CLKAB	3B				
	3B	3A				
	CLKBA	3A				

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

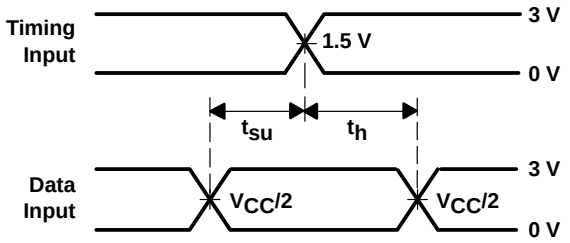
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
A PORT

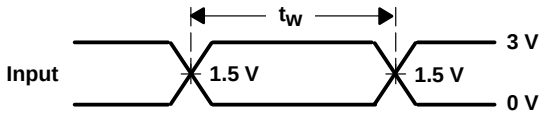


LOAD CIRCUIT

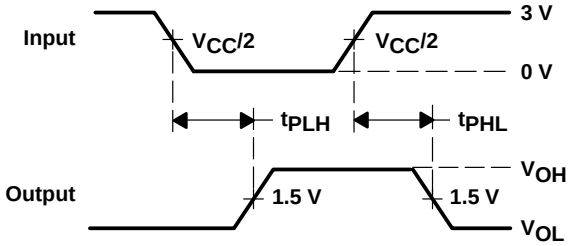
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
B-to-A Skew	Open



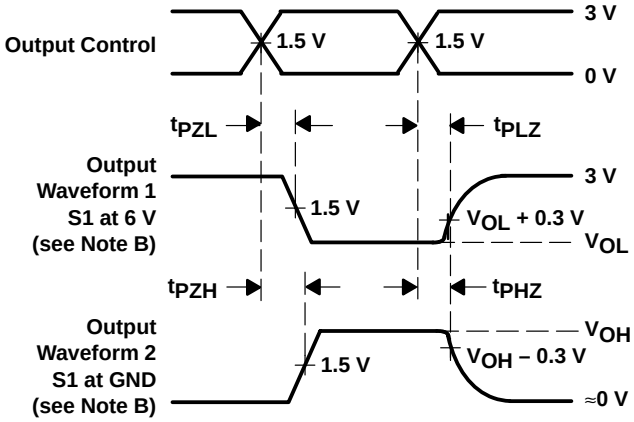
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

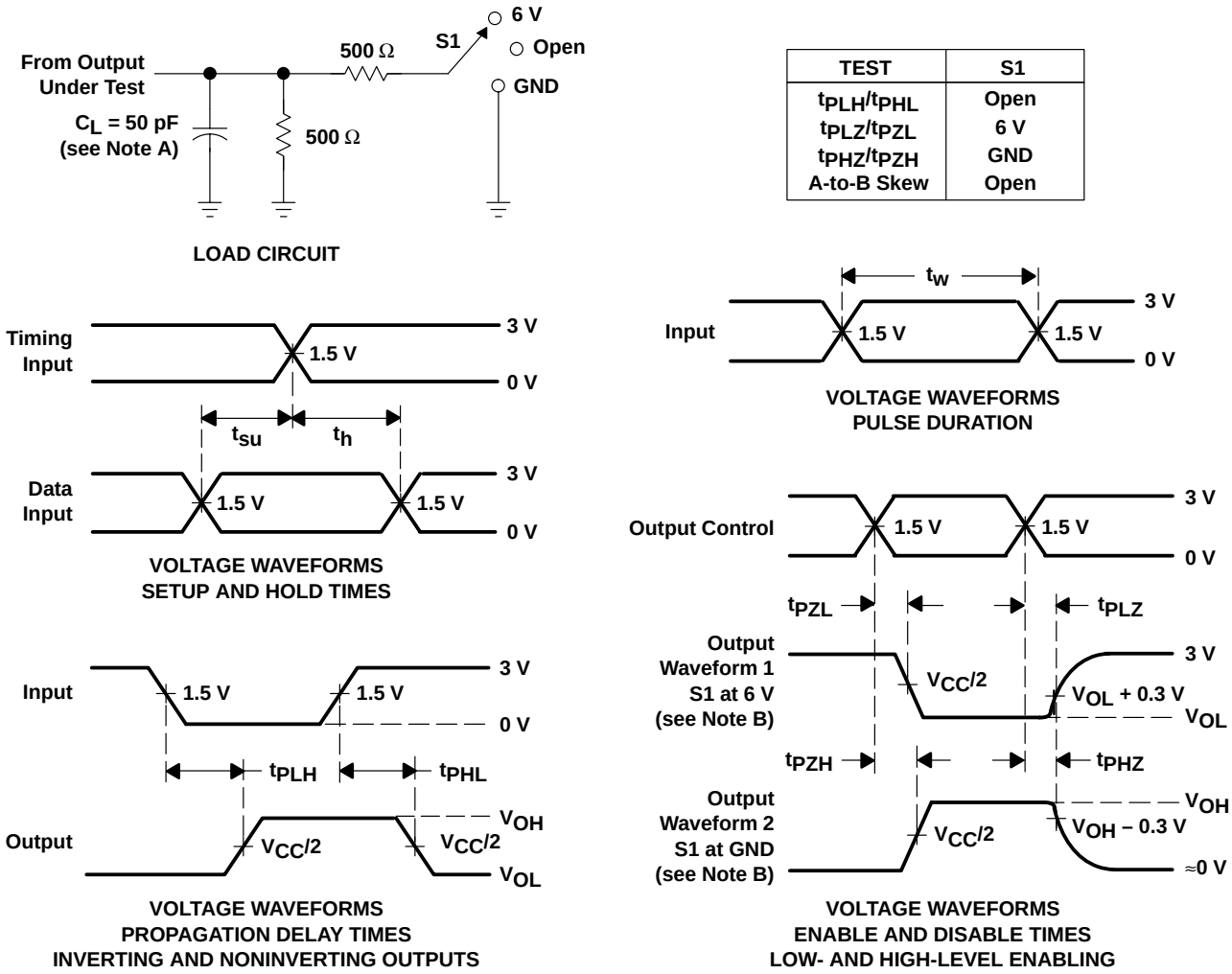


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
B PORT



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
A-to-B Skew	Open

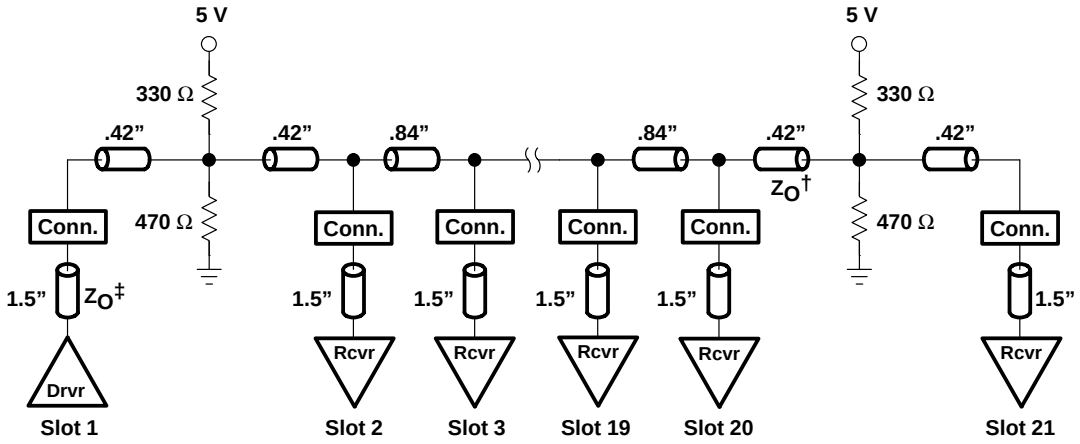
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics tables show the switching characteristics of the device into the lumped load shown in the parameter measurement information (PMI) (see Figures 1 and 2). All logic devices are currently tested into this type of load. However, the designer's backplane application is probably a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 3.



† Unloaded backplane trace natural impedence (Z_O) is 45 Ω. 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.
‡ Card stub natural impedence (Z_O) is 60 Ω.

Figure 3. VME64x Backplane

The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane. See www.ti.com/sc/etl for more information.

driver in slot 11, with receiver cards in all other slots (full load)

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP§	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.9		8.5	ns
t_{PHL}			5.5		8.7	
t_r¶	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t_f¶	Transition time, B port (90%–10%)		8.9	9	10.8	ns

§ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
¶ All t_r and t_f times are taken at the first receiver.

driver in slot 11, with receiver cards in all other slots (full load) (continued)

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	3A	3B	6.2		8.9	ns
t_{PHL}			5.6		9	
t_{PLH}	LE	3B	6.1		9.1	ns
t_{PHL}			5.6		9	
t_{PLH}	CLKAB	3B	6.2		9.1	ns
t_{PHL}			5.7		9	
t_r‡	Transition time, B port (10%–90%)		9	8.6	11.4	ns
t_f‡	Transition time, B port (90%–10%)		8.9	9	10.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			2.5	ns
$t_{sk(HL)}$					3	
$t_{sk(t)}$§	1A or 2A	1B or 2B		0.5	3.4	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B				ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2.4	ns
$t_{sk(HL)}$					3.4	
$t_{sk(LH)}$	CLKAB	3B			2.7	ns
$t_{sk(HL)}$					3.4	
$t_{sk(t)}$§	3A	3B		0.5	3.4	ns
	CLKAB	3B		0.6	3.5	
$t_{sk(pp)}$	3A	3B				ns
	CLKAB	3B				

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

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driver in slot 1, with one receiver in slot 21 (minimum load)

switching characteristics over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	1A or 2A	1B or 2B	5.5		7.4	ns
t_{PHL}			5.3		7.4	
t_r‡	Transition time, B port (10%–90%)		3.9	3.4	4.4	ns
t_f‡	Transition time, B port (90%–10%)		3.7	3.4	4.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

switching characteristics over recommended operating conditions for UBT (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
t_{PLH}	3A	3B	5.8		7.9	ns
t_{PHL}			5.5		7.7	
t_{PLH}	LE	3B	5.9		8	ns
t_{PHL}			5.5		7.8	
t_{PLH}	CLKAB	3B	5.9		8.1	ns
t_{PHL}			5.5		7.7	
t_r‡	Transition time, B port (10%–90%)		3.9	3.4	4.4	ns
t_f‡	Transition time, B port (90%–10%)		3.7	3.4	4.8	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ All t_r and t_f times are taken at the first receiver.

skew characteristics for bus transceiver for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	1A or 2A	1B or 2B			1.7	ns
$t_{sk(HL)}$					2.1	
$t_{sk(t)}$§	1A or 2A	1B or 2B		0.2	2.1	ns
$t_{sk(pp)}$	1A or 2A	1B or 2B				ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
§ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

skew characteristics for UBT for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
$t_{sk(LH)}$	3A	3B			2	ns
$t_{sk(HL)}$					2.3	
$t_{sk(LH)}$	CLKAB	3B			2.1	ns
$t_{sk(HL)}$					2.4	
$t_{sk(t)}$‡	3A	3B		0.2	2.5	ns
	CLKAB	3B		0.2	2.9	
$t_{sk(pp)}$	3A	3B				ns
	CLKAB	3B				

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.
‡ $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

By simulating the performance of the device using the VME64x backplane (see Figure 3), the maximum peak current in or out of the B-port output as the devices switch from one logic state to another was found to be equivalent to driving the lumped load shown in Figure 4.

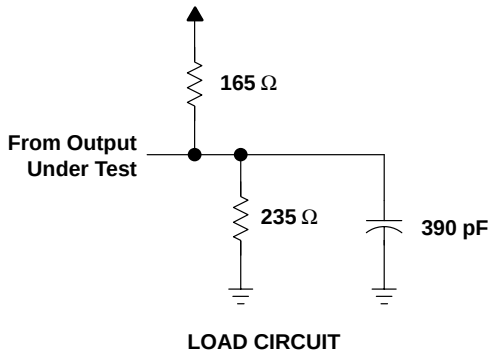

Figure 4. Equivalent AC Peak Output Current Lumped Load

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driver in slot 1, with one receiver in slot 21 (minimum load) (continued)

In general, the rise- and fall-time distribution is shown in Figure 5. Since VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see Figures 1 and 2).

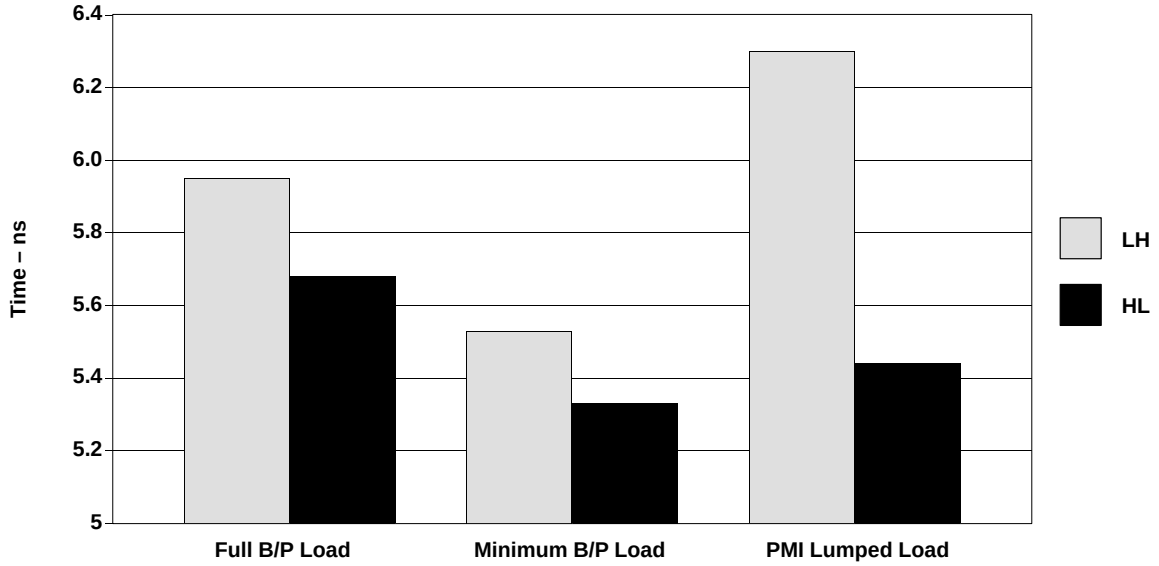

Figure 5

Characterization-laboratory data in Figures 6 and 7 show the absolute ac peak output current with different supply voltages as the devices change output logic state. Strong, nominal, and weak process variations are shown to demonstrate the devices' capability.

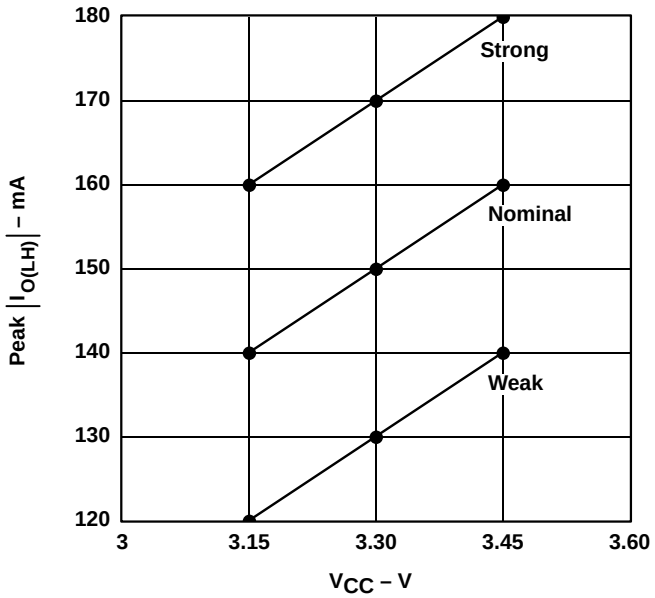

Figure 6

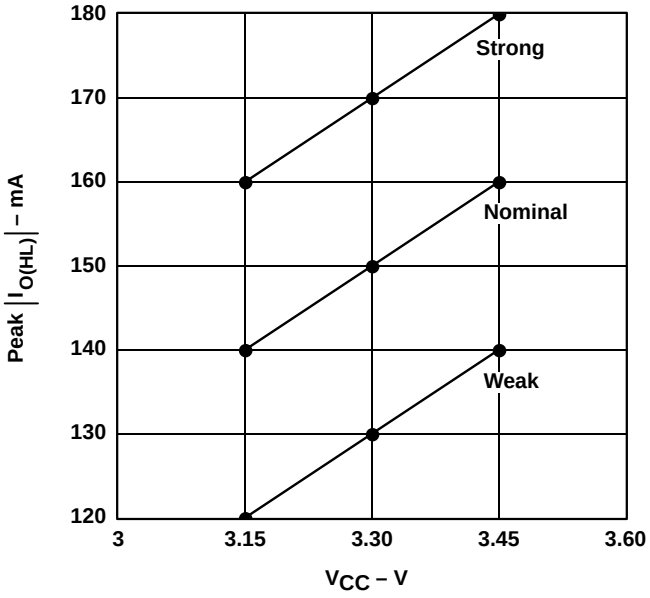

Figure 7

TYPICAL CHARACTERISTICS

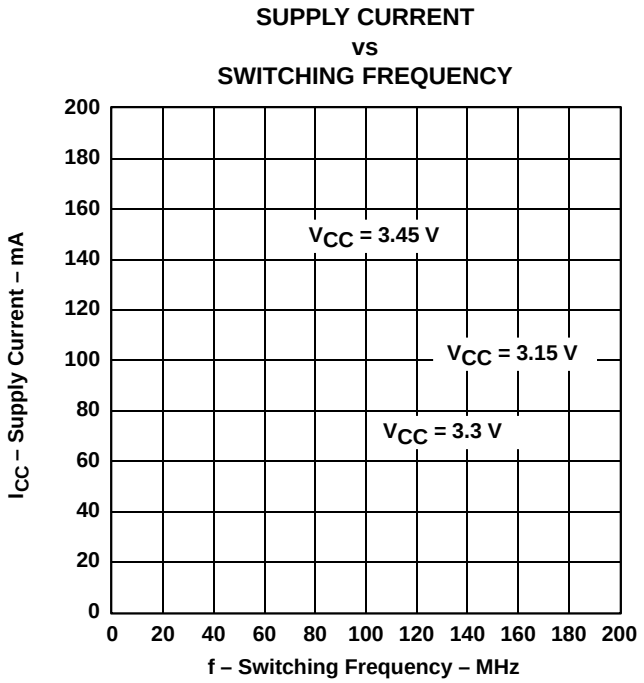

Figure 8

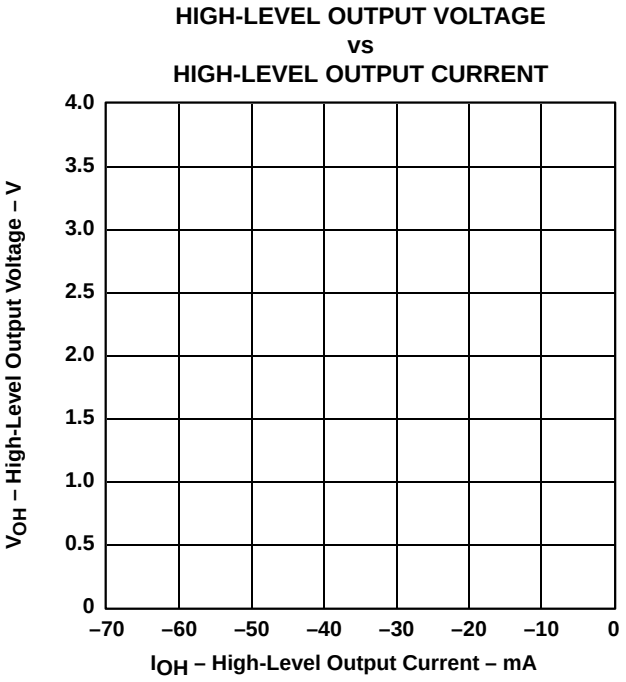

Figure 9

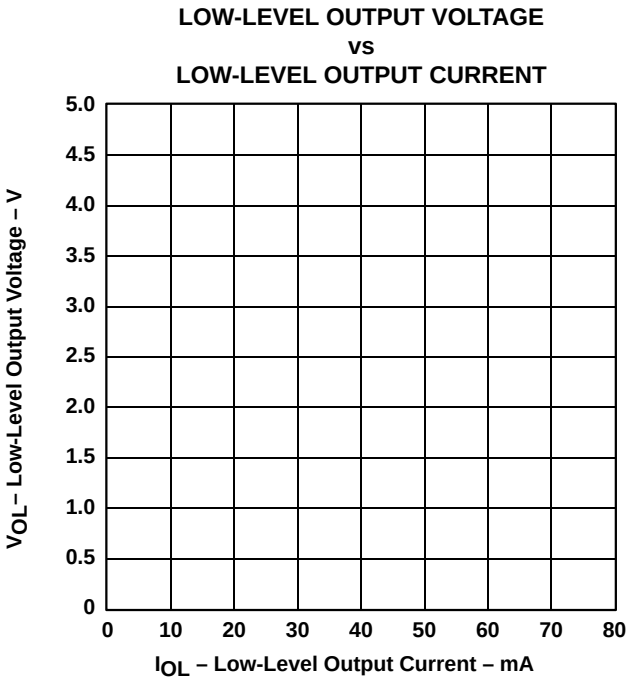

Figure 10

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PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

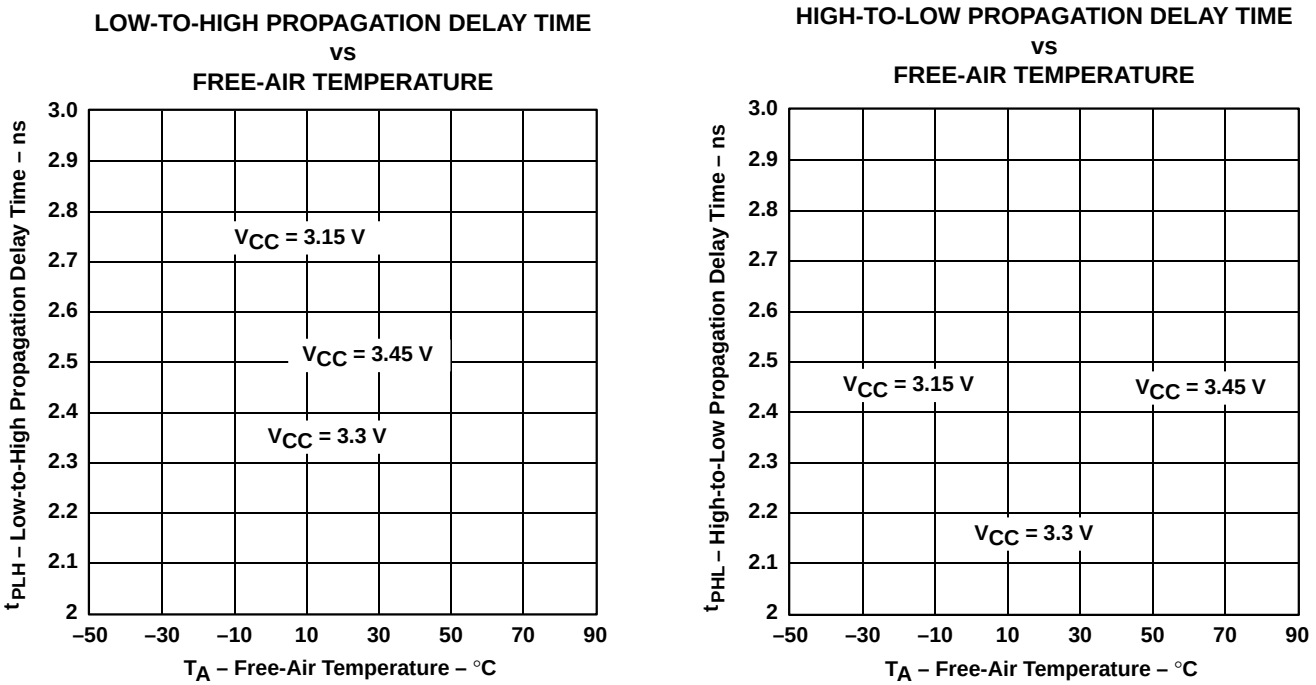

Figure 11. Bus Transceiver Propagation Delay

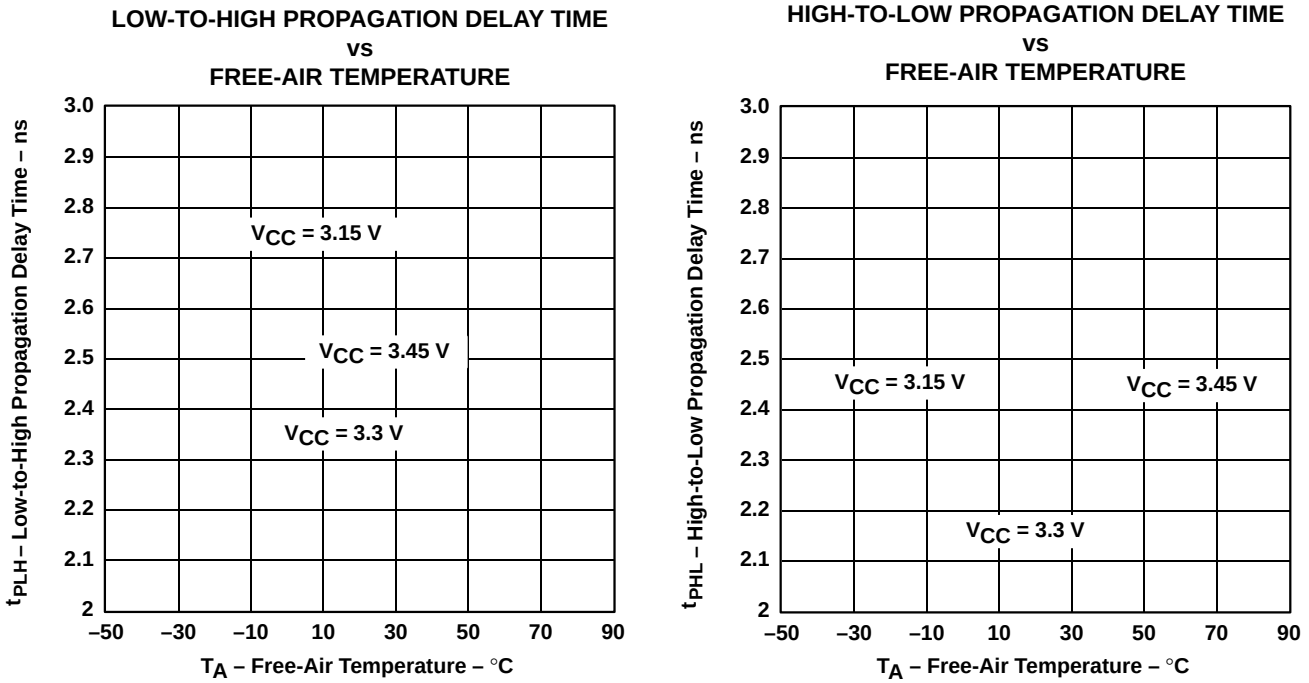

Figure 12. UBT Propagation Delay

VMEbus SUMMARY

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola VERSA bus architecture that owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations: single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbyte/s. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 Mbyte/s, or more. The new specification, VITA 1.5-199X [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgement of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 Gbyte/s, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane.

From BLT to 2eSST –A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com. TI, in conjunction with VITA, is designing the SN74VMEH22501 to support the 2eSST protocol in either the traditional VME64x distributed-capacitance backplane or the new star-configuration VME320 lumped-capacitance backplane.

maximum data transfer rates

DATE	TOPOLOGY	PROTOCOL	DATA BITS PER CYCLE	DATA TRANSFERS PER CLOCK CYCLE	PER SYSTEM (Mbyte/s)	FREQUENCY (MHz)	
						BACKPLANE	CLOCK
1981	VMEbus IEEE-1014	BLT	32	1	40	10	10
1989	VME64	MBLT	64	1	80	10	10
1995	VME64x	2eVME	64	2	160	10	20
1997	VME64x	2eSST	64	2-No Ack	160–320	10–20	20–40
1999	VME320	2eSST	64	2-No Ack	320–1000	20–62.5	40–125

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protocol

The basic single-cycle VMEbus data-transfer protocol is straightforward. The master puts addresses on the bus, delays a minimum of 35 ns, then asserts address strobe (AS*). For a write operation, the master puts data on the bus, delays a minimum of 35 ns, then asserts one or both of its data strobes (D50* and/or DS1*). All slave cards on the bus monitor the addresses. Each slave is set up to decode a unique address. The assertion of AS* tells the slave that the address is valid. In a write cycle, the selected slave must then read data off the bus. The assertion of data strobe tells the slave that data is valid on the bus and can be strobed into memory. The slave then asserts DTACK* to signal that the data has been captured.

The 2eVME protocol uses the same asynchronous protocol as the basic single-cycle protocol, but clocks data across the bus on both the rising and falling edges of the data strobes, thus, gaining a 2× speed up for each cycle. 2eSST, on the other hand, uses a synchronous protocol that clocks data using DS0* for writes and DTACK* for reads. 2eSST increases the speed of the clocks to speed up the data transfers and requires the use of a backplane that ensures monotonic signals, such as provided by the VME320 star-configuration backplane.

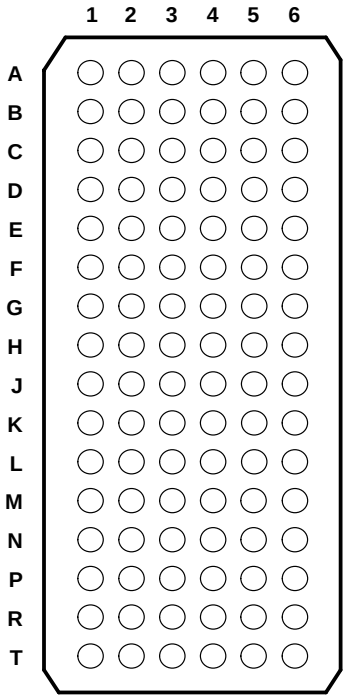
applicability

Target applications for VME backplanes and ETL devices include industrial controls, military, aerospace, transportation, telecommunications, simulation, medical, high-energy physics, office automation, and instrumentation systems.

APPLICATION INFORMATION

The SN74VMEH3222501KR is a two-die solution of the SN74VMEH22501 in the 96-ball LFBGA package (GKER). More information on the LFBGA package can be found at www.ti.com/sc/lfbga.

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Y	1A	1/OEBY	1OEAB	$1V_{CC}$	1B
B	2Y	2A	GND	GND	BIAS V_{CC}	2B
C	3A1	2/OEBY	$1V_{CC}$	$1V_{CC}$	2OEAB	3B1
D	3A2	1LE	GND	GND	$1V_{CC}$	3B2
E	1/OE	3A3	GND	GND	3B3	$1V_{CC}$
F	1CLKBA	3A4	$1V_{CC}$	$1V_{CC}$	3B4	1CLKAB
G	3A6	3A5	GND	GND	3B5	3B6
H	3A7	3A8	1DIR	$1V_{CC}$	3B8	3B7
J	4Y	4A	4/OEBY	4OEAB	$2V_{CC}$	4B
K	5Y	5A	GND	GND	BIAS V_{CC}	5B
L	6A1	5/OEBY	$2V_{CC}$	$2V_{CC}$	5OEAB	6B1
M	6A2	2LE	GND	GND	$2V_{CC}$	6B2
N	2/OE	6A3	GND	GND	6B3	$2V_{CC}$
P	2CLKBA	6A4	$2V_{CC}$	$2V_{CC}$	6B4	2CLKAB
R	6A6	6A5	GND	GND	6B5	6B6
T	6A7	6A8	2DIR	$2V_{CC}$	6B8	6B7

There has been no decision to release the SN74VME3222501KR. For completness of the design-goal data sheet, the pinout has been included. A separate data sheet will be generated if the SN74VMEH3222501KR is released.

PRODUCT PREVIEW

VITA 2.1 SIMULATION PROPOSAL FOR THE SN74VMEH22501

introduction

This document is intended to form the basis of a statement of work for performance of simulation studies on standard VME64x backplanes using VITA 1.5 (draft, 2eSST) protocol.

scope

The scope of this VITA 2.1 simulation effort is to:

- Determine the optimum driver characteristics (rise/fall time, rise/fall time variation, or output current) that will support 2eSST protocol over a maximum number of slots (goal is 21 slots) with the SN74VMEH22501 model and a standard VME64x backplane. This will be performed over worst-case variations in backplane loading, unbalanced signal loading, driving slot, transceiver drive strength, transceiver rise/fall time, and line impedance.
- Verify support of 2eSST protocol over 21 slots with SN74VMEH22501 model and a standard VME64x backplane. This will be performed over worst-case variations in backplane loading, unbalanced signal loading, driving slot, transceiver drive strength, transceiver rise/fall time, and line impedance.

topology

The exact topology and transceiver loading need to be defined. The strawman proposal is that we use:

- Single-line connector models for all slots except driver and monitored receiver slots, and except for the crosstalk simulation, which requires multiline connector models for all slots
- Multiline connector models for all driver and monitored receiver slots
- 0.841-in. backplane traces at 174-ps/in. single-line model, except for crosstalk simulation, which requires multiline coupled transmission-line models for backplane, based on two traces routed between rows of the DIN connector
- 1.5-in. VME board traces at 174 ps/in.
- 1.5 pF for the via on the backplane associated with the press-fit connector hole
- 0.5 pF for the via on the VME board that brings the inner-layer trace to the surface-mount receiver pad
- 0.5 pF for the via on the VME board associated with press-fit connector hole
- TI driver model with adjustable rise/fall time and adjustable drive strength
- TI diode model for the receiver clamp diode
- 8-pF lumped receiver load (total, including the capacitance of diode model). This does not represent worst case of all legacy boards, but is representative of modern designs.
- Drive strength for weak and strong start out using TI-defined values. This must be defined before work can start (defined in the models, action complete).
- TI to define process variation (percentage process variation from minimum to maximum) for high/low drive strength and rise/fall time. This must be defined before work can start (defined in the models, action complete).

simulation matrix

The simulation matrix of the adjustable-transceiver study shows the range of simulations to be carried out. Each case might have a number of different simulation runs, for example, multiple rise times in search of the boundary condition.

For cases 1 and 2 of the adjustable-transceiver study, the weak-driver high and/or low output current is increased, if required, to find a case that works. If this is required, the strong-driver output current is increased, based on TI's defined percentage process variation from minimum to maximum, and these values are used in subsequent cases for the weak and strong models.

All simulations are performed with the five-row DIN connector.

adjustable-transceiver study

CASE	BACKPLANE LOADING	UNBALANCED SIGNAL LOADING	DRIVING SLOT	TRANSCEIVER DRIVE STRENGTH	TRANSCEIVER RISE/FALL TIME	LINE (Ω)	MAX FREQUENCY (MHz)	
							9-15-00	10-10-00
1	All slots	All lines	11	Weak	Find fastest that works 4 ns to 8 ns. If no case works, increase weak driver current until a case works.	45	–	20
2	All slots	All lines	1	Weak	Find fastest that works 4 ns to 8 ns (start at fastest that works above). If no case works, increase weak driver current until a case works.	45	20	20
3	All slots	All lines	1	Strong	Find fastest that works 4 ns to 8 ns (start at fastest that works above)	45	–	20
4	All slots	All lines	11	Strong	Find fastest that works 4 ns to 8 ns (start at fastest that works above)	45	–	20
5	Slots 11 and 12	All lines	11	Strong	Find fastest that works 4 ns to 8 ns (start at fastest that works above)	45	–	20
6	Slots 1 and 21	All lines	1	Strong	Find fastest that works 4 ns to 8 ns (start at fastest that works above)	45	–	20
7	Slots 1, 11, and 17–21	All lines	1	Strong	Find fastest that works 4 ns to 8 ns (start at fastest that works above)	45	20	20

PRODUCT PREVIEW

Contents

Application Report
SCBA015A - March 2001

Fast GTLP Backplanes With the GTLPH1655

Peter Forstner and Johannes Huchzermeier *Standard Linear & Logic*

ABSTRACT

This revision of the *Fast GTL Backplanes With the GTL1655* application report addresses improvements, such as the improved OEC™ circuitry and implementation of the Texas Instruments TI-OPC™ circuitry, that have been incorporated in the GTLPH1655 device. These improvements significantly improve signal integrity in distributed loads.

This application report describes the physical principles of fast bus systems and the problems that can arise in their development. These descriptions are based on line theory, and various specifications of TTL, backplane transceiver logic (BTL), Gunning transceiver logic (GTL), and Gunning transceiver logic plus (GTLP) integrated circuits are compared.

In addition, this application report presents the performance of the SN74GTLPH1655. This new UBT™ device provides an optimum solution for the design of backplanes for future high-speed bus systems.

Comprehensive measurement results of the SN74GTLPH1655 also are included in this application report.

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Introduction

Since the 1970s, bus systems have been used in every microprocessor system. In the early systems, the delay time of the driver was in the range of 15 ns to 20 ns, and the frequency of the system clock was about 1 MHz. The speed of the total system was determined primarily by the delay time of the active electronics, for example, the processor, gates, and bus drivers.

With increasing clock rates, the bus began to limit the performance of the total system. To circumvent this limitation, numerous improvements have been introduced in modern bus systems:

Pipelining	By pipelining, instructions and data are transmitted continually from the memory to the processor.
Cache memory	To avoid having the fast processor continually waiting for the slow main memory (DRAM, EPROM), an intermediate storage of the current data is implemented in a fast cache memory.
Block transfer	The transfer of individual words of data is replaced by the transmission of complete data blocks.
Multimaster	Every device connected to the bus can initiate the transmission of data. The cumbersome and slow route of transferring data exclusively via the CPU is, therefore, no longer necessary.
Bus width	The bus width has grown from 8 bits to 64 bits, and larger.
Clock rate	The clock rate of the backplane has increased into the range of many tens of megahertz, e.g., with a PCI bus to 33 MHz or 66 MHz. The processor itself operates internally at far higher clock rates, e.g., at 400 MHz. The memory is connected by a dedicated bus that operates at very high clock rates, e.g., up to 400 MHz. The memory is connected by a special bus (e.g., the Direct *RAMBUS*™), operating at 800 MHz) to the processor.

The first sections of this application report deal exclusively with general physical principles and conditions. The engineer developing a bus system must be concerned with these to achieve high data rates on the bus.

Circuit solutions based on TTL, BTL, and GTL logic families are compared. Particular attention is devoted to the GTLP transceiver circuit having increased drive capability and support for live insertion.

The SN74GTLPH1655 is presented and examined in detail.

Direct *RAMBUS* is a trademark of Rambus Inc.

Physical Principles

In data sheets, the delay times of driver circuits are commonly given with a load circuit of 50 pF and 500 Ω at the outputs. However, this load circuit does not correspond well to the actual effective loads in current application. Rather, it is intended to match the conditions existing with IC testers. In particular, a load of this kind does not correspond to reality with bus systems. If the connecting line between two components is compared with the relationship on a bus line, significant differences exist.

Does a Line Behave Like a Capacitive Load?

The conditions shown in Figure 1 represent a typical connecting line between two components. If the connecting line is 20 cm long, then there is a very small capacitive load of 12 pF. As shown in Figure 2, modules are connected to a bus line with a 2-cm space between them, and these contribute an additional capacitive loading of 20 pF/2 cm (= 10 pF/cm) (see Table 1). A typical bus line on the backplane wiring of a 19-inch rack having a length of 40 cm, therefore, has a total capacitance of 424 pF (10.6 pF/cm × 40 cm).

The development engineer needs to know the effect of the capacitive load on the signal delay of drivers under the previously mentioned conditions (C_L = 12 pF, or C_L = 424 pF). The delay times given in data sheets assume a load of 50 pF.

However, now the line cannot be considered a capacitive load, but instead must be treated from the point of view of transmission-line theory. With the bus line described previously, a signal delay of 10 ns (25 ns/m × 0.4 m) from one end of the line to the other is observed. If a pulse edge is applied at the beginning of the line having a rise time of 2 ns, the signal proceeds 8 cm (2 ns/25 ns/m) within this rise time. During this pulse edge, nothing happens over the length of the rest of the bus line (32 cm). Therefore, during this time, the capacitance of a 32-cm line (340 pF) has not been charged. The capacitance of this part of the line has no influence on the waveform or the signal delay of the driver circuit.

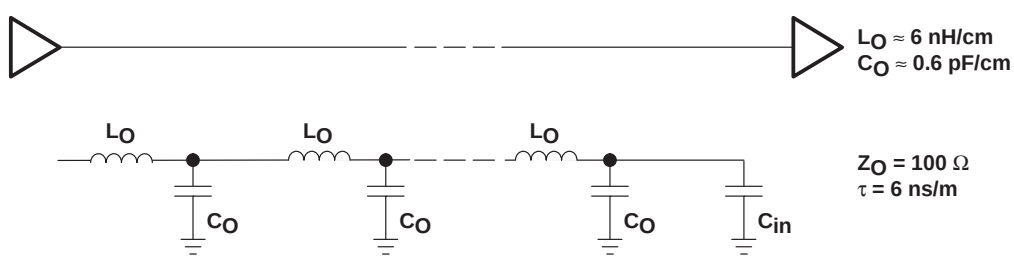

Figure 1. Physical Relationships on a Connecting Line Between Two Components

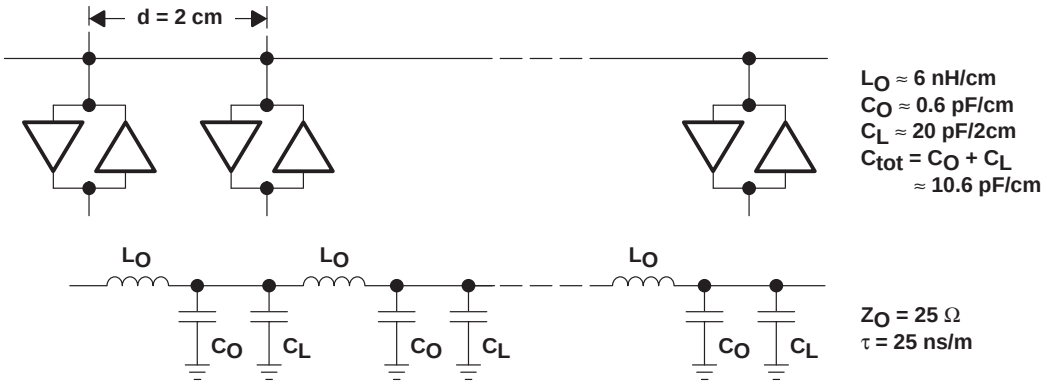

Figure 2. Physical Relationships on a Bus Line

Table 1. Additional Capacitive Loading of a Bus Line by a Module

CONTRIBUTOR	CAPACITANCE (pF)
Capacitance of the connector plug	≈5
Capacitance of the feedline from the driver I/O	≈5
Capacitance of the driver I/O	≈10
Capacitive loading from a module (total)	≈20

To illustrate this situation, Figure 3 shows a comparison between the waveform on a line with that from a load consisting of a lumped capacitance. It can be seen clearly in the diagram on the left that the length of a line and, therefore, its capacitance, has no influence on the waveform. To better observe the various loads, the rising edge is shown shifted by 10 ns. In the diagram on the right, instead of a line, a capacitor having the equivalent total capacitance value has been connected to the output of the test circuit. In this case, the output edge takes the form of a capacitor-charging curve. If the two measurement results are compared, it is clear that signals on a line behave very differently than in the case of a capacitive load. Therefore, an analysis using transmission-line theory is necessary.

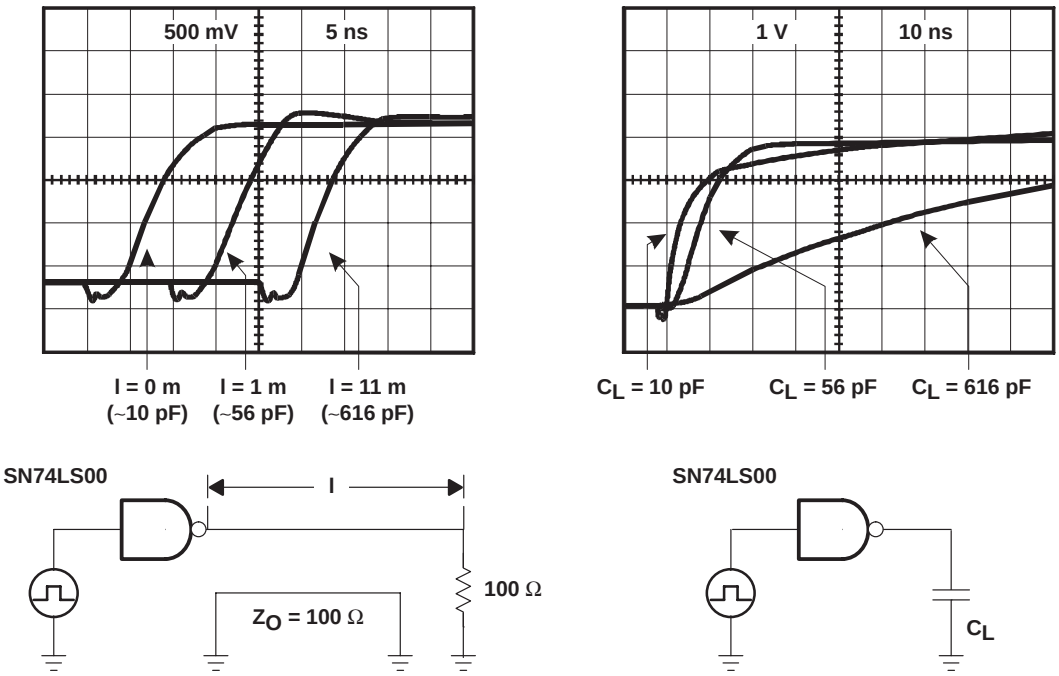

Figure 3. Waveform on a Line Compared to Waveform With a Load Capacitor

Transmission-Line Theory in Practice

With lines of more than a certain length, the behavior of signals must be analyzed using transmission-line theory. There is a simple rule that applies in this situation:

> *If the rise time or fall time of a signal is shorter than twice the line propagation delay time, transmission-line theory must be used.*

In practice, transmission-line theory must be used for a bus line with a propagation delay of 25 ns/m and a signal with an edge rise time of 2 ns, from a line length of 4 cm (2 ns/25 ns/m $\times$ 2). Because buses usually are longer than 4 cm, transmission-line theory is a necessary basis for examining the physical characteristics of bus lines.

With the frequencies and lengths of lines that now are used commonly in bus systems, the transmission-line theory can be simplified by neglecting any resistive component of the impedance. Equations 1 and 2 can be used for lossless lines with sufficient accuracy. Table 2 lists typical values for the characteristic properties of point-to-point lines between two components and bus lines.

$$Z_O = \sqrt{\frac{L'}{C'}} \quad (1)$$

$$\tau = \sqrt{L' \times C'} \quad (2)$$

Where:

Z_O = impedance of the line (Ω)
τ = propagation delay of the line (ns/m)
L' = inductive component of the line (nH/cm)
C' = capacitive component of the line (pF/cm)

Table 2. Typical Characteristic Properties of Lines

	L′ (nH/cm)	C′ (pF/cm)	Z_O (Ω)	τ (ns/m)
Point-to-point line between two components	5 to 10	0.5 to 1.5	70 to 100	≈5
Bus line	5 to 10	10 to 30	20 to 40	10 to 20

If a signal edge is fed into the beginning of the line (see Figure 4), a signal amplitude is created that can be calculated from the simple voltage divider, consisting of the internal resistance of the signal generator and the impedance of the line (Equation 3). The termination resistor R_{TT} has no influence on the edge because, at this point, the edge changes the voltage only at the beginning of the line, and at the end of the line no voltage change occurs.

$$U_i = U_G \frac{Z_O}{Z_O + R_G} \quad (3)$$

Where:

U_i = amplitude of the incident wave (V)
U_G = open-circuit voltage of the signal generator (V)
R_G = output resistance of the signal generator (Ω)
Z_O = impedance of the line (Ω)

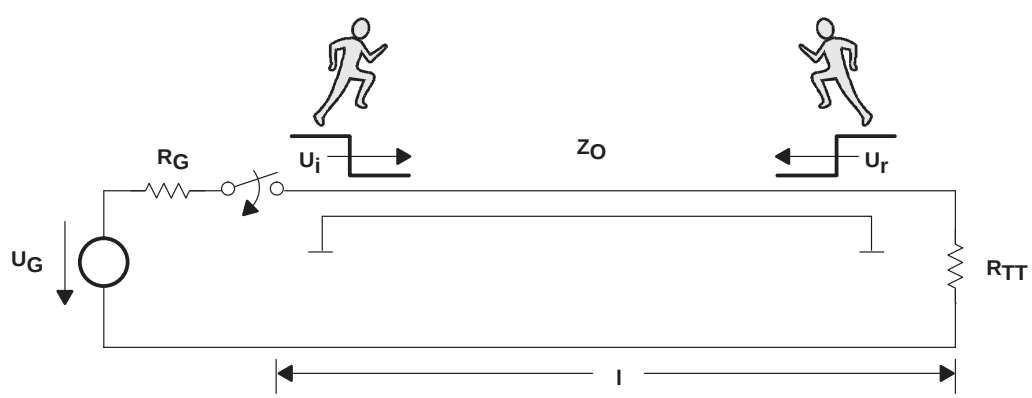

Figure 4. Wavefronts on Lines

This voltage edge now runs from the beginning of the line to the end. This first wave is called the incident wave. When the voltage wave reaches the end of the line, a reflected voltage wave is generated, the amplitude of which can be calculated from the reflection factor ρ, as shown in Equations 4 and 5.

$$\rho = \frac{R_{TT} - Z_O}{R_{TT} + Z_O} \tag{4}$$

$$U_r = U_i \times \rho \tag{5}$$

Where:

U_r = amplitude of the reflected wave (V)
U_i = amplitude of the incident wave (V)
ρ = reflection factor
R_{TT} = termination resistor at the end of the line (Ω)
Z_O = impedance of the line (Ω)

Using Equations 3, 4, and 5, results at the end of the line can be predicted:

$R_{TT} = 0 \Rightarrow \rho = -1$ (see Figure 5a)

The incident wave is inverted and reflected at the end of the line. Incident and reflected waves therefore cancel out each other, and there is no voltage increase at the end of the line.

$R_{TT} = Z_O \Rightarrow \rho = 0$ (see Figure 5b)

No line reflections occur. The end of the line is perfectly terminated.

$R_{TT} = \infty \Rightarrow \rho = +1$ (see Figure 5c)

The incident wave is fully reflected at the end of the line. There is a doubling of the amplitude at the end of the line.

A detailed analysis follows in *End of the Line: The Reflected Wave*.

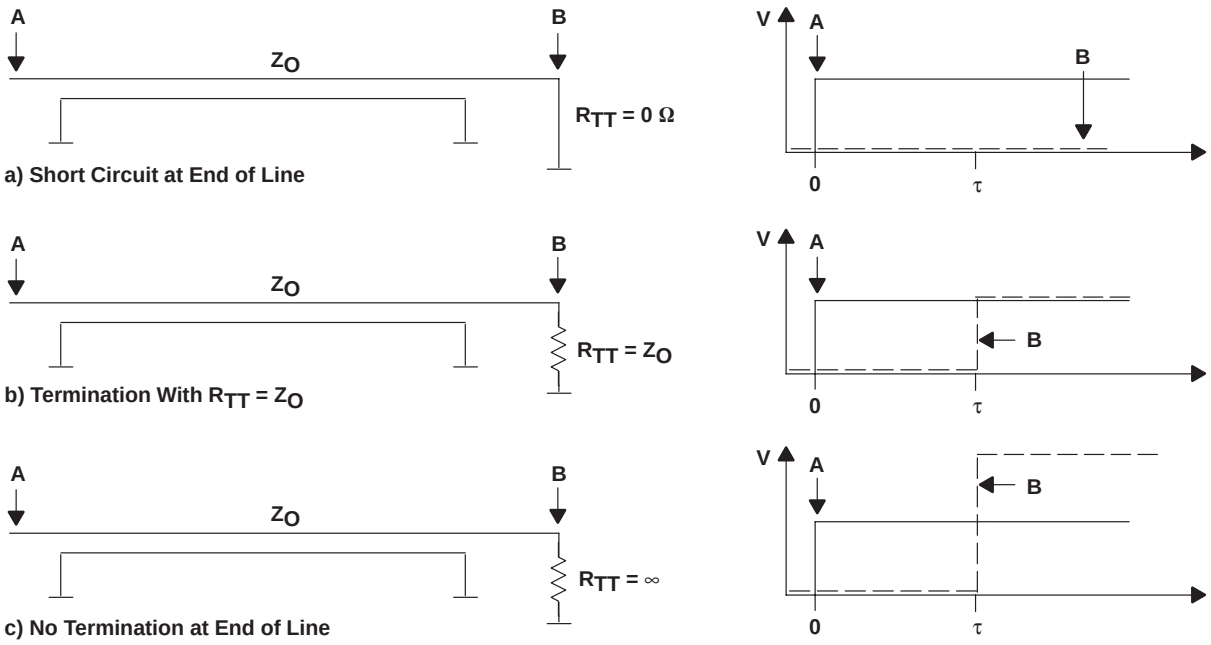

Figure 5. Signals at End of the Line

Effects on Bus Lines

Beginning of the Line: The Incident Wave

A fundamental characteristic of bus drivers is their output resistance. Together with the line impedance, this forms a voltage divider (Equation 3) and, thus, is responsible for the amplitude of the incident voltage wave.

If the driver can generate an incident voltage edge that has an amplitude above (below) the defined voltage threshold for the high logic state (low logic state), the logic level of all inputs that are connected on the bus will be changed over with the incident wave. For TTL-compatible bus systems, the rising edge of the incident voltage wave must exceed 2 V, and the falling edge must fall below 0.8 V. To calculate the maximum signal delay on the bus for an incident-wave-switching system, only the simple line propagation delay must be added to the delay time of the driver circuit (see Table 3).

Table 3. Signal Delay Using Figure 6 as an Example

	SWITCHING WITH THE INCIDENT WAVE	SWITCHING WITH THE REFLECTED WAVE
A⇒B	t_{pd} Driver + t_{pd} Receiver = 5 ns + 5 ns = 10 ns	t_{pd} Driver + t_{pd} Line + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 10 ns + 5 ns = 30 ns
A⇒C	t_{pd} Driver + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 5 ns = 20 ns	t_{pd} Driver + t_{pd} Line + t_{pd} Receiver = 5 ns + 10 ns + 5 ns = 20 ns
Worst case	20 ns	30 ns

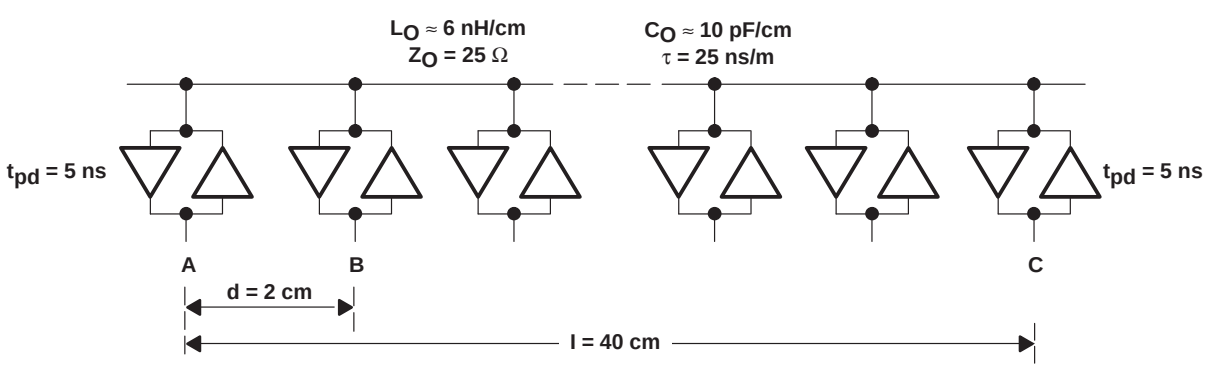

Figure 6. Example of a Bus Line

However, if the amplitude of the incident wave is insufficient, it is necessary to wait until the reflected wave returns from the end of the line to the beginning. Only then is a valid logic level reached on the entire bus line. In the example of Figure 6, according to Table 3, the signal delay time of 30 ns maximum results. Thus, when compared with switching with the incident wave, the signal delay time of the system is increased by 10 ns, or 50%.

This demonstrates one of the basic problems of bus systems. Since the amplitude of the incident wave depends on the voltage divider between the output resistance of the driver and the impedance of the line (≈25 Ω), a driver is needed with a particularly low output impedance. Only then is it possible to switch over a bus line with the incident wave. This is made more difficult because there are only two bus drivers at the beginning or end of the line. Most drivers sit in the middle of the bus line and, from there, must effectively drive two lines, one to the left and one to the right (see Figure 7). In this case, the resulting load impedance for drivers in the middle of the bus line effectively is halved (≈12.5 Ω).

Taking into account the voltage-divider rule for the incident wave, with TTL-compatible systems, an output resistance of <10 Ω is needed for the rising edge, and <4 Ω for the falling edge; the assumption here is that V_{OH} = 3.5 V, V_{OL} = 0 V. Even the most modern bus-driver families (such as the ABT family) do not have an output resistance that meets this requirement. For such applications, Texas Instruments (TI™) offers special TTL-compatible circuits, featuring the low output resistances that are needed: the incident wave switching (IWS) devices from TI, SN74ABT25xxx, for example, the SN74ABT25245. All other circuits that have the required low-resistance outputs were developed for new bus systems that are not TTL compatible. Examples of these new bus systems include BTL and GTLP.

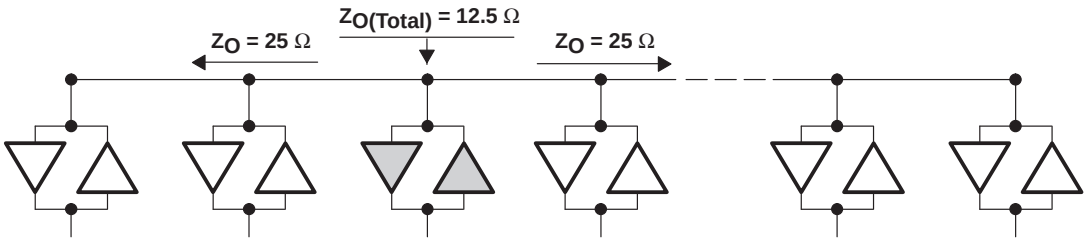

Figure 7. Load on a Driver in the Middle of the Bus is 0.5 × Z_O

TI is a trademark of Texas Instruments.

End of the Line: The Reflected Wave

As explained in *Transmission-Line Theory in Practice*, a voltage wave is reflected at the end of a line, and this reflected wave moves back to the beginning of the line. The amplitude of the reflected wave is determined by the amplitude of the incident wave and the reflection factor (Equation 5). This reflection factor is determined by the line impedance and the termination resistance (Equation 4). Therefore, the termination resistance has a major influence on the waveform of a bus line.

For the case of no termination resistance at the end of the line ($R_{TT} = \infty$), as shown in Figure 8a, the reflection factor is $\rho = 1$. The amplitude of the reflected wave is, therefore, exactly the same as the amplitude of the incident wave. In practice, this means that a low-resistance driver that generates an incident wave of 3 V, generates a reflected wave that also has an amplitude of 3 V. This results in an overshoot at the end of the line of 6 V ($V_{incident} + V_{reflected} = 3\ V + 3\ V$). The worst case would be a very low-resistance CMOS driver with an incident wave of 5 V, which would result in an overshoot of 10 V at the end of the line.

If the value of the termination resistance is assumed to be exactly the same as that of the line impedance, a reflection factor of $\rho = 0$ (Figure 8b) results. In this case, no reflection of the arriving wave occurs; thus, it is an ideal line termination. However, this method cannot be used with TTL and CMOS-compatible bus systems, because the impedance of the line would make it necessary to have a termination resistor of 25 Ω. With bidirectional lines, it would be necessary to connect this termination resistor at both ends, and each driver then would have to drive a load of 12.5 Ω. The maximum current through these resistors would be 280 mA (3.5 V/12.5 Ω) per line. Because, in practice, a bus often has more than 100 lines, the maximum total current of the bus termination would be >28 A. For this reason, with TTL systems, one operates with other terminating networks (Figure 8c to 8f) and, in such cases, accepts a mismatch ($R_{TT} > Z_O$).

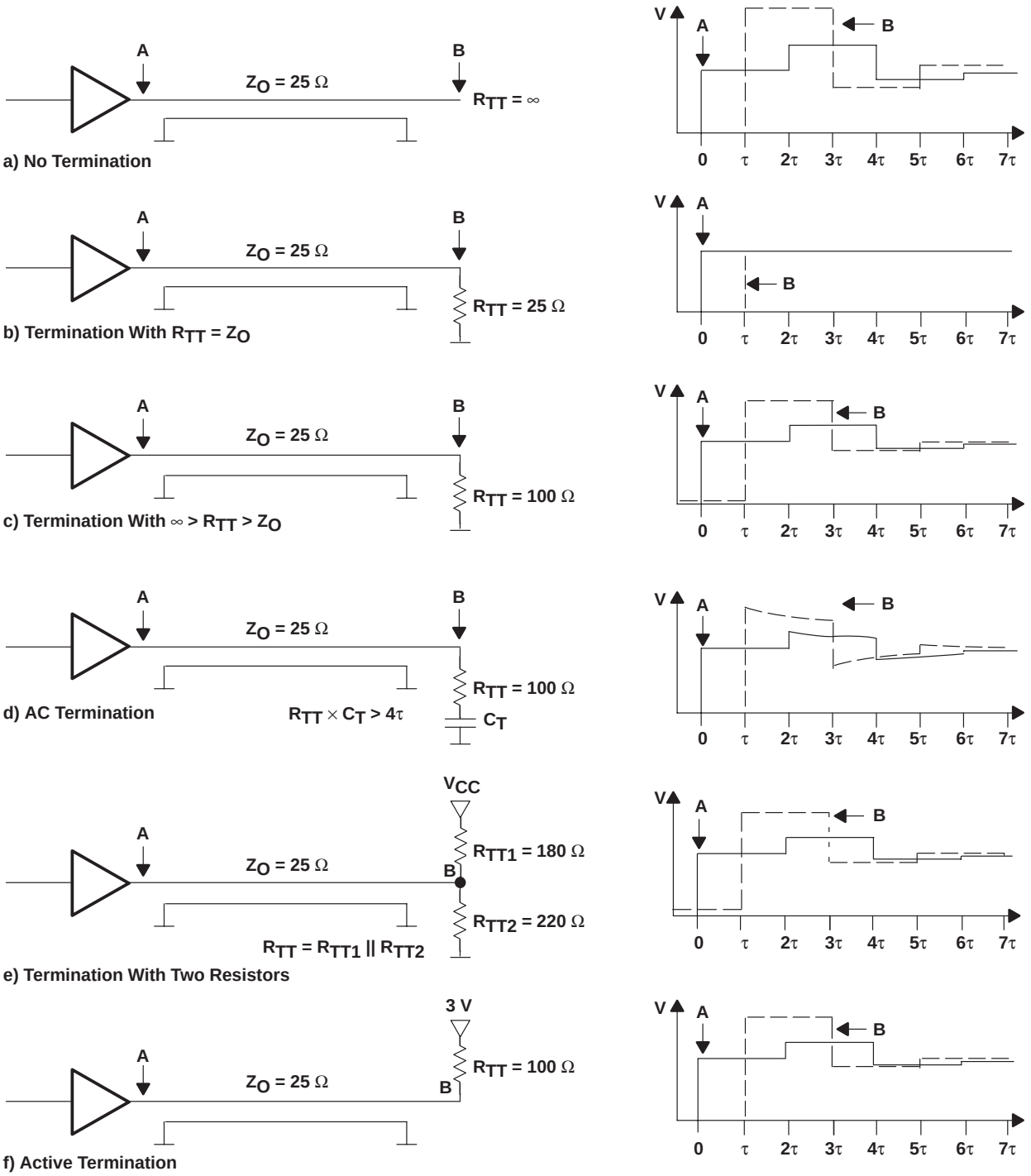

Figure 8. Termination Methods With TTL and CMOS Circuits

New Bus Systems Are Needed

The cause of most problems with bus lines is the distributed capacitive loading on the line by the modules connected to it. The impact on TTL and CMOS buses is:

- Very low signal speed on the line (about 25 ns/m, instead of 5 ns/m)
- The impedance of the line is reduced from about 80 Ω to about 25 Ω.
- As a result of the low impedance, adequate incident-wave amplitude is possible only with extremely low-resistance drivers.
- Correct termination is not possible because, otherwise, excessively high currents would flow through the terminating resistors.

It is not possible to solve these problems adequately with the circuit techniques commonly used with TTL- and CMOS-compatible circuits. With the commonly used techniques, it always would be necessary to accept a compromise in the circuit layout.

To develop a new bus system meeting the requirements imposed by the situation mentioned above requires the following:

- The capacitance of a module must be reduced, and also the capacitance of the I/O pins of the bus-driver circuit.
  - Because of the reduced capacitive component of the bus line, the impedance is reduced only to about 30 Ω.
  - The smaller capacitive component also results in less degradation of the signal speed (to about 20 ns/m).
- The drivers must be of low resistance to switch the bus with the incident wave.
- The signal amplitude must be reduced to allow correct termination of the line impedance. For example, with a signal amplitude of 1 V, a termination resistor of 30 Ω is adequate because the current flowing is only 33 mA per signal line.

The two bus systems that meet these basic physical requirements are BTL and GTL.

BTL Bus

The specification of the BTL bus was conceived especially for large backplane systems. The basic circuit layout of a BTL bus is shown in Figure 9.

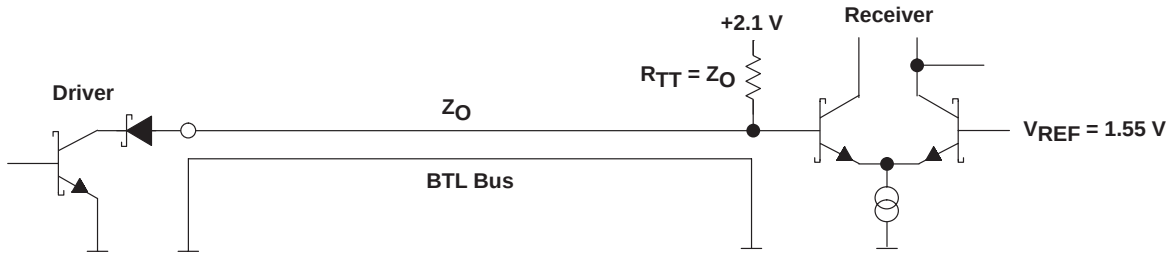

Figure 9. Circuit Concept of BTL Bus

The outputs of a BTL driver are provided with open-collector pins. The maximum capacitance of an I/O pin was fixed at 5 pF. To attain this goal, a diode is connected in series with the output transistor. The series connection of the capacitance of the transistor with the capacitance of the diode results in a reduction of the total capacitance. This circuit results in a low level of 1 V.

To allow switching of the bus lines with the incident wave, the specification for the drive capability was fixed at I_{OL} = 100 mA.

The high level is generated using a terminating resistor connected to 2.1 V at the end of the line. With bidirectional lines, a termination resistor must be provided at both ends of the line. As a result of the low signal amplitude of 1.1 V, the bus line can be terminated correctly with BTL systems. The maximum output current (I_{OL} = 100 mA) allows driving a terminating resistor of as low as 11 Ω (1.1 V/100 mA). If the BTL driver is in the middle of the bus line, the lower limit for the impedance is 22 Ω. This is sufficient for all bus systems that are used, particularly when the impedance and the signal speed are kept high, as a result of the limitation in the I/O capacitance.

By definition, the threshold voltage is 1.55 V, exactly midway between the low and high levels.

In large systems, it is essential that it be possible to remove and reinsert boards during system operation (live insertion). To meet this requirement, the precharge function has been implemented in BTL circuits. By means of this function, the capacitance of the pin, the stub line, and the I/O pin on the insertable board can be charged to the threshold voltage (1.55 V) before this pin comes in contact with the signal line on the backplane. Thus, it is possible to prevent signals on the backplane wiring from being so seriously interfered with that the data is corrupted.

The most serious disadvantage of the BTL bus is its high power consumption. If the transistor of a driver stage is operated to the limits of its specification, at the low level, a current of 100 mA can flow, with a voltage drop of 1 V. This results in the output stage dissipating 100 mW. If a 16-bit bus driver is used, in the worst case, 1.6 W may be consumed in the output transistors alone. With small surface-mounted components, this power consumption makes it necessary to use packages with a special heat sink.

GTL Bus

As shown in Figure 10, the basic circuit layout of the GTL bus is very similar to that of BTL. In this case, there also is a system with open-drain drivers and correct bus termination. The voltage levels of the logic states are 0.4 V in the low-logic state, and 1.2 V in the high-logic state. The signal amplitude is reduced to 0.8 V, whereby the threshold voltage lies exactly between the low and high levels, also at 0.8 V.

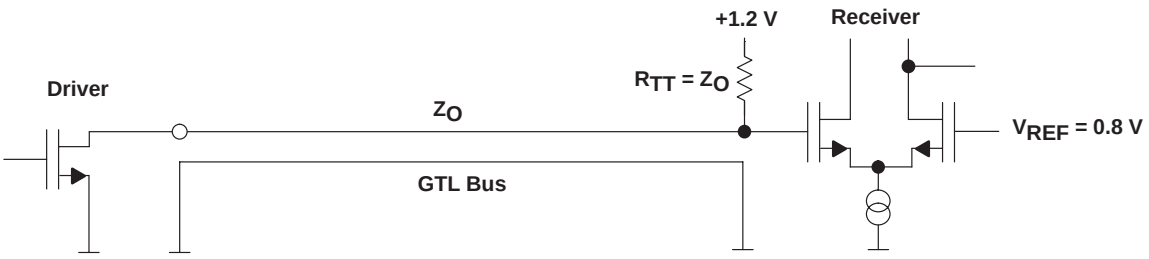

Figure 10. Circuit Concept of GTL Bus

In contrast to the BTL circuits, the drive capability of the output transistor is 40 mA. Therefore, the lower limit of the termination resistance (also of the line impedance) is 20 Ω (0.8 V/40 mA). For a driver connected to the middle of a bus line, the limit for the impedance of the line is 40 Ω. To attain impedance of the bus lines of 40 Ω, the capacitive component of the line must not be too high. Therefore, GTL is not the first choice when driving extensive backplane wiring with many modules.

Since the GTL bus was conceived for smaller buses on a circuit board, for example a memory bus between CPU and memory modules, the specification does not include the precharge function. The reason is that, when the bus is on a circuit board, there is no question of withdrawal and reinsertion during operation.

Comparison Between BTL and GTL

The structure of the two bus concepts (BTL and GTL) is similar. Both operate with open-collector/open-drain outputs and correct line termination. The most obvious difference is the definition of the logic voltage levels (Figure 11). The characteristics are listed and compared in Table 4. For large backplane wiring systems, the BTL circuits have the better characteristics, whereas the GTL bus features significantly lower power consumption. The target applications, which were considered when designing each of these bus systems, are apparent: BTL for large backplane systems, and GTL for smaller buses on a circuit board.

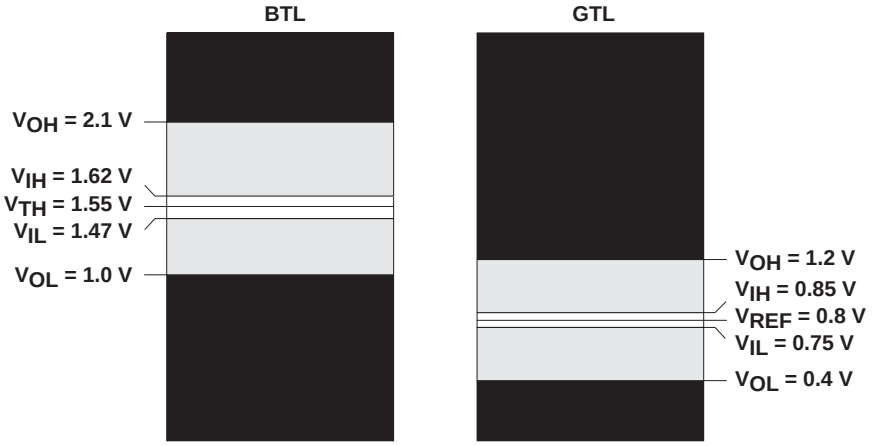

Figure 11. Comparison of Logic Voltage Levels of BTL and GTL

Table 4. Comparison of Characteristics of BTL and GTL

CHARACTERISTICS	BTL	GTL
Capacitance of an I/O pin	5 pF	Not defined, typically 5 pF to 9 pF
I_{OL}	100 mA	40 mA
Maximum power consumption of an output driver	100 mW	16 mW
Minimum Z_O for point-to-point connection	11 Ω	20 Ω
Minimum Z_O for a bus system	22 Ω	40 Ω
Precharge for withdrawing and reinserting boards during operation	Yes	No

New Backplane Solution: SN74GTLPH1655 From TI

It would be ideal to have a bus concept that combines all the desirable characteristics of both BTL and GTL. Meanwhile, TI offers a new generation of GTLP drivers that is compatible with existing GTL systems, but provides both the advantages of BTL and also the positive aspects of GTL drivers. A comparison is given in Table 5.

- The logic levels are compatible with GTL buses, and also bus systems with GTLP levels. GTLP represents a modification of the GTL specification that uses different termination voltage (V_{TT}) and reference voltage (V_{REF}) (see Table 6).
- Low capacitive loading of the bus (typical 6 pF)
- High drive capability (100 mA)
- Switching of a 11-Ω unidirectional line with the incident wave
- Switching of a 22-Ω bidirectional line with the incident wave
- Built-in precharge function

Table 5. SN74GTLPH1655 Compared With BTL and GTL

CHARACTERISTICS	BTL	GTL	GTL1655	GTLP MEDIUM	GTLP HIGH
Supply	5 V	5 V/3.3 V	3.3 V	3.3 V†	3.3 V†
I_{CC}	120 mA	120 mA	80 mA	50 mA	40 mA
I/O capacitance	<6 pF	<9 pF	8 pF	<9 pF	<9 pF
I_{OL}	100 mA	40 mA	100 mA	50 mA	100 mA
Maximum power consumption per output driver	100 mW	16 mW	40 mW	20 mW	55 mW
Minimum line impedance for point-to-point connection	11 Ω	20 Ω	11 Ω	19 Ω	9.5 Ω
Minimum line-impedance bus system	22 Ω	40 Ω	22 Ω	38 Ω	19 Ω
Precharge for line insertion	Yes	No	Yes	Yes	Yes
Overshoot-protection circuit	No	No	No	Yes	Yes
Edge-rate control (ERC)	No	No	Yes	Yes	Yes
Bus hold (A port)	No	Yes	Yes	Yes	Yes
Backplane switching characteristics in data sheet	No	No	No	Yes	Yes
Operational frequency on the backplane	≤30 MHz	≤40 MHz	~100 MHz	~100 MHz	~100 MHz

† Features 5-V tolerance at A port

The individual characteristics of the SN74GTLPH1655 are discussed in detail in the following sections.

Features of the SN74GTLPH1655

Functional Description: SN74GTLPH1655 – UBT

The SN74GTLPH1655 is described as a UBT, i.e., a bus driver for a wide variety of applications.

The function of this component can be controlled and changed in accordance with the signals and static voltage levels applied to the various control inputs.

By means of the control inputs OE, $\overline{OEAB}$, $\overline{OEBA}$, LEAB, and LEBA, one of the following three operating modes for the SN74GTLPH1655 can be selected:

- Transparent mode

  The SN74GTLPH1655 behaves like a bidirectional bus driver, for example, the ’245.

- Level-sensitive storage (latch) mode

  The SN74GTLPH1655 behaves like a level-sensitive register (latch), for example, a ’373. However, in this case, it can be used bidirectionally.

- Edge-triggered storage (flip-flop) mode

  The circuit behaves like an edge-triggered register, for example, a ’374. In this mode, it can be used bidirectionally.

The operating mode can be set separately for each direction of transmission. An example of a typical application is shown in Figure 12.

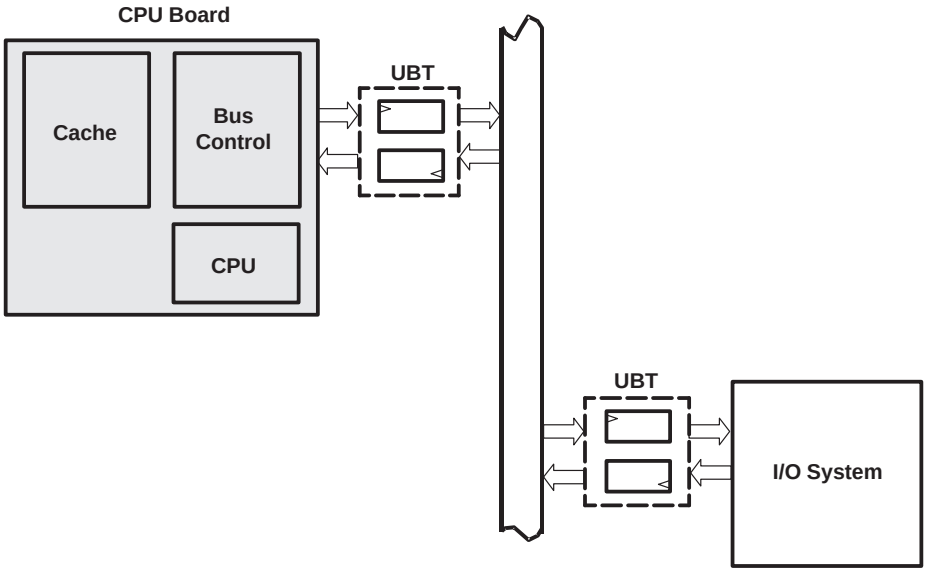

Figure 12. Typical Bus Application for a UBT

SN74GTLPH1655: Link Between a GTLP Backplane and an LVTTL Module

The SN74GTLPH1655 converts LVTTL-level signals (A port) into GTL- or GTLP-level signals (B port), and *vice versa*. The user decides, by choosing the termination voltage and the reference voltage, which level will be provided on the B-port side (see Table 6). The A port is, in every case, compatible with LVTTL.

This conversion is useful when continuing to work with LVTTL levels on the module, while the GTL and GTLP levels, specially developed for this application, are transmitted on the backplane. The low-voltage TTL and GTLP signal levels are shown in Figure 13. The SN74GTLPH1655 needs 3.3 V as the operating voltage.

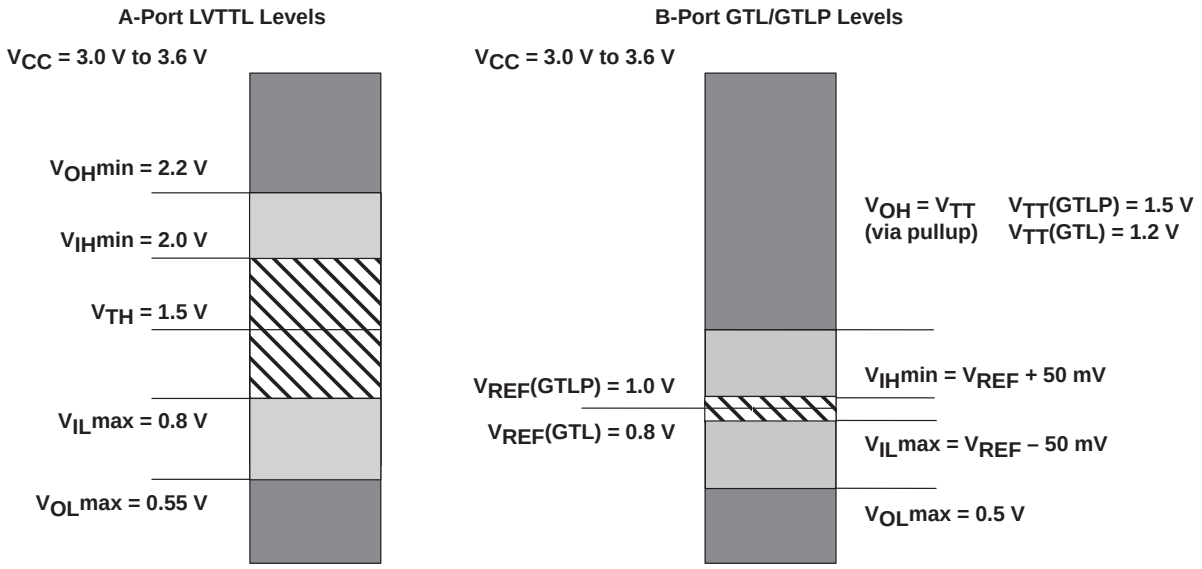

Figure 13. LVTTL and GTLP Signal Levels of SN74GTLPH1655

Table 6. Choice of GTL/GTLP Level (Using V_{TT} and V_{REF})

LEVEL		MIN	TYP	MAX	UNIT
GTL	V_{TT}	1.14	1.2	1.26	V
	V_{REF}	0.74	0.8	0.87	
GTLP	V_{TT}	1.35	1.5	1.65	V
	V_{REF}	0.87	1	1.1	

Termination Voltage, V_{TT}

There are various rules and techniques regarding proper line termination that should be observed for a successful development using SN74GTLPH1655.

The termination voltage (V_{TT}) should be derived from a voltage regulator. The current requirements, e.g., up to 100 mA per output, must be observed. There are various voltage regulators available that meet these requirements. Depending on the application, the regulators should be situated either directly on the backplane or on the module boards connected to it.

If several signal lines are switched simultaneously, considerable current fluctuations may occur at the termination voltage. For this reason, bypass capacitors should be provided close to the termination resistors (Figure 14).

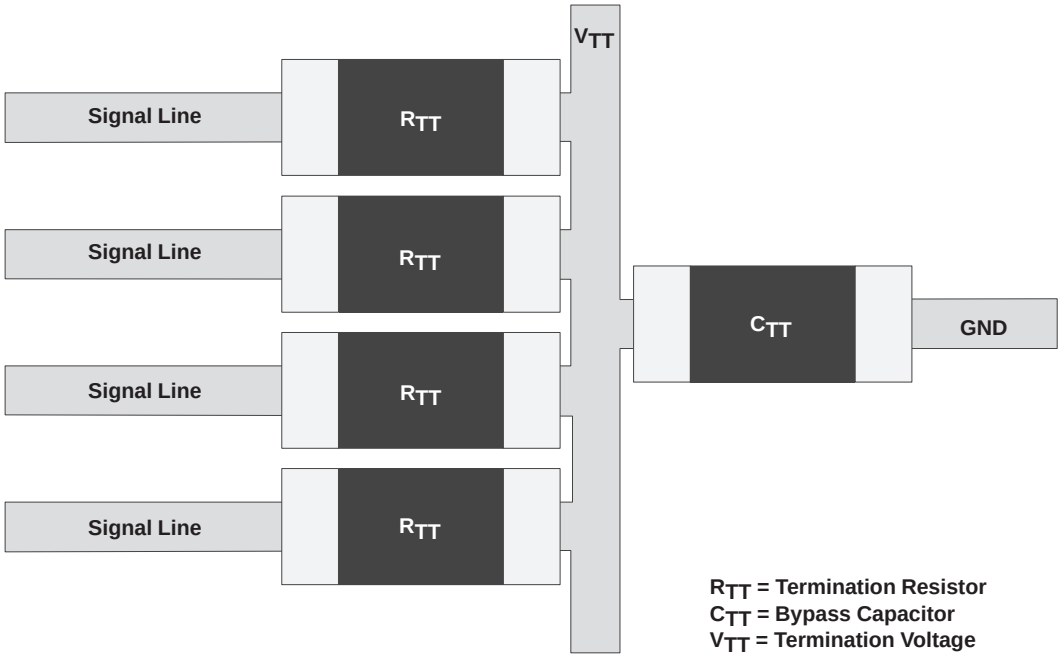

Figure 14. Proposed Layout of Termination Resistors and Bypass Capacitor on a Circuit Board

Since the bypass capacitor should have the lowest possible inductance, it is recommended that ceramic capacitors in surface-mount packages be used. The value of capacitance can be calculated from Equation 6.

$$C = I\frac{\Delta t}{\Delta U} \tag{6}$$

I = 50 mA — For bidirectional lines with a termination resistor at both ends of each line, a maximum of one-half the output current of an SN74GTLPH1655 (I_O = 100 mA) can flow through one of the two termination resistors.

ΔU = 10 mV — In this example, the collapse of the termination voltage V_{TT} must not exceed 10 mV.

Δt = 4 ns — The collapse of the termination voltage V_{TT} should be postponed for at least 4 ns.

$$C = I\frac{\Delta t}{\Delta U} = 50\ mA \times \frac{4\ ns}{10\ mV} = 20\ nF \tag{7}$$

If 82-nF ceramic capacitors are used, a bypass capacitor should be provided for every four signal lines. A proposed layout for the four termination resistors and the bypass capacitor on a circuit board is shown in Figure 14.

Reference Voltage, V_{REF}

The GTL or GTLP reference voltage (V_{REF}) can be derived, using a simple voltage divider and a bypass capacitor (0.01 µF to 0.1 µF), from the termination voltage. The circuit shown in Figure 15 has the advantage that V_{REF} follows voltage fluctuations of the termination voltage, V_{TT}. In this way, the maximum possible signal-to-noise ratio (SNR) always is ensured, even with an unstable termination voltage. Since only a very small current (maximum 10 µA) flows in the V_{REF} pin of the SN74GTLPH1655, the pin can be connected to the voltage divider without adversely affecting the GTL/GTLP reference voltage.

Ensure that the bypass capacitor is placed as close as possible to the V_{REF} pin of the SN74GTLPH1655.

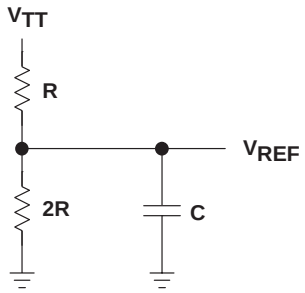

Figure 15. Suggested Connection of V_{REF} Pin

Static Characteristics of the SN74GTLPH1655

An understanding of the static characteristics of a component is necessary for a circuit development to be successful. The input and output characteristics of the SN74GTLPH1655 were, therefore, measured under laboratory conditions.

Input Characteristics

In principle, the input characteristics appear identical on both sides (A and B ports) of the device.

In Figure 16, the input protection diode easily is recognized; it is found both at the inputs of the LVTTL side (A port) and also at the inputs of the GTLP side (B port) of the device. The diode circuit provides protection against high negative-voltage spikes, which can occur as the result of electrostatic discharges or line reflections. In such cases, the diode conducts and prevents more-sensitive components from being destroyed.

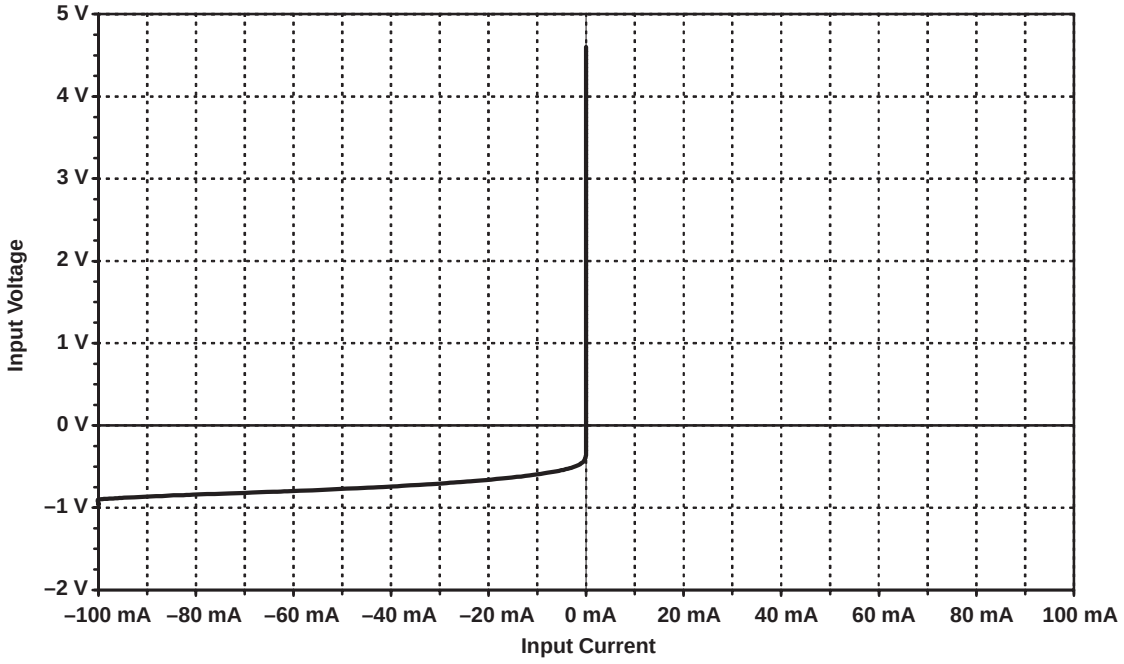

Figure 16. Input Characteristics of SN74GTLPH1655

Bus-Hold Circuit

If the input characteristics of the LVTTL side (A port) are recorded in small increments, and over a narrow range of current, the curve shown in Figure 17 results. This curve clearly demonstrates the effectiveness of the bus-hold circuit.

To change the logic state stored by the bus-hold circuit, a current of about 250 µA must be overridden.

This circuit is useful when, for example, all drivers on the bus are in a high-impedance state. Thus, an undefined state can be prevented.

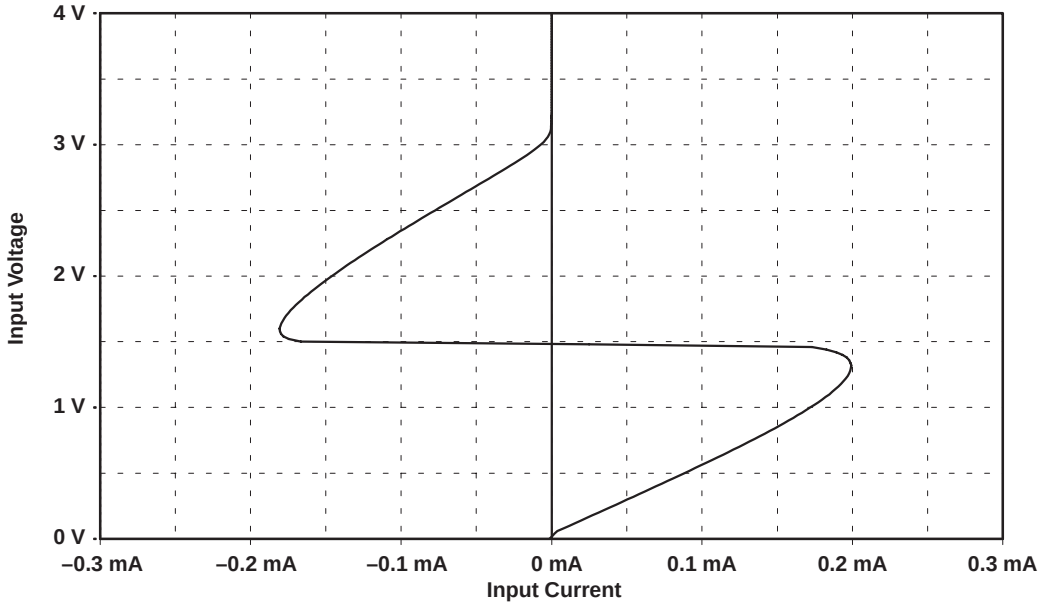

Figure 17. Bus-Hold Characteristics at LVTTL Input of SN74GTLPH1655

There is no bus-hold circuit on the GTLP side (B port). A bus-hold circuit on the GTLP side would defeat the principle of operation of the open-drain outputs, which take on the high-impedance state to allow the bus to achieve a logic high state (via the pullup resistors).

GTLP Output Characteristics

Because the SN74GTLPH1655 has been conceived as an interface between LVTTL partial systems and a GTLP backplane, the output characteristics of both sides are shown here. The characteristics for the various logic states of the output stage are shown in a single voltage-current diagram.

The principle of the GTLP bus is based on open-drain drivers, as shown in Figure 18.

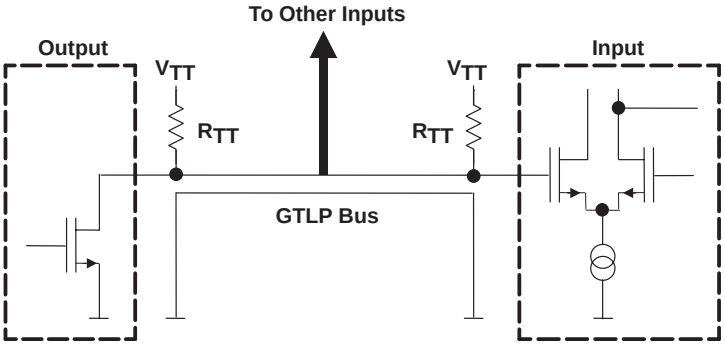

Figure 18. GTLP Bus: An Open-Drain Bus

The device actively drives only the low state on the bus; whereas, for the high state, the required current flows directly from the termination voltage source, V_{TT}. The current is limited only by a pullup resistor (R_{TT}), which usually is of very low resistance. According to the specification, the pullup resistor must be not less than the minimum value of 22 Ω. A primary purpose of resistor R_{TT} is to provide an optimum termination of the bus to avoid line reflections (see *Transmission-Line Theory in Practice*).

Figure 19 shows that in the low state, the output resistance of the GTLP output stage is in the range of about 4 Ω.

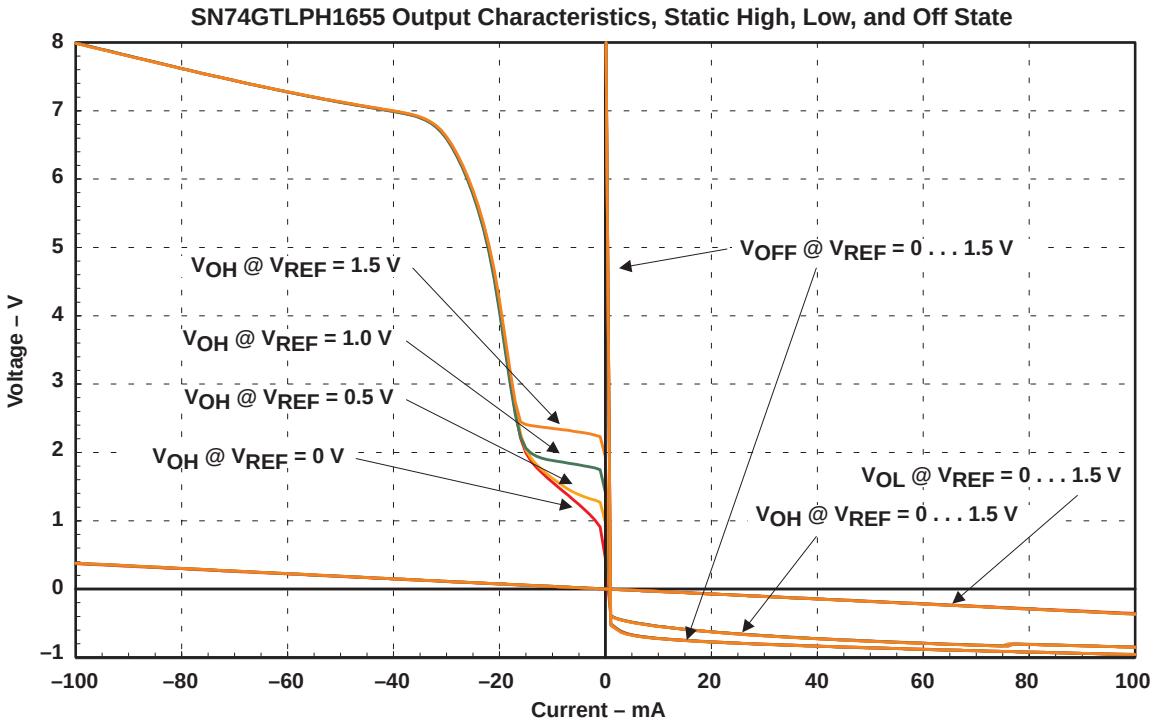

Figure 19. Output Characteristics of GTLP Port of SN74GTLPH1655

In the high state, the output transistor is blocking up to V_{REF} + one diode forward voltage. Thus, the output is at a very high resistance, as shown in Figure 19. Above V_{REF} + 0.7 V, a low resistive part follows, and then a high-resistive section, up to 7 V. Above 7 V, the curve again shows diode behavior. The special curve of output characteristics is caused by implementation of the TI-OPC into the GTLP outputs.

Because of the bidirectionality of the SN74GTLPH1655, the input protection diode also can be seen at the output during off state (for V_{CC} = 0 V) and 3-state. The outputs and inputs of the device are connected together and routed to a single pin.

LVTTL Output Characteristics

The output characteristics of the LVTTL output side of the SN74GTLPH1655 are shown in Figure 20, recorded with a supply voltage V_{CC} = 3.3 V. The output resistance for the low state is around 10 Ω, and in the case of the high state, a value of about 25 Ω is typical.

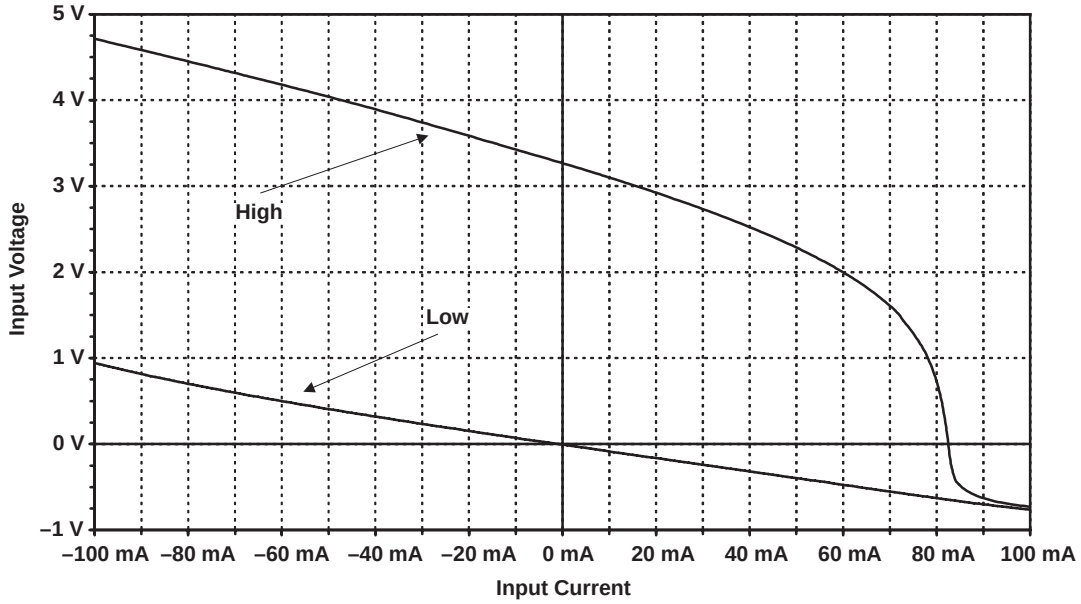

Figure 20. Output Characteristics of LVTTL Side of SN74GTLPH1655

TI-OPC Circuitry

TI-OPC circuitry is a new feature of the GTLP backplane family.

This circuit improves signal integrity by using a control circuit that compares the output voltage at the GTLP port with the reference voltage. The principle is shown in Figure 21.

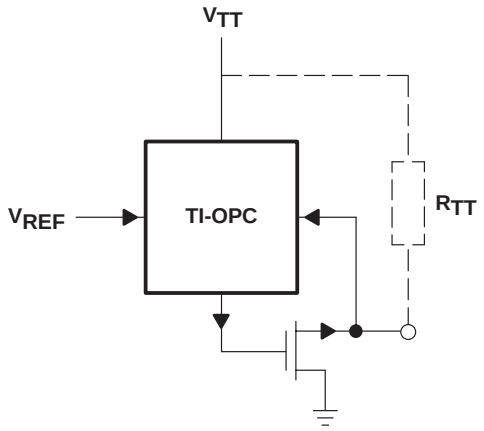

Figure 21. TI-OPC Circuitry Replacement of GTLP

If the output voltage exceeds about one diode forward voltage referred to the reference voltage, the TI-OPC circuitry limits currents below about 14 mA to the voltage to $V_{REF} + V_{diode}$. If this output current is exceeded, the output resistance increases again rapidly (compare to Figure 19).

Edge-Rate Control (ERC)

In the GTLP output stage, a circuit is included that allows two different values of edge rate to be set. With the use of the ERC input pin, different rise and fall times can be set, allowing the optimum configuration under various loading conditions of the backplane. If the SN74GTLPH1655 ERC is connected to the supply voltage (V_{CC}), the GTLP outputs are switched with longer rise and fall times than when it is connected to GND. Some GTLP devices have the $\overline{ERC}$ feature, which is the opposite of ERC. If $\overline{ERC}$ is connected to GND, the GTLP outputs are switched with a longer rise and fall time.

In two series of measurements, the voltage at the control input ERC was varied to determine the influence of the ERC circuit on the behavior of the signal.

As shown in Figure 22, the measurements on the SN74GTLPH1655 were made with a single device under no-load conditions, using GTLP voltage levels. During the measurement, only the 25-Ω pullup resistor was at the GTLP output. There were LVTTL signals from a signal generator at the A port of the device, each having different rise and fall times: t_r, t_f = 2 ns and t_r, t_f = 10 ns.

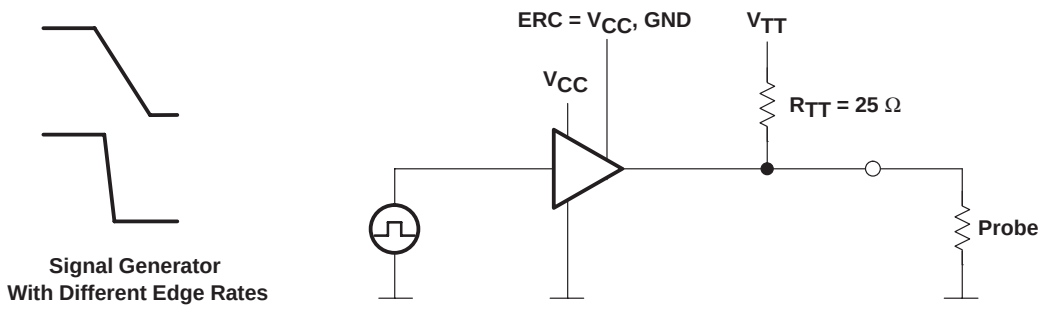

Figure 22. Setup for Measuring Edge Rate at GTLP Side of SN74GTLPH1655

Additional measurement results on the SN74GTLPH1655 test board are presented in a later section, which explains the behavior with a bus under realistic conditions.

The measurement results for falling edges are shown in Figures 23 and 24; Figures 25 and 26 show the curves for rising edges.

Using the definition of edge rate (slew rate) $dV/dt = (V_{OH} – V_{OL})/t_r, t_f$, a slew rate results in 0.2 V/ns for slow edge rate (ERC = V_{CC}) and 0.35 V/ns for fast edge rate (ERC = GND). As a comparison, these values are significantly less than those of standard TTL devices, which are usually about 1 V/ns, or more.

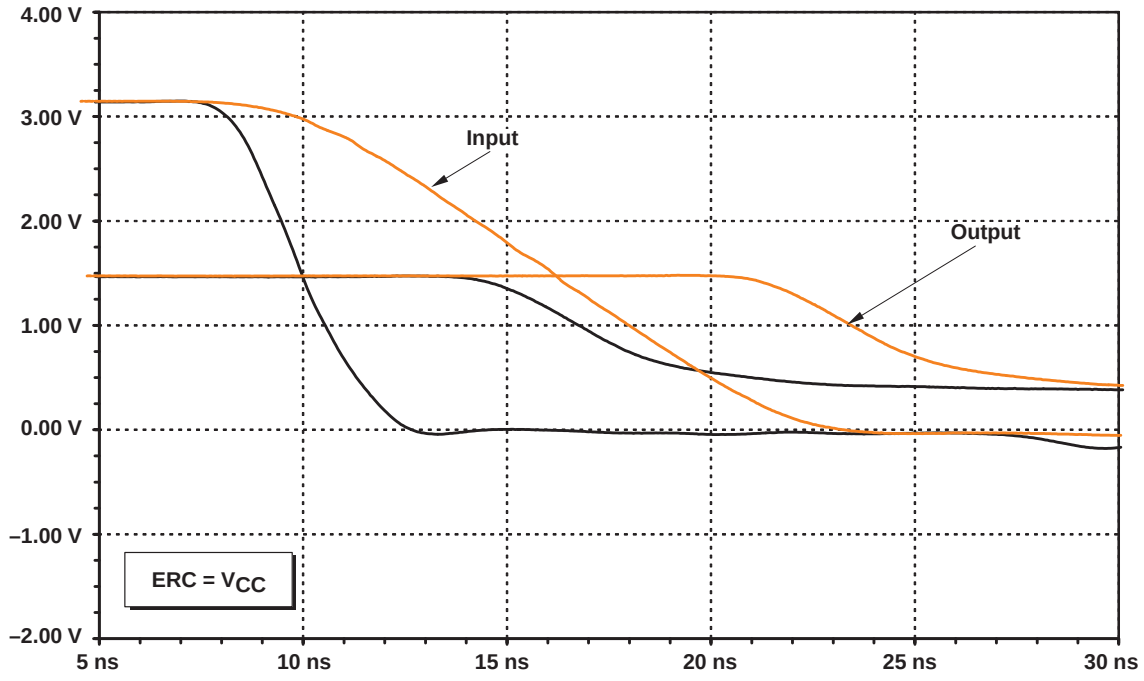

Figure 23. Falling Edge, ERC = V_{CC} (Slow Edges), Input Signals t_f = 2 ns, 10 ns

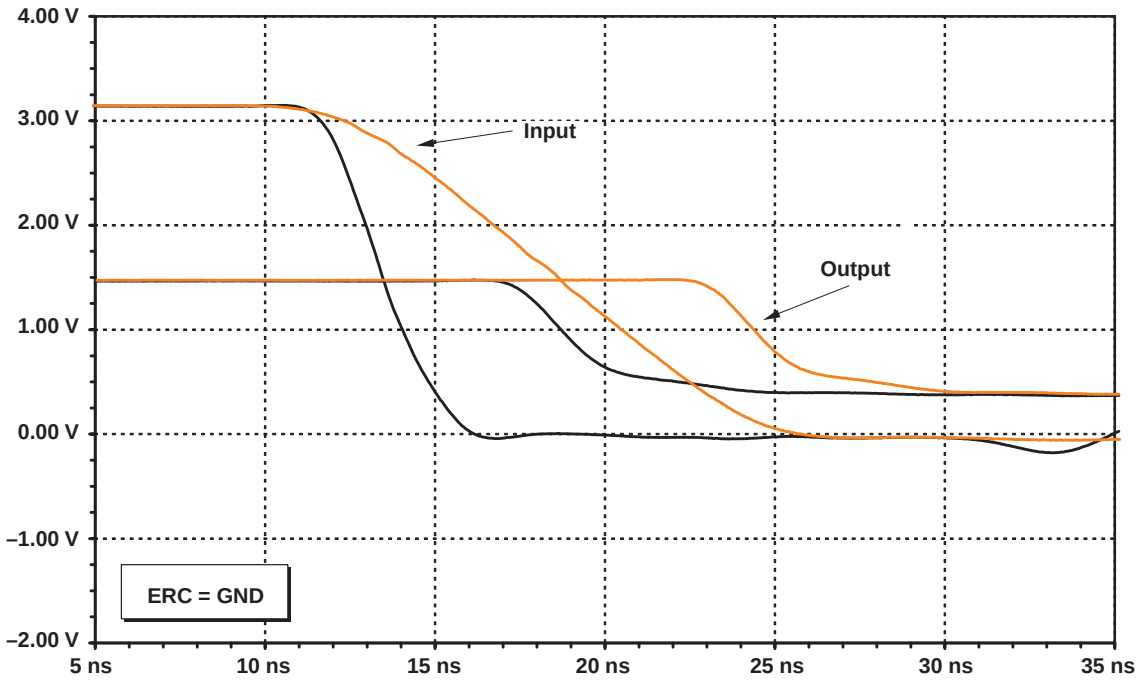

Figure 24. Falling Edge, ERC = GND (Fast Edges), Input Signals t_f = 2 ns, 10 ns

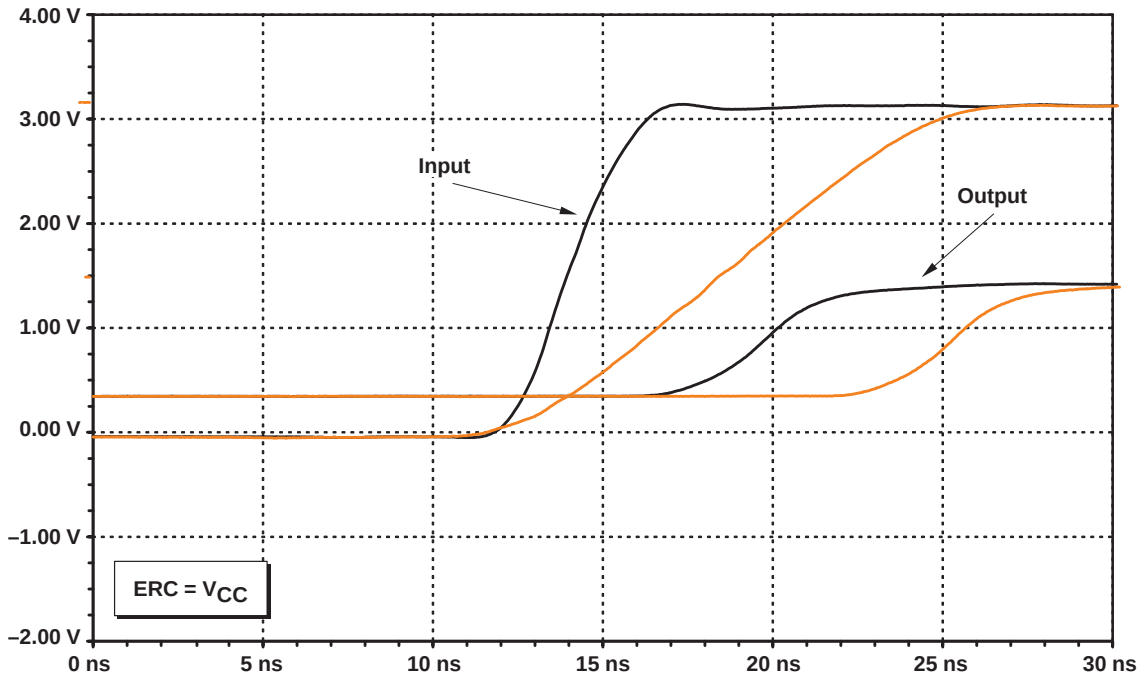

Figure 25. Rising Edge, ERC = V_{CC} (Slow Edges), Input Signals t_r = 2 ns, 10 ns

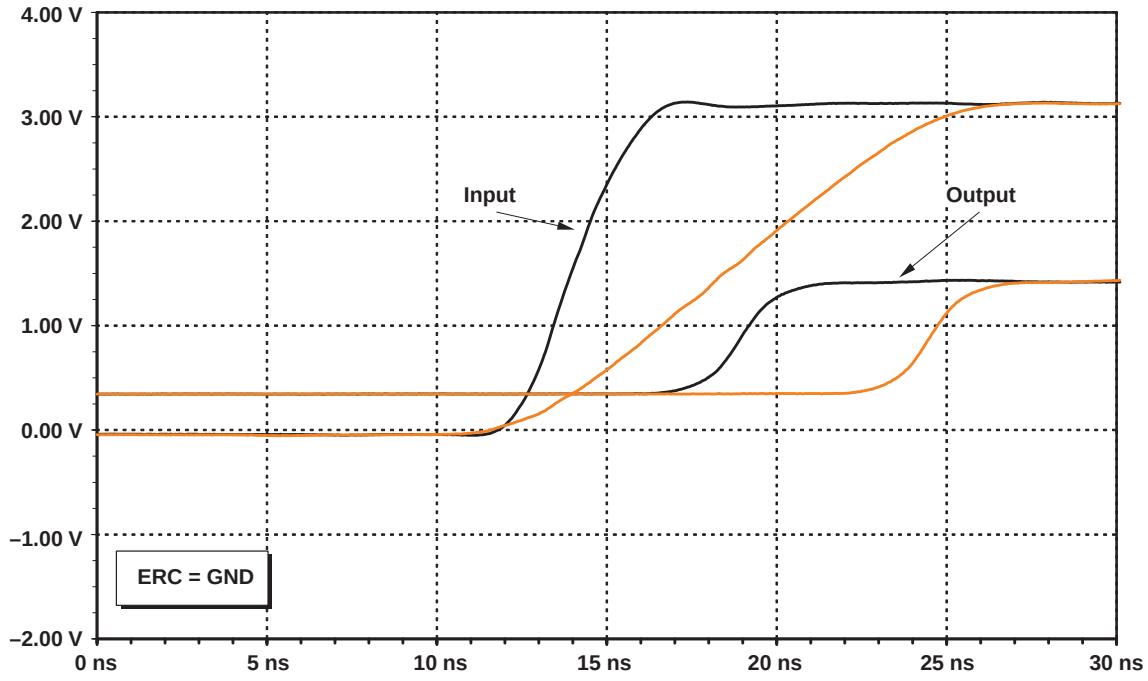

Figure 26. Rising Edge, ERC = GND (Fast Edges), Input Signals t_r = 2 ns, 10 ns

Removal and Insertion Under Voltage and Partially Switched-Off Systems

If it is possible to remove and reinsert plug-in boards in a system while it remains in operation (live insertion), special precautions must be taken with the signal lines.

- The outputs of the boards to be inserted or removed must be at a high impedance when the boards are inserted or removed.
- Before inserting a board, all pins must be charged to the threshold voltage (1.5 V with TTL-compatible systems, or $V_{CC}/2$ with CMOS-compatible systems). Thus, destructive voltage spikes on the signal line in excess of the threshold voltage range, which might otherwise corrupt the data on the bus, can be avoided.

Figure 27 shows this principle. The data pins are charged to the switching threshold (V_{TH}). As a maximum, the switching threshold can be reached when inserting; however, it no longer can be exceeded as a result of a voltage spike.

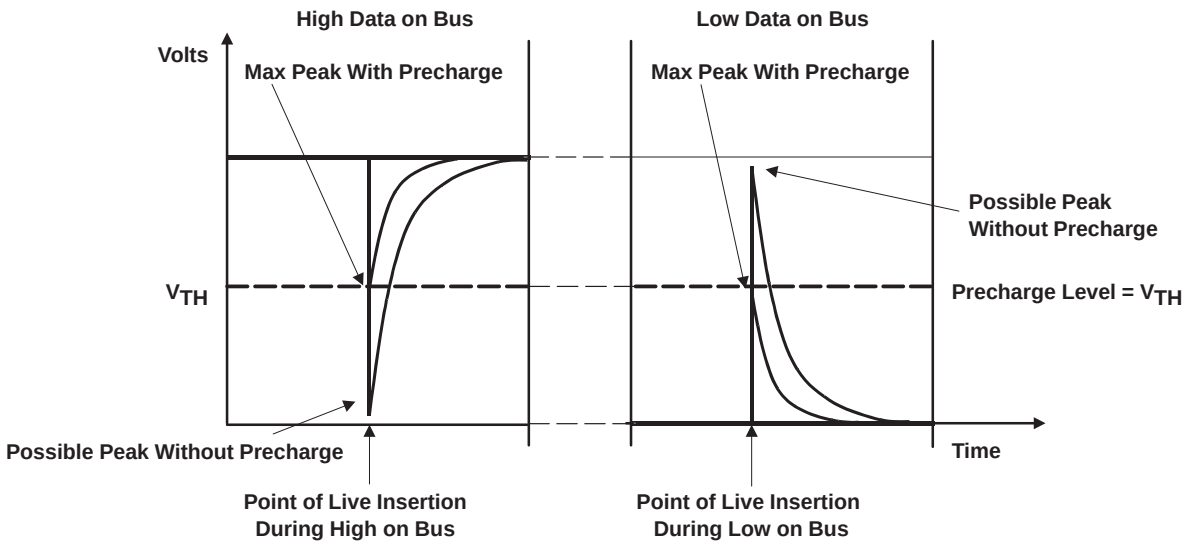

Figure 27. Influence of Precharge Function on Bus Signal

The SN74GTLPH1655 has the characteristics discussed above, which are necessary for the successful development of a live-insertion application.

Using the OE control input, it is possible to set the outputs of the SN74GTLPH1655 on both sides simultaneously to a high-resistance state. As a result of the integrated power-up 3-state circuit, the device is definitely inactive at a V_{CC} of less than 1.5 V.

To ensure that there is also a definite high-resistance state at a supply voltage between 1.5 V and the operating voltage, it is recommended that OE be connected to V_{CC} via a pullup resistor.

High-impedance outputs can be precharged to a definite voltage level by means of the precharge circuitry (BIAS V_{CC}). Disturbances to the active bus arising from insertion (charging/discharging of the I/O capacitance) will thus be kept to a minimum.

In a similar fashion, in modern applications, particular parts of a system are switched off from the source of power without having first removed them from the complete system. This is a partial switching off of the system, or a partial power down.

If a device is used in a partial power-down application, the inputs and outputs for V_{CC} = 0 V must be at high impedance, and thus be able to tolerate active bus signals.

The property of being partial-power-down compatible is reflected in the parameter I_{OFF}, which specifies the maximum leakage current in an input or output.

I_{OFF} is defined as:

- The device is disconnected from the operating voltage (V_{CC} = 0 V), and
- A logic level is applied to the input or output.

With the SN74GTLPH1655, the maximum value of I_{OFF} is 100 µA.

Refer to the TI application report *Live Insertion,* literature number SDYA012, which discusses this subject in detail.

Measurements on GTLPH1655 Test Board

A GTLPH1655 test board has been constructed to examine the characteristics of the SN74GTLPH1655 in a practical application. The principle of this board is shown in Figure 28.

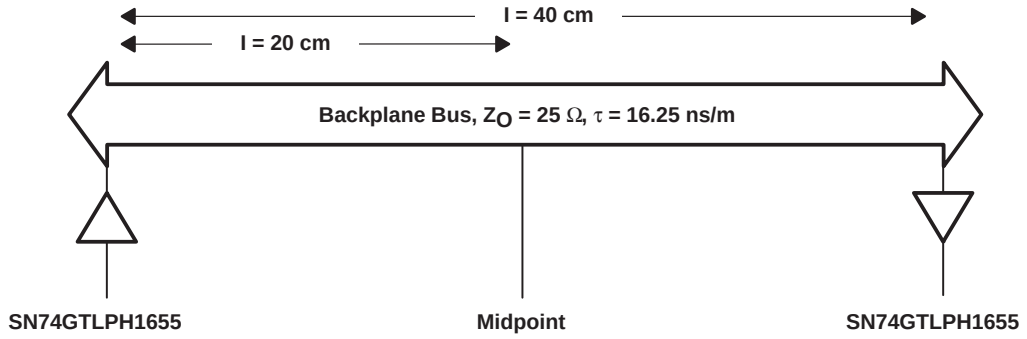

Figure 28. Principle of Construction of GTLP Bus on GTLPH1655 Test Board

This bus consists of a straight connecting line, 40 cm long, between two SN74GTLPH1655 devices.

In practice, a backplane wiring system provides the option for multiple plug-in modules. The bus impedance is reduced as a result of the additional input capacitances of the modules that are connected to it (see Figure 2). This effect can be approximated by connecting capacitors between the bus line and ground at intervals of 2 cm.

Both sides of the bus are provided with termination resistors that are connected to V_{TT}. The termination voltage is set at 1.5 V. A 1-V reference voltage (V_{REF}) was chosen. In this way, GTLP signals are transmitted on the bus.

The termination resistors for this setup were chosen to match the line impedance, which, for a fully loaded backplane, results in Z_O = 25 Ω. This case provides optimum line termination, with a reflection factor very close to ρ = 0.

For the measurements, the slew rate of the GTLP output stage was varied by means of the edge-rate control input ERC. The measurements were carried out under two different bus conditions: a fully loaded bus (with distributed capacitors) and the bus unloaded (without capacitors). The clock frequencies used were 10 MHz, 50 MHz, and 160 MHz, the last being close to the maximum value of 175 MHz specified in the data sheet.

For the case of a fully loaded bus, the result is a line impedance of about 25 Ω, and a delay time on the line of about 7 ns.

With the bus unloaded, i.e., operated without capacitors connected to it, the line impedance is about 30 Ω, and the delay time on the line reaches a value below 3 ns.

The measurement results presented in Figures 29 through 52 show:

- The LVTTL input signal of the SN74GTLPH1655 that drives the bus line, together with the LVTTL output signal of the SN74GTLPH1655 receiver that is situated at the end of the GTLP bus. For this, the load of the receiver was varied. The diagrams show the curves for $R_L = \infty$ (unloaded output) and for $R_L = 50\ \Omega$.
- Waveforms on the GTLP bus line:
  - GTLP output signal of the SN74GTLPH1655 that drives the bus line, i.e., the signal at the beginning of the line
  - Bus signal in the middle of the GTLP bus
  - Signal at the end of the GTLP bus line, which also is applied to the input of the SN74GTLPH1655 receiver device.

All curves are shown together for the frequencies 10 MHz, 50 MHz, and 160 MHz, and for the two different edge-rate settings (with ERC = V_{CC} and ERC = GND).

For these measurements, care was taken to ensure that the timing relationships between them remained constant. A summary of the measurement results is given in Table 7.

Table 7. Measurement Results on SN74GTLPH1655 Demonstration Board

	SIGNAL	BUS LINE UNLOADED (WITHOUT CAPACITORS)		BUS LINE LOADED (WITH CAPACITORS)	
		SLOW EDGE RATE ERC = V_{CC}	FAST EDGE RATE ERC = GND	SLOW EDGE RATE ERC = V_{CC}	FAST EDGE RATE ERC = GND
f = 10 MHz	I/O LVTTL level	Figure 29	Figure 31	Figure 41	Figure 43
	Beginning, middle, end of GTLP bus	Figure 30	Figure 32	Figure 42	Figure 44
f = 50 MHz	I/O LVTTL level	Figure 33	Figure 35	Figure 45	Figure 47
	Beginning, middle, end of GTLP bus	Figure 34	Figure 36	Figure 46	Figure 48
f =160 MHz	I/O LVTTL level	Figure 37	Figure 39	Figure 49	Figure 51
	Beginning, middle, end of GTLP bus	Figure 38	Figure 40	Figure 50	Figure 52

Measurement Results With an Unloaded Backplane (Z_O = 30 Ω, R_{TT} = 25 Ω)

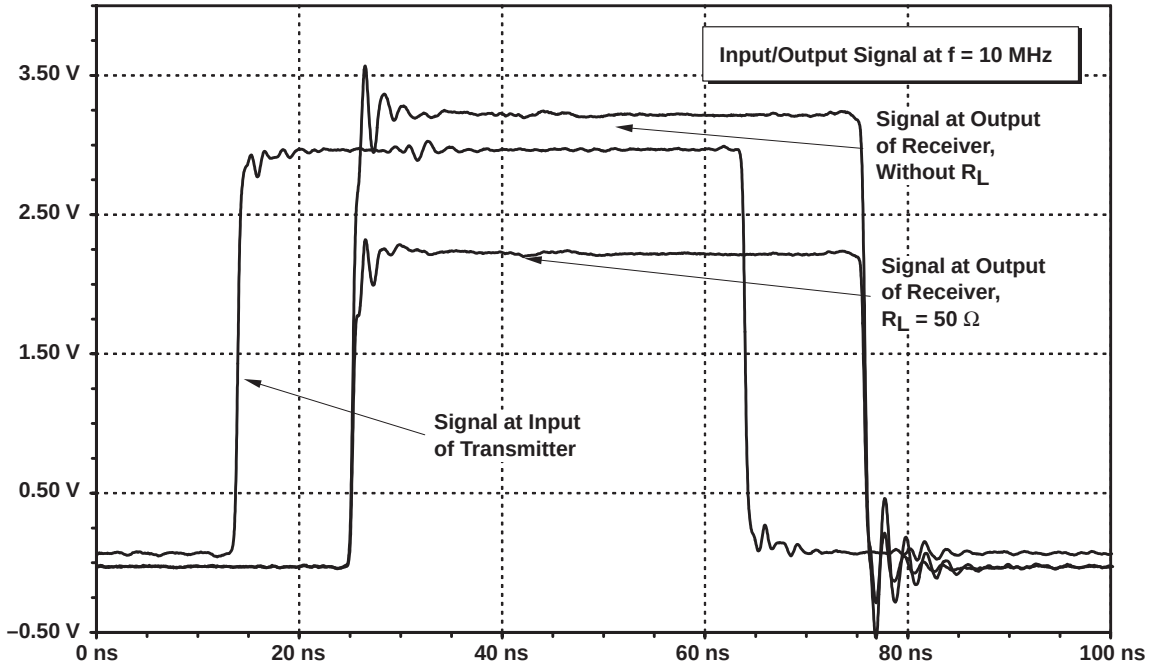

Figure 29. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 10 MHz

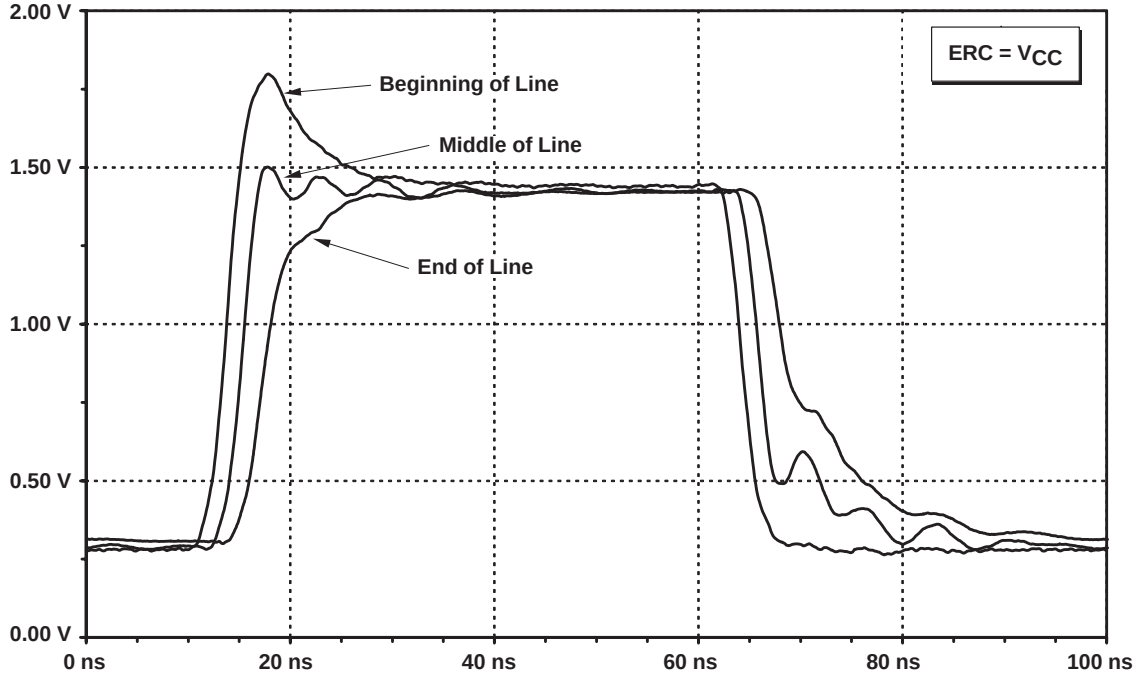

Figure 30. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 10 MHz

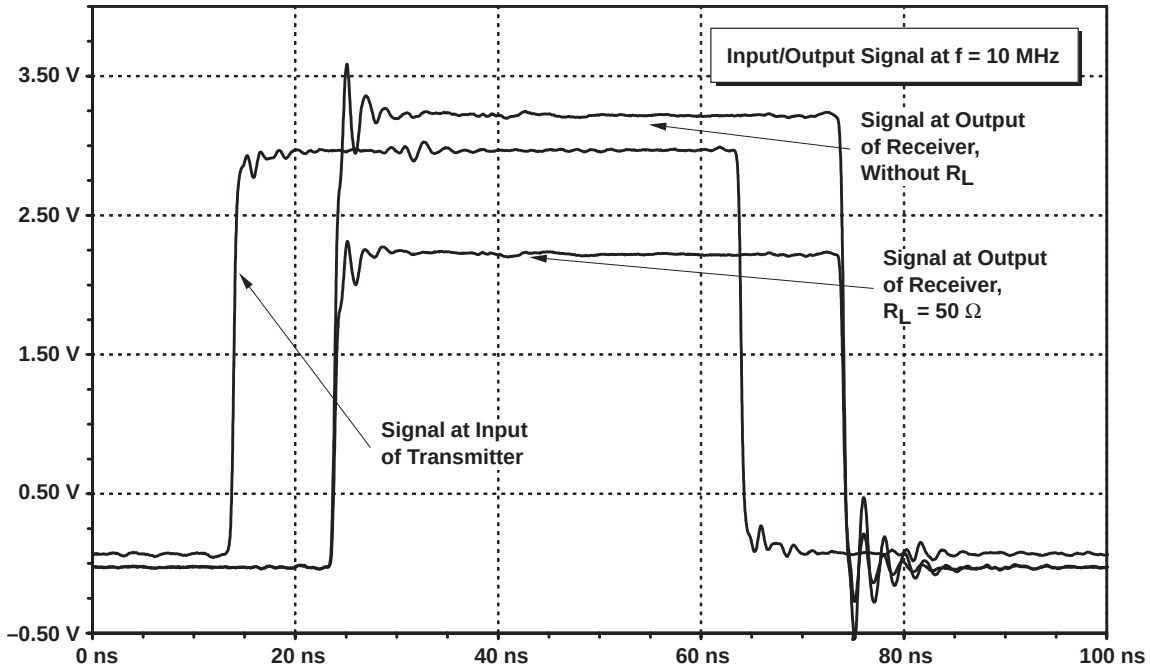

Figure 31. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 10 MHz

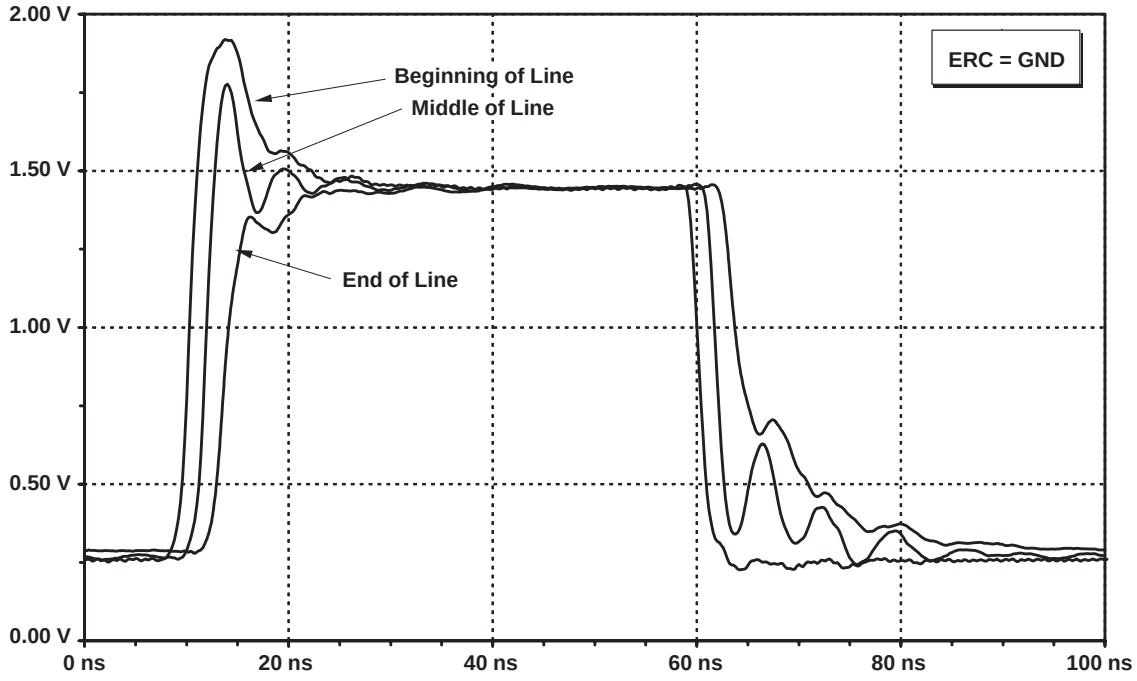

Figure 32. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 10 MHz

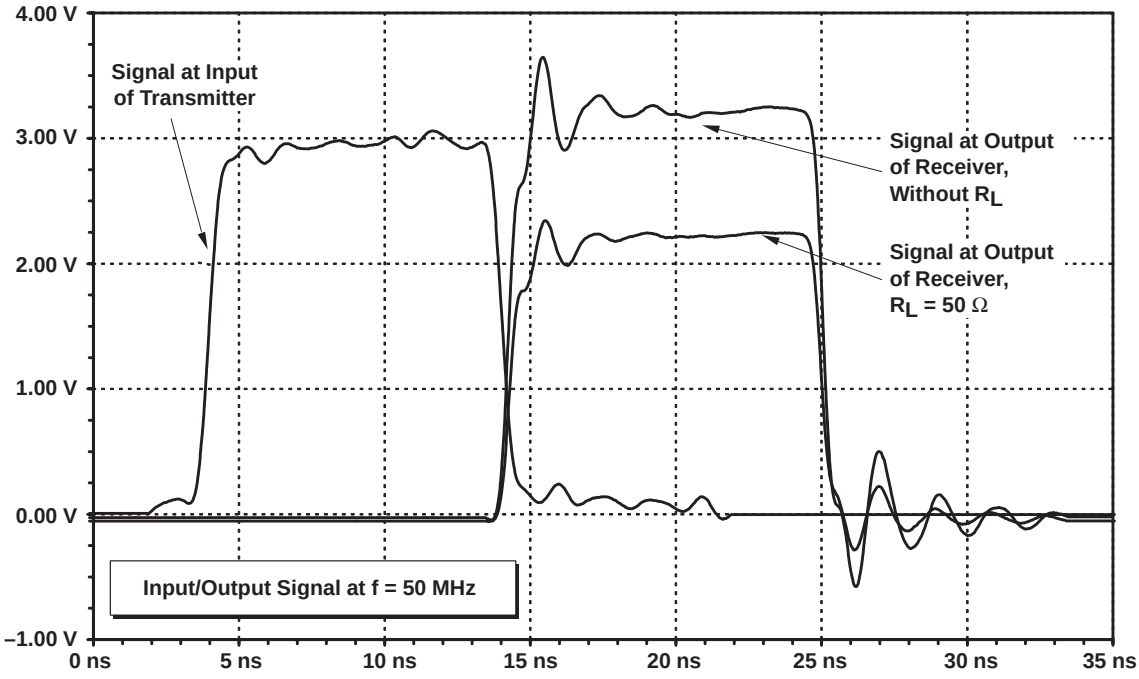

Figure 33. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 50 MHz

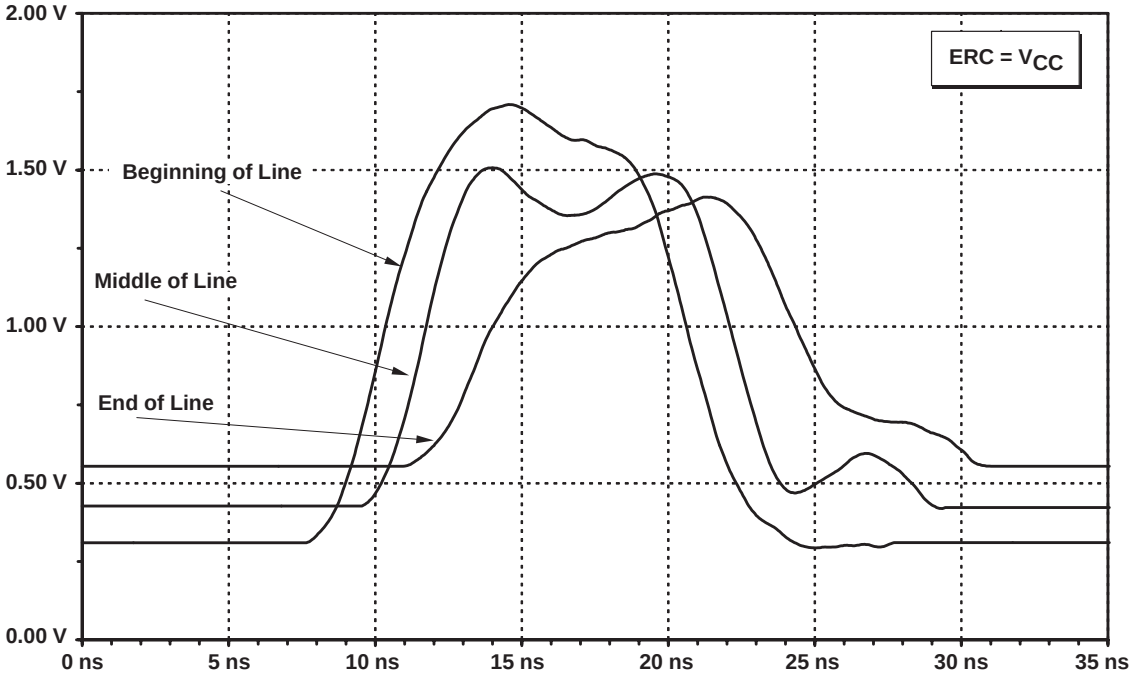

Figure 34. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 50 MHz

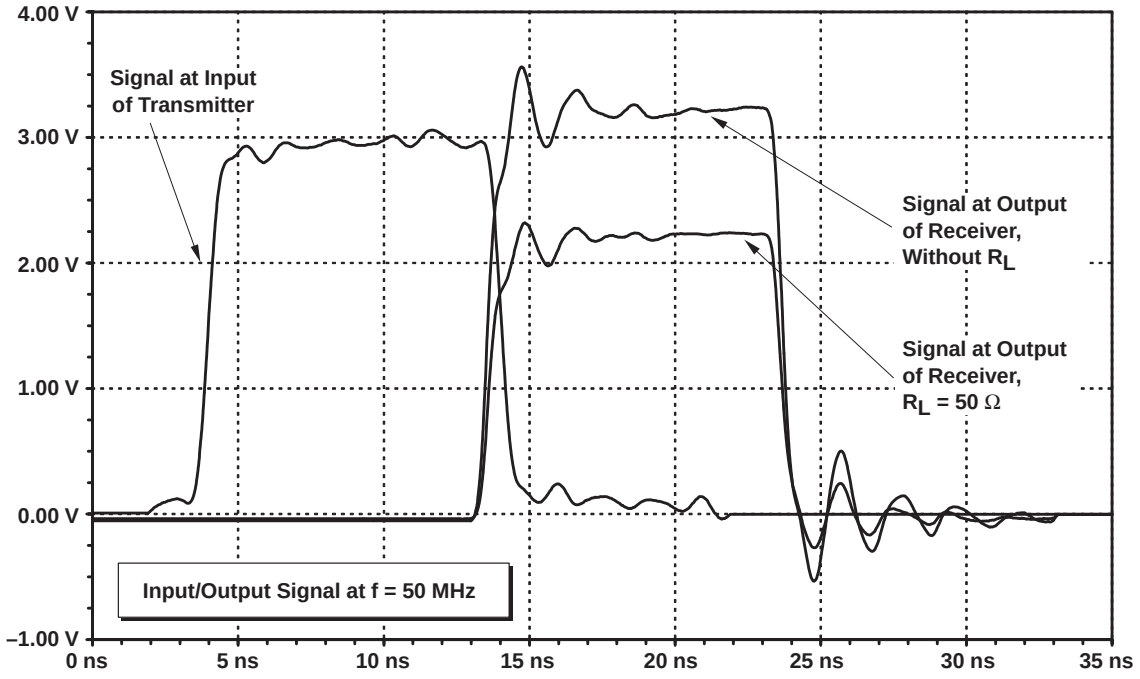

Figure 35. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 50 MHz

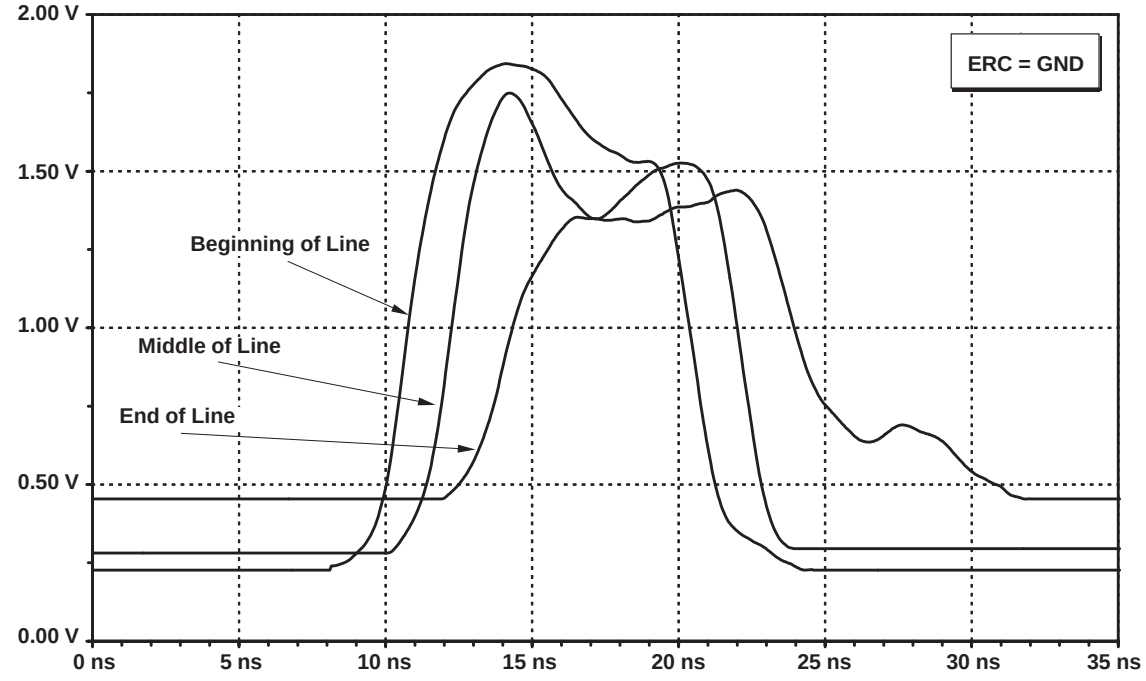

Figure 36. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 50 MHz

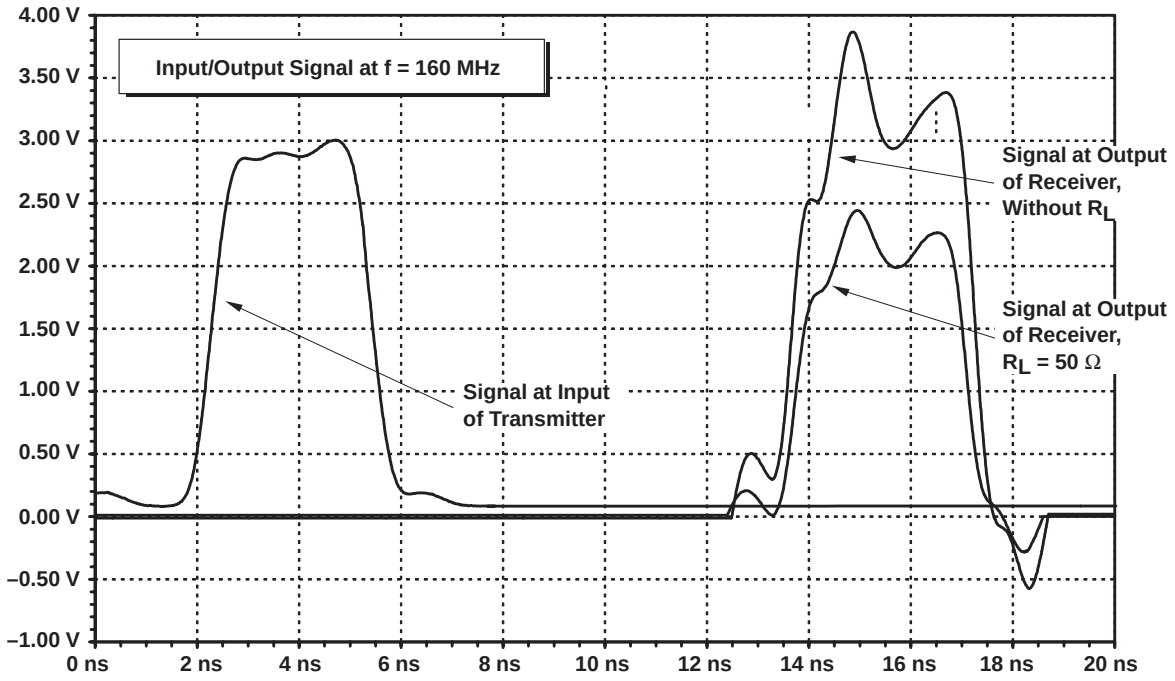

Figure 37. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Unloaded, 160 MHz

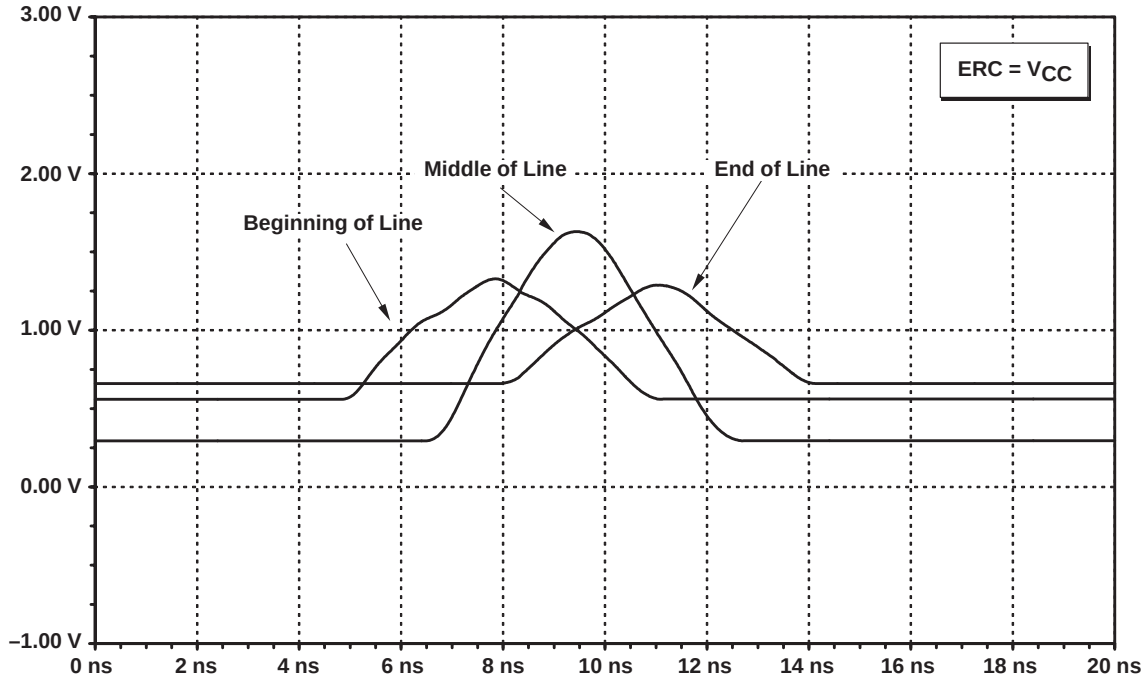

Figure 38. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Unloaded, 160 MHz

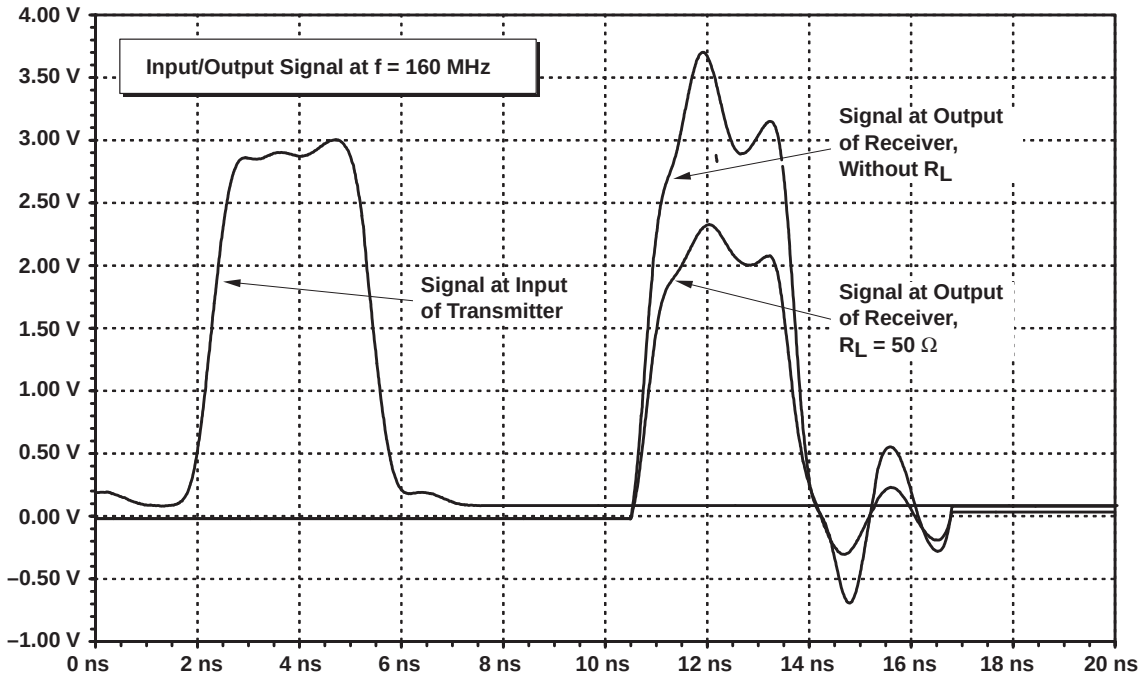

Figure 39. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Unloaded, 160 MHz

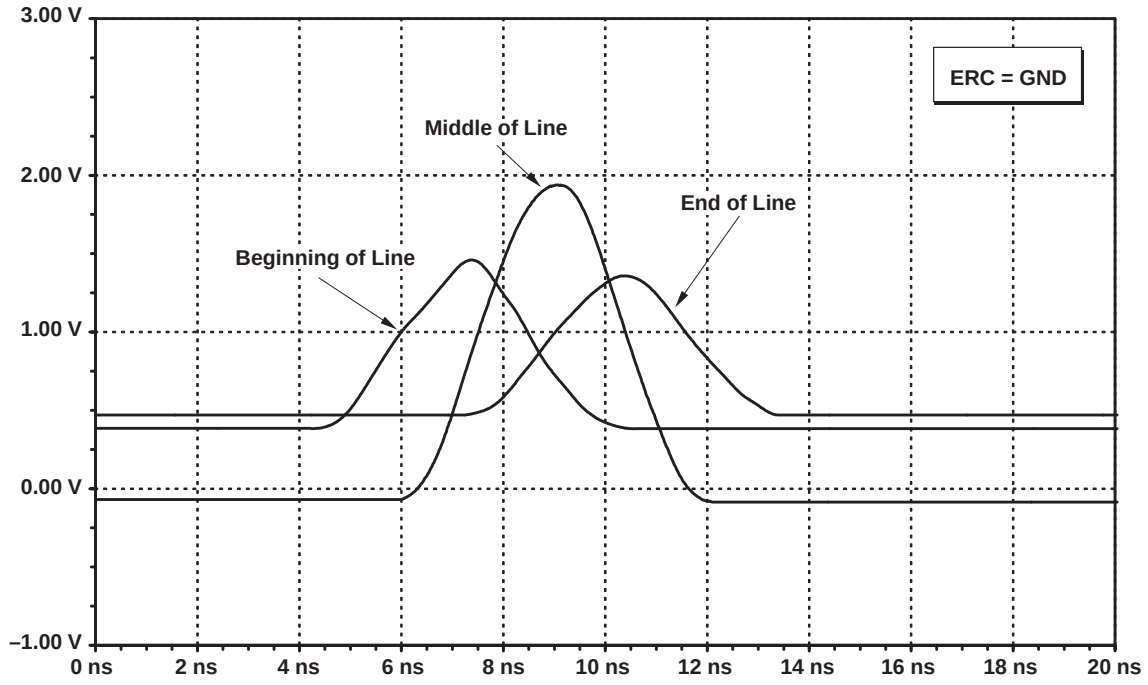

Figure 40. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Unloaded, 160 MHz

Measurement Results With a Loaded Backplane (Z_O = 25 Ω, R_{TT} = 25 Ω)

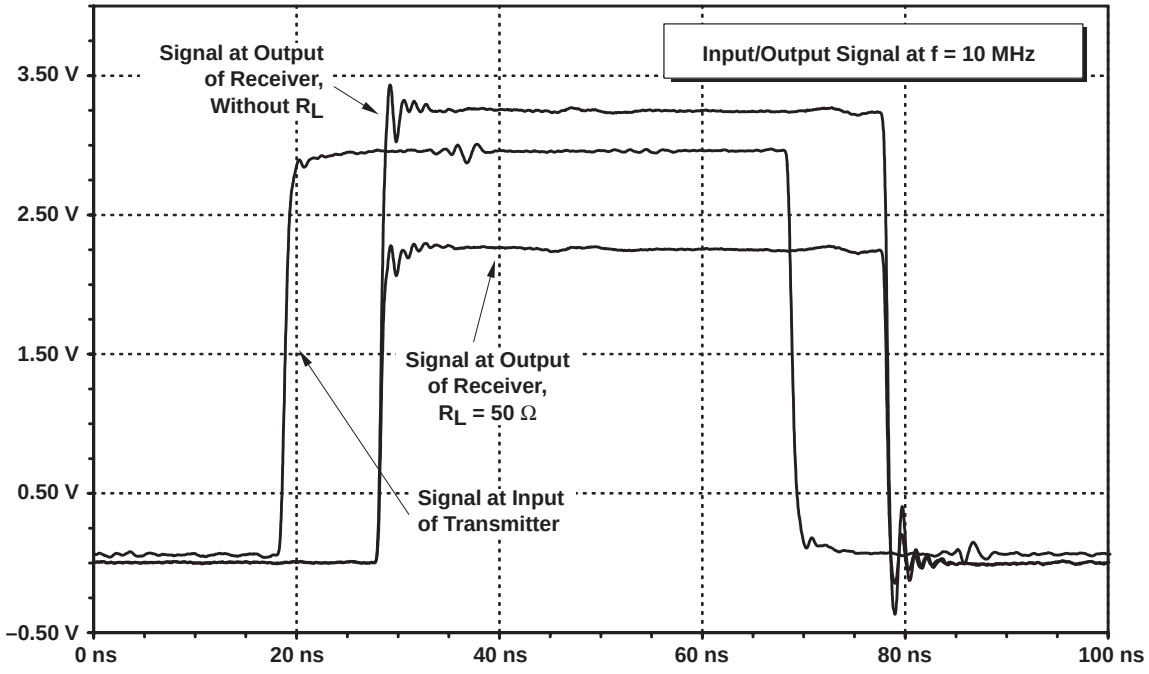

Figure 41. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 10 MHz

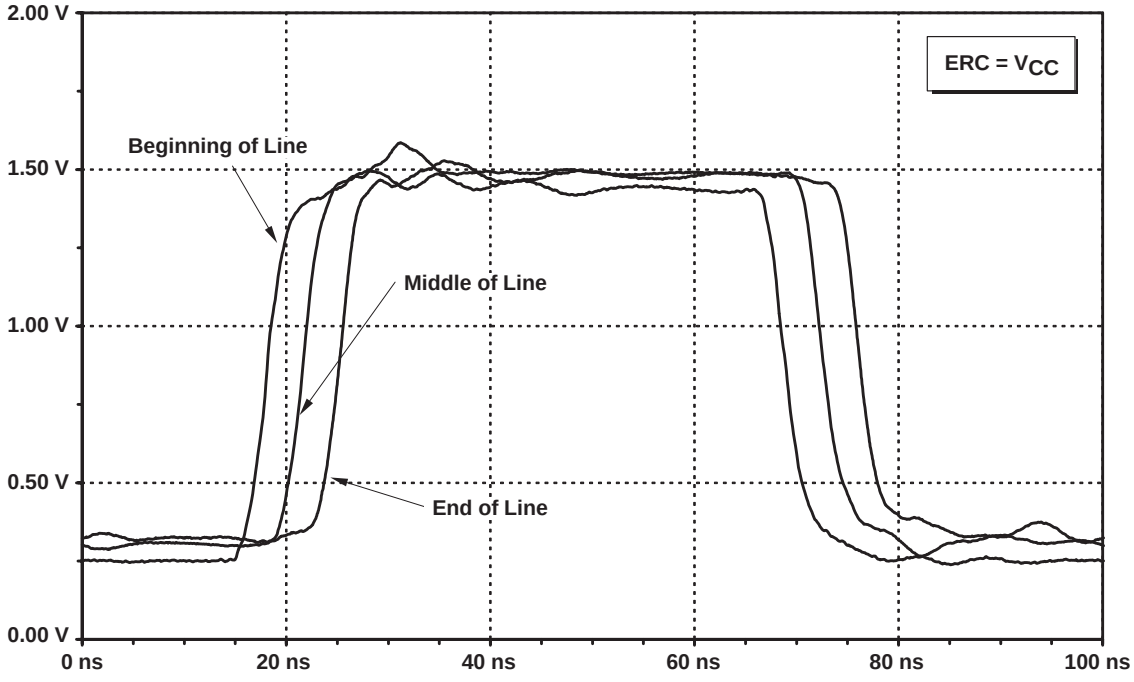

Figure 42. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 10 MHz

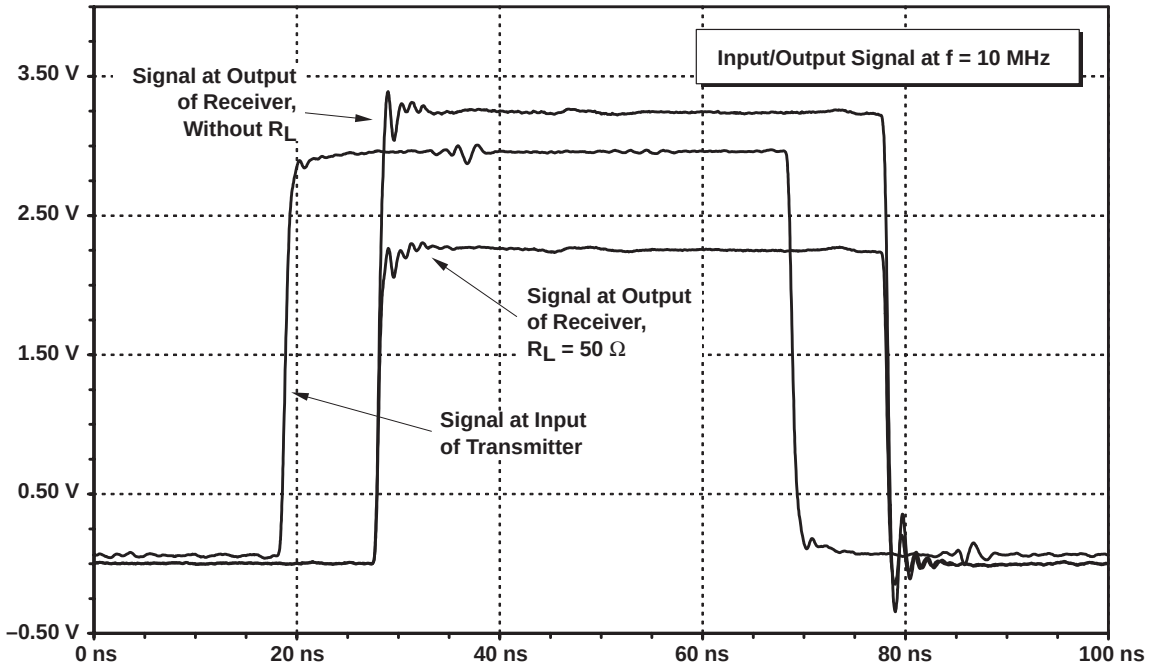

Figure 43. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 10 MHz

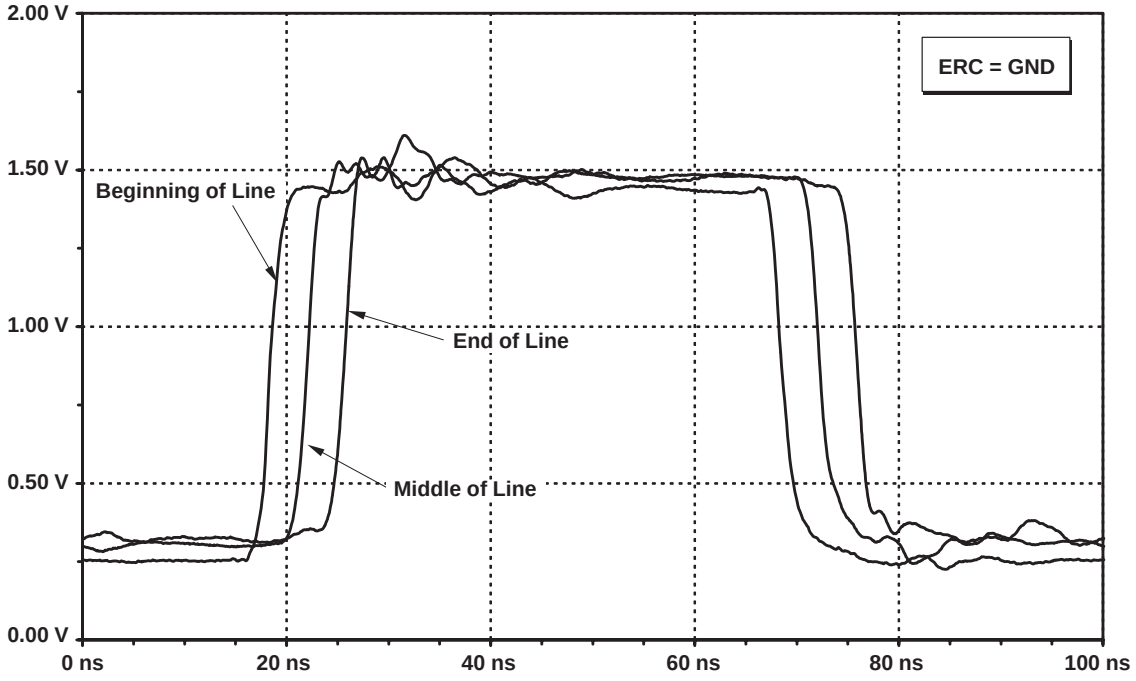

Figure 44. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 10 MHz

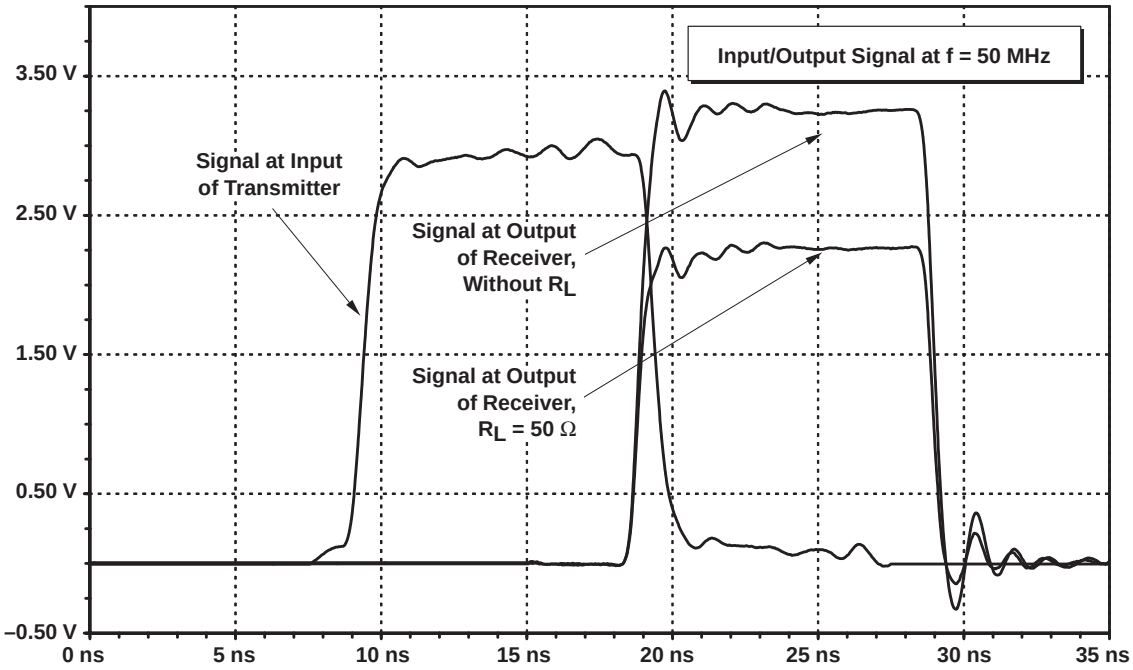

Figure 45. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 50 MHz

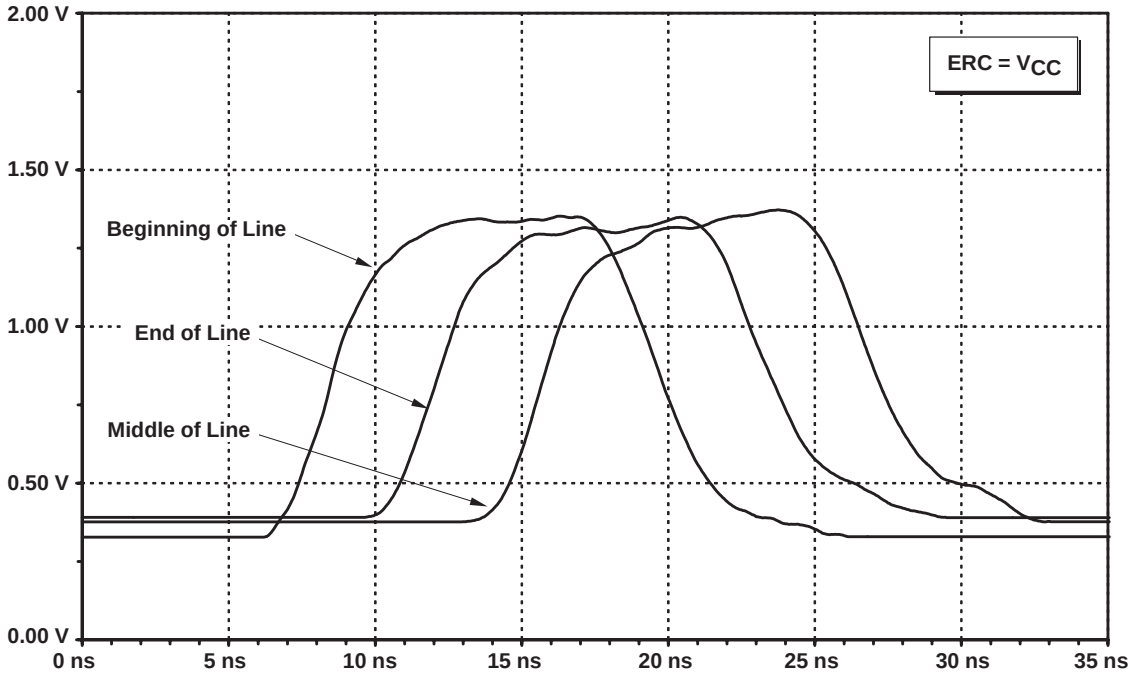

Figure 46. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 50 MHz

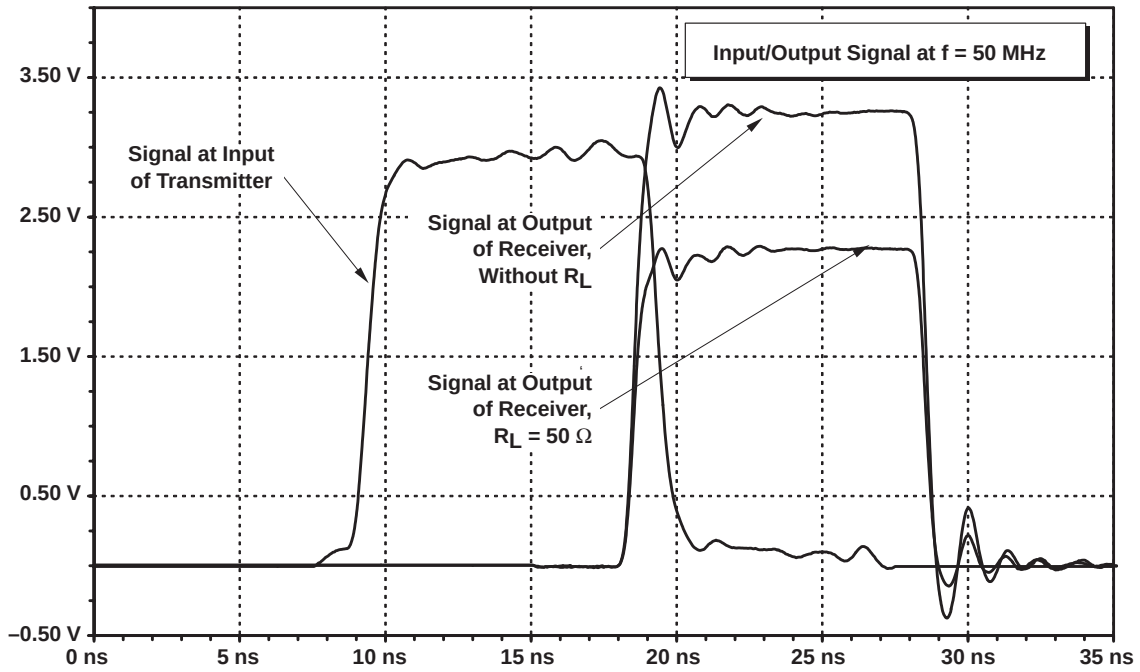

Figure 47. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 50 MHz

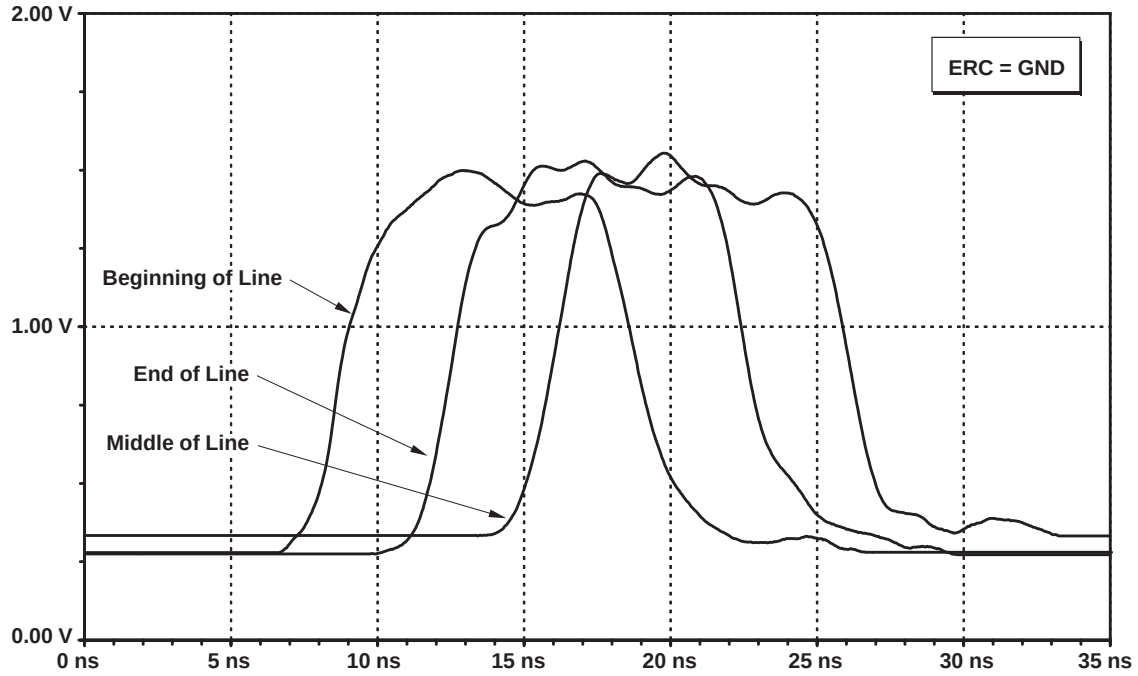

Figure 48. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 50 MHz

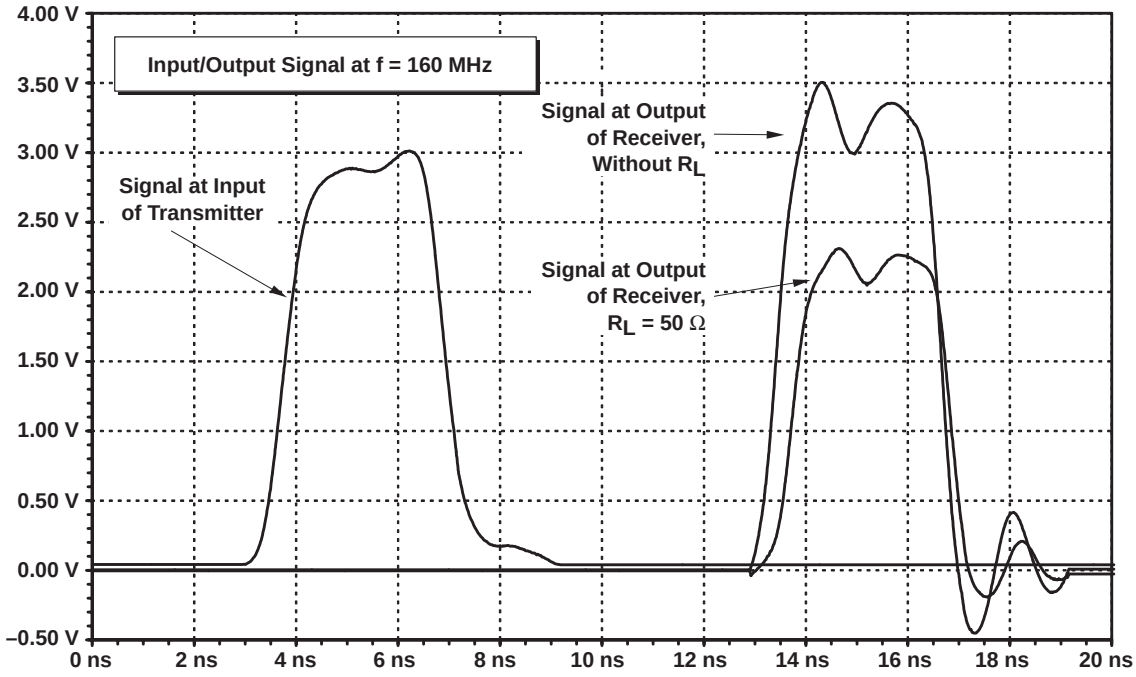

Figure 49. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = V_{CC}, Loaded, 160 MHz

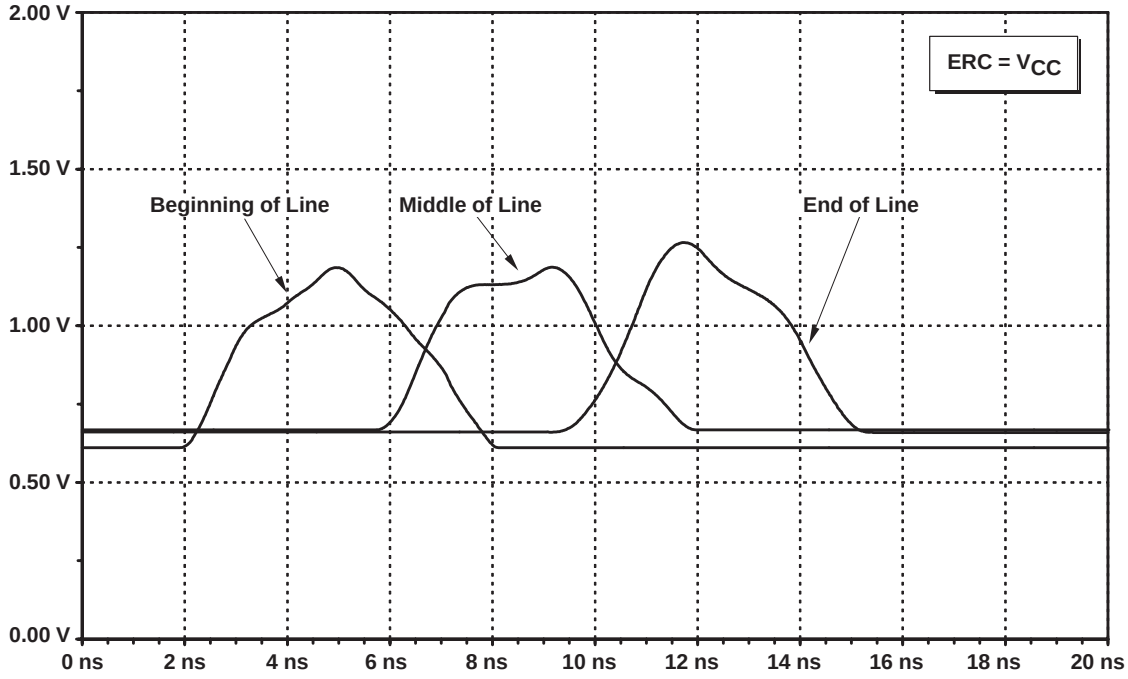

Figure 50. GTLP Bus Signal, Slow Rise and Fall Times, ERC = V_{CC}, Loaded, 160 MHz

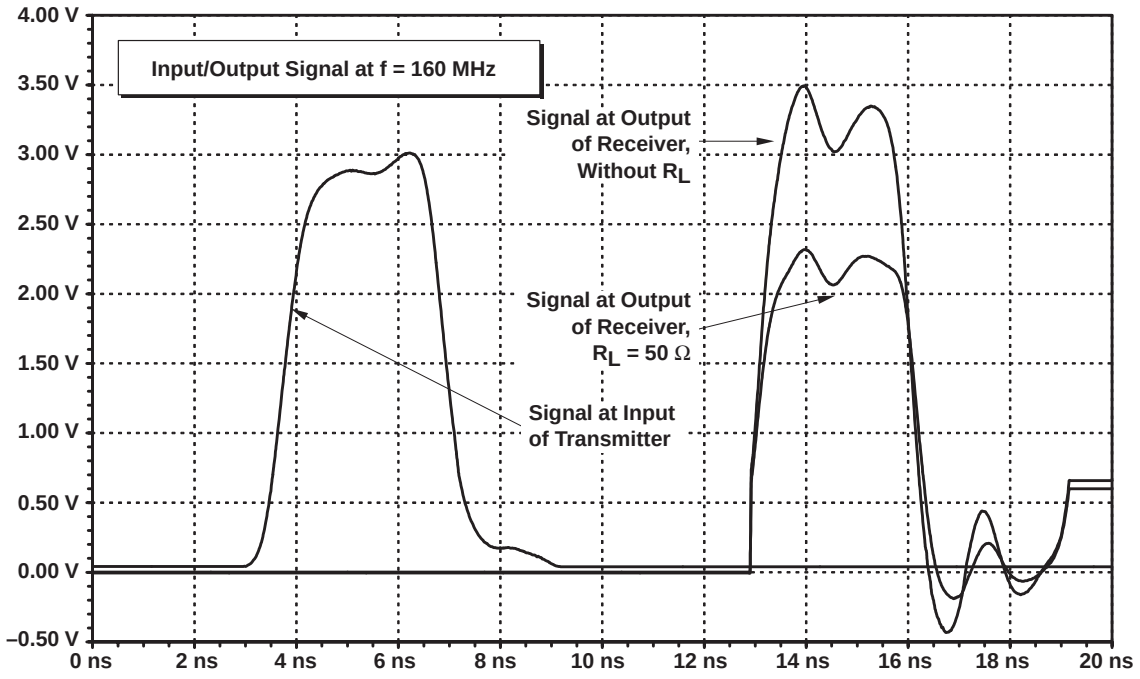

Figure 51. LVTTL Input and Output Signal of SN74GTLPH1655, ERC = GND, Loaded, 160 MHz

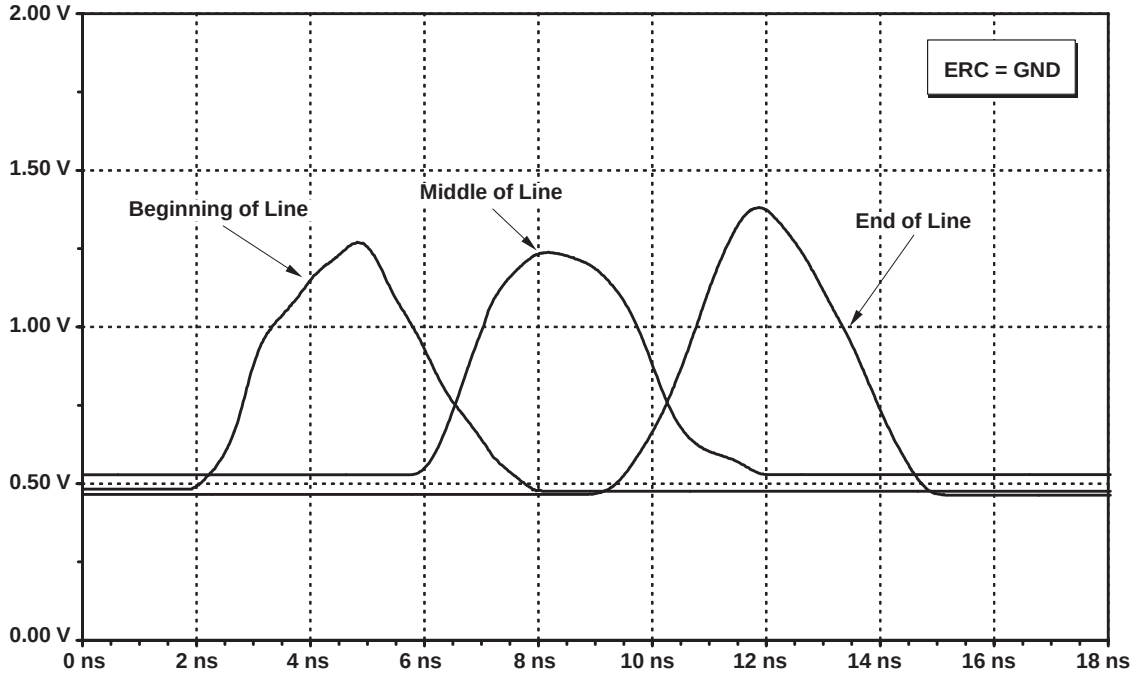

Figure 52. GTLP Bus Signal, Fast Rise and Fall Times, ERC = GND, Loaded, 160 MHz

Summary

The SN74GTLPH1655 from TI provides engineers who develop fast and complex bus systems with a high-performance bus driver that is particularly suitable for the design of modern low-voltage systems.

Very high signal-propagation speeds are possible, as a result of the increased drive capability of 100 mA, compared with standard GTL circuits (40 mA), and the selectable edge rate. Bus lines with low line impedances of about 22 Ω can be used with the SN74GTLPH1655.

Bus lines with low line impedances of about 22 Ω can be matched using GTLP drivers that have a four-digit identifier, such as the SN74GTLPH1655. The four digits indicate the high drive capability of I_{OL} = 100 mA, while all other GTLP devices have a drive capability of 50 mA.

The four-digit GTLP devices allow optimum termination of low-impedance bus lines, thereby preventing interference and signal distortion that may otherwise occur as a result of line reflections. Reduced signal-voltage amplitude improves signal integrity.

The power-up 3-state and precharge functions provided by the SN74GTLPH1655 and, also, the bus-hold cells at the input of the LVTTL side, allow the design of modern high-speed systems requiring minimum development effort.

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Glossary

BTL	Backplane Transceiver Logic
ERC	Edge-Rate Control
GND	Ground potential
GTL	Gunning Transceiver Logic
GTLP	Gunning Transceiver Logic Plus
I/O	Input/Output
Live insertion	Removal and reinsertion of modules during operation
LVTTL levels	3.3-V logic levels, compatible with TTL logic levels
Partial power down	Switching off parts of a system that is in operation without removing them from the system
Precharge	Charging I/O pins to the threshold voltage
TTL	Transistor-Transistor Logic
V_{CC}	Supply voltage

High-Performance Backplane Design With GTL+

SCEA011A
October 1999

Texas Instruments

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Contents

List of Illustrations

Abstract

Results from a system that demonstrates the performance of GTL+ devices in a backplane are provided. The Texas Instruments (TI™) GTL16622A is the example used in the design of the physical backplane. The TI backplane demonstration system is a useful tool for designers in understanding issues related to loading effects, termination, signal integrity, and data-transfer rate in a high-performance backplane environment. Simulation results are compared to laboratory measurements to validate the performance of TI GTL+ devices, and simulation results for the new TI GTL16612A in a very high-performance backplane are provided.

Introduction

High-performance backplane is becoming common terminology in the rapidly evolving data-communications market. Designers are developing innovative methods for multiplexing data to achieve higher throughput on the system bus or backplanes. High-speed backplanes that can handle large amounts of data are extremely important to high-performance systems.

The backplane is a physical and electrical interconnection between various modules in a system. Each module in the backplane communicates with other modules through the backplane bus. The backplane traces and the load capacitance affect signal integrity.

The discussion of the backplane demonstration system in this application report describes the various issues that should be considered while designing a backplane. The type of termination, backplane topology and layout, connector capacitance and stub lengths, along with the effect of the number of loads, all are investigated in this report. This report explains a demonstration backplane and its elements, followed by results that have been obtained using the TI GTL+ devices. HSPICE, a simulation tool, is used to model the performance of the system and to compare it to the hardware.

Background

In the past, increased throughput was achieved by increasing the frequency, or clock rate, or by increasing the bit width of the bus. Logic families that were used as backplane drivers included Advanced BiCMOS Technology (ABT), Fast CMOS Technology (FCT), Advanced CMOS Technology (ACT) and Backplane Transceiver Logic (BTL). These backplane drivers do not perform well in backplanes operating at frequencies over 33 MHz, but are sufficient for lower throughput requirements. With the trend toward higher system bandwidth requirements, into the hundreds of multimegabits per second, using a technology that supports these higher performance requirements is essential.

These increased speeds and performance requirements in designs created a need for higher-speed devices. Newer technologies developed by TI have helped to create devices that can drive these high-performance backplanes.

GTL/GTL+

Gunning Transceiver Logic (GTL), a technology invented by William Gunning at Xerox Corporation and standardized by JEDEC, was a low-swing input/output (I/O) driver technology that helped address these high-performance requirements. This technology was further modified by Intel™ and TI by increasing the voltage swing to create the GTL+ switching standard (see Figure 1). Subsequently, the standard was used by TI and Fairchild to create stand-alone devices to drive backplanes.

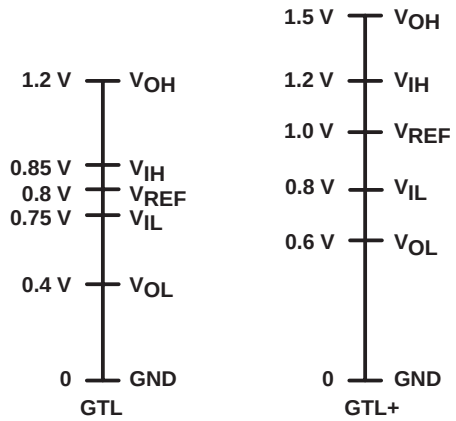


Figure 1. GTL/GTL+ Switching Levels

GTL+ achieves high performance with the help of the low signal voltage swing.[1] The typical swing for GTL+ is from 0.6-V low (V_{OL}) to 1.5-V high (V_{OH}) maximum. TI uses tighter threshold regions, V_{IH} at 1.05 V, V_{IL} at 0.95 V, and V_{OL} at 0.55 V, to provide better signal integrity in its stand-alone devices. This report demonstrates the performance of the newest TI GTL+ devices operating at clock rates of 100 MHz, providing bit rates of up to 10 Gbit/s in a 100-bit-wide backplane bus.

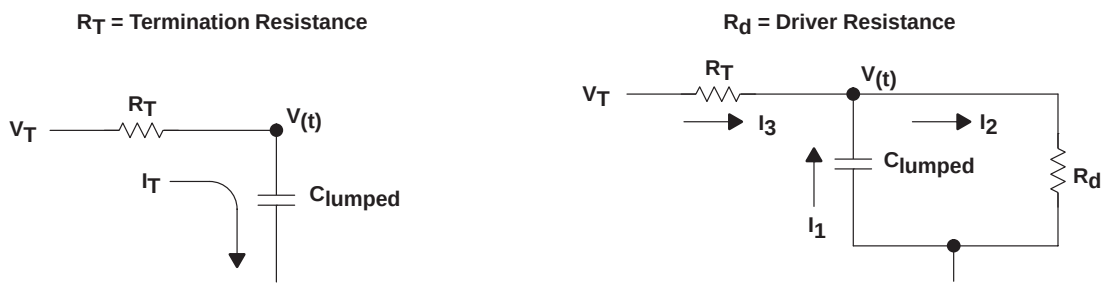
The TI GTL family offers edge control, which reduces signal noise and electromagnetic interference (EMI). The basic GTL output structure is an open-drain transistor, whereas the input is a differential receiver.[2] Also, the GTL I/Os have been designed to minimize their capacitance, an extremely important factor for distributed-load high-performance backplanes.

Backplane Design Considerations

This section covers the electrical elements of the backplane. The backplane bus connects the different modules in a backplane. The wires and traces on the bus and the traces on the modules are electrical elements that are a connection point for the various electrical modules. It is necessary to understand these electrical elements (such as impedance, capacitance, inductance, termination, connectors, stub lengths, vias, and driver and receiver characteristics) to design a successful backplane.

All of the above parameters contribute to the performance of the backplane. Backplanes can be categorized as low performance, medium performance, or high performance. A low-performance backplane can be modeled as a lumped load; medium- and high-performance backplanes must be viewed as a distributed load, by applying transmission-line theory.

With a low-performance backplane, the backplane driver sees the load as a lumped capacitance. The capacitive load in many cases is still distributed; however, it is modeled as a lumped load. This lumped model is used where the rise time of the signal is small compared to the transition time along the backplane. Here, only the final state matters, and bus performance is not the highest concern. The lumped capacitance is charged or discharged by the driver (see Figure 2) and is controlled by the RC time constant. The low-to-high signal transition is indicated by $1 - e^{-t/RC}$ and the high-to-low signal transition is of the form $e^{-t/RC}$. This lumped capacitance is referred to in the industry as a lumped load.



$$V_{(t)} = V_T\left(1 - e^{-t/RC}\right)$$

$$V_{(t)} = V_T\left[\frac{R_d}{R_d + R_T} + \left(\frac{R_T}{R_d + R_T}\right)e^{-t/RC}\right], \text{ where } R = \frac{R_T R_d}{R_d + R_T}$$

Figure 2. Lumped-Load Effects

Medium- and high-performance backplanes can be modeled as a distributed load. This is because performance drives a multidrop architecture, where the capacitance is distributed over the length of the backplane. To design an optimized medium- or high-performance backplane, a few concepts must be understood. These include the characteristic impedance of the backplane, (Z_o), the characteristic delay per unit length (τ_o), and the reflection coefficient (ρ), defined as the ratio of the amplitude of the reflected wave to the incident wave.

Figure 3 shows the transmission line as a distributed inductance and capacitance. The backplane driver charges the capacitance and is delayed by the inductance along the line. The signal sees the line as a characteristic impedance, given as:

$$Z_o = \sqrt{(L_o/C_o)} \quad (1)$$

Where:

L_o, C_o = distributed inductance and capacitance per unit length

The current flowing into the transmission line is of the form:

$$I = V_{in}/Z_o \quad (2)$$

The transition time or the time it takes for the signal to travel along the transmission line is:

$$\tau_o = \sqrt{(L_o/C_o)} \quad (3)$$

The intrinsic per-unit delay along the line is multiplied by the distance to give the overall delay across the line.

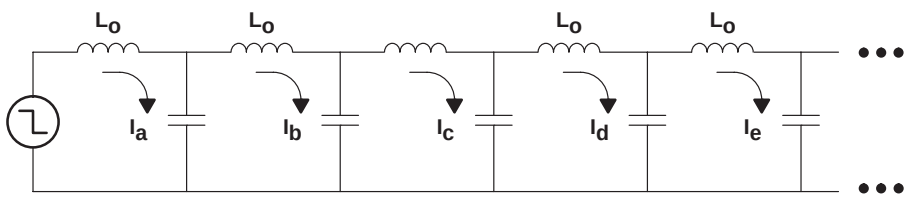


Figure 3. Transmission Line

The connectors on the backplane connect the backplane traces to branch transmission lines called stubs. These stubs are the communication ports between the backplane and the plug-in modules. These stubs, which have inductance and capacitance, change the overall impedance of the transmission line, and affect the signals that feed into the plug-in modules. This lumped capacitance changes the impedance and delay constants along the line by the following relationships:

$$Z_L = Z_o/\sqrt{(1 + C_d/C_o)} \quad (4)$$

$$\tau_d = \tau_o\sqrt{(1 + C_dC_o)} \quad (5)$$

Where:

C_d = added capacitance per unit length
C_o = intrinsic capacitance (as defined previously)

A point on the backplane where the impedance changes is called a discontinuity. A discontinuity on a backplane can occur if the drivers are placed too far from the backplane, there is improper termination, or the driver and receiver characteristics are not properly matched. At each point where a voltage wave that travels down the backplane meets a discontinuity, some of the signal is reflected, while the rest is transmitted along the backplane. The reflection coefficient determines the amount of signal that is reflected and is defined as the ratio of the reflected wave to the incident wave.

Figures 4 and 5 show the effects described above by using the GTL16622A to drive lumped and distributed loads, respectively. The lumped load consists of 25 Ω to 1.5 V, 30 pF to GND, whereas, the backplane (distributed load) consists of 16 slots separated by 0.875 in. Each load is approximately 14 pF.

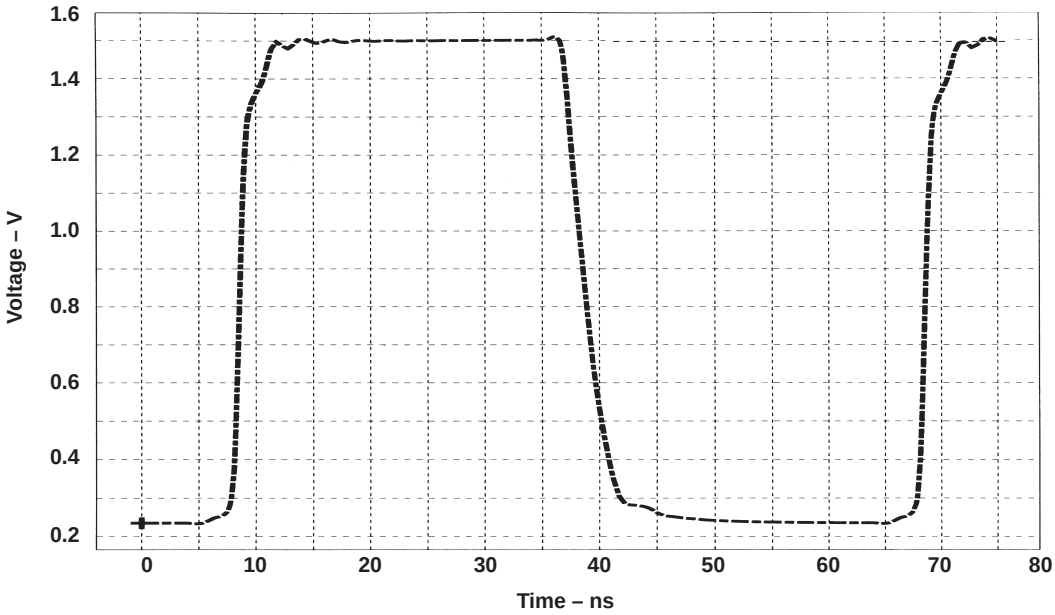


Figure 4. GTL16622A H-SPICE Simulation (Lumped Load, 33 MHz)

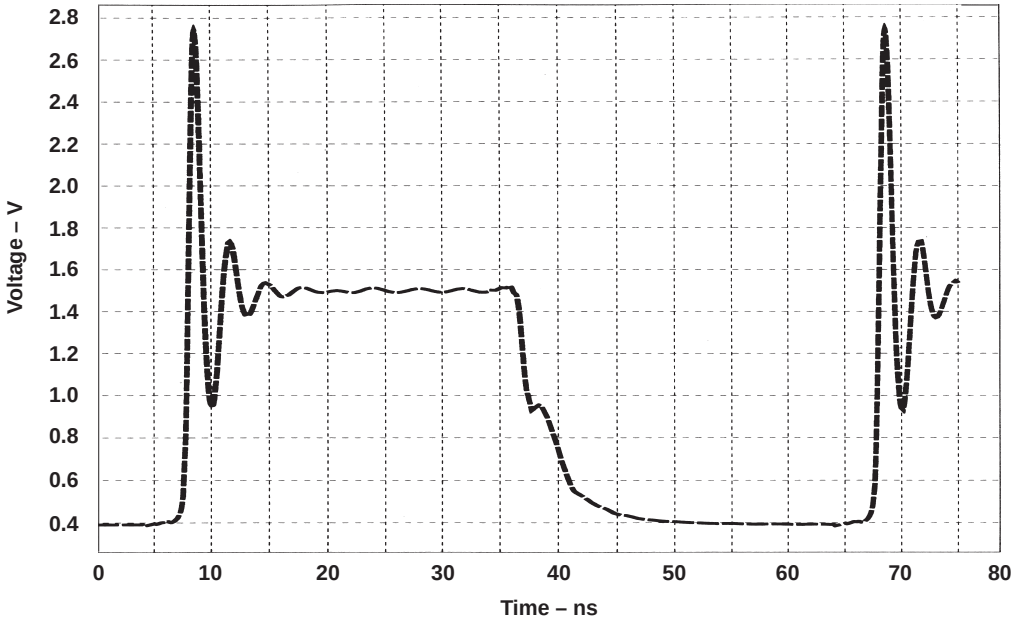


Figure 5. GTL16622A H-SPICE Simulation of a Backplane (Distributed Load, 33 MHz)

The added capacitance and inductance in the distributed load cause reflections that result in problems that include reduced noise margins.[3] In this case, the signal on the bus must settle before being sampled, hence, the bus settling time is required before valid data can obtained. Table 1 shows the comparison for the noise margins obtained for GTL and GTL+. GTL+ provides a wider noise margin than GTL, an important factor for designing signal-integrity-critical applications. In high-performance backplane designs, termination voltage, bus impedance, termination resistance, stub lengths, and driver and receiver characteristics must be controlled carefully to achieve good signal integrity, so that valid data can be presumed at the incident wave of the signal.

Table 1. Noise-Margin Comparison

DEVICE TYPE	NOISE MARGIN (mV)	
	UPPER	LOWER
GTL	350	350
GTL+	450	400

Another issue to consider in backplane design is crosstalk. Crosstalk, an effect of capacitive coupling in backplanes, can also result in false switching. Crosstalk between signal lines can be approximated as being inversely proportional to the distance between the signal lines and directly proportional to the distance between the signal lines and the ground plane. The most popular technique used to avoid crosstalk is fine-line technology that increases the distance between the signal lines while decreasing the distance between the signal line and the reference plane.

Backplane Demonstration System

The TI backplane demonstration board represents a typical industry backplane. The following section explains the elements of the demonstration backplane.

Architecture

Backplane Driver/Receiver (GTL16622A)

The GTL16622A 18-bit LVTTL-to-GTL/GTL+ bus transceiver translates between GTL/GTL+ signal levels and LVTTL or 5-V TTL signal levels. The device supports mixed-mode signal operation (3.3-V and 5-V signal) on the A port and control pins and is hot insertable with an output drive capability of 50 mA.[4] The device is used as both the driver and the receiver on the individual plug-in modules in the backplane.

Backplane Motherboard

The TI backplane demonstration board was constructed after studying various backplane loads. The 36-bit backplane consists of 14-in. traces with 16 slots separated by 0.875-in. pitch. Figure 6 shows the physical layout of the backplane board and its elements. The power supplies are represented as PS1 (5 V) and PS2 (3 V) and connectors by points P1 to P16. The connectors host the driver/receiver cards.

The clock drivers are U1, U2, and U3. U1 and U2 each distribute the clock to eight loads, while U3 is configured to supply the data at one-half the clock rate. The crystal oscillator (X1) supplies the clock and the data to the backplane board. The crystal oscillator can be changed to configure the clock rates at any frequency. The frequencies that have been used to test the demonstration board are 50 MHz, 66 MHz, 80 MHz, and 100 MHz. One of the plug-in cards is a driver, while the remaining cards are receivers. The GTL16622A is used as both driver and receiver. The position of the driver card on the backplane can be varied to study the loading effects and signal integrity on the backplane.

The 1.5-V termination voltage (V_{TT}) for GTL+ is from a 5-V regulated power supply. The 3.3-V power supply provides power to the GTL device on board. The voltage reference, V_{REF}, is generated from V_{TT}, using a simple voltage-divider circuit with an appropriate bypass capacitor (0.1 µF) placed as close as possible to the V_{REF} pin.[2] TI recommends placing the voltage-divider circuitry on each daughter card, because this eliminates the noise introduced by the backplane trace.

The intrinsic, unloaded, backplane trace impedance is 50 Ω and has a loaded impedance of 25 Ω with 16 loaded slots. The backplane is dc terminated using a 25-Ω resistor to V_{TT} to match the loaded impedance of the backplane. The 36-bit backplane is used to transmit data from the driver to each receiver card at the frequency of the crystal oscillator.

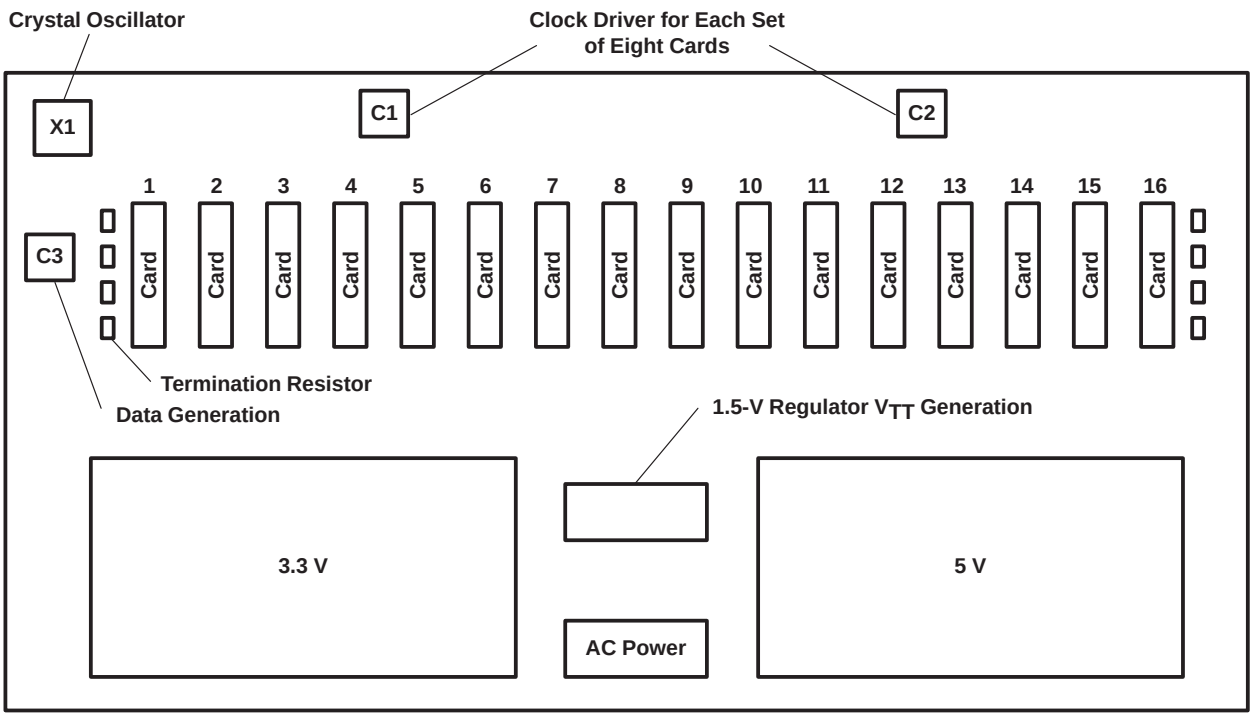


Figure 6. Backplane Demonstration Board Physical Layout

Interconnect and Impedance Calculations

Figure 7 is a graphical summary of the network that provides the physical dimensions of the backplane. Each element introduces additional capacitance on the board, which increases the loading on the backplane, eventually affecting signal integrity. The physical representation of the demonstration backplane shows the slots separated by 0.875 in. of backplane trace (B). There is a 0.0625-in. stub between the backplane trace and the connector (C), followed by approximately 1 in. of microstripline card stubs (D), and a total stub length of 1.0625 in. (as shown in the impedance calculator in Figure 8).

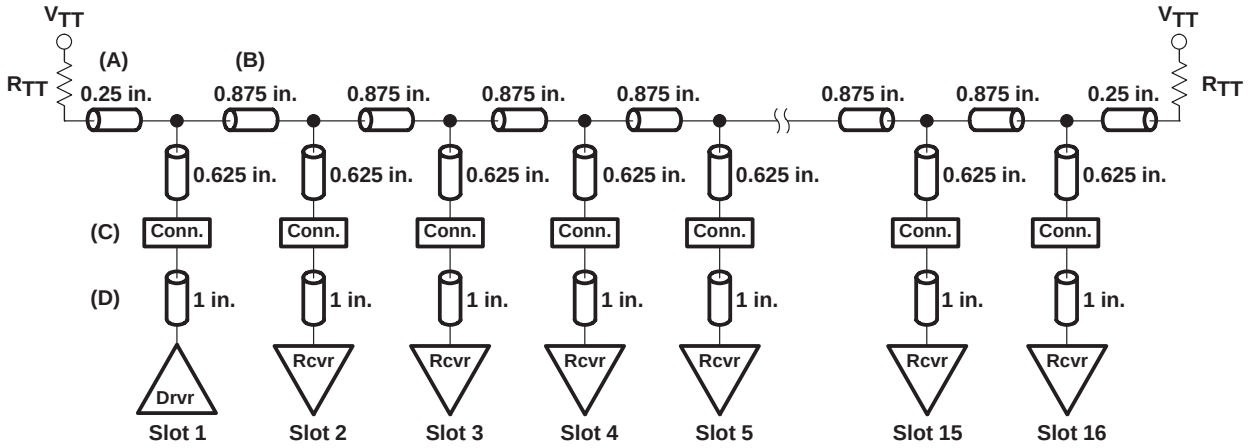


Figure 7. Backplane Physical Representation

Unloaded Line Impedance

		Inputs			Outputs	
Line	Z_o =	50.00		L_o (pH) =	10250.00	/in.
Line	C_o (pF) =	4.10	/in.	t_{pd} (ps) =	205.00	/in.
Device	C_{io} (pF) =	6.00				
Load Spacing	D1 (in) =	0.875		C_t (pF) =	10.96	
Stub Length	D2 (in) =	1.0625		C_d (pF) =	12.53	
Stub	C_o (pF) =	2.60	/in.			
Connector	C_C (pF) =	0.70				
Connector Pads	C_P (pF) =	1.00				
Via	C_{via} (pF) =	0.50				

Effects of C_d on Impedance (Loaded)

t_{pd} (ps) =	412.85	/in.	Z_o (eff) =	24.8	R_T

Figure 8. Impedance Calculator

The impedance calculator is a spreadsheet that is created using the previous equations to show the effects of distributed capacitance. The spreadsheet shows that the initial impedance of the 50-Ω backplane trace introduces a delay of 205 ps/in. (see equation 3) and has a C_o of 4.1 pF/in. The introduction of backplane loads increases the distributed capacitance (C_d) to 12.53 pF/in., which increases the propagation delay (t_{pd}) to 412.85 ps/in. and reduces the backplane impedance to 24.83 Ω (see equation 4). The backplane loading is a factor of the input/output capacitance of the driver or receiver (C_{io}), stub capacitance, via capacitance, and connector capacitance. Both ends of the backplane trace are terminated by a stub (A), using a 25-Ω pullup resistor to the termination voltage (V_{TT} = 1.5 V).[5]

Results

Laboratory data were taken using the demonstration backplane and compared to HSPICE simulation results to validate the performance of the GTL16622A on the backplane. Figure 7 is the reference to give the position of driver and receiver cards in the backplane. Results for TI's newest addition, the GTL16612A, demonstrate the throughput capability in a very high-performance backplane.

Laboratory

Figure 9 shows the laboratory results for the GTL16622A, with all 36 bits switching on the fully loaded backplane board with the driver card in slot 1. The worst-case signal was observed in the receiver card closest to the driver card (slot 2), while the best-case signal was seen in the receiver card farthest from the driver (slot 16). The throughput obtained at 50 MHz is 1.8 Gbit/s.

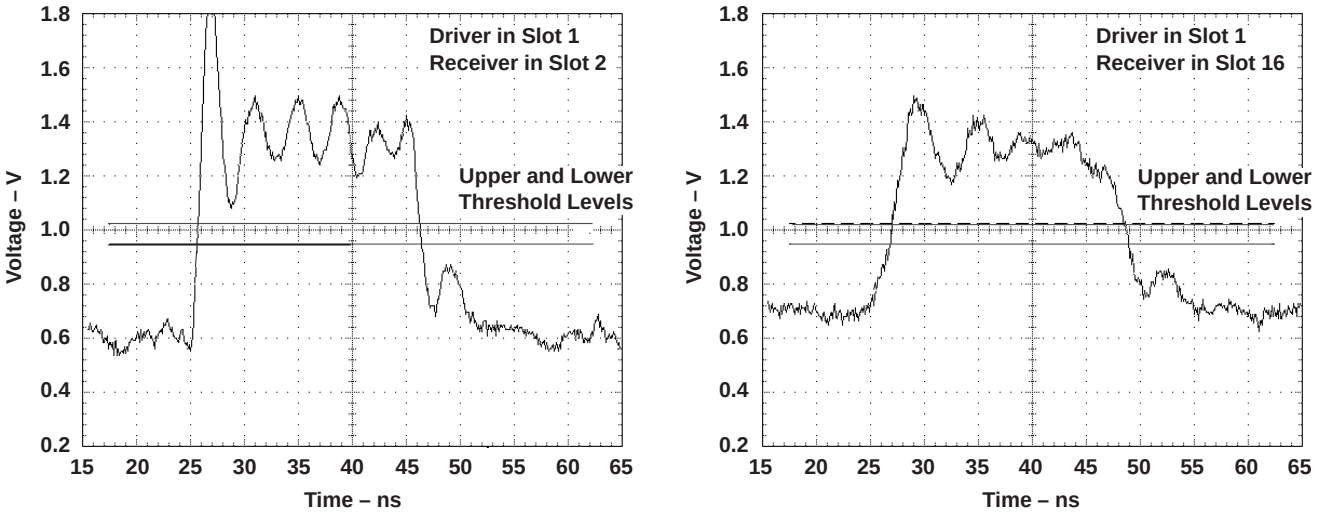


Figure 9. GTL16622A Signal Integrity (Laboratory Results)

Simulation

Figure 10 shows the HSPICE simulation results for the GTL16622A, which correlate closely with results observed in the laboratory with the demonstration hardware. The simulation results are observed after modeling the backplane using HSPICE for single-bit switching.

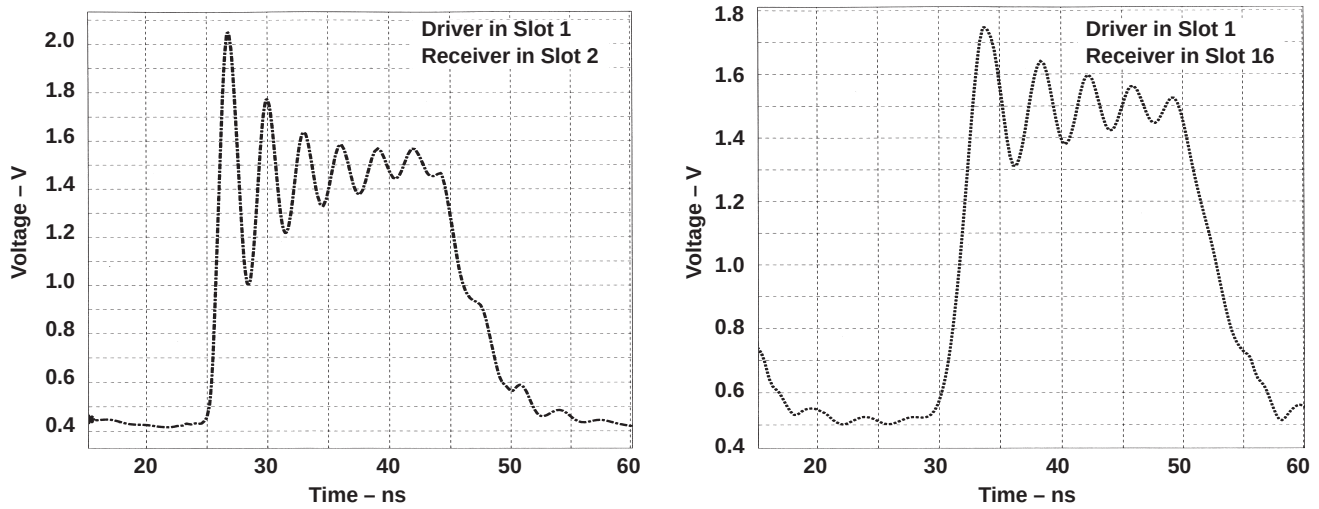


Figure 10. GTL16622A Signal Integrity (HSPICE Simulation Results)

The slot closest to the driver (slot 2) shows the worst-case ringing because it sees the fastest rise time of the IC driver compared to the slots that are farther away from the driver. The worst-case signal at slot 2 also is due to the effect of reflected energy that is maximum in the receiver closest to the driver.[3]

Correlation

Figure 11 shows laboratory versus simulation results for the GTL16622A on the demonstration board. The results shown are for the receiver at slot 2 (closest to the driver card). Here, as the frequency is increased, the time available for the data to be sampled decreases, making good signal integrity necessary at these high frequencies.

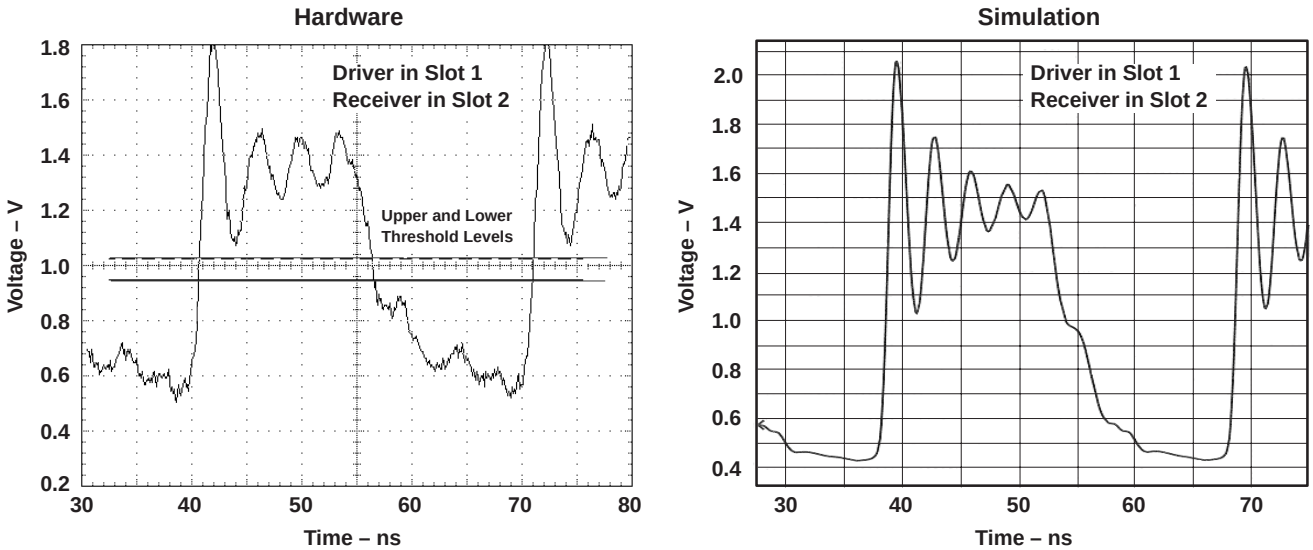


Figure 11. GTL16622A Signal Integrity (Hardware vs Simulation at 66 MHz)

Moving Forward With the GTL16612A

TI has continued to improve the characteristics and features of the GTL family to provide higher throughput rates at backplane frequencies up to 80 MHz. These higher frequencies allow designers to transmit increased amounts of data on their board, achieving high bit rates in their systems. The newest device in the GTL family, the GTL16612A, an improved version of the GTL16612, is capable of operating at frequencies as high as 80 MHz. The features of this device include output edge control (OEC™) on the rising and the falling edge, and optimization for high-performance distributed-load applications. Simulation results that provide a comparison between the GTL16622A and the GTL16612A are shown in Figures 12 and 13 at 50 MHz and 66 MHz, respectively.

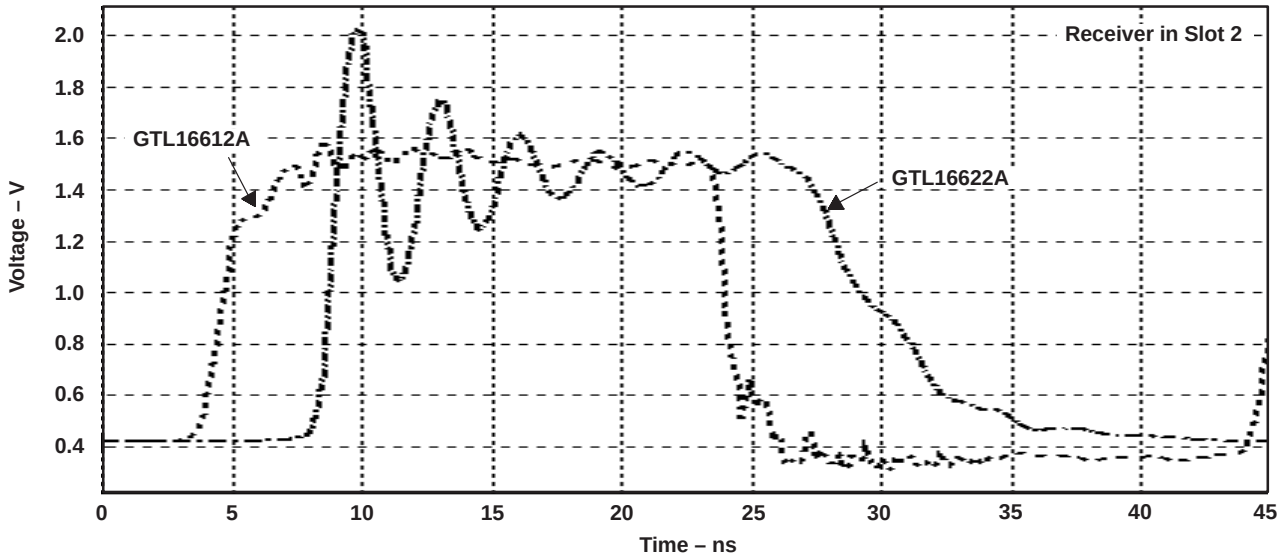


Figure 12. GTL16622A vs GTL16612A (50 MHz)

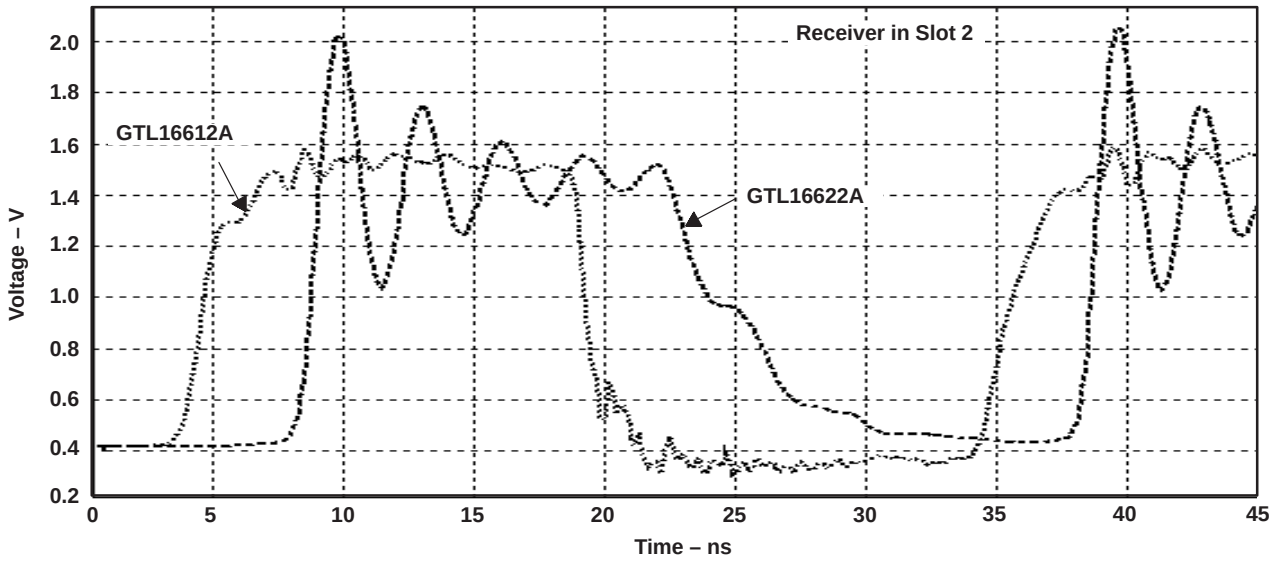


Figure 13. GTL16622A vs GTL16612A (66 MHz)

OEC is a trademark of Texas Instruments Incorporated.

Figure 14 shows simulation results for the GTL16612A operating at high clock rates of 80 MHz and 100 MHz. The innovative design of the 18-bit device provides for extremely high throughput on a backplane if the timing requirements of the board can be met.

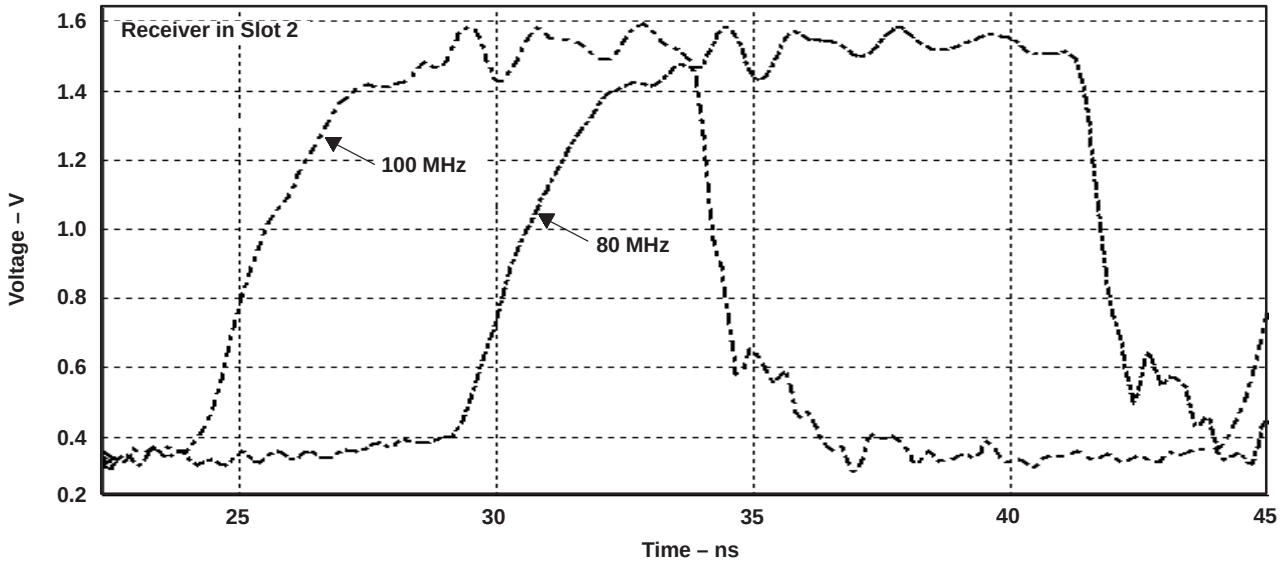


Figure 14. GTL16612A Simulation Results at 80 MHz and 100 MHz

Summary

The demonstration board has clarified backplane design issues and has provided unique insight into the capability of the GTL+ technology. With the escalation of requirements for high-speed data transfer, and a transition from low and medium performance to high performance, the backplane will be a critical component in the performance equation. The TI GTL16622A has served as a backplane driver for medium- and high-performance applications, while the new GTL16612A overcomes the problems in a very high-performance backplane to provide good signal integrity. Clearly, GTL+ is the next-generation technology, capable of accurately moving large amounts of data on the backplane with high speeds, while achieving the bit rates that will be required by new designs.

Acknowledgment

The authors of this application report are Shankar Balasubramaniam, Ramzi Ammar, and Ernest Cox.

The authors recognize the contributions and assistance provided by Adam Ley, Gene Hintershcer, and Mac McCaughey.

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2 Texas Instruments, *GTL/BTL: A Low Swing Solution for High Speed Digital Logic* application report, literature number SCEA003, September 1996.

3 Vantis, *High Speed Board Design Techniques*, August 1997.

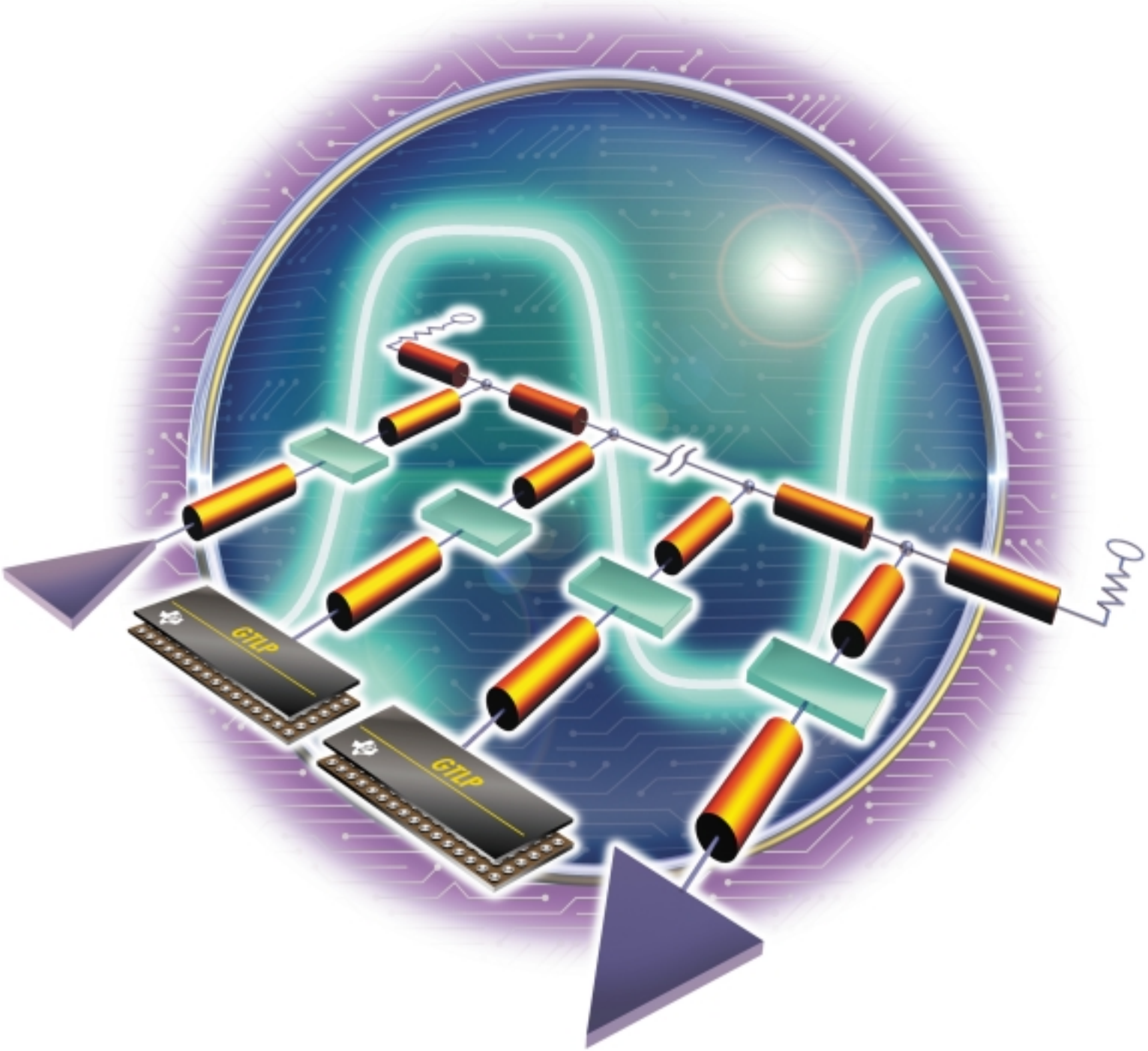
4 Texas Instruments, SN74GTL16622A data sheet, literature number SCBS673.

5 California Micro Devices, “Termination Techniques for High Speed Buses”, *Electronic Design News*, February 1998.

Glossary

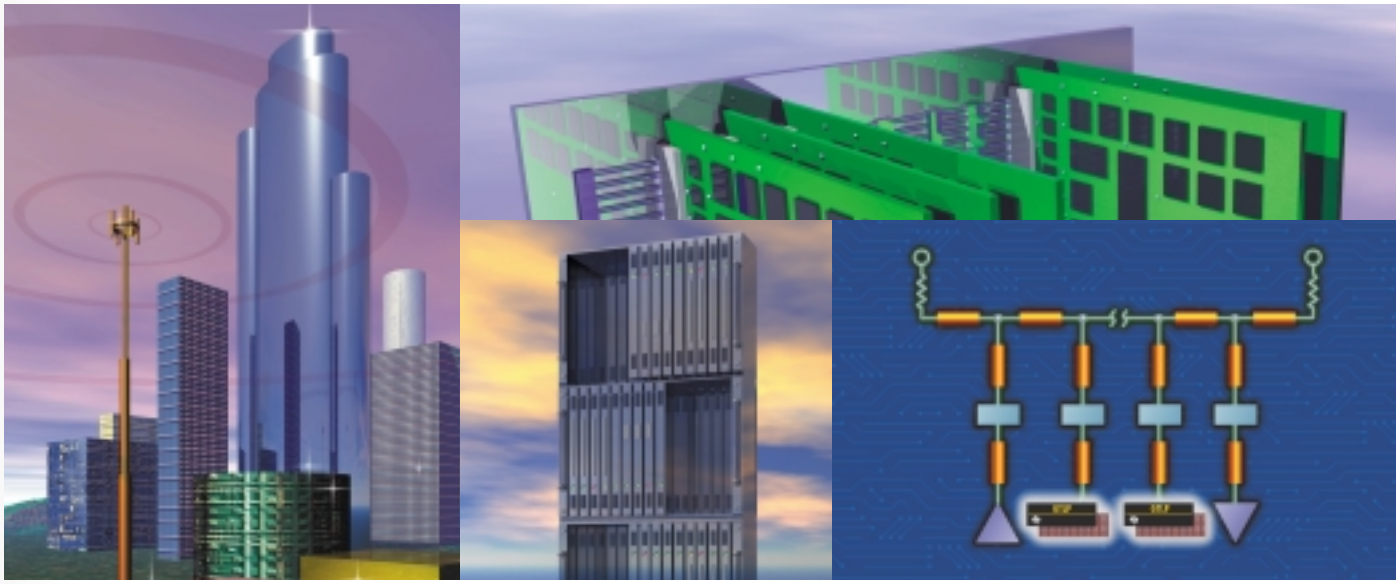
Incident-wave switching	Voltage transition that is strong enough to switch the input of the receiver on the first edge of the wave. This implies that subsequent reflections do not change the state of the receiver to its previous state.
Noise margin	Difference between the driver or receiver threshold voltage and the voltage on the bus. A noise margin comparison for the GTL/GTL+ technologies is shown in Table 1. The increased noise margin for GTL+ is preferred because it can result in better signal integrity.
Stub	Path on the board between the driver/receiver card and the backplane. This includes the trace on the board, the connectors, and the lumped capacitance of the driver or the receiver. The length from the driver/receiver to the backplane is the stub length.
Throughput	Data rate that is achieved on the bus or the backplane. It can be calculated on a parallel-bus architecture as the product of the number of bits and the frequency of transmission.

Increase the speed of parallel backplanes 3x with GTLP



For high-speed parallel backplanes, GTLP is the answer.

Users of the Internet, wireless communications or the traditional wireline infrastructure are clamoring for more bandwidth. As a result, the parallel backplanes used in switches, routers, hubs and other communications equipment is quickly evolving to faster speeds. GTLP logic is an easy first step toward higher data throughput.



Migrate to next-generation speed

In today's interconnected, bandwidth-hungry world, designers can easily increase by two to three times the data throughput speed of their networking, communications and telecommunications systems by migrating to TI's new GTL-Plus (GTLP) logic family for parallel backplanes. And since GTLP is backwardly compatible with traditional logic such as ABT, ALVT, LVT, LVC and FutureBus+, the migration to higher throughput is simple and direct.

Building upon its pioneering work with Gunning Transceiver Logic (GTL), TI has optimized the Output Edge Control™ circuitry and added live insertion and removal capabilities to produce devices specifically designed for medium and heavily loaded parallel backplanes.

GTLP brings the benefits of GTL – higher frequencies and lower EMI and transmission noise - to parallel backplanes in excess of 20 slots. Combining Output Edge Control circuitry with GTLP's narrow signal voltage swing gives GTLP clock speeds in excess of 80 MHz and data throughput rates of at least 3.2 gigabytes per second (Gbps) across a 32-bit backplane.

Improving on a good thing

In recent years, GTL logic has become increasingly popular in point-to-point applications and backplane systems with a limited number of slots. Now, GTLP brings the high-speed advantages of GTL to medium- and heavily loaded parallel backplanes.

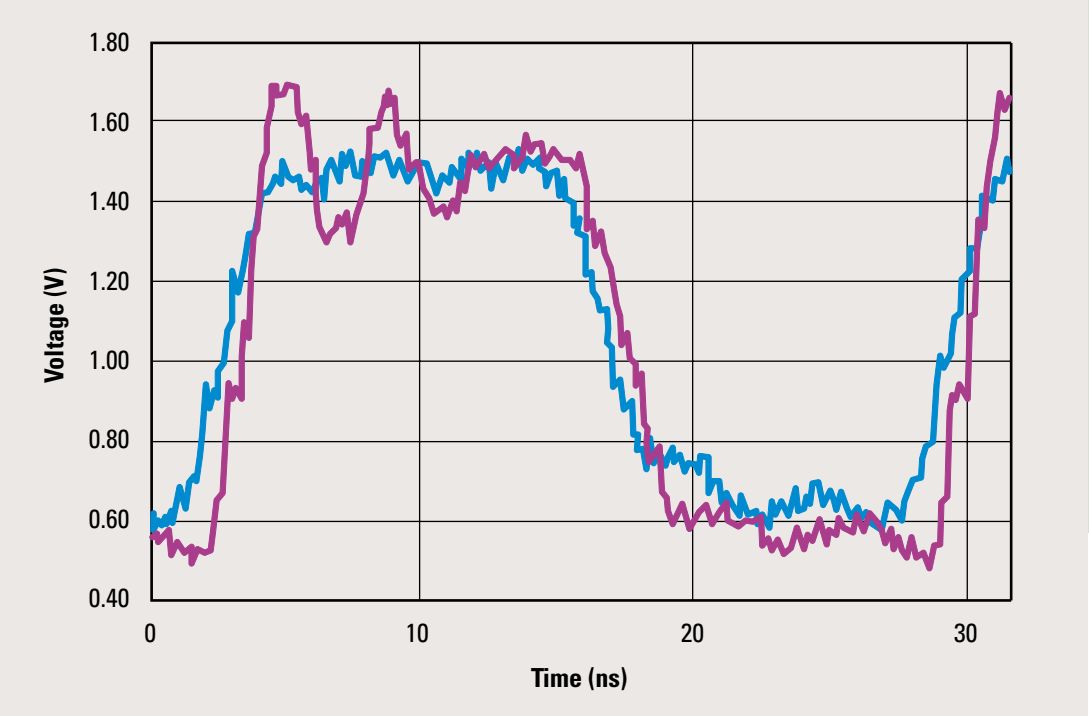
GTLP transceivers are differential input, open-drain n-channel devices. TI has optimized the Output Edge Control circuitry in GTLP transceivers to ensure good signal integrity (See chart below), reduce line reflections and limit the electromagnetic emissions at frequencies greater than 80 MHz.

GTLP devices have been optimized for a narrow signaling range between 0.55 and 1.5V with a threshold at 1.0V. Additionally, GTLP transceivers will operate at the GTL signal levels of 0.4 to 1.2V with a threshold at 0.8V.

GTLP transceivers are 3.3V CMOS devices, but they have 5V-tolerant LVTTL inputs and outputs which allows them to act as 5V-to-GTLP translators or 3.3V LVTTL-to-GTLP translators. As CMOS devices, GTLP transceivers consume less than a third of the power that is typical for BiCMOS GTL devices.

Designing GTLP transceivers into next-generation systems with significantly higher data throughput speeds is relatively easy because GTLP is backwards compatible with the logic currently used in parallel backplanes.

Output Edge Control (OEC™) Circuitry Comparison (V_{TT} = 1.5V)



Optimized OEC

Original OEC

The many packaging options as well as pin-outs that are similar to previous-generation devices simplify the designer's task.

Matching your backplane needs

For maximum flexibility in matching the needs of your backplane, the GTLP family comes in medium- and high-drive devices. High-drive devices sink 100 milli-Amperes (mA) of current, while medium-drive devices sink 50mA. Low impedance, heavily loaded backplanes achieve better data throughput performance with high-drive GTLP devices.

High-drive GTLP devices also feature TI's innovative variable edge rate control circuitry which allows you to adjust the signal's edge rate to better match the conditions of your backplane.

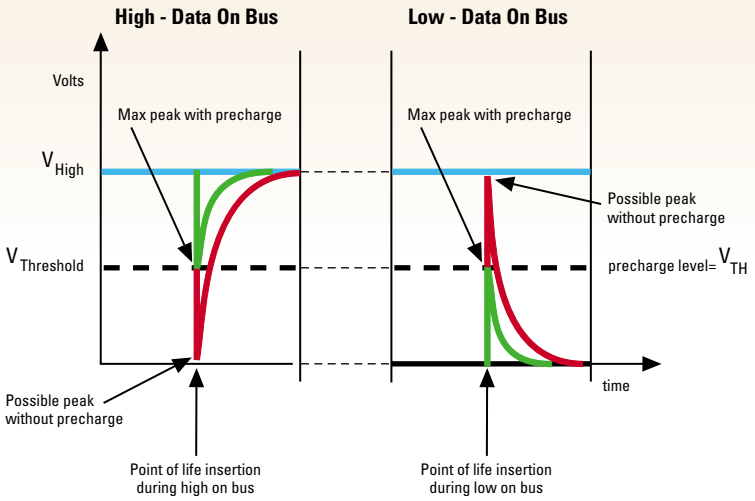
An Easy Migration

To help the designer make an easy migration to GTLP, this new logic family is fully supported with tools like application notes, application support, free samples, demonstration backplane models, and IBIS and SPICE simulation models.

Live board insertion

Many backplane systems are used in communication and networking applications where availability 24 hours a day, seven days a week (24/7) is a must. As a result, boards must be inserted or removed from the system while it is still running. TI has included three kinds of internal circuitry to accomplish fault-proof live insertion.

First, by including a blocking diode and removing a clamping diode, unexpected device behavior is eliminated when power is fully or partially removed. Second, new circuitry avoids driver conflict by ensuring that outputs are disabled during power up or down. And third, an internal pre-charging circuit prevents data corruption which can result from voltage spikes caused by inserting a board into a live backplane.



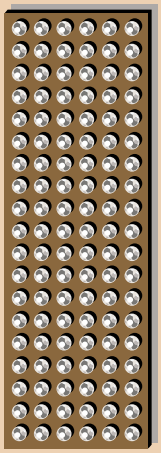
***For more information on the GTLP family of high-speed parallel backplane logic or to find out how TI can help you make the switch to GTLP logic, visit our web site at* www.ti.com/sc/gtlp *or to reserve a copy of our GTLP Product Information book visit* www.ti.com/sc/gtlpbook.**

GTLP Chip Configurations

GTLP Device	*LVTTL-to-GTLP Function*	*Pin Count*	*SOIC*	*SSOP*	*TSSOP*	*TVSOP*	*LFBGA*
		Medium Drive (50 mA)					
SN74GTLP817	GTLP to LVTTL 1 to 6 Fanout Driver	24	✔		✔	✔	
SN74GTLPH306	8-Bit Bus Transceiver	24	✔		✔	✔	
SN74GTLPH16945	16-Bit Bus Transceiver	48		✔	✔	✔	
SN74GTLPH16912	18-Bit Universal Bus Transceiver	56		✔	✔	✔	
SN74GTLPH32945	32-Bit Bus Transceiver	96					✔
SN74GTLPH32912	36-Bit Universal Bus Transceiver	114					✔
		High Drive (100 mA)					
SN74GTLP1394	2-Bit 3-Wire Transceiver	16	✔		✔	✔	
SN74GTLPH1645	16-Bit Bus Transceiver	56		✔	✔	✔	
SN74GTLPH1655	16-Bit Universal Bus Transceiver	64			✔		
SN74GTLPH1612	18-Bit Universal Bus Transceiver	64			✔		
SN74GTLPH3245	32- Bit Bus Transceiver	114					✔

The Pluses of GTLP

- Two to three times faster data throughput on heavily loaded parallel backplanes
- 3.2 gigabits per second (Gbps) with a 32-bit backplane
- Easy migration path from traditional backplane logic like ABT, FCT, LVT, ALVT, LVC or FutureBus+
- Live insertion of cards into GTLP backplanes for high-availability systems
- Wide selection of high drive devices
- Wide selection of packaging options
- Consumes one-third the power of BiCMOS GTL devices



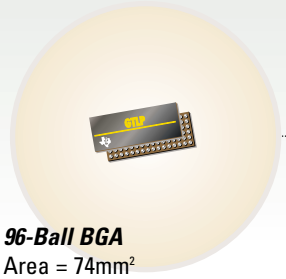
A wide range of GTLP packaging options is available to satisfy all design needs. TI's MicroStar BGA™ package reduces by 45 to 65 percent the board space needed for traditional surface mount packages.

With an easy migration to Texas Instruments' new Gunning Transceiver Logic-Plus (GTLP) family, designers can increase the data throughput of parallel backplane systems by 100 to 200 percent. GTLP extends the success of GTL logic in point-to-point applications to parallel backplane systems without requiring a radical redesign of the system.

And for high-availability systems in communications, telecommunications and networking, GTLP supports live insertion and removal of boards into a backplane.

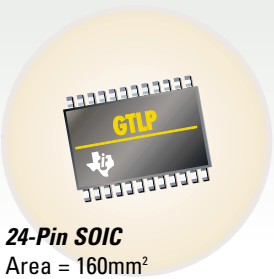
Three times the speed - That's what a simple migration to GTLP logic can do for your parallel backplane system.

Packaging Options



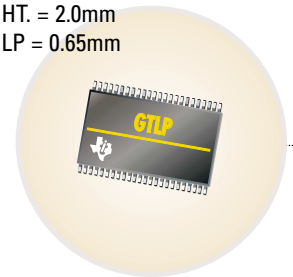
96-Ball BGA
Area = 74mm²
HT. = 1.4mm
LP = 0.8mm

114-Ball BGA
Area = 88mm²
HT. = 1.4mm
LP = 0.8mm



24-Pin SOIC
Area = 160mm²
HT. = 2.65mm
LP = 1.27mm

48-Pin SSOP
Area = 171mm²
HT. = 2.0mm
LP = 0.65mm



48-Pin TSSOP
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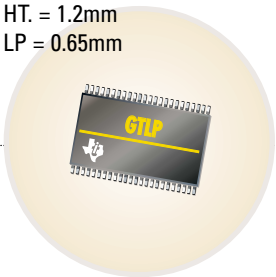
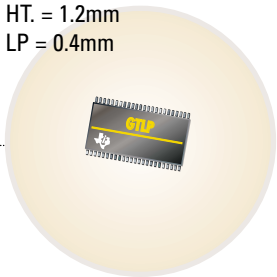
HT. = 1.2mm
LP = 0.65mm



48-Pin TVSOP
Area = 63mm²
HT. = 1.2mm
LP = 0.4mm



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Singapore	800-0111-111	-800-800-1450
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Application Report
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Texas Instruments GTLP Frequently Asked Questions

Steve Blozis
Standard Linear & Logic

ABSTRACT

Using a question-and-answer format, advantages of TI's GTLP devices, particularly for backplane applications, are presented, as well as differences between GTLP and GTL/LVDS devices. Applicable topics include data throughput rates, synchronous clocks, price and alternative sources, bus transceivers, live insertion, power consumption, backplane termination, voltage translation, IBIS and HSPICE models, and sample availability.

Table of Contents

Introduction

This information on GTLP and backplane design is presented in the frequently asked-question (FAQ) format. The GTLP FAQs allow the novice backplane user to learn more about parallel backplanes and allows the experienced backplane user to better design-in and use the higher performance of GTLP devices. Any questions not adequately addressed or applications you want highlighted can be sent to GTLP@list.ti.com for action and possible future insertion into the FAQs.

1 What is a backplane?

A backplane is a physical and electrical system bus that interconnects several printed circuit boards though a series of connectors. These buses can vary by the number of layers and traces and by electrical architecture. Generally, backplanes are passive, particularly in the telecom market, in which reliability concerns force designers to minimize the number of backplane components. Backplane transceivers/buffers drive data onto and receive data directed to PC boards located along the backplane.

2 What is a backplane protocol?

The protocol decides the electrical, logical, and mechanical characteristics of a backplane. In addition to the standard protocols, many backplane designers prefer to employ proprietary protocols and architectures. Some of the more popular standard protocols are BLT, MBLT, 2eVME, and 2eSST on VME64x backplanes, PCI, cPCI, PMC, ISA, Multibus, PC/104, and PC/104+. Of these, VME, PCI and cPCI, collectively, dominate the market. cPCI combines the robust, rugged VME backplane physical configurations with the electrical performance of the PCI backplanes.

3 Should I use a parallel or serial architecture?

Part of choosing a protocol is deciding which type of backplane architecture is suited best to your application. You must choose between parallel and serial architectures, or a combination of both, and select point-to-point, multidrop, or multipoint data-distribution methods. Parallel systems require less protocol overhead, which is useful when sending status or control bits over short distances. Serial implementations offer board saving through the reduction in the number of board traces (if SERDES devices are used) and supply higher data throughput over greater distances.

4 If I use a parallel single-ended backplane, why do I need to use backplane-optimized transceivers and not just typical LVT or FCT devices?

The physics involved with a distributed-capacitance load limits the maximum frequency, unless the device is optimized with slower edge rates that ring less in these environments. FCT or LVT can offer only up to about 25 MHz, and, even then, signal integrity might be poor. The new VME and GTLP families are optimized with slower edge rates and provide much better signal integrity in a backplane environment. VME devices can operate up to about 40 MHz and are compatible with existing TTL/LVTTL backplane logic. GTLP is a derivative of GTL, and can operate at up to 175 MHz.

5 What is VME?

VME is short for VERSA bus architecture and owes its heritage to the Motorola 6800 microprocessor. It is a standardized 21-slot, 64-bit backplane architecture, coordinated and controlled by the VMEbus International Trade Association (VITA). TI is working with VITA on the SN74VMEH22501, a new backplane-optimized device that supports the 2eVME and 2eSST protocols. More information on VITA can be obtained at http://www.vita.com. More information on the new VME device can be obtained at http://www.ti.com/sc/etl.

6 What is GTL?

GTL is a reduced-voltage-swing (<1 V), open-drain/collector, differential-input JEDEC standard that allows higher frequency operation than TTL devices in point-to-point and lightly loaded memory-interface-bus applications. The reduced voltage swing reduces EMI and allows higher frequencies. For best signal integrity, the open-drain/collector arrangement facilitates matching the termination resistor (R_{TT}) to the trace impedance (Z_O). As shown in Figure 1, the open-drain/collector pulls the signal low when the device is turned on, but when the device is turned off, the pullup termination resistor is required to pull the signal high to the termination voltage (V_{TT}). The GTL standard is V_{TT}/V_{OH} = 1.2 V, V_{OL} = 0.4 V, and V_{IH} and V_{IL} set ±50 mV around the GTL differential-input reference voltage (V_{ref}) of 0.8 V.

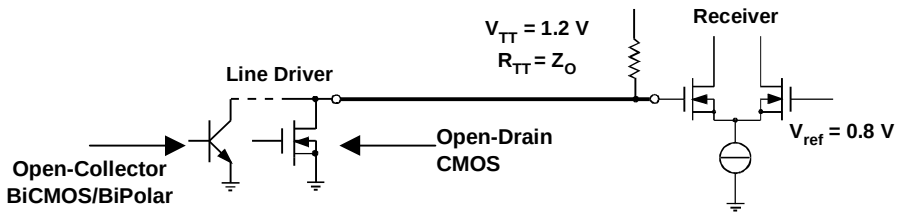

Figure 1. GTL Open-Drain/Collector Differential-Input Device

Open-drain and open-collector devices operate in exactly the same way to sink energy to ground. Open drain refers to CMOS transistors, while open collector refers to bipolar transistors. GTL devices can be manufactured using either process.

GTL+ is a variation on GTL that moves V_{ref} from 0.8 V to 1.0 V so that it is farther from the ground-bounce region. GTL+ voltage swing improves the upper and lower noise margins. Voltage swing is from V_{OL} = 0.55 V to the termination voltage of V_{TT}/V_{OH} = 1.5 V.

Any device that operates at GTL signal levels also can operate at GTL+ signal levels, and vice versa, with GTL+ being the preferred signal level due to its higher noise margins. In unusually noisy situations, V_{ref} can be adjusted to other than 0.8 V or 1.0 V in either standard to equalize, and, therefore, maximize both the upper and lower noise margins.

GTL devices are bidirectional translators (see Figure 2). A-Port (daughter-card side) input can be 5-V CMOS, TTL, or LVTTL logic levels; output is LVTTL, which is compatible with TTL logic levels. B-Port (backplane side) input and output is GTL or GTL+ signal levels.

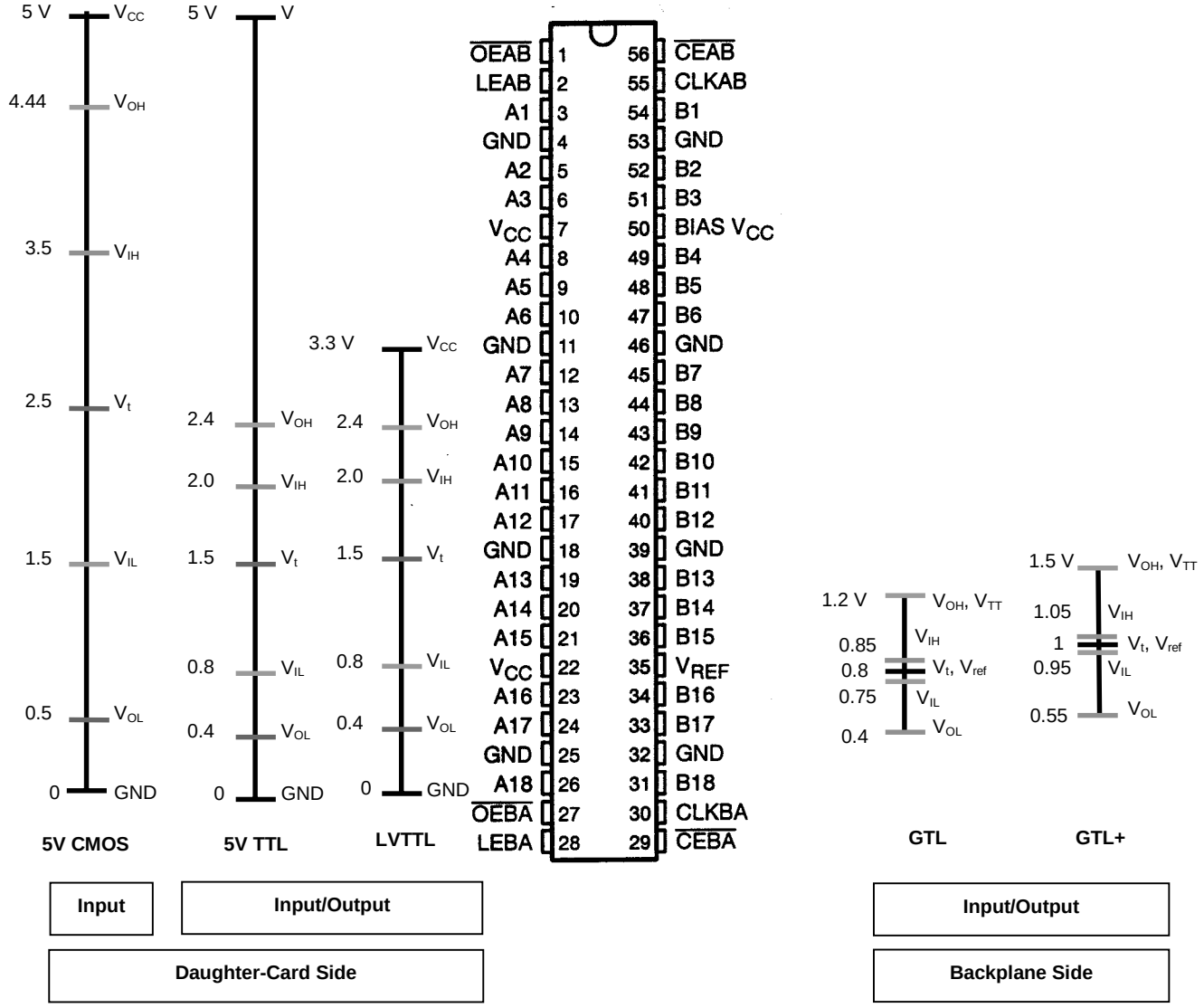

Figure 2. GTL Bidirectional Translator

As shown in Figure 3, V_{ref} is set by an R/2R resistor network between V_{TT} and GND. The resistor network maintains balanced upper and lower noise margins for any termination-voltage fluctuations. A 0.1- to 0.01-µF bypass capacitor buffers voltage fluctuations and should be as close to the V_{ref} pin as possible.

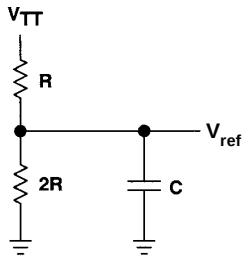

Figure 3. GTL R/2R Resistor Network

V_{ref} is generated locally on each card, using size 805 1-kΩ and 2-kΩ ±1% resistors. Each device V_{ref} input takes, at most, 10 µA, so one resistor network per card is acceptable. The card resistor network takes V_{TT} from the backplane through a connector power pin. Do not distribute the V_{ref} power across all cards from one resistor network.

7 What is the difference between GTLP and GTL?

TI introduced the GTL family of devices in 1993. GTL devices were designed with faster edge rates to drive a lumped load. Originally, these devices were designed for small buses on a board, e.g., memory applications, and did not support hot insertion. The devices rang excessively when used in larger multipoint distributed-capacitance backplane applications because of the faster edge rate. Maximum backplane frequency was limited to about 30 MHz.

GTLP devices were introduced in 1997 to serve distributed-capacitance backplane applications. GTLP is a subset of GTL devices, with one major difference. GTLP incorporates improved output edge-control (OEC) circuitry that slows the edge rate and reduces ringing, which allows maximum possible frequencies above 80 MHz in backplane applications. GTLP devices can operate at GTL signal levels, but are optimized for, and normally only specified at, GTL+ signal levels (V_{OL} = 0.55 V to V_{OH} = 1.5 V, with V_{ref} = 1.0 V). GTLP backplane-optimized devices normally refer to GTLP instead of GTL+ as the 1.5-V V_{OH}/1.0-V V_{ref} standard, while GTL lumped-load optimized devices refer to GTL+ at this voltage level.

The waveforms in Figure 4 demonstrate the difference between the TI SN74GTL16612 and the newer SN74GTLPH16612, and how the backplane-optimized edge rates improve signal integrity in a distributed load.

Test results for the competitor's GTLP16612, a pin-for-pin functional equivalent of the SN74GTLPH16612, is shown in Figure 4 for comparison. These receiver waveforms were obtained using a fully loaded 16-slot demonstration backplane, with Z_O = 50 Ω, R_{TT} = 24 Ω, slot spacing = 0.9 inch, and data frequency of 37.5 MHz. The driver card was in slot number 8 and the receiver card was in slot number 1.

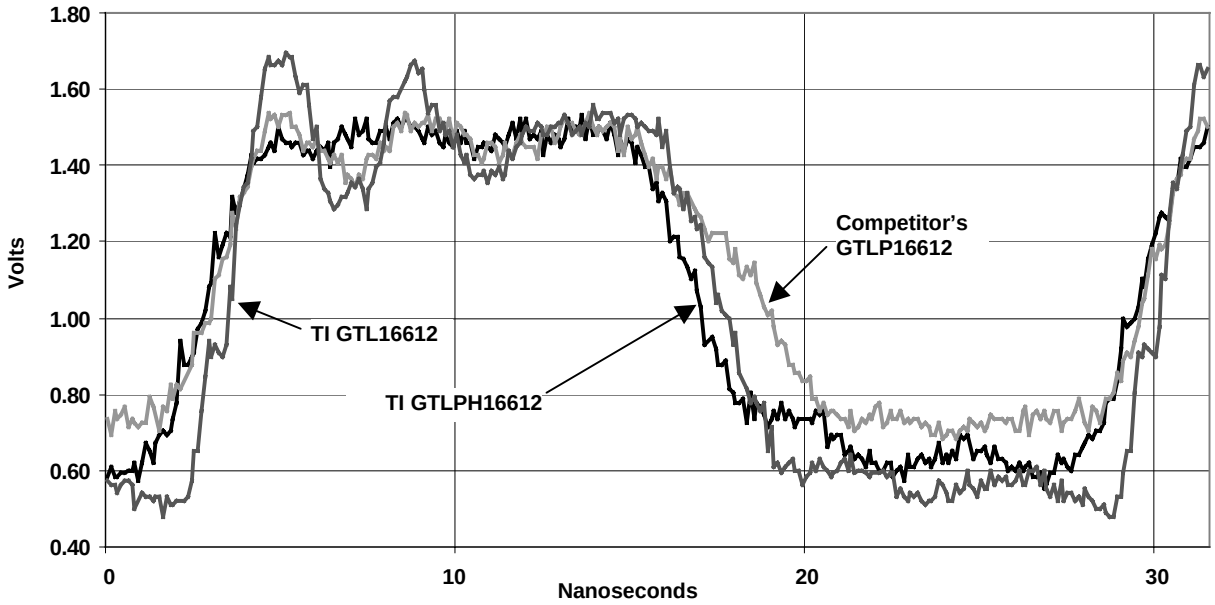

Figure 4. Demonstration of Output Edge Control

All three devices shown in Figure 4 have bus hold on the LVTTL A port. But, only the newer TI GTLP family uses H in the part number to denote bus hold, because there are several devices in the GTLP family without bus hold. All TI GTL devices have bus hold, while the competitor's GTL or GTLP family has some of both; the only way to determine the configuration is by referring to the data sheet.

A typical single-bit distributed-capacitance open-drain/open-collector backplane physical representation is shown in Figure 5. Normally, backplanes are 4, 16, 32, 64, 128, or more bits wide, with each bit identical to the representation in Figure 5. Both GTL and GTLP devices need a pullup resistor to pull the bus high. In this representation, the device in slot 1 is on, pulling the trace below 0.55 V, and providing a valid low. Receivers in slots 2 through 20 detect that the signal is low and, if not in the high-impedance state, transmit a low logic level to the A-port daughter-card side. Although not shown, each driver/receiver on the daughter card is a transceiver that can be configured to transmit or receive signals from the backplane. When the device in slot 1 is turned off, the bit is pulled high to 1.5-V by the 22-Ω termination resistors. The receivers in slots 2 through 20 detect that the signal is now high and transmit a high logic level to the daughter card. This process is repeated multiple times, with any card being able to transmit low signals onto the backplane. This can be done, even with multiple devices at the same time (wired-OR), without bus contention. This example assumes true logic.

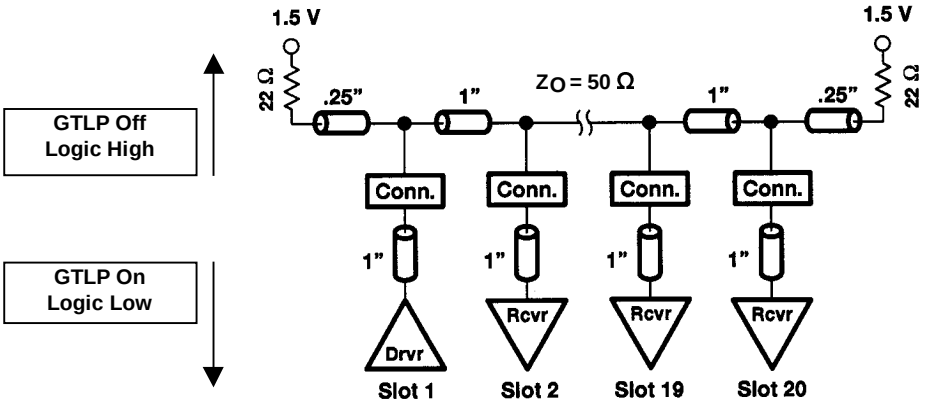

Figure 5. GTLP Open-Drain Backplane Physical Representation

GTLP devices are offered in two drive levels to match the termination-resistance value. For best signal integrity and incident-wave switching, the termination resistor should match or be smaller than the effective trace impedance. The effective trace impedance and, hence, the optimum termination-resistance value, varies, based on stub length, device C_{io}, slot pitch, and type of connector. Medium-drive (50 mA) devices are good replacements for existing TTL/LVTTL devices where higher frequencies are needed, but lower power consumption is a concern. These devices should be used with termination-resistor values ≥38-Ω. High-drive (100 mA) devices are best for replacing ABTE/FB+ devices where lower termination resistor values (22 Ω to 38 Ω) are required. Either medium- or high-drive devices can be used with higher resistance (e.g., 60 Ω) termination resistors, with the only outcome being the device pulls V_{OL} to a lower level, closer to GND, and probably poorer signal integrity, unless the effective trace impedance also is 60 Ω.

Incident-wave switching ensures that the first received signal during a transition (low to high or high to low) is valid, and reduces wait time. Reflected-wave switching requires additional wait time as shown in Figure 6.

	SWITCHING WITH THE INCIDENT WAVE	SWITCHING WITH THE REFLECTED WAVE
A⇒B	$t_{pd\ Driver} + t_{pd\ Receiver}$ = 5 ns + 5 ns = 10 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 10 ns + 5 ns = 30 ns
A⇒C	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns
Worst case	20 ns	30 ns

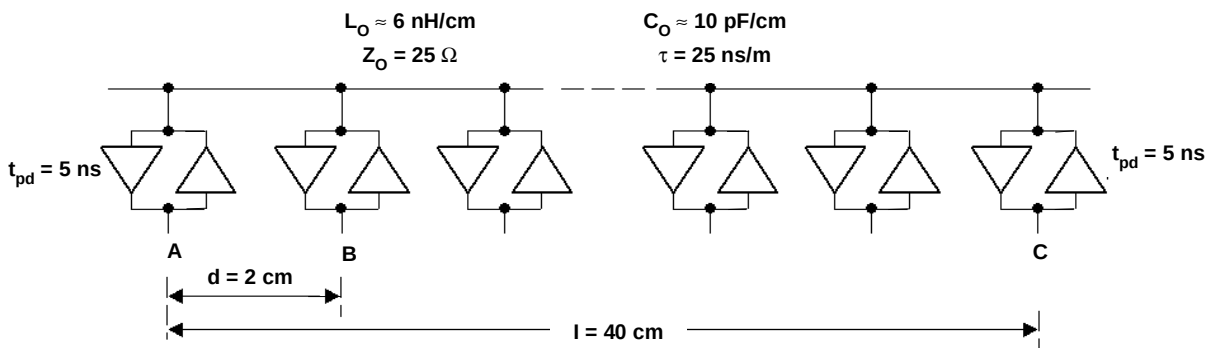

Figure 6. Reflected-Wave Switching

Additional information on incident-wave switching is in the *Fast GTLP Backplanes With the GTLPH1655* application report, literature number SCBA015A.

In summary, GTLP is a bidirectional translator (5-V CMOS, TTL or LVTTL to GTLP, and GTLP to LVTTL or TTL) that facilitates significantly higher frequencies (>80 MHz) and higher data throughput in multipoint, heavily loaded, distributed-capacitance backplane applications because the B-port GTLP output transistors produce these features:

- Reduced voltage swing (<1 V), which reduces EMI over TTL solutions.
- Optimized OEC with low slew rates (0.35 to 0.5 V/ns), which minimizes overshoot in distributed loads.
- Open-drain configuration with matched termination resistors (≥22 Ω high drive or ≥38 Ω medium drive), which ensures incident-wave switching and optimum signal integrity.
- I_{OFF}, PU3S, and BIAS V_{CC} precharge circuitry prevent data disturbance during card insertion or removal, permitting full live-insertion capability.

8 What is distributed capacitance?

Figure 7 is a simplified backplane physical representation, where an equivalent capacitive load of 12 pF replaces the receivers. The transmitter also has an equivalent capacitive load of 12 pF.

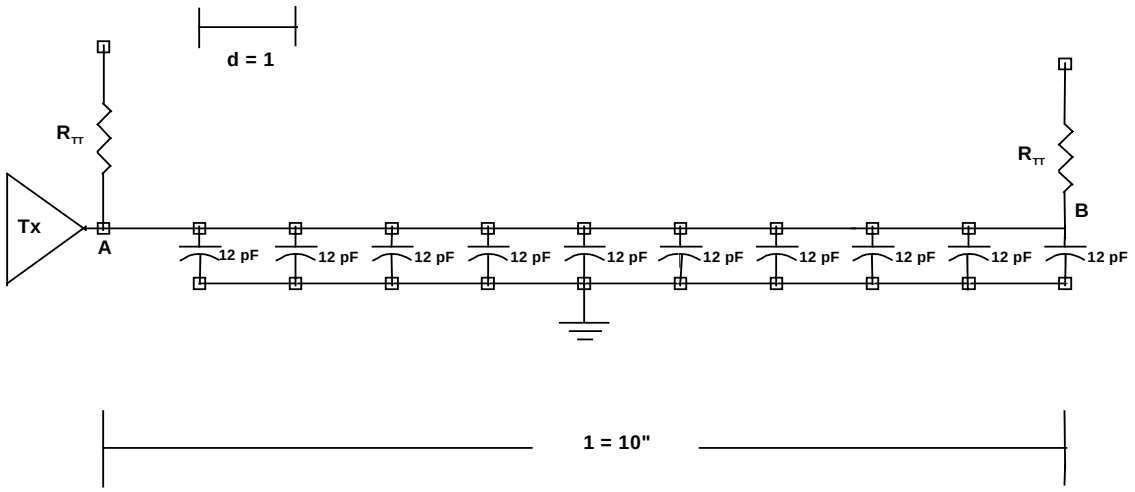

Figure 7. Simplified Backplane Physical Representation

The total capacitance (C_t) of each card is calculated by summing all the capacitive components associated with the transceiver and the connection to the backplane. Figure 8 shows a typical connection scheme between the backplane stripline and the transceiver device on the daughter card. Point C is the connection to the backplane stripline, and point D is the connection to a transceiver integrated circuit. The total capacitance at point C is the sum of each of the elements in the connection chain.

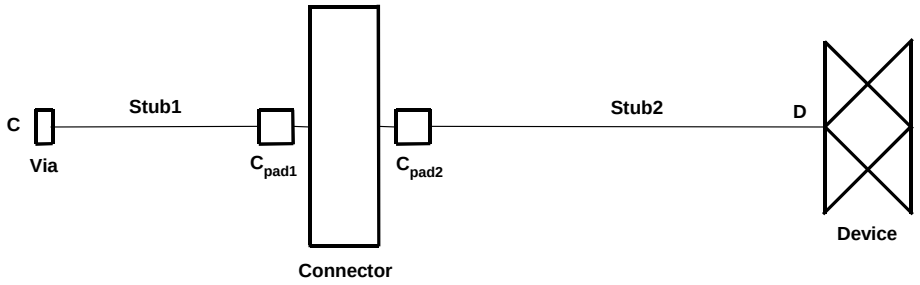

Figure 8. Typical Backplane Connection Scheme

The capacitance in the chain illustrated in Figure 8 is summed as follows:

C_{via} = capacitance of via = 0.5 pF

C_{stub1} = capacitance of Stub1 = 0.0625 inch $\times$ 2.6 pF/inch = 0.16 pF

C_{cpad1} = capacitance of C_{pad1} = 0.5 pF

C_{con} = capacitance of connector = 0.74 pF

C_{cpad2} = capacitance of C_{pad2} = 0.5 pF

C_{stub2} = capacitance of Stub2 = 1 inch $\times$ 2.6 pF/inch = 2.6 pF

C_{io} = typical input/output capacitance of device = 7 pF

$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io}$

$C_t = 0.5 + 0.16 + 0.5 + 0.74 + 0.5 + 2.6 + 7$

C_t = 12 pF

This total capacitance (C_t) of 12 pF is placed at point C on the backplane for every transceiver. With all the slots filled, the 10-inch transmission line has ten 12-pF capacitors and one transmitter (12 pF) distributed at 1-inch intervals.

Total capacitance then can be distributed uniformly across the transmission line at an equivalent rate of capacitance per inch (C_d). The total capacitance per distance is the distributed capacitance. The higher the total card capacitance and the closer the card spacing (slot pitch) the heavier the backplane loading.

The distributed capacitance equals the total capacitance divided by the separation, or $C_d = C_t/d$. In our example, C_d = 12 pF per 1 inch or 472 pF per meter. The new effective trace impedance $Z_{O(eff)}$ and effective propagation delay ($t_{pd(eff)}$) can be calculated using the following equations. C_o is the characteristic capacitance, which is dependent on Z_O and is fixed.

$$Z_O(eff) = Z_O \Big/ \sqrt{1 + (C_d/C_o)}$$

$$t_{pd}(eff) = t_{pd} \times \sqrt{1 + (C_d/C_o)}$$

The distributed capacitance (C_d) affects both the propagation delay and the characteristic impedance of the transmission line. A larger C_d (higher C_t and/or smaller d) results in lower effective trace impedance ($Z_{O(eff)}$) and a higher effective propagation delay ($t_{pd(eff)}$).

This illustrates why the termination-resistor values should be lower than the typical 50-Ω natural transmission-line impedance in multipoint applications. Matching the termination resistor with the effective trace impedance ensures incident-wave switching and better signal integrity. Higher-drive (100 mA) devices are offered because termination values lower than 38 Ω often are required.

For example, in a 20-slot, slot pitch = 0.94 inch backplane, the characteristics in Table 1 are observed.

Table 1. Backplane Characteristics, 20 Slots at 0.94-Inch Slot Pitch

Unloaded (Natural) Embedded Microstrip Trace			Trace and 20 Empty Connectors at 0.94 Inch		Fully Loaded With 20 Cards at 0.94 Inch		Card C_t† (pF)
Z_O (Ω)	t_{pd} (ns/in)	C_O (pF/in)	$Z_{O(eff)}$ (Ω)	t_{pd} (ns/in)	$Z_{O(eff)}$ (Ω)	t_{pd} (ns/in)	
48	142	2.99	37	183	18	382	15
90	165	1.84	62	239	26	570	16.2

† Different stub lengths provide a unique C_t for each bit on the same daughter card.

Table 1 clearly shows that, in a heavily loaded backplane with the 48-Ω natural Z_O, the termination resistance should go as low as 18 Ω, but is limited to 22 Ω by the GTLP high-drive maximum recommended I_{OL}. Increasing the natural Z_O to 90 Ω can change the termination resistor to 26 Ω, a value that is within the capacity of the high-drive devices and better approximates what the medium-drive devices can handle. The disadvantage is that the backplane time of flight is about 50% higher. Typical card capacitance will be between 12 pF and 18 pF, depending on device C_{io} and stub length, with stub length being most critical. Stub length always should be less than one inch for best backplane performance. Lower C_t always is better.

For best signal integrity, termination resistor R_{TT} should equal the loaded-trace impedance ($Z_{O(eff)}$). A lower value for R_{TT} could be used to compensate for possible variations of the device typical C_{io}, up to the maximum C_{io} value.

The waveforms in Figure 9 show the effect on signal integrity in over-matched and under-matched termination conditions. R_{TT} should be less than or equal to $Z_{O(eff)}$ for optimum signal integrity and upper noise margin.

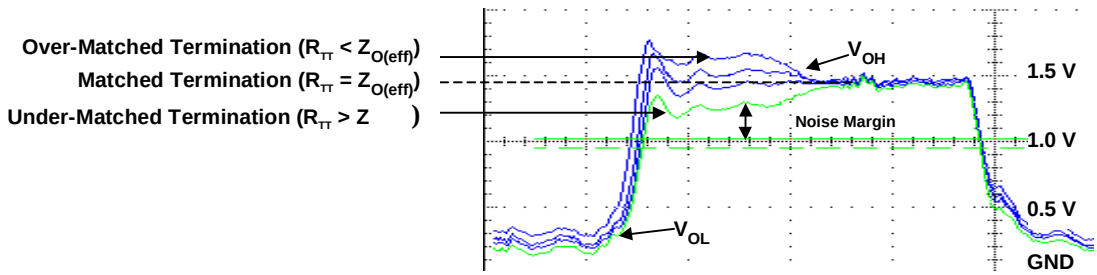

Figure 9. GTLP Waveform Under Different R_{TT} Conditions

The result of using an under-matched termination is that V_{OL} will be closer to ground and the upper noise margin will be less, as is clearly shown in Figure 9.

The result of a matched termination is optimal upper and lower noise margins.

The result of using an over-matched termination is that V_{OL} on the card farthest from the driver is higher and the lower noise margin is reduced.

More information on calculating distributed capacitance is in the *Basic Design_Considerations for Backplanes* application report, literature number SZZA016A, at www.ti.com/sc/docs/apps/logic/appnotes.html under backplane logic.

9 What are you going to do with GTL now that you have GTLP?

TI will continue to support and expand the GTL family because these devices are well suited for voltage-level translations, point-to-point applications, and lightly loaded bus onboard-memory applications, e.g., Intel™ Pentium™ microprocessors operate at GTL+ signal levels. Customers can switch between GTL and GTLP families, but must be aware of the differences in the edge rates. GTLP devices can be used in memory applications, but, due to the slower edge rates, the device propagation delay is longer. GTL devices should not be used in high-frequency heavily loaded backplanes.

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10 How should I terminate GTL devices in short-distance applications?

GTL products are open drain, so they must be connected to V_{TT} via proper R_{TT} termination resistors. One question is that if GTL or GTLP is used to transmit signals on a daughter card, the distance is very short, about 4 cm to 6 cm. Do we need to position a R_{TT} termination resistor at both the driver and receiver? If so, can you provide the R_{TT} based on your experience? In such a condition, how can better results be obtained?

You need only to put the R_{TT} termination resistor at the receiver end of the transmission line. On the backplanes we recommend putting the termination resistors on both ends of the backplane because you do not know when slot 1 or 20 will be the transmitter or receiver, so you have to cover both cases. The R_{TT} value should equal the loaded-trace impedance whether or not you use one or two R_{TT} termination resistors. If two are used, the effective resistance is reduced by a factor of two (i.e., 50 Ω at either end, the driver will see 25-Ω effective resistance) which means simply that the driver has to be able to sink more current. For this short trace and lower loading you could probably use a single termination resistor at the receiver that is about 10 Ω less than the natural trace impedance (i.e., If Z_O is 50 Ω, use 40 Ω.). Using the GTLP EVM, we have removed the driver termination and the signal integrity was satisfactory, however, when the receiver termination was removed and only the driver side was terminated, signal integrity was poor. As you would expect, it did not work when both terminations were removed.

11 What is the advantage of using GTLP in my backplane?

Increasing bandwidth and data throughput speeds are major issues today for many systems, as our world becomes increasingly interconnected. TI has taken what it has learned about the use of GTL over the last four years and applied this expertise and knowledge to future backplane-based applications using GTLP devices.

TI's GTLP family has been designed specifically for optimum signal integrity in multipoint, heavily loaded, distributed-capacitance backplanes like those shown in Figure 10. These improvements allow higher data throughput in the same bit-width backplanes that are currently being used and provide an easy migration from current TTL/LVTTL and BTL/FB+ backplane drivers to GTLP devices.

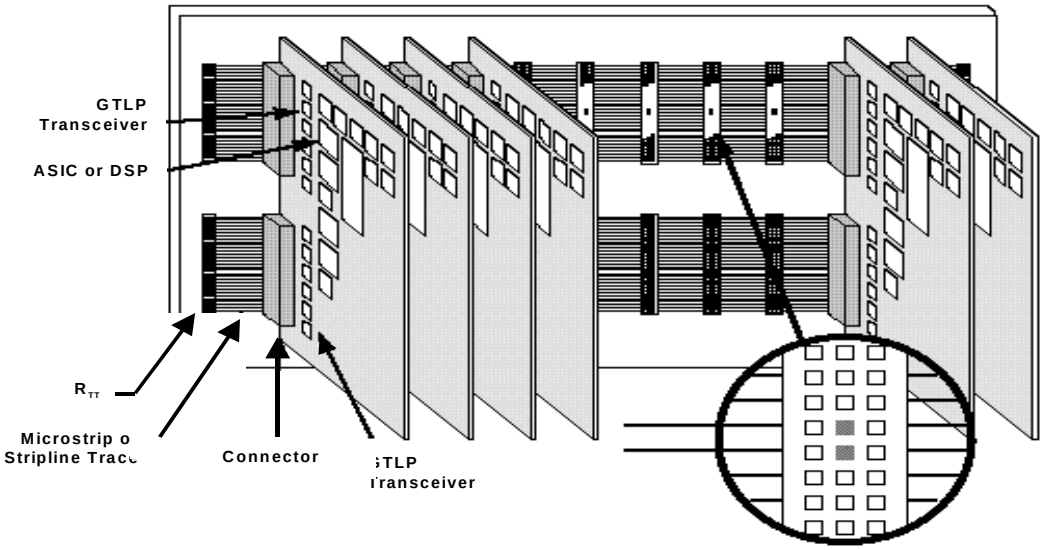


Figure 10. Heavily Loaded, Distributed-Capacitance Backplane Installation

GTLP devices allow higher frequencies on the backplane because of the improved signal-integrity/incident-wave switching the results from the reduced swing (<1 V), lower slew rate (0.35 V/ns to 0.5 V/ns), and matched termination resistors.

Additionally, GTLP fully supports live insertion, a capability that is imperative in high-availability communications and networking applications. I_{off} and PU3S provide hot-insertion capability, while the BIAS V_{CC} precharge circuitry precharges the B-port input/outputs to the threshold voltage. This protects active data on the backplane from voltage spikes or glitching, and provides true live-insertion capability.

GTLP devices are designed and manufactured in an advanced CMOS process that reduces static-power consumption.

GTLP devices are 5-V tolerant because, although most applications are migrating to 3.3 V, or lower, some existing circuits/devices on the board remain at 5 V.

GTLP is offered in a wide variety of packaging options and pinouts that are similar to previous-generation devices. This helps simplify the designer's task of migrating to a GTLP-based backplane. High-drive devices are identical to the comparable medium-drive devices, except for the addition of five ground, two V_{CC}, and one edge-rate control (ERC) pins. The additional ground and V_{CC} pins reduce ground and V_{CC} supply noise, thus providing additional noise margin. The ERC pin allows the selection of either a slow or fast edge rate by holding the control pin at V_{CC} or ground. The faster edge rate reduces the propagation delay and allows higher frequency operation in an optimally terminated backplane.

Lumped loads normally are associated with point-to-point applications. However, GTLP devices have been designed into actual backplane netlists and a resistance/inductance/capacitance (RLC) network that closely matches the results in a backplane. TI's GTLP devices are tested into a lumped load, as are all other devices offered by TI and other semiconductor manufacturers. Engineers are using GTLP devices in high-performance distributed-capacitance loads and the actual switching characteristics are radically different from the lumped loads that are specified in the data sheet. TI SPICE-modeled values using the RLC network are included in the data sheet to better help engineers understand backplane effects. In summary, the data-sheet switching-characteristics into the lumped-load parameter values are going to look ugly but the actual performance of the device in a distributed load is going to be beautiful.

12 What is the difference between GTLP and LVDS?

GTLP is a single-ended low-voltage-swing (<1 V) standard, whereas LVDS is a differential low-voltage-swing (350 mV, typical) standard. Single-ended devices require only one trace per bit of data, while differential devices require two traces for each bit of data. Differential devices, e.g., LVDS, LVDM (backplane optimized LVDS), SERDES, Wizard, etc., work well for high-speed data transmission over long cables, such as between cabinets, cards, or racks, as shown in Figure 11, but they do not fit all applications where simplicity and lower cost of implementation indicate that single-ended devices are better for use in multislot backplane applications.

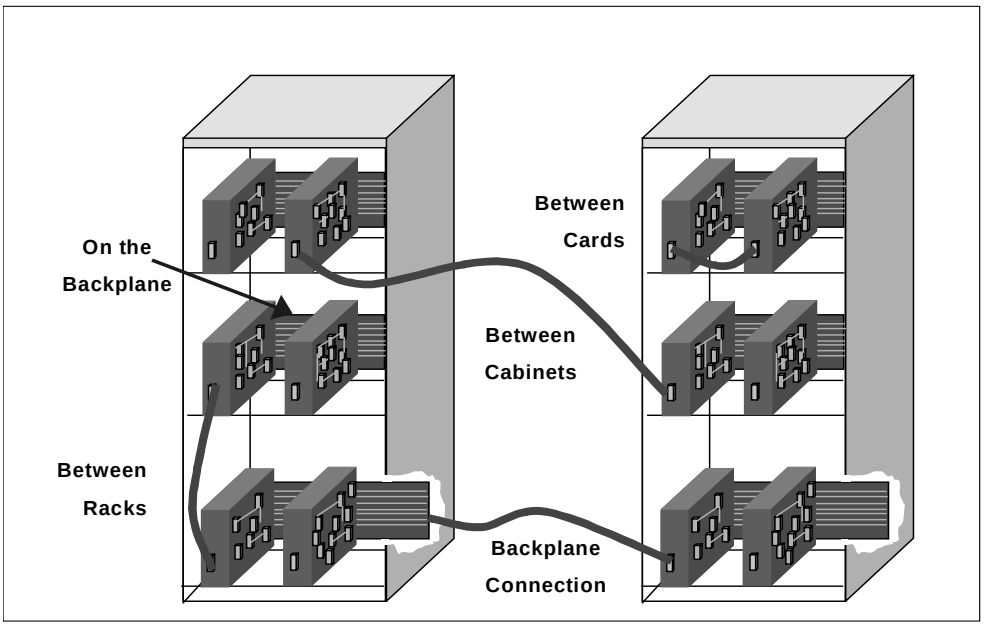


Figure 11. Various Equipment Connections

13 How does GTLP compare to other single-ended and differential bus solutions?

Reduced voltage swing, lower slew rate, and open-drain construction allow GTLP devices to operate at higher frequencies than TTL devices in parallel-backplane architecture. GTLP offers an alternative to high-data-throughput differential devices where parallel backplanes are the best solution and higher data throughput is now required (see Table 2).

Table 2. Comparison of Single-Ended vs Differential Bus-Interface Solutions

Device (typically 16245 function)	Bidirectional (B) or Unidirectional (U)	V_{CC} (V)	Tolerant to	Hot Insertion	Live Insertion	Number of Pins in the Package	Number of Bits	Cost ($ in DGG qty 999 Internet Price)	Card Interface Drive (mA)	BP Interface Drive (mA)	I_{CC} (mA - Output Low)	C_{io} (pF - max)	Freq. Max BP (MHz)	Data Throughput Per Package (Mbps - Transparent Mode)	Data Throughput per Bit-$ (Mbps/bit$)	Data Throughput per Bit (Mbps/bit)
Single-Ended Bus Interface Solution																
ABT	B	5	5	Y	N	48	16	$1.92	-32/+64	-32/+64	32	6 -typ	33	1,056	34	66
LVT	B	3.3	5	Y	N	48	16	$2.17	-32/+64	-32/+64	5	10 - typ	33	1,056	30	66
ALVT	B	3.3	5	Y	N	48	16	$3.09	-32/+64	-32/+64	5	6 - typ	40	1,280	26	80
GTLP Medium Drive	B	3.3	5	Y	Y	48	16	$5.00	-24/+24	50	35*	9	80	2,560	32	160
ABTE	B	5	5	Y	Y	48	16	$5.01	-12/+12	-60/+90	48	8	45	1,440	18	90
BTL/FB+	B	5	5	Y	Y	52	8	$10.47	-3/+24	100	70	5	50	800	10	100
GTLP High Drive	B	3.3	5	Y	Y	56	16	$5.85	-24/+24	100	35*	10	100	3,200	34	200
Differential Bus Interface Solution																
ECL/PECL	U	5	5	N	N	24	8	$10.20	-3/+24	-25	69		80	640	8	80
TLK2500	B	2.5	3.3	Y	N	64	16	$36.70	-1/+1	1 Serial	135	Serial		2,500	4	156
LVDS386/387	U	3.3	5	Y	Y	64	16	$9.58	-8/+8	16 - Serial	70	Serial		10,080	66	630
LVDS93/94 SERDES	U	3.3	5	Y	Y	64	28	$3.50	-4/+4	5 - Serial	84	Serial		1,820	19	65

The maximum backplane frequency is based on good backplane construction and termination techniques. The TLK, LVDS, and SERDES data throughputs are theoretical maximum values; actual data throughput rates are less.

Comparison of cost of GTLP versus other single-ended technologies shows that GTLP data throughput per bit-dollar is about the same as the most popular parallel technologies, such as ABT. Although GTLP costs about three times more than ABT, the GTLP data throughput is more than three times greater than ABT in heavily loaded backplanes. GTLP also is an excellent replacement for ABT or LVT in low-frequency applications where signal integrity is an important consideration.

Strong interest in point-to-point differential-backplane connections in high-end networking and 3G wireless base-station applications has been seen, although that requires dozens to hundreds of connections along a 19-inch backplane. Typically, telecom engineers dislike single-ended solutions because of past EMI, maximum system frequency, and power-consumption difficulties with older TTL solutions. The tradeoff is the ease of design of the single-end solution versus the low EMI, higher frequency, and lower power consumption of differential designs. GTLP provides massive throughput at lower EMI and power-consumption levels than TTL, which is what they're thinking of when they think single-ended. Throughput on the backplane using GTLP devices at lower cost and without serious EMI or crosstalk effects compares very favorably with point-to-point serial schemes.

Figure 12 allows you to pick the bus solution technology offered by TI that would be most appropriate, based on throughput and transmission distance.

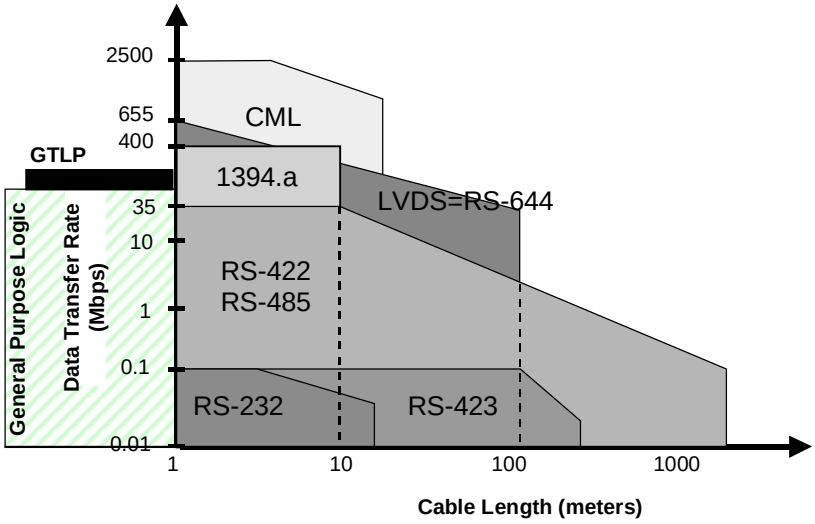


Figure 12. Data Transfer Rate (Mbps)

More information on TI's vast array of parallel and serial technologies can be found in the *Comparing Bus Solutions* application report, literature number SLLA067.

More information on LVDS, LVDM, SERDES, Gigabit CMOS, and 1394 can be found on TI's semiconductor internet home page at www.ti.com/sc.

More information on GTLP can be found on TI's GTLP internet home page at www.ti.com/sc/gtlp.

14 What is the maximum data throughput using GTLP?

Data throughput is a function of clock frequency times the bit width of the backplane. Increasing the maximum frequency or backplane bit width increases data throughput. GTLP devices can operate at speeds up to 175 MHz into a distributed load with good signal integrity.

A 32-bit backplane operating at 110-MHz clock frequency has a data transfer rate of 1.76 Gbit/s in single-edge latched-mode (data is transferred at one-half the clock frequency) applications to 7 Gbit/s in dual-edge transparent-mode applications.

Data throughput in GTLP backplanes is now limited by timing requirements, not signal integrity, as in past backplane devices. Maximum frequency is a function of device maximum propagation delay (t_{pd}), pin-to-pin skew, backplane construction or length, and how the clock is distributed (see Figure 13).

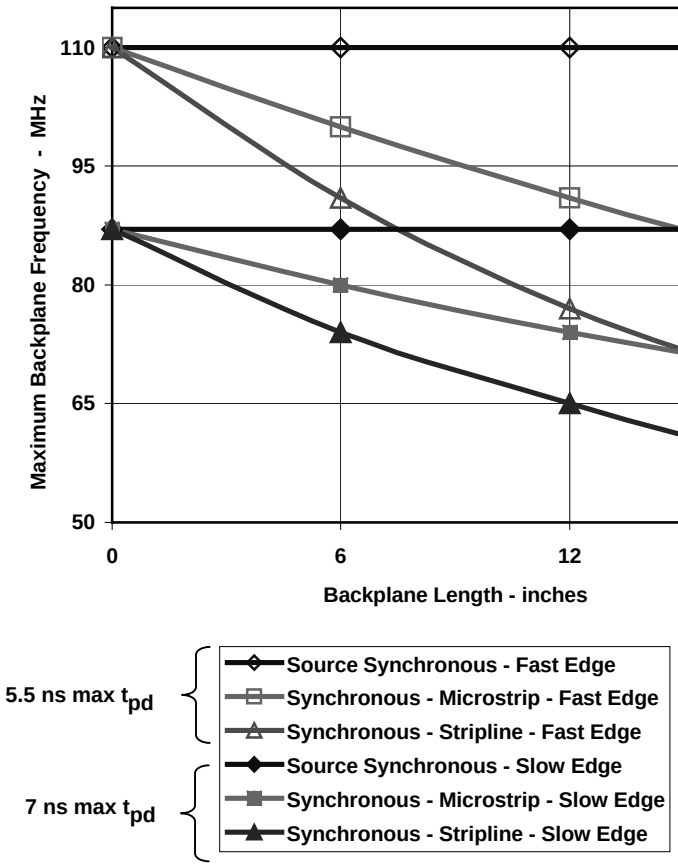


Figure 13. Maximum Backplane Frequency

Propagation delay is a function of the edge rate. Only high-drive GTLP devices are able to operate at both slow and fast edge rates, with a maximum t_{pd} of about 7 ns and 5.5 ns, respectively. Medium-drive devices operate only at the slow edge rate, with a maximum t_{pd} of about 7 ns. These are design goals, and actual values may be different.

Setup and hold times and skew are inherent in the device.

Backplane flight time depends on backplane length and construction (microstrip or stripline). Microstrip places the trace on top of the printed circuit board and does not reduce the flight time as much as stripline, but it is more susceptible to EMI. Stripline places the trace between printed circuit board dielectric layers and is less susceptible to EMI, but the signals are slower and, consequently, flight time is longer. Most high-quality backplanes use stripline construction to minimize EMI. Proper backplane layout and stub lengths of less than 1 inch help minimize backplane capacitance.

Most backplanes use a system clock that provides an absolute clock signal to all cards at the same time. Maximum system frequency is reduced based on backplane length, as shown in Figure 13, to accommodate the difference between the time-of-arrival of the driver card and receiver card clock signal (flight time), respectively. Source-synchronous operation is a technique in which the clock is sent with the system data as a relative clock signal. This means that there is no delay due to backplane flight time because the clock is sent along with the data. Flight time always is zero; therefore, maximum frequency is independent of backplane length.

Studies performed using the 19-inch 20-slot GTLP EVM with the SN74GTLPH1655 DGGR device show that the maximum frequency is 46 MHz in system-clock mode and 120 MHz in source-synchronous clock mode, and, for short time periods, 160 MHz in asynchronous mode.

In summary, maximum frequency (MHz) is the inverse of the maximum delay time (ns), i.e., 10 ns = 100 MHz. Maximum delay time depends on the sum of these factors:

- Maximum propagation delay
  - Fast edge (5.5 ns)
  - Slow edge (7 ns)
- Setup time (2.5 ns)
- Skew time (1 ns)
- Backplane flight time
  - Source synchronous - flight time is zero and is independent of backplane length because the clock is sent with the data
  - Microstrip (1 ns/6 inches)
  - Stripline (~2 ns/6 inches)

To improve backplane performance, review the *High-Performance Backplane Design With GTL+* application report, literature number SCEA011A, and *Basic Design Considerations for Backplanes* application report, literature number SZZA016A.

Additional information on calculating backplane impedance can be found at www.ultracad.com. There is detailed information on microstrip and stripline calculations and an impedance calculator that can be downloaded.

15 What is the difference between synchronous clock and source-synchronous clock?

Synchronous clock is an **absolute** clock in which each card receives the same clock signal at exactly the same time. A clock generator with clock lines running to each card provides this absolute clock. For the clock signal to arrive at each card at exactly the same time, the line length must be exactly the same. For cards closer to the clock board, the lines are mitered (run up and down, parallel to each other) to add distance to the line.

Source-synchronous clock is a **relative** clock. The driver card uses the incoming absolute clock signal for timing, but all receiver cards use the clock sent from the driver card. Since the driver card data and slightly delayed clock signal are sent at the same time, backplane length or flight time is not a factor in timing calculations, unlike the absolute clock, which has to account for the backplane length or flight time between the driver and receiver.

Additional information on source-synchronous operation was presented by Lee Sledjeski at DesignCon 2000, in which he discussed private source-synchronous clocks for every 16 bits of data to minimize delays due to device skew. The paper can be viewed at http://www.fairchildsemi.com/products/backplane/designcon/lsdcon2k.pdf. These private clocks can be implemented easily with the GTLPH16916 or the high-drive GTLPH1616; each has one delayed buffered clock bit for every 17 bits of data. This paper also discusses reducing the clock signal transmitted across the backplane by a factor of one-half as a way to transfer data at the full system clock rate, i.e., data rate equals clock rate, which is 110 MHz.

16 What GTLP devices are available and how much will they cost?

The first wave of TI's GTLP devices comprises seven medium-drive and six high-drive devices. They are offered in ultra compact (LFBGA/VFBGA), small (TVSOP), medium (TSSOP), or large (SOIC or SSOP) packages. Pricing is two to three times higher than standard LVTTL/TTL backplane drivers, but GTLP devices allow two to four times higher maximum backplane frequencies, providing higher data throughput without migrating to more complex serial devices. Because signal integrity is superior in distributed loads, it also makes sense to use GTLP in low-frequency applications where the noise margin using HC, ABT, or LVT is not acceptable because of the weaker drive and poorer signal integrity. GTLP pricing is the same or less than TI's current GTL pricing (see Table 3).

Obtain the data sheet at www.ti.com/sc/gtlp. Go to www.ti.com/sc/package for package drawings, symbolization, layout, and thermal-performance information.

Table 3. GTLP Family Offerings

SN74GTLP	Function	Bits	Pin Count	SOIC	SSOP	TSSOP	TVSOP	BGA	Suggested Resale Price (1000 Quantity)
Medium Drive (50 mA)									
H306	Bus Transceiver	8	24	DW		PW	DGV		$4.65
817	1:6 Fanout Driver	NA	24	DW		PW	DGV		$5.40
H16612	Universal Bus Transceiver	18	56		DL	DGG			$7.35
H16912	Universal Bus Transceiver	18	56			DGG	DGV		$7.90
H16916	UBT with Buffered Clock	17	56			DGG	DGV		$7.90
H16945	Bus Transceiver	2 x 8	48			DGG	DGV	GQL	$5.00
H32945	Bus Transceiver	4 x 8	96					GKE	$10.50
High Drive (100 mA)									
1394	Transceiver	2	16	D		PW	DGV		$3.75
H1612	Universal Bus Transceiver	18	64			DGG			$9.15
H1616	UBT with Buffered Clock	17	64			DGG			$9.15
H1645	Bus Transceiver	2 x 8	56			DGG	DGV	GQL	$5.85
H1655	Universal Bus Transceiver	2 x 8	64			DGG			$9.15
H3245	Bus Transceiver	4 x 8	114					GKF	$12.25

Relevant package application information is contained in the following reports:

Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C.

32-Bit Logic Families in LFBGA Packages 96 and 114 Ball Low-Profile Fine-Pitch BGA Packages application report, literature number SCEA014.

Comparison of Electrical and Thermal Parameters of Widebus SMD and LFBGA Packages application report, literature number SCYA007.

17 These function numbers are different. How do they compare to normal logic functions?

When the GTL family was introduced, it was decided to differentiate GTL function numbers from other similar logic functions because of the V_{ref} pin and the reduced B-port GTL signal levels. The first GTL device (SN74GTL16612) has exactly the same pinout as the 3.3-V V_{CC} '16601 universal bus transceiver, except that the two V_{CC} pins on the B-port side serve different purposes. Pin 34 is used for the GTL differential V_{ref} input and pin 50 is used for the 5-V V_{CC} that powers the GTL circuitry. The first GTLP device is the SN74GTLPH16612, which is identical to the SN74GTL16612, except for the improved B-port circuitry that allows better performance in distributed loads. Based on the SN74GTLPH16612, other existing GTL devices, and TI's device-naming convention, the names of the additional GTLP devices were selected as shown in the migration summary below.

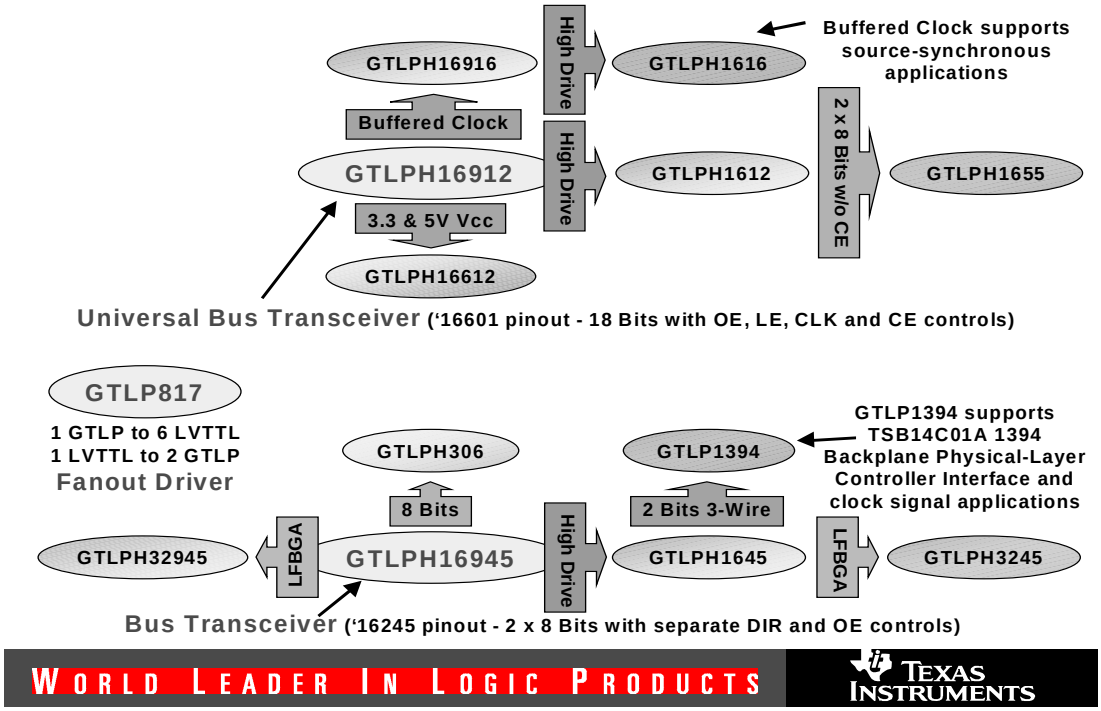


Figure 14. GTLP Migration Summary

GTLP device naming considerations are:

- The 16XXX and 32XXX function numbers signify Widebus™ (16 to 18 bits) and Widebus+™ (32 to 36 bits) bit widths. Typically, octals are XXX only.
- Function numbers of XX9XX signify single-V_{CC} operation and the incorporation of BIAS V_{CC}.
- Medium-drive devices are either three or five digits. High-drive devices have the "9" removed and are four digits long to conform to the prior BTL/FB+ high-drive device-naming convention.
- The 2-bit high-drive 1394 is designed uniquely to support the 1394 backplane physical-layer controller and, therefore, was named GTLP1394. Application information is included in the data sheet. The GTLP1394 is also very useful in providing 2-bit GTLP clock signals in backplane applications.
- "H" is added after the GTLP family name if bus hold is featured on the A-port I/O pins. Typical 1394 and 817 applications do not require bus hold, so bus hold was not included in these devices. Bus hold is not required on B port I/O pins because the termination resistors keep the bit high if it is not actively pulled low by the device.

18 I know what a bus transceiver is, but what is a UBT™?

A UBT™ device performs numerous functions that are done by other logic functions by proper selection of their OE, LE, and CLK control pins (‘16500 or ‘16501 functions) or their OE, LE, CLK, and CE control pins (‘16600 or ‘16601 functions). The ‘16601 logic function is shown in Table 4.

Table 4. ’16601 Logic Functions

FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

UBT, Widebus, and Widebus+ are trademarks of Texas Instruments.

UBT devices can be used for many different logic functions, reducing the number of different devices you have to buy. This reduces the number of other types of devices that must be maintained in inventory. Ordering larger quantities of UBT devices can reduce the price. However, simpler functions normally are less expensive. Backplane applications usually require only bus-transceiver functionality. Other applications might need more complex functions. The functions available from a UBT device or UBT device with clock enable are listed in Table 5.

The GTLPH306 is a functional equivalent of the ‘245, the GTLPH16945 is a pin-for-pin functional equivalent of the ‘16245, and the GTLPH16912 is a pin-for-pin functional equivalent of the ‘16601.

Table 5. UBT Equivalent-Functions Table

Function	8 Bit	9 Bit	10 Bit	16 Bit	18 Bit
Transceiver	‘**245**, ‘623, ‘645	‘863	‘861	‘**16245**, ‘16623	‘16863
Buffer/driver	‘214, ‘244, ‘541		‘827	‘16241, ‘16244, ‘16541	‘16825
Latched transceiver	‘543			‘16543	‘16472
Latch	‘373, ‘573	‘843	‘841	‘16373	‘16843
Registered transceiver	‘646, ‘652			‘16646, ‘16652	‘16474
Flip-flop	‘374, ‘574		‘821	‘16374	
Universal bus driver					‘16835
Standard UBT					‘16500, ‘16501
GTLPH1655 replaces above functions and is similar to the ’16501 standard UBT (OEAB, OEBA, LEAB, LEBA, CLKAB, CLKBA), but is at GTLP levels on the B port and is split into two 8-bit sections.					
Registered transceiver with clock enable	‘2952			‘16470, ‘16952	
Flip-flop with clock enable	‘377	‘823			‘16823
Standard UBT with clock enable					‘16600, ‘16601
GTLPH16612, ’169121/6, and ’1612/6 replace all above functions and are identical to the ’16601 Standard UBT with clock enable, but are at GTLP levels on the B port.					

19 I need an alternate source. Are there any?

Several companies manufacture GTL and GTLP devices. Fairchild (FSC) entered the market in 1997. Pericom and Philips also recently entered the market.

Pericom's two released offerings closely match the FSC GTLP data-sheet specifications, and it is assumed that their other planned offerings will also.

Philips markets their GTL devices toward the bus on the card/microprocessor interface market much like TI's existing GTL family. The GTL family has faster edge rates and is not optimized for backplane applications.

TI offers a wide range of medium-drive GTLP devices, a wider range of high-drive GTLP devices, and the widest range of packaging offerings. These devices support the needs of the emerging high-data-throughput parallel-backplane market. Additionally, TI has included a BIAS V_{CC} feature in the medium- and high-drive GTLP devices in place of one of the V_{CC} pins, to support true live insertion. The BIAS V_{CC} circuitry is disabled when V_{CC} is applied; therefore, except for the precharge feature, the TI device is fully functional in competitors' sockets.

All devices occupying the comparable bit width/drive box in Table 6 are pin-for-pin functional equivalents.

All 816/817 devices have the same pinout. They are one GTLP input to six TTL/LVTTL outputs and one TTL/LVTTL input to two GTLP outputs, but are various drives and V_{CC}. Refer to the data sheet, then test each device to pick the best one for your application.

Table 6. GTLP Device Cross-Reference

Bit Width	TI - SN74GTLP		Fairchild - GTLP		Pericom - GTLP	
	Medium Drive	High Drive	Medium Drive	High Drive	Medium Drive	High Drive
32	H32945	H3245				
18	H16912	H1612	✸ *18T612*		*18T612*	
	✸ H16612		✸ 16612		✸ 16612A	
17	H16916	H1616	✸ *17T616*			
			✸ 16616		16616	
			✸ 16617		16617	
16		✸ H1655		✸ *16T1655*		*16T1655*
	H16945	H1645				
8	H306		✸ 8T306		8T306	
6	817		✸ 6C817			
			✸ *6C816A*			
			✸ 6C816		✸ 6C816	
2		✸ 1394				

Legend	
H16612 (underline)	= 3.3- and 5-V or 5-V V_{CC} operation
✸	= Released to Market
H16912 (black)	= 3.3-V V_{CC} while *18T612* (blue italics) is 3.3-V V_{CC} but not 5-V tolerant
Medium Drive = 50 mA, High Drive = 100 mA	

20 Are the alternate-source devices identical?

While all GTLP devices operate in the same manner and have the same pinout and functionality, they are not all designed equally. The most important characteristic in GTLP devices is the B-port OEC circuitry and the corresponding edge rate. Faster edges perform poorly in backplane. In our demonstration backplane under the same conditions, the SN74GTLPH16612 had better signal integrity than the FSC GTLP16612, and the SN74GTLPH1655 had better signal integrity than the FSC GTLP16T1655. We believe that TI's GTLP devices exhibit excellent signal integrity due to the improved OEC and TI-OPC™ circuitry. If the design is optimized for the worst-case performance of all devices that are used, FSC or Pericom GTLP can be used as an alternate source.

Additional differences in other manufacturers' devices are shown in Table 7.

Table 7. Comparison of GTLP Features

Features	Number of Devices		
	TI	**Fairchild**	**Pericom**
Total number of GTLP devices	13	10	7
3.3-V V_{CC} operation	12	5	3
Inputs/outputs 5-V tolerant	All	6	5
I_{off} – Partial power down *(protect device)*	All	All	All
PU3S - Hot insertion *(protect equipment)*	12	4	1
LFBGA package option	3	None	None
Backplane (GTLP/B-Port) Options			
BIAS V_{CC} - Live insertion *(protect data)*	10	1	1
Output edge control	All	All	All
TI-OPC circuitry	11	None	None
Edge-rate control	7	1	1
Medium drive (34/50 mA)	7	9	6
High drive (100 mA)	6	1	1
Functionality			
Transparent mode	12	7	6
Clocked mode	5	6	5
Latched mode	5	6	5
Clock enabled mode	4	5	4
Buffered clock option	2	3	2
1-to-6 TTL/LVTTL fanout driver	1	3	1

TI-OPC is a trademark of Texas Instruments.

21 What is important about live insertion?

Many backplane systems in communications applications must remain operational 24 hours a day, 7 days a week. These systems cannot be shut down when a board is inserted or removed from the system, as frequently happens during regular maintenance or system upgrades, nor can active backplane data be disturbed.

GTLP devices fully support live insertion with I_{off}, PU3S, and BIAS V_{CC} circuitry.

BIAS V_{CC} circuitry allows easy internal precharging of the daughter-card backplane connections to mid-threshold levels to prevent glitching active data during card insertion or removal.

In the typical connection sequence shown in Figure 15, the GND and BIAS V_{CC} connections are made first to establish the GND plane and precharge the GTLP I/Os through the BIAS V_{CC} circuitry to the 1.0-V ±50-mV threshold voltage. Next, the GTLP I/O pins are connected. Because the outputs are precharged to 1.0-V before connecting with the backplane, they do not glitch any active backplane data as they are mated. Finally, V_{CC} is connected. As V_{CC} ramps up, the BIAS V_{CC} precharge circuitry is disabled and the device starts operating, presenting valid signals on the backplane.

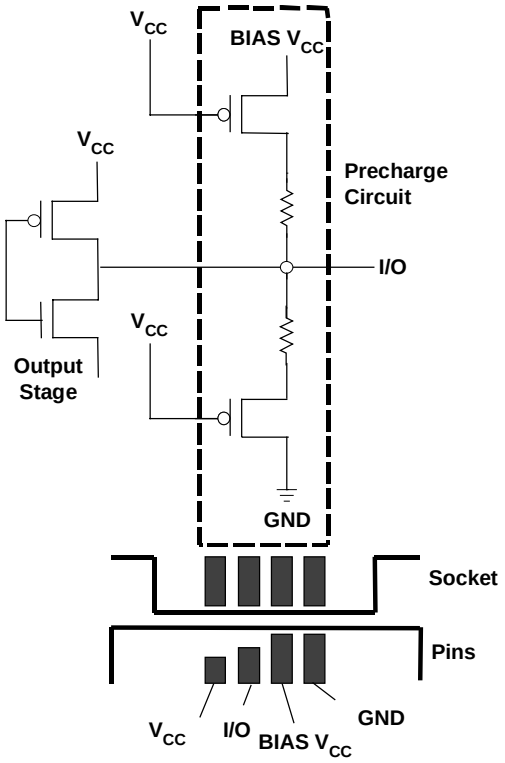


Figure 15. Typical BIAS V_{CC} Connection Sequence

22 What is the total power consumption of an 18-bit GTLP driver?

When you look at backplane performance, you must take into consideration static drive and dynamic drive. The static output drive is the current needed to maintain a steady-state dc voltage level on an output. Dynamic output drive is the current available when an output switches output states. This drive is necessary to overcome reactive loading effects and can determine the switching speeds in your applications.

Total power consumption is defined as the sum of the static (measured by the device I_{CC}), dynamic (measured by the device internal transistor switching), and output (measured by the external capacitive load) power of the device.

Static Power

$P_{STAT} = \Sigma \{V_{CC} [share_L(k) \times I_{CCL} + share_H(k) \times I_{CCH} + share_Z(k) \times I_{CCZ}]\} / n$

Where:

Σ = Sum of k = 1 to n

V_{CC} = Supply voltage

$share_L(k)$ = Average percentage share of the kth output in a low state

$share_H(k)$ = Average percentage share of the kth output in a high state

$share_Z(K)$ = Average percentage share of the kth output in a high-impedance state

I_{CCL} = Device current consumption for static low at output

I_{CCH} = Device current consumption for static high at output

I_{CCH} = Device current consumption for high-impedance state at output

n = Total number of outputs in the device

Example 1:

A 50% duty cycle output waveform on all outputs force $share_L(k)$ and $share_H(k)$ to be 0.5 each. $Share_Z(k)$ is zero. Therefore, for an 18-bit device, sum k = 1 to 18, static power is:

$P_{STAT} = \Sigma [V_{CC} (0.5 \times I_{CCL} + 0.5 \times I_{CCH} + 0 \times I_{CCZ})]/18 = 0.5\ V_{CC} (I_{CCL} + I_{CCH})$

Example 2:

A 50% duty cycle output waveform on nine outputs and nine outputs at a fixed static low. $share_Z(k)$ is zero. Therefore, for an 18-bit device, sum k = 1 to 9, the static power is:

$P_{STAT} = \Sigma [V_{CC} (0.5 \times I_{CCL} + 0.5 \times I_{CCH} + 0 \times I_{CCZ})] / 18 + \Sigma [V_{CC} (1 \times I_{CCL} + 0 \times I_{CCH} + 0 \times I_{CCZ})] / 18$

$P_{STAT} = 0.5 \times 0.5 \times V_{CC} (I_{CCL} + I_{CCH}) + 0.5 \times V_{CC} (I_{CCL}) = V_{CC} (0.75 \times I_{CCL} + 0.25 \times I_{CCH})$

I_{CCL}, I_{CCH}, and I_{CCZ} are identical for CMOS devices, but different for BiCMOS/bipolar devices. Normally, these are combined in CMOS-device data sheets, but, because both the GTL and GTLP families include both CMOS and BiCMOS devices, all values are included to preclude questions about whether all values are the same or only the maximum value was included.

Dynamic Power

While switching the outputs, most of the dynamic power is generated in the output structure of devices that have totem-pole configurations. Because GTL and GTLP devices have open-drain/collector outputs and no active pullup transistors, dynamic power caused by current spikes due to internal charging and discharging processes within the GTLP circuit can be approximated as a very small value that, in comparison to the static and output power, is negligible.

The Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C, March 1997, at www.ti.com/sc/docs/psheets/abstracts/app/scba009.htm, provides more information on how to calculate dynamic power consumption for devices with totem-pole outputs.

Output Power

Output power per bit is:

$P_{OUT} = I_{OL} \times V_{OL} \times (1 – \text{output duty cycle})$

Where

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2)$

Example:

For an output duty cycle of 60% (output stays high 60% of the cycle),

assuming $V_{TT} = 1.5$ V, $V_{OL} = 0.55$ V, and $R_{TT} = 38\ \Omega$, then:

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2) = (1.5\text{ V} – 0.55\text{ V}) / (38\ \Omega / 2) = 50\text{ mA}$

$P_{OUT} = I_{OL} \times V_{OL} \times (1 – \text{output duty cycle}) = 50\text{ mA} \times 0.55\text{ V} \times (1 – 0.6) = 11\text{ mW per bit}$

For an 18-bit device running all 18 bits at 60% output duty cycle,

$P_{OUT} = 18 \times 11\text{ mW} = 198\text{ mW}$

Total Power Consumption

Total power consumption for an 18-bit device operating at 3.3-V V_{CC} is calculated using the following equations. Nine outputs are switching at a 50% duty cycle with the other nine outputs at a fixed static low:

I_{CC} = 50 mA, V_{TT} = 1.5 V, V_{OL} = 0.55 V, and R_{TT} = 38 Ω

$P_{STAT} = V_{CC}\ (0.75 \times I_{CCL} + 0.25 \times I_{CCH}) = 3.3\ V\ (0.75 \times 50\ mA + 0.25 \times 50\ mA) = 165\ mW$

$I_{OL} = (V_{TT} – V_{OL}) / (R_{TT} / 2) = (1.5\ V – 0.55\ V) / (38\ \Omega / 2) = 50\ mA$

P_{OUT} switching = $I_{OL} \times V_{OL} \times$ (1 – output duty cycle) = 50 mA × 0.55 V × (1 – 0.5) = 13.75 mW/bit

P_{OUT} static low = $I_{OL} \times V_{OL} \times$ (1 – output duty cycle) = 50 mA × 0.55 V × (1 – 0) = 27.5 mW/bit

There are nine switching outputs and nine static low outputs, therefore:

P_{OUT} = 13.75 mW × 9 bits + 27.5 mw × 9 bits = 123.75 mW + 247.5 mW = 371.25 mW

The total power consumption is:

$P_{TOT} = P_{STAT} + P_{DYN} + P_{OUT}$ = 165 mW + 0 mW + 371.25 mW = 536.25 mW

The junction temperature of the device never must exceed 150°C. To determine if the total power consumption exceeds the maximum junction temperature for a certain package, calculate junction temperature using the following equation:

$T_J = R_{\Theta JA} \times P_{TOT} + T_A$

In the previous example, assuming a 56-pin TSSOP (DGG) package with high-K board and no airflow, the junction temperature is:

$T_J = R_{\Theta JA} \times P_{TOT} + T_A$ = 64°C/W × 0.53625 W + 25°C = 34.32°C + 25°C = 59.32°C

The $R_{\Theta JA}$ for all packages can be found at www.ti.com/sc/package

23 How should I generate the termination voltage?

GTLP backplanes require a high-current 1.5-V termination voltage that typically is driven from the 3.3-V V_{CC}. Typically, a 1.5-V, 7.5-A switcher provides the 1.5-V reference voltage. Currently, TI uses the LT1083CP (Linear Tech) for bus termination on our 48-bit high-drive SN74GTLPH1655 demonstration backplane. The high current is needed because there could be many open-drain GTLP outputs simultaneously sinking current on the bus, but, overall, it is less than Thevenin-terminated backplanes, such as are used with LVT devices. Unitrode also provides two devices that can be used. They offer low dropout at given current (500-mV dropout, maximum, at 5 A), ability to handle transients with tight regulation, high current capability, fast transient response, separate bias and V_{IN} pins, and 5-pin TO-220 and TO-263 packages with Kelvin sensing. The UC382 provides 3-A capacity; the UC385 provides 5-A capacity with fixed (1.5 V, 2.1 V, or 2.5 V) or adjustable output-voltage capability (see Figure 16).

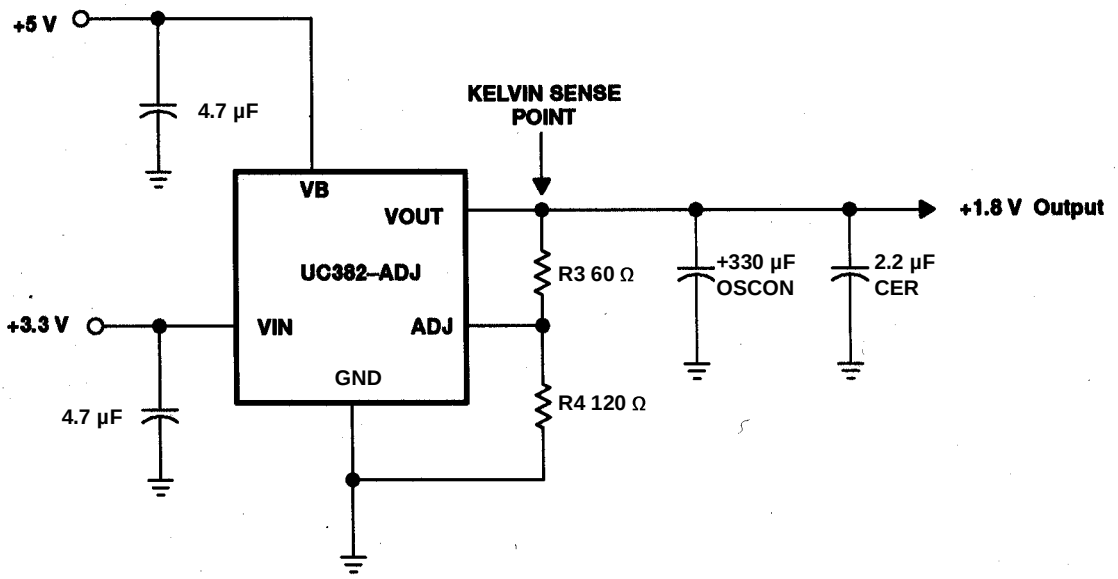


Figure 16. Kelvin-Sensing Circuit

24 Why not use Thevenin voltage dividers for termination?

Thevenin voltage dividers can be used as a termination scheme; resistors are easy to obtain and can be connected to the readily available 3.3-V power supply. However, this is not the optimal termination scheme. There are several reasons why voltage regulation is essential on GTLP backplanes:

- Static dc current through the termination - A Thevenin equivalent of two 50-ohm resistors to 3.3 V, with the backplane tied to the center connection, yields about 33 mA of constant dc current while the output driver is off (high state). Typically, terminations are the two extremes of the backplane, so the total is 66 mA for the backplane. When the device's output is on (low output state), current increases to about 112 mA because the lower termination resistor is bypassed through the 4-ohm GTLP device.

  Now, consider a 1.5-V regulated termination scheme. In the off output state, zero current flows because there is no path to ground from V_{TT} (termination voltage). While in the on state, this produces 80 mA of current. Therefore, as the output is switching states from low to high and vice versa, the average current flowing through the voltage-regulated termination is considerably lower than the Thevenin voltage-divider termination.

- Noise considerations - If the Thevenin voltage divider is tapped off the supply voltage of 3.3 V and the backplane termination voltage, V_{TT}, is taken from the center connection, any noise that is riding on the supply has now been coupled to V_{TT}. This could prove to be a problem because, if the noise is large enough, potentially it could interfere with the switching thresholds of the GTLP inputs. Voltage regulation eliminates this problem with a reliable voltage source. Ideally, a voltage regulator should be mounted at each end.

- Impedance matching – This probably is the most important reason for voltage regulation, because matching the loaded impedance of the backplane is essential to reduce or totally eliminate reflections that occur with improper termination. Using a Thevenin voltage divider is more difficult because one also has to adjust V_{TT} to be 1.5 V. The numbers used above are for V_{TT} of 1.65 V (half of 3.3 V), so the resistors have to be chosen to produce a 1.5 V V_{TT} and terminate the backplane properly. Although it sounds easy, in practice, it is not.

25 Tell me more about bus hold.

All GTLPH devices have bus hold on the A port and are described in the data sheet as "Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended." However, a note in the data sheet states "All unused inputs of the devices must be held at V_{CC} or GND to ensure proper operation." Don't these statements conflict?

No, A-port data inputs with bus-hold cells should not use a pullup or pulldown resistor, but, if required, a properly sized resistor that overrides the bus-hold cell can be used. The note refers to the control inputs, not the data inputs. The control inputs always must be tied low or high if unused or undriven and never allowed to float because the device would not operate properly. There is no bus-hold cell on any control input on any TI device.

26 Tell me more about power-up 3-State (PU3S).

Your GTLP data sheet states, "When /OEAB is low, the outputs are active." However, in the next paragraph about PU3S, the data sheet states: "To ensure the high-impedance state during power up or down, /OE should be tied to V_{CC} through pullup resistor," which means that /OE is high. This contradicts the previous statement. Should /OEAB be high or low?

The /OE should be pulled high to keep the device in the high-impedance state, even though it is featured with PU3S, which keeps the device in the high-impedance state, when V_{CC} is zero to 1.5 V, to prevent bus contention. The first statement assumes you are going to overdrive the pullup resistor when you want the outputs to be active and pull /OE to GND.

27 Should I tie GTLPH16612 control inputs to 3.3 V or to 5 V?

I need to tie the SN74GTLPH16612GR LEAB (pin 2) high for transparent operation and am not sure what voltage it should be tied to.

See the "V_I except B Port" specification in the data sheet, which is 5.5 V maximum. Confusion might arise because the GTLPH16612 has both a 3.3-V and 5-V V_{CC}. Other GTLP devices are 3.3-V V_{CC} only, and they list the nominal V_I as V_{CC} and maximum V_I as 5.5 V to show that the V_I normally is connected to 3.3 V, but you can go up to 5.5 V. In either case, you can use 3.3 V or 5 V, depending on which voltage is most convenient, but you would normally use 3.3 V for any GTLP device.

28 What do I do with unused or undriven GTLP A- or B-port I/Os?

As with any other logic device, it is important that unused or undriven inputs or inputs/outputs (I/Os) not be left floating. This prevents high current flow through the device if the input should reach the threshold level. There is no need to prevent the transistor outputs from floating as long as its input is tied to V_{CC} or GND. The following is recommended and summarized in Table 8:

- A port (LVTTL side of the device)
  - I/Os on all devices with bus hold
    Unused or undriven - No action required, bus hold will maintain last known logic state
  - Inputs on all devices without bus hold with inverted signals (currently, SN74GTLP817 only)
    Unused or undriven - Tie pin to V_{CC} with a 220-Ω up to 1-kΩ pullup resistor to maintain a logic high.
  - Inputs on all devices without bus hold with selectable true/complementary feature (currently, SN74GTLP1394 only)
    Unused or undriven - Tie pin to V_{CC} or GND with a 220-Ω up to 1-kΩ pullup resistor to maintain a logic high or low, depending on whether the device is in true or inverted mode of operation, and if signals are unidirectional or bidirectional, to keep the B port in its tied condition.

- B port (GTLP side of device)
  - I/Os on all devices
    Unused - Tie pin to ground with a 220-Ω up to 1-kΩ pulldown resistor to maintain a logic low.
    Undriven - No action required because the pin is pulled high to V_{TT} by the termination resistors.

Table 8. Control of Undriven or Unused Pins

	A I/O				B I/O	
	Bus Hold		No Bus Hold			
	True	Inverted	True	Inverted	True	Inverted
Undriven	No action required		Pull up to V_{CC}	Pull down to GND.	No action required	
Unused					Pull down to GND.	

Precharge - Each B-port I/O pin has its own precharge circuitry if the device is equipped with a BIAS V_{CC} pin. Because the precharge current is very low (<10 uA), if the pin is connected to GND, it does not reach 1-V precharge. However, other B-port I/O pins that are not connected to GND are properly precharged to 1 V.

29 Can I connect the SN74GTLPH16612GR unused I/O pins of the A ports and B ports directly to GND?

I have seen FSC's reference design and the unused pins were connected directly to ground. Per the GTLP FAQ, we cannot do that because there should be a resistor for safety purposes.

The A ports and B ports can be connected directly to GND on unused pins. Historically, there has always been a resistor used when tying the pin to V_{CC} or GND because it is required for bipolar inputs. It is not required for CMOS inputs (like those used on all GTLP devices) and the inputs can be tied directly to GND or V_{CC}. FSC's proposal to tie unused pins on both the A ports and B ports of the GTLPH16612 to GND is acceptable. Our GTLPH16612, is identical to the FSC GTLP16612, but with better B-port edge-rate slew control.

30 How does an extender card affect signal integrity?

I am designing a new card basket using GTLP and need to provide for an extender card. Should I leave it unterminated and hope it works OK, or terminate it lightly? How about terminating with a resistor in series with a capacitor? The dc pullup to 1.5 V will be taken care of on the backplane.

Leave it unterminated. There will be signal integrity problems if the extender card is used on the driver card, but the signal integrity will be OK if used on a receiver card. There will be about 20 pF extra loading and some additional line delay caused by the longer stub trace, but the receiver signal integrity should be close to what it was without the extender card, and other receiver cards should be mostly unaffected.

31 What is the transistor count for GTLP devices?

Table 9. GTLP Transistor Count

SN74GTLP	Function	Transistor Count
Medium Drive (50 mA)		
H306	Bus Transceiver	1246
817	1:6 Fanout Driver	266
H16612	Universal Bus Transceiver	3922
H16912	Universal Bus Transceiver	3325
H16916	UBT with Buffered Clock	3302
H16945	Bus Transceiver	2242
H32945	Bus Transceiver	4484
High Drive (100 mA)		
1394	Transceiver	367
H1612	Universal Bus Transceiver	3371
H1616	UBT with Buffered Clock	3371
H1645	Bus Transceiver	2062
H1655	Universal Bus Transceiver	3389
H3245	Bus Transceiver	4124

32 Can I use GTLP as a low-voltage translator?

Bidirectional voltage translations between 3.3-V LVTTL and low-voltage CMOS (LV-CMOS) are possible with GTLP devices. GTLP has a larger noise margin than general LV-CMOS interface devices and can support shift-up level conversion through the use of active transistors.

Two things must be considered:

- In the A-to-B (LVTTL to LV-CMOS) direction, V_{ref} must be within 0.6 V of the termination voltage because of the TI-OPC circuitry.
  - TI-OPC circuitry is featured on most GTLP devices (except ’817, ’16612, and GTL devices) and actively ports backplane energy to GND when the signal level is greater than 0.7 V above V_{ref}. This prevents large overshoots on improperly terminated or unevenly loaded backplanes during low-to-high signal transitions, which limits the subsequent undershoot that would reduce the upper noise margin. The TI-OPC circuitry is integrated into the design and cannot be deactivated, but is inactive when the B port is disabled. Except for the absolute maximum values, which must be met in all cases, there are no V_{TT} to V_{ref} voltage-difference restrictions in the LV-CMOS to LVTTL direction. Only in the LVTTL to LV-CMOS direction must V_{ref} be set within 0.6 V of the termination voltage.

- The data-sheet recommended termination voltage is limited to 1.14 V minimum and 1.65 V maximum to correspond to GTL and GTLP standards. So, these recommended data-sheet limits must be exceeded to translate at higher or lower voltages.
  - The GTLP design team reviewed the TI SPICE simulations at voltages outside the normal GTL/GTLP operating range and saw very little speed change when the termination voltage is out of the normal range. There should be no degradation in device reliability as long as the termination voltage does not exceed 2.75 V and the recommended current limit is observed. However, TI’s policy is not to recommend applications outside of data-sheet recommended limits. For some TI devices, we are looking at expanding the GTLP data sheet dc limits to cover these level-translation applications.

Table 10 shows the LV-CMOS device levels and possible voltage-translation combinations using GTLP devices. The recommended GTLP device V_{ref} settings for bidirectional and unidirectional A-to-B cases are shown. Normally, V_{ref} should be equal to the LV-CMOS threshold voltage (V_t), but it is adjusted to be within 0.6 V of the termination voltage V_{CC} to prevent activating TI-OPC circuitry in a steady-state condition.

Table 10. Bidirectional or Unidirectional B-to-A Voltage Translations

LV-CMOS Device		GTLP Device
Supply Voltage (V_{CC})	**Threshold Set Point (V_t)**	**Set V_{ref} To**
2.5 V	1.25 V	1.9 V
1.8 V	0.9 V	1.2 V
1.5 V	0.75 V	0.9 V
1.2 V	0.6 V	0.6 V
1.0 V	0.5 V	0.5 V
0.8 V	0.4 V	0.4 V

Table 11 shows possible voltage-translation combinations and recommended GTLP device V_{ref} settings for the unidirectional B-to-A case where TI-OPC circuitry is inactive. Additionally, since TI-OPC circuitry is not featured in the GTLP817, GTLPH16612, or any GTL devices, this table also can be used in all cases.

Table 11. Unidirectional B-to-A Voltage Translations

LV-CMOS Device		GTLP Device
Supply Voltage (V_{CC})	**Threshold Set Point (V_t)**	**Set V_{ref} To**
2.5 V	1.25 V	1.25 V
1.8 V	0.9 V	0.9 V
1.5 V	0.75 V	0.75 V
1.2 V	0.6 V	0.6 V
1.0 V	0.5 V	0.5 V
0.8 V	0.4 V	0.4 V

A pullup termination resistor is required only if operating in the A-to-B direction and can be between 50 Ω to 1 kΩ, depending on the transition times needed for the circuit.

Normally, V_{IH} and V_{IL} are ±50 mV around V_{ref} but expands to ±200 mV at 0.4 V as V_{ref} is reduced below 0.7 V.

33 What is the voltage input range I can apply to the B port if V_{ref} is set at 0.8 V?

I'm using the SN74GTLP1394 to convert a 1.2-V GTL and 1.5-V CMOS signal to LVTTL. Signal direction always is B to A. V_{ref} is set at 0.8 V. I'm concerned that the 1.5-V CMOS signal will be too high and that it will forward-bias ESD diodes on the B-port input.

GTLP devices can be used over a range of V_{TT} and V_{ref} voltages and this application is perfectly acceptable, with no danger to the ESD diodes. In the B-to-A direction, TI-OPC is disabled and there is no restriction on V_{TT} vs V_{ref} if they are within data-sheet limits. In the A-to-B direction, V_{TT} vs V_{ref} should be maintained at less than 0.6 V.

34 Can I use GTLP as a replacement for FB+ devices?

BTL-signal-level applications are extensions of the voltage-translation application. Normally, GTLP devices are not compatible with FB+ devices, as shown in Figure 17. However, closer inspection reveals that the upper and lower noise margin is about the same, and only threshold and termination voltages are different.

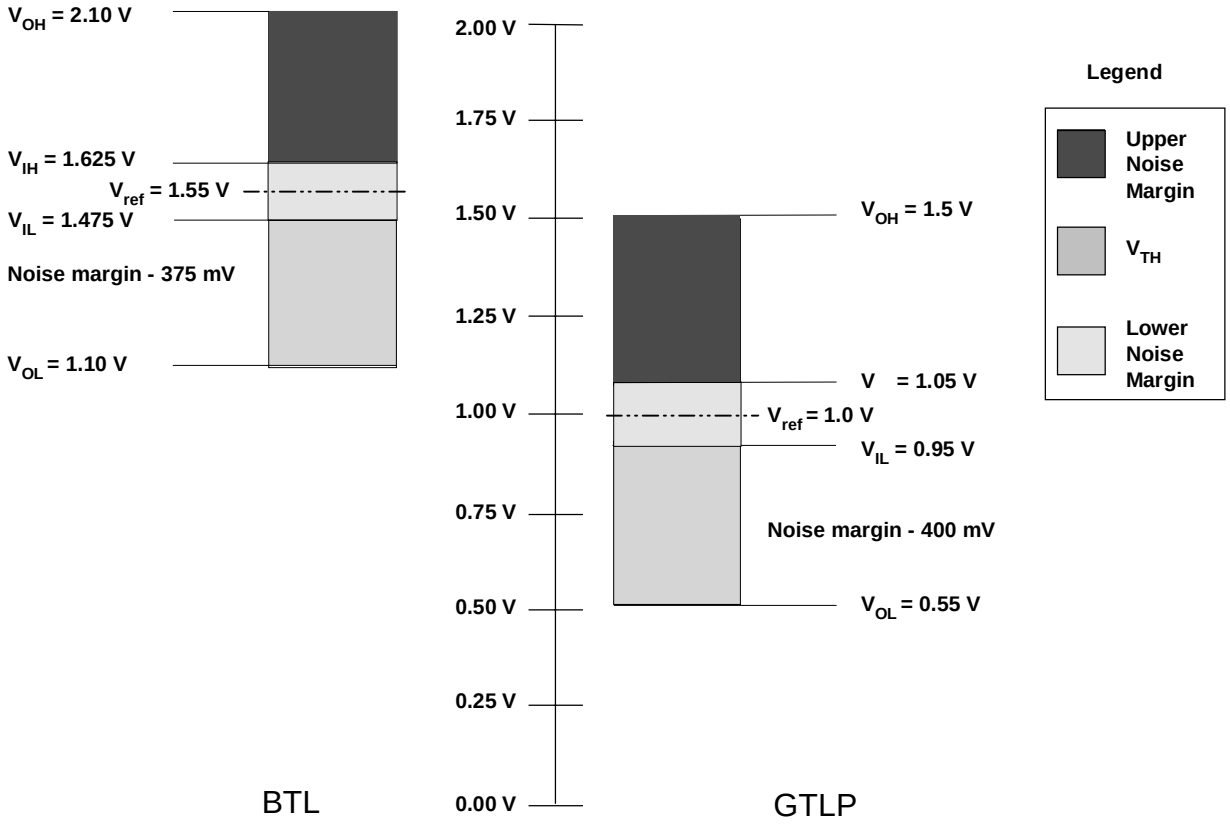


Figure 17. Comparison of BTL to GTLP Signal Levels

FB+ devices have a fixed differential input set at 1.55 V, whereas GTLP devices have a variable differential input that is set via the external V_{ref} control pin. GTLP V_{ref} is normally two-thirds of the termination voltage so that when V_{TT} is 1.5 V, V_{ref} is 1.0 V.

When GTLP devices are used in FB+ device applications, the resistor network is changed to R/3R so that V_{ref} is set at 1.575 V when V_{TT} is 2.1 V. The process is reversed easily from BTL to GTLP signal levels by changing the 3R resistor to 2R. Only high-drive GTLP devices should be used because FB+ devices also sink 100 mA of current. In actual applications, the high-drive GTLP device pulls the B-port V_{OL} lower than 1.1 V, with a corresponding increase in I_{OL}, so a higher-value termination resistor might be needed. SN74GTLPH1655 has been operated in the GTLP EVM at BTL levels with excellent signal integrity and a duty cycle of 50%.

TI's policy is not to recommend applications outside of data-sheet recommended limits, so, for some TI GTLP devices, we are expanding the GTLP data sheet dc limits to cover this application.

These expanded limits also will help in the cases where there may already be a 1.8-V or 2.0-V power supply on the board and the designer is hesitant to use GTLP because that means a 1.5-V power supply will have to be added. In this case, just use the 1.8-V power supply for V_{TT}.

35 I'm trying to determine which 3.3-V logic family will best fit my needs, and I'm still not quite clear on what choice I should make.

I'm looking for bus interface chips (e.g., 244s, 245s) to drive a backplane (tri-stateable bus). There will be five cards on the bus [one power-supply card, one microcontroller card (uC), one PCM card, and two fibre-channel interface cards (FCi)]. The bulk of the signals are between the two FCi cards and the PCM card. The FC data bus is the critical bus at 40 MHz, or maybe 80 MHz (undecided at this time). The data is sourced by one of the two FCi cards and passed to the PCM card. The data is synchronous with the system clock (40 MHz or 80 MHz) generated at the PCM card and goes to both FCi cards. It's important to maintain the phase relationship between this clock and the FC data-bus data. We will have a 72-bit unidirectional and 8-bit bidirectional bus, plus control signals. We have used FCT devices before and could get only up to about 25 MHz or so, and because this is a new design, there is a lot of flexibility on what we can choose. Other considerations include: 3.3-V power supply with some 5-V devices on the board, need industrial temperature range (prefer military) and desire high-density packages.

What device family would you recommend and why?

GTLP would work at both 40 and 80 MHz and is optimized for backplane applications. It uses a 3.3-V V_{CC} power supply and is 5-V tolerant. It is offered in industrial temperature ranges in several surface-mount and BGA packages. Military-temperature-range devices are being considered and can be requested at gtlp@list.ti.com.

What are the advantages and disadvantages?

There is excellent signal integrity at higher frequencies, pullup-resistor termination draws less power than totem-pole devices, there is no danger of bus contention on open-drain devices, and the BIAS V_{CC} pin provides for live insertion. The cost is two to three times higher than FCT or LVT, but, because these TIER-3 solutions didn't work, you need to move to a TIER-2 solution. Because you have so few cards, you could also consider a point-to-point solution with LVDS or SERDES devices. They will provide higher data throughput with lower skew, but at a higher cost. If you are comfortable with parallel single-ended devices, such as FCT, you will be very comfortable designing with GTLP, which provides a cost-effective solution at this performance node.

What devices would you recommend?

Use five SN74GTLPH16945GR (TSSOP) devices or two SN74GTLPH32945KR (LFBGA) and one SN74GTLPH16945KR (VFBGA) medium-drive devices. The SN74GTLPH16945GR is identical to the standard '16245 (48-pin 2 x 8 bit bus transceiver), except for the BIAS V_{CC} and V_{ref} pins in place of two of the V_{CC} pins. Out of the 80 possible bits, use 72 bits for the buffer (DIR is fixed) and 8 bits for the 8-bit transceiver. The minimum R_{TT} is 38 Ω for medium-drive devices and that should be acceptable for this backplane loading. If an even lower termination resistance is required to improve signal integrity or you need a slightly faster t_{pd}, the high-drive SN74GTLPH1645DGGR and/or the SN74GTLPH3245GKFR could be used. These are 100-mA versions of the medium-drive (50 mA) GTLPH16945/32945, with an edge-rate-control selection pin that allows for a slightly faster edge rate and reduced t_{pd}.

36 How do I get a GTLP data sheet?

GTLP product-preview data sheets, GTL production data sheets, and GTL1655/backplane design application reports are in the *GTL/GTLP Logic High-Performance Backplane Drivers* product information book, literature number SCED009, which can be ordered at http://www.ti.com/sc/gtlpbook or by calling the literature fulfillment center at 1-800-477-8924.

GTLP product-preview data sheets were revised in January 2001, with the latest copies available on the internet at http://www.ti.com/sc/gtlp. It is recommended that the most current data sheet be obtained after device selection.

GTLP product-preview data sheets do not contain ac specifications because the device is in development and the parameter values have not been finalized. Please contact your TI Technical Sales Representative, or the GTLP Team directly at gtlp@list.ti.com, if you need more specific information before the GTLP production data sheets are available on the internet.

GTL data sheets are available on the internet at http://www.ti.com/sc/gtl.

To conserve file space and save paper, package diagrams are included at the back of every data book and product information book, but are not included in the downloadable data sheets. Applicable package drawings can viewed, printed, or downloaded from the internet on the Logic Packaging Options page at http://www.ti.com/sc/package, under Package Drawings.

Also included on the Logic Packaging Options page are hyperlinks for Standard Packing Quantities, JEDEC Outlines, Package Thermal Data, Symbolization Guidelines, and PCB Design Guidelines.

37 When will GTLP models and devices be available?

GTLP devices are in various stages of development, with staggered HSPICE/IBIS model, preproduciton sample, and production sample availability. Please review the device summary table on the GTLP home page for model availability and the individual GTLP device data-sheet page on the Internet for device status (preview or active) or contact your TI sales representatives or the GTLP Team directly at gtlp@list.ti.com for the most up-to-date information and assistance.

38 How do I get IBIS Models?

IBIS models for all TI logic devices can be downloaded from the Internet at http://www.ti.com/sc/docs/tools/logic/models/ibis.htm.

Please ensure that the correct package and signal level (GTL or GTL+) is selected for GTL models.

IBIS models of the GTLP devices are available only at the GTLP signal levels, but all packages are included in the file, and they can be downloaded on the IBIS page.

39 How do I get HSPICE Models?

TI has pioneered new modeling technology and will offer encrypted Level-37 HSPICE models that can be downloaded directly from the internet without a confidentiality agreement. Encrypted HSPICE models for all GTLP devices will be available directly from the IBIS home page.

HSPICE models provide better device modeling capability than IBIS models. Generally, HSPICE is used for device simulation and IBIS is used for integrated board-level simulation. Unencrypted Level-37 HSPICE models require confidentiality agreements to protect TI device technology. Multiple files (device, package, process, other, readme, up to 12 total for each device) are sent for HSPICE models.

40 Why does the unencrypted Level-37 HSPICE model require a confidentiality agreement?

Confidentiality agreements are required because proprietary information that TI does not want disclosed to competitors is contained in the HSPICE model. The confidentiality agreement must be approved by both parties prior to sending a nonencrypted HSPICE model. Most GTL HSPICE models require a confidentiality agreement, whereas no GTLP HSPICE models do.

41 How should I request a confidentiality agreement?

Contact your TI Sales Representative or the GTLP technical team at gtlp@list.ti.com for assistance.

42 What does the encrypted HSPICE model zipped file contain?

The encrypted HSPICE model zipped file (for example, GTLPH16612) contains the following files:

GTLPH16612INC.INC
ASL2BSN37INC.INC
ASL2BSS37INC.INC
ASL2BSW37INC.INC
TSSOP56MOD
README.TXT
RUN.SP

Both encrypted and unencrypted Level-37 process models require a one-time patch from Avant!. for the HSPICE simulation software. Provide the following information to Jeff Brunson (jeffb@ti.com) (972-480-2481) and the patch will be provided at no charge:

Company Name:
Full Address:
Contact Name:
Contact E-mail:
Node ID:

43 If the file is encrypted, why do we need the one-time patch from Avant!?

Level 37 is a model TI created to work under HSPICE. Avant! licenses Level 37 to TI and requires TI to provide authorization to distribute the Level-37 model. This method gives TI and Avant! legal protection. The Level-37 patch is required, regardless of whether or not the model is encrypted.

The license process requires that:

- TI customer must have their own copy of Avant! HSPICE.
- TI requests that the Level-37 license be sent to the TI customer.
- The license is good for 1 year and is renewable.

44 How do I request preproduction samples?

There is no charge for preproduction samples. We generally try to limit the number to five or fewer, but you can request more if required for your application. Please contact your Texas Instruments Technical Sales Representative, the GTLP Team directly at gtlp@list.ti.com, or use the GTLP sample request form on the GTLP home page.

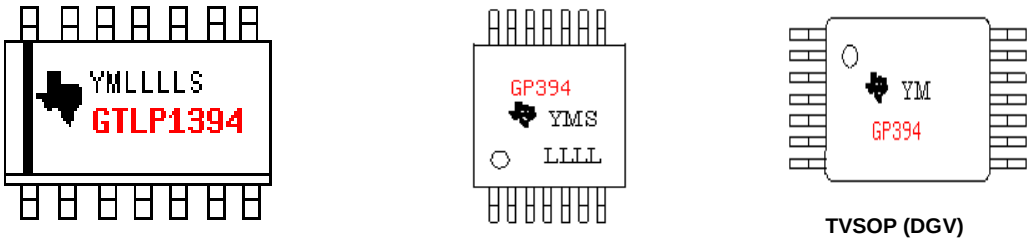
45 How do I request production samples?

Request production samples through the Extranet and your TI&Me account.

To sign up for TI&Me visit: https://www-a.ti.com/apps/ti_me/signin.asp?referer=corp

46 I requested the SN74GTLP1394, but the topside marking is GP394.

The 16-pin packages are too small to accommodate the full device name, so SN74GTLP1394 is shortened as shown in Figure 18 (not to scale or with correct pin count). Lot codes also are marked on the D and PW packages (Y = year, M = month, LLLL = lot code, S = assembly site). Only the year and month are marked on the DGV packages due to space constraints.



Narrow Body SOIC (D) TSSOP (PW) TVSOP (DGV)

Figure 18. SN74GTLP1394 Top-Side Marking

Device symbolization is explained on the Texas Instruments SLL Logic Package Options page at http://www.ti.com/sc/package under Symbolization Guidelines.

Package case assignment is found on the Package Name Rule Assignments page at http://www.ti.com/sc/docs/products/logic/package/pkrule.htm

Case A, B, and C symbolization names can be found on the Device Name Rules page at http://www.ti.com/sc/docs/products/logic/package/namerule.htm

As a convenience, GTLP device symbolization is listed in Table 12.

Table 12. GTLP Device Symbolization

SN74GTLP	SOIC	SSOP	TSSOP	TVSOP	LFBGA
Medium Drive (50 mA)					
H306	GTLPH306		GH306	GH306	
817	GTLP817		GT817	GT817	
H16612		GTLPH16612	GTLPH16612		
H16912			GTLPH16912	GL912	
H16916			GTLPH16916	GL916	
H16945			GTLPH16945	GL945	GL945
H32945					GM945
High Drive (100 mA)					
1394	GTLP1394		GP394	GP394	
H1612			GTLPH1612		
H1616			GTLPH1616		
H1645			GTLPH1645	GL45	GL45
H1655			GTLPH1655		
H3245					GM45

Updated GTLP data sheets include a new table that provides an orderable part number and top-side marking for every package combination.

47 How can I request additional technical support?

These and other helpful application reports to be released in the future are at http://www.ti.com/sc/docs/apps/logic/appnotes.html under Backplane Logic:

- Thin Very Small-Outline Package (TVSOP) application report, literature number SCBA009C
- 32-Bit Logic Families in LFBGA Packages 92- and 114-Ball Low Profile Fine-Pitch BEA Package application report, literature number SCEA014
- Fast GTLP Backplanes With the GTLPH1655, literature number SCBA015A
- High-Performance Backplane Design With GTL+, literature number SCEA011A
- Basic Design Considerations for Backplanes, literature number SZZA016A

Specific technical questions not covered by the application reports, or any general question, can be sent directly to the GTLP team at gtlp@list.ti.com.

Understanding Advanced Bus-Interface Products

SCAA029
May 1996

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In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

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Introduction

The purpose of this application report is to assist the designers of high- or low-performance digital logic systems in using the Advanced System Logic (ASL) families: LV, LVC, LVT, ALVC, ABT, ABTE, ALB, GTL, FB, and CBT. A family introduction, followed by a detailed comparison of the electrical characteristics, is provided to help designers understand the differences between these products. In addition, typical data is provided to give the hardware designer a better understanding of how these families operate under various conditions.

Device Family Overview

ABT Family

The ABT family is Texas Instruments (TI) second-generation family of BiCMOS bus-interface products. It is manufactured using the latest 0.8-µ BiCMOS process, and provides high drive up to 64 mA and propagation delays below the 5-ns range, while maintaining very low power consumption. ABT products are well suited for live-insertion applications with an I_{off} specification of 0.1 mA. To reduce transmission-line effects, the ABT family has series-damping resistor options. Furthermore, there are special ABT parts that provide extremely high-current drive (180 mA) to transmit down to 25-Ω transmission lines. Advanced bus functions, such as universal bus transceivers (UBT™), perform a wide variety of bus-interface functions. Multiplexing options for memory interleaving and bus upsizing or downsizing also are provided. ABT devices are available in octal, Widebus™, or Widebus+™. Widebus™ and Widebus+™ packages feature higher performance with reduced noise and flow-through pinout for easier board layout. In addition, Widebus+™ devices have bus-hold circuitry on the inputs to eliminate the need for external pullup resistors for floating inputs.

ABTE Family

ABTE provides wider noise margins and is backward-compatible with existing TTL logic. ABTE devices support the VME64-ETL specification, with tight tolerances on skew and transition times. ABTE is manufactured using the latest 0.8-µ BiCMOS process and provides high drive up to 90 mA. Other features include a bias pin and internal pullup resistors on control pins for maximum live-insertion protection. Bus-hold circuitry eliminates external pullup resistors on the inputs and series-damping resistors on the outputs damp reflections.

ALVC Family

The highest performance 3.3-V bus-interface family is the ALVC family. These specially designed 3-V products are processed in 0.6-µ CMOS technology, giving typical propagation delays of less than 3 ns, along with current drive of 24 mA and static power consumption of 40 µA for bus-interface functions. ALVC devices have bus-hold cells on inputs to eliminate the need for external pullup resistors for floating inputs. The family also includes innovative functions for memory interleaving, multiplexing, and interfacing to synchronous DRAMs. The ALVC family is available in the Widebus™ footprint with advanced packaging, such as shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP).

CBT Family

In today's computing market, power and speed are two of the main concerns. CBT addresses both of these issues in bus-interface applications. CBT enables a bus-interface device to function as a very fast bus switch, effectively isolating buses when the switch is open, and causing very little propagation delay when the switch is closed. These devices function as high-speed bus interfaces between computer-system components such as the central processing unit (CPU) and memory. CBT devices also can be used as 5-V to 3.3-V translators, allowing designers to mix 5-V or 3.3-V components in the same system. CBT devices are available in advanced packaging, such as SSOP and TSSOP for reduced board area.

FB Family

The Futurebus (FB)-series devices are used for high-speed bus applications and are fully compatible with the IEEE 1194.1-1991 (BTL) standard. These transceivers are available in 7-, 8-, 9-, and 18-bit versions with TTL and BTL translation in less than 5-ns performance. Other features include drive up to 100 mA and bias pins for live-insertion applications.

GTL Family

GTL technology is a new reduced-voltage switching standard that provides high-speed, point-to-point communications, with low power dissipation. TI offers GTL/TTL translators to interface with the TTL-based subsystems. Designers use the GTL-switching standards for speed-sensitive subsystems, and use the translators to interface with the rest of the system. GTL devices feature innovative circuitry, such as bus hold on the TTL inputs, to eliminate the need for external pullup resistors for floating inputs, which reduces power, cost, and board-layout time. Output edge-rate control (OEC™) is offered on the outputs to reduce electromagnetic interference (EMI) caused by the high frequencies of GTL. Industry-leading packaging, such as SSOP and TSSOP, is available for higher performance and reduced board space.

LV Family

TI's LV CMOS technology products are specially-designed parts for 3-V power supply use with the same 5-V performance characteristics of HCMOS logic. The LV family is a 2-µ CMOS process that provides up to 8 mA of drive, and propagation delays of 18 ns maximum, while having a static power consumption of only 20 µA for both bus-interface and gate functions.The LV family is available in the octal footprint with advanced packaging, such as small-outline integrated circuit (SOIC), SSOP, and TSSOP.

LVC Family

TI's LVC logic products are specially designed parts for 3-V power supply use, with about the same performance as the 5-V 74F family. The LVC family is a high-performance version with 0.8-µ CMOS process technology, 24-mA current drive, and 6.5-ns maximum propagation delays for driver operations. The LVC family includes both bus-interface and gate functions, with 50 different functions planned.The LVC family is available in the octal and Widebus™ footprints with advanced packaging, such as SOIC, SSOP, and TSSOP. Many LVC devices are available with 5-V tolerant inputs and outputs.

LVT Family

The specially designed 3-V LVT family uses the latest 0.8-µ BiCMOS process technology for bus-interface functions. Like its 5-V ABT counterpart, LVT provides up to 64 mA of drive, 4-ns propagation delays, and in addition, consumes less than 100 µA of standby power. The bus-hold feature eliminates external pullup resistors and I/Os that can handle up to 7 V, which allows them to act as 5-V/3-V translators.The LVT family is available in octal and Widebus™ footprints with advanced packaging, such as SOIC, SSOP, and TSSOP.

LVTZ Family

The LVTZ family offers all of the features found in TI's standard LVT family. In addition, LVTZ incorporates circuitry to protect the devices in live-insertion applications. The device goes to the high-impedance state during power up and power down, which is called power-up 3-state (PU3S). The LVTZ family is available in the octal footprint with advanced packaging, such as SOIC, SSOP, and TSSOP.

Detailed Comparison

The major subject areas covered in this application report are:

- Input characteristics
- Maximum input slew rate
- Output characteristics (drive capability)
- 5-V tolerant inputs/outputs
- Power consideration
- Package power dissipation
- Output capacitance
- ac characteristics
- Advanced packaging
- Bus hold
- Partial power down and live-insertion capability
- Power-up and power-down high impedance
- Additional design considerations for GTL and BTL/FB

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such. All devices used in this application report are of the Widebus™ families, except for LV, which uses octal devices instead (Widebus™ packages are not available).

For more information on TI logic products, please contact your local TI field sales office or an authorized distributor, or call Texas Instruments at 1-800-336-5236.

This application report provides engineers with the information necessary for a better understanding of TI advanced logic products. These products vary from low speed; low drive to high speed; and high drive with multiple power grades, depending on the technology, as well as the power supply. This report discusses in more detail the characteristics of these families, including:

- I/O structure and impedance
- Maximum input slew rate that is tolerated before the device begins to oscillate
- Ability of I/Os to retain data when powered down (selected families only)
- Ability of output to remain in high-impedance state when V_{CC} is ramping up or down
- Ability of 3.3-V inputs and outputs to withstand and drive 5-V signals
- Live-insertion capability (selected families)
- ac characteristics, such as power consumption, noise immunity, capacitive loading, speed, ground bounce, rise and fall time, skew, and packaging

Each family performs uniquely, depending on the design application. Understanding these characteristics will help designers choose the right family for the best design. This comparison reveals that TI provides a compelling solution in both point-to-point and backplane environments.

Several devices from each family were used to study the various performance levels. Characterization boards with standard loads (as specified in data sheets) were used in most cases to perform the laboratory work supporting this application report. A 10-MHz input frequency was used, unless otherwise noted. A resistive termination to both V_{CC} and GND was used, except for FB and GTL, which require a resistive load to V_{CC} only. Figure 1 illustrates all switching standards that are used in this application report.

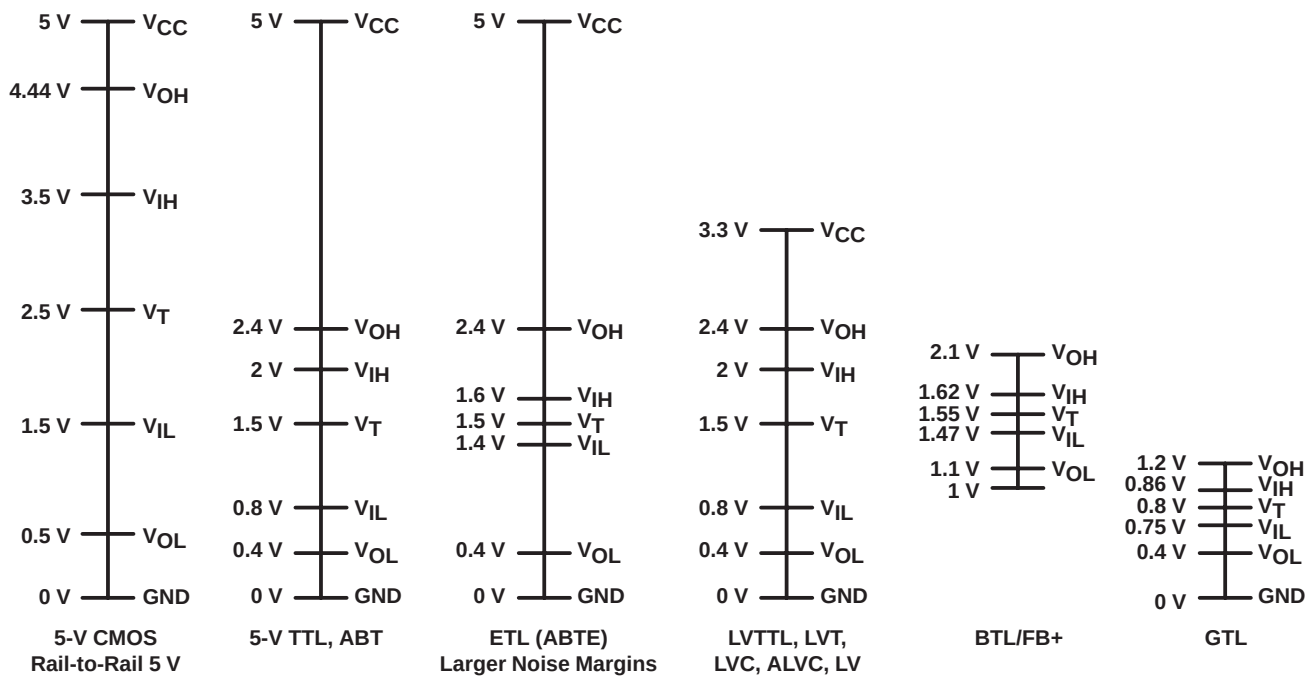


Figure 1. Switching Standards With Guaranteed Thresholds

Input and Output Characteristics

In recent years, CMOS and BiCMOS logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. However, when designing with such technologies, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer stipulates, as well as designing within the data sheet specifications. Since data sheets do not cover the input and output behavior in detail, this section explains the input and output characteristics of CMOS, BiCMOS, GTL, and BTL/FB families. Understanding the behavior of these inputs and outputs results in more robust designs and fewer reliability concerns.

CMOS and BiCMOS Input Characteristics

Both advanced CMOS (ALVC, LVC, and LV) and BiCMOS (ABT, LVT, GTL A port and FB A port) families have a CMOS input structure. The input is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND, as shown in Figures 2 and 3. When a low level is applied to the input, the p-channel transistor is ON and the n-channel is OFF, resulting in the current flowing from V_{CC} and pulling the node to a high state. When a high level is applied, the n-channel transistor is ON and the p-channel is OFF and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to be turned on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 V to 2 V). The supply current (I_{CC}) can rise up to several milliamperes (mA) per input, peaking at approximately 1.5-V V_{IN} (see Figure 4). However, this is not a problem when switching states at the data-sheet-specified input transition time (see Table 1).

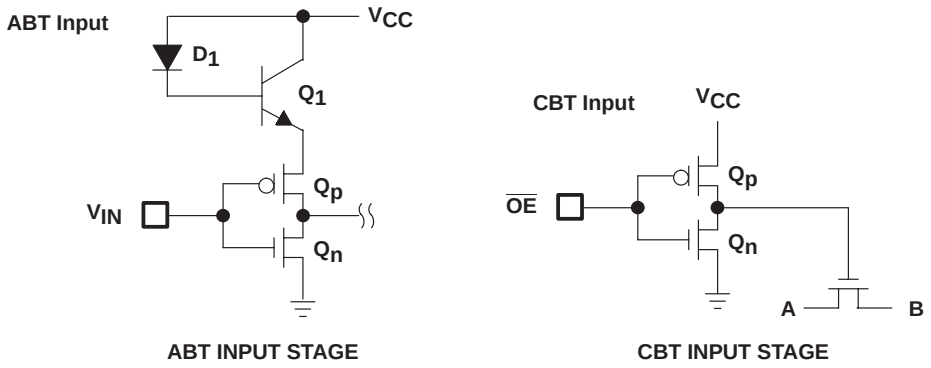


Figure 2. Typical Input Cell for 5-V Families

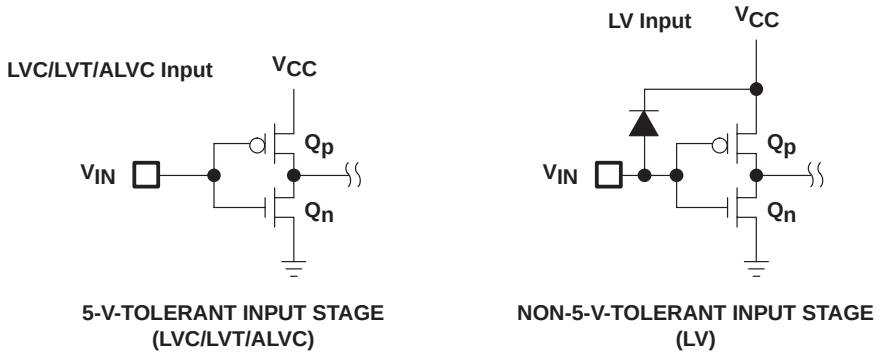


Figure 3. Typical Input Cell for 3.3-V Families

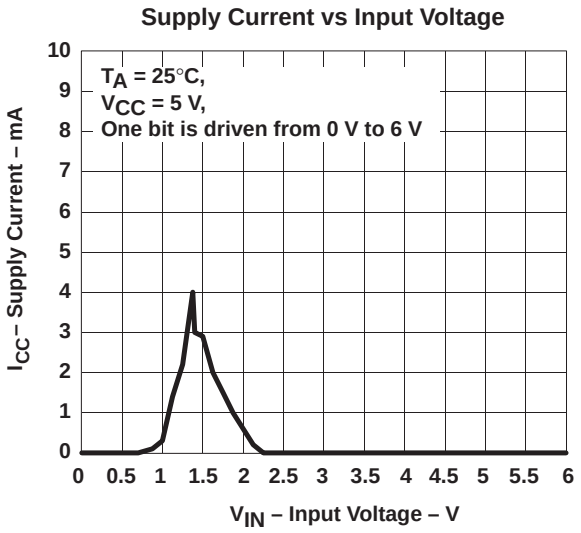


Figure 4. Supply Current vs Input Voltage (ABT – One Input)

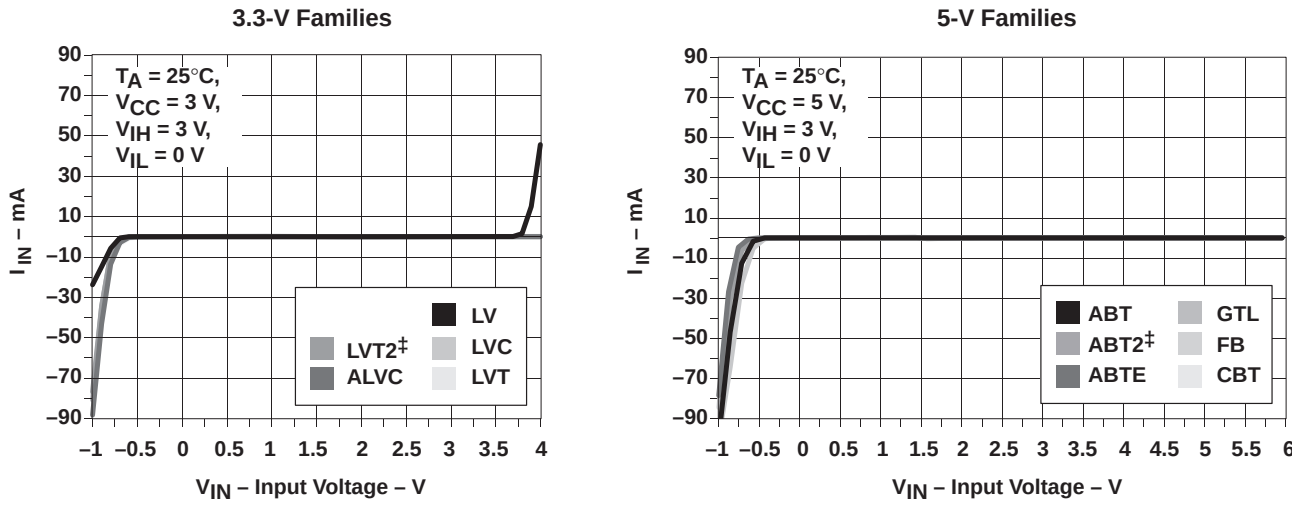
Table 1. Input Transition Rise or Fall Rate as Specified in Data Sheets

recommended operating conditions

		MIN MAX	UNIT
$\Delta t/\Delta v$ Input transition rise or fall rate†	ABT octals, FB (A port)	5	ns/V
	ABT Widebus™, Widebus+™	10	
	LVT, LVC, ALVC, GTL (A port)	10	
	LV	100	

† Unless otherwise noted in data sheets

Figure 5 shows the input characteristic impedance of both 3.3-V and 5-V families. One can see the effect of the clamping diodes when the input is below ground (all families) and above V_{CC} for LV only.



‡ Octal, Widebus, and Widebus+ devices with series damping resistor on the output (25 Ω typical)

Figure 5. Input Characteristics Impedance of 3.3-V and 5-V Families

BiCMOS Output Characteristics (ABT and LVT)

Figure 6 is a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low, turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 will charge the base of Q2, pulling it high and turning on the Darlington pair, consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications. LVT I/Os have characteristics similar to ABT, with added CMOS pullup and pulldown for rail-to-rail switching.

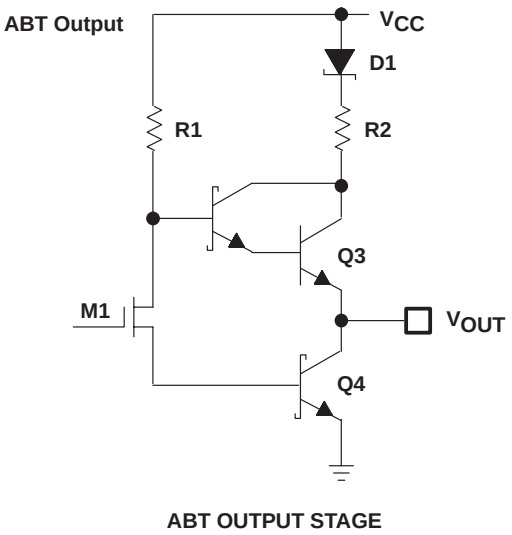


Figure 6. Typical Output Cell for 5-V Families

Figure 7 shows a simplified LVT output and illustrates the mixed-mode capability designed into the output stage. This combination of a high-drive TTL stage, along with the rail-to-rail CMOS switching, gives the LVT series exceptional application flexibility. These parts have the same drive characteristics as 5-V ABT devices and provide the dc drive needed for existing 5-V backplanes. Thus, using LVT is a simple way to reduce system power via the migration to 3.3-V operation. Not only can LVT devices operate as 3-V- to 5-V-level translators by supporting 5-V input or I/O voltages (V_{CC} = 2.7 V to 3.6 V), but also the inputs can withstand 5.5 V, even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down and live-insertion applications.

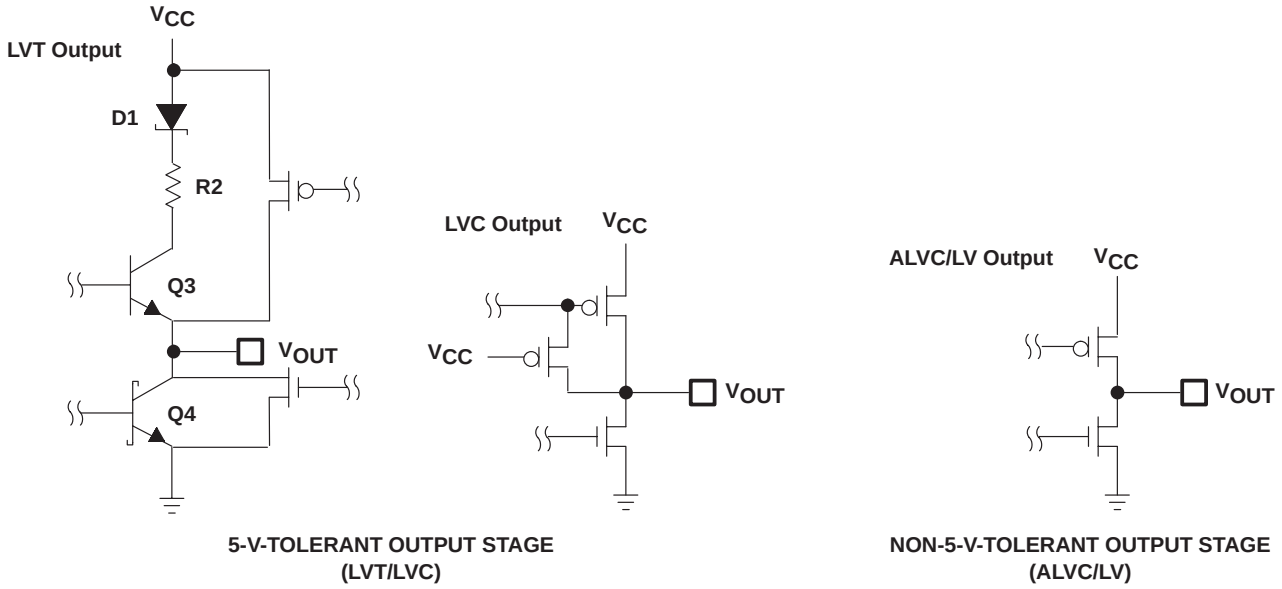


Figure 7. Typical Output Cell for 3.3-V Families

CMOS Output Characteristics (ALVC, LVC, and LV)

Figure 7 also shows a simplified LV, LVC, and ALVC output stage. LV and ALVC are pure 3.3-V families. They cannot be used to translate between 5-V and 3.3-V environments. ALVC is currently the fastest CMOS logic available. It is used primarily for high-speed memory and point-to-point applications with medium drive capability (±24 mA). LV is designed for low-speed, low-drive (±8–6 mA) applications. It is similar to HC and HCT. LVC, on the other hand, is used for on-board and memory applications that require medium performance and medium drive logic, as well as translation between 5-V and 3.3-V signals. These parts have the same drive characteristics as ALVC devices. Not only can LVC devices operate as 3-V- to 5-V-level translators by supporting 5.5-V input or I/O voltages (V_{CC} = 3 V to 3.6 V), but the inputs can withstand 5.5 V, even when V_{CC} = 0 V. This permits the devices to be used under partial system power-down and live-insertion applications.

The I_{OH}/V_{OH} and I_{OL}/V_{OL} curves for the above familes are shown in Figures 8 and 9. With their specified I_{OL} and I_{OH}, some of these families will accommodate many standard bus specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave. CBT, on the other hand, has no drive capability; its output impedance is purely resistive (V = I*R) as shown in Figures 2, 8, and 9.

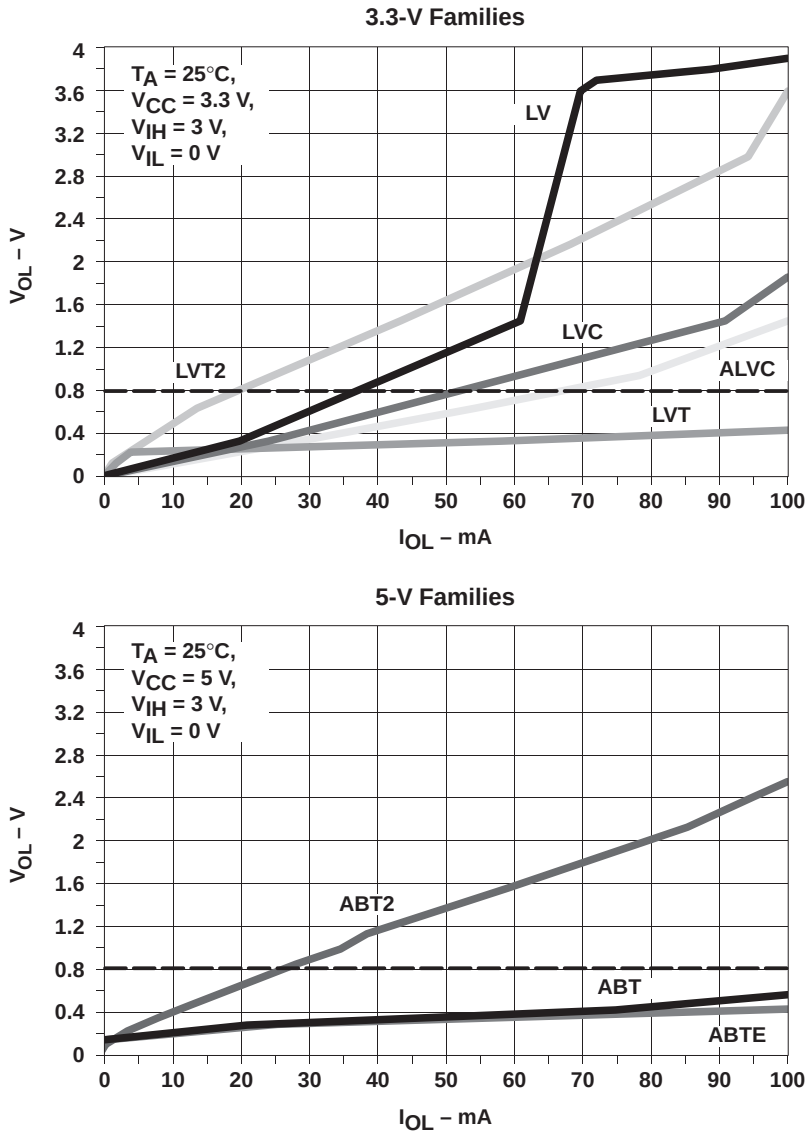


Figure 8. Output-Low Characteristic Impedance of 3.3-V and 5-V Families

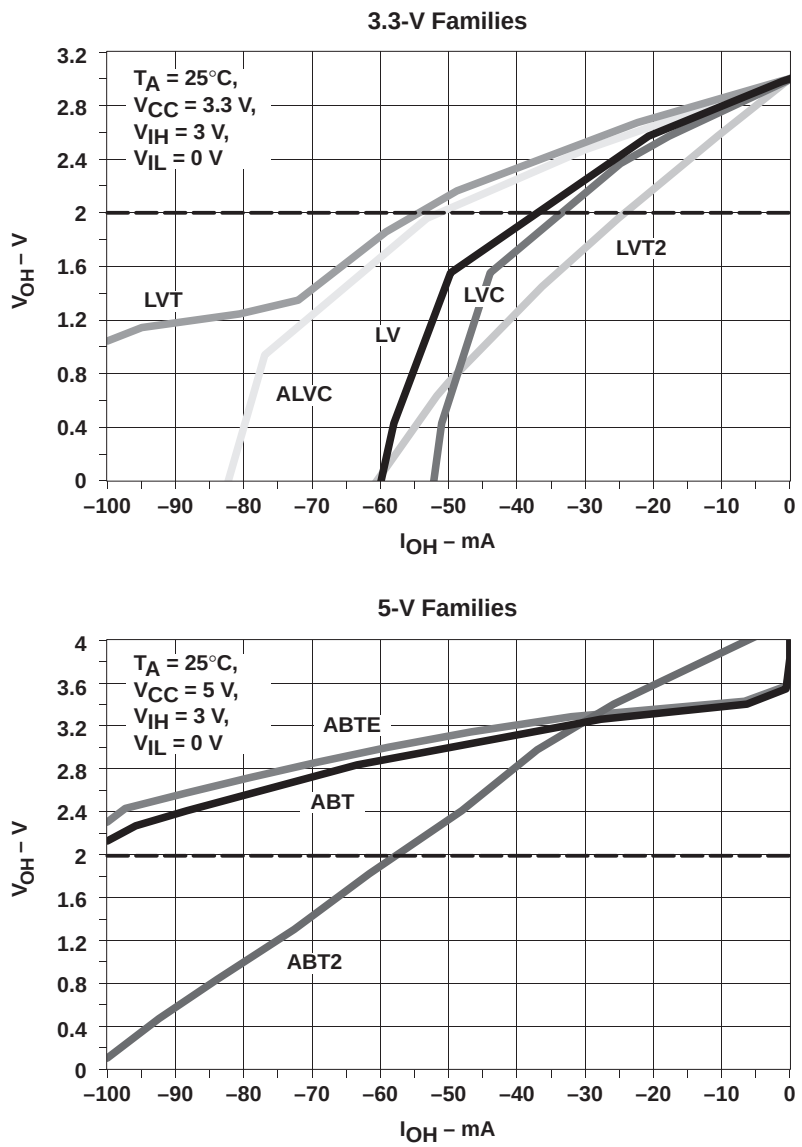


Figure 9. Output-High Characteristic Impedance of 3.3-V and 5-V Families

Incident-Wave Switching

Incident-wave switching ensures that, for a given transition (either high-to-low or low-to-high), the output reaches a valid V_{IH} or V_{IL} level on the initial wave front (i.e., does not require reflections). Figure 10 shows potential problems a designer might encounter when a device does not switch on the incident wave. A shelf below V_{IL}(max), signal A, causes the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case where there is a shelf in the threshold region. When this happens, the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. Signal C will not cause a problem because the shelf does not occur until the necessary V_{IH} level has been attained.

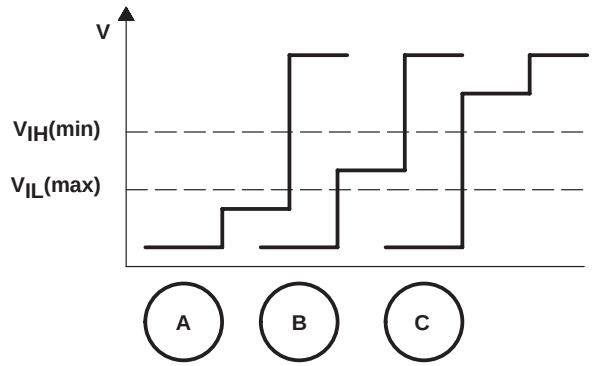


Figure 10. Reflected-Wave Switching

Using typical V_{OH} and V_{OL} values, along with data points from the curves, one can calculate the typical impedance the device can drive. For example, an ABT device can typically drive a line (from either end) in the 25-Ω range on the incident wave. However, if the same line is driven from the middle, the effective impedance seen by the driver is half its original value (12.5 Ω), which requires more current to switch it on the incident wave.

For a low-to-high transition, (I_{OH} = 85 mA @ V_{OH} = 2.4 V):

$$Z_{LH} = \frac{V_{OH}(\text{min}) - V_{OL}(\text{typ})}{I_{OH}} = \frac{2.4\ \text{V} - 0.3\ \text{V}}{85\ \text{mA}} = 25\ \Omega \quad (1)$$

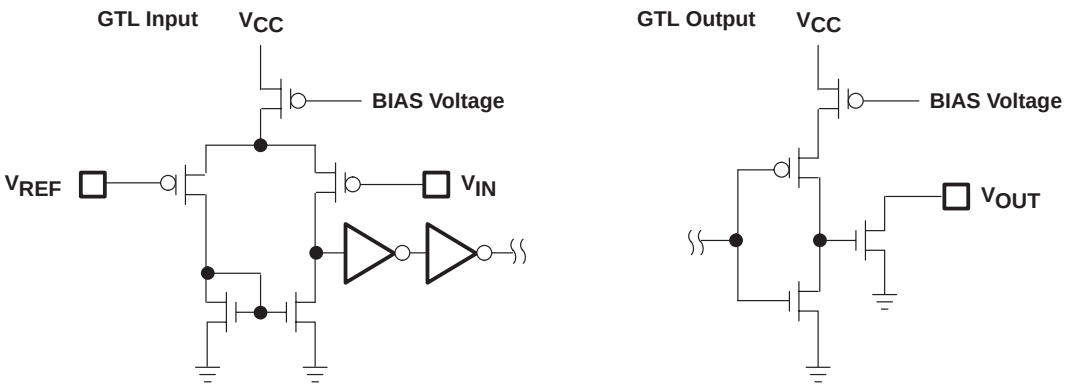
For a high-to-low transition, (I_{OL}= 135 mA @ V_{OL}= 0.5 V):

$$Z_{HL} = \frac{V_{OH}(\text{typ}) - V_{OL}(\text{max})}{I_{OL}} = \frac{3.5\ \text{V} - 0.5\ \text{V}}{135\ \text{mA}} = 22\ \Omega \quad (2)$$

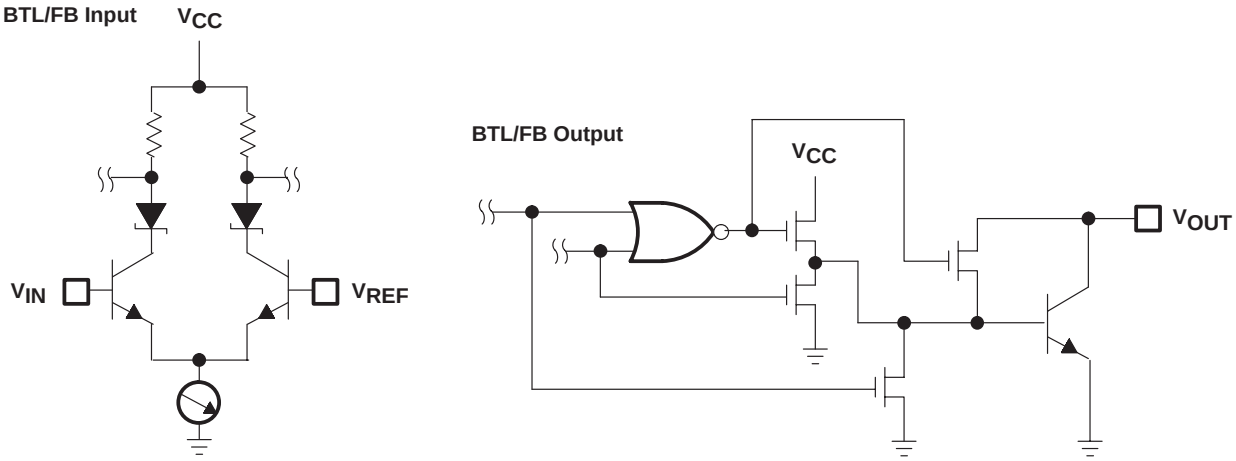
GTL and BTL Input/Output Structure

BTL and GTL buffers are designed with minimal output capacitance (5-pF max), compared to a TTL output buffer (8-pF to 15-pF typ). A TTL or a CMOS output capacitance, coupled with the capacitance of the connectors, the traces, and the vias, reduces the characteristic impedance of the backplane. For a high-frequency environment, this phenomenon makes it difficult for the TTL or CMOS driver to switch the signal on the incident wave. A TTL or CMOS device needs a higher drive current than is presently available to be able to switch the signal under these conditions. However, increasing the output drive clearly increases the output capacitance. This scenario again reduces the characteristic impedance even more. That is why a lower-signal-swing family with reduced output capacitance, like BTL or GTL, is recommended when designing high-speed backplanes.

The GTL input receiver is a differential comparator with one side connected to the reference voltage (V_{REF}), which is provided externally (0.8-V typ). The threshold is designed with a precise window for maximum noise immunity (V_{IH} = V_{REF} + 50 mV and V_{IL} = V_{REF} – 50 mV). The output driver is an open-drain n-channel device that, when turned off, is pulled up to the output supply voltage (V_{TT} = 1.2-V typ), and when turned on, the device can sink up to 40 mA of current (I_{OL}) at a maximum output voltage (V_{OL}) of 0.4 V. The output is designed for a doubly-terminated 50-Ω transmission line (25-Ω total load). The I/Os are designed to work independently of the device's V_{CC}. They can communicate with devices designed for 5-V, 3.3-V, or even 2.5-V V_{CC}. The TTL input is a 5-V-tolerant, 3.3-V CMOS inverter (can interface with 5-V TTL signals). Bus hold is also provided on the TTL port to eliminate the need for external resistors when the I/Os are unused or floating. The TTL output is a bipolar output. It is similar to the LVT output structure. The family requires two power supplies to function: a 5-V supply [$V_{CC(5)}$] for the GTL I/Os and 3.3-V supply [$V_{CC(3.3)}$] for the LVTTL I/Os. The 5-V supply is used only on the GTL16612 and GTL16616. The maximum frequency at which the current family operates is 95 MHz (GTL16612 and GTL16616). Future functions such as GTL16622 and GTL16922, will be available as samples in early 1996 and will be released at the end of the year. They run as high as 200 MHz in both directions (GTL-to-TTL or TTL-to-GTL) and have a single 3.3-V power supply. GTL16922 has 5-V-tolerant TTL I/Os. Figure 11 shows a typical GTL input and output circuit and Figure 12 shows their characteristic impedance. Since GTL has an open-drain output, only the I_{OL}/V_{OL} curve is displayed.



GTL B-PORT INPUT AND OUTPUT STAGE



BTL/FB B-PORT INPUT AND OUTPUT STAGE

Figure 11. Typical GTL and BTL/FB Input and Output Cells

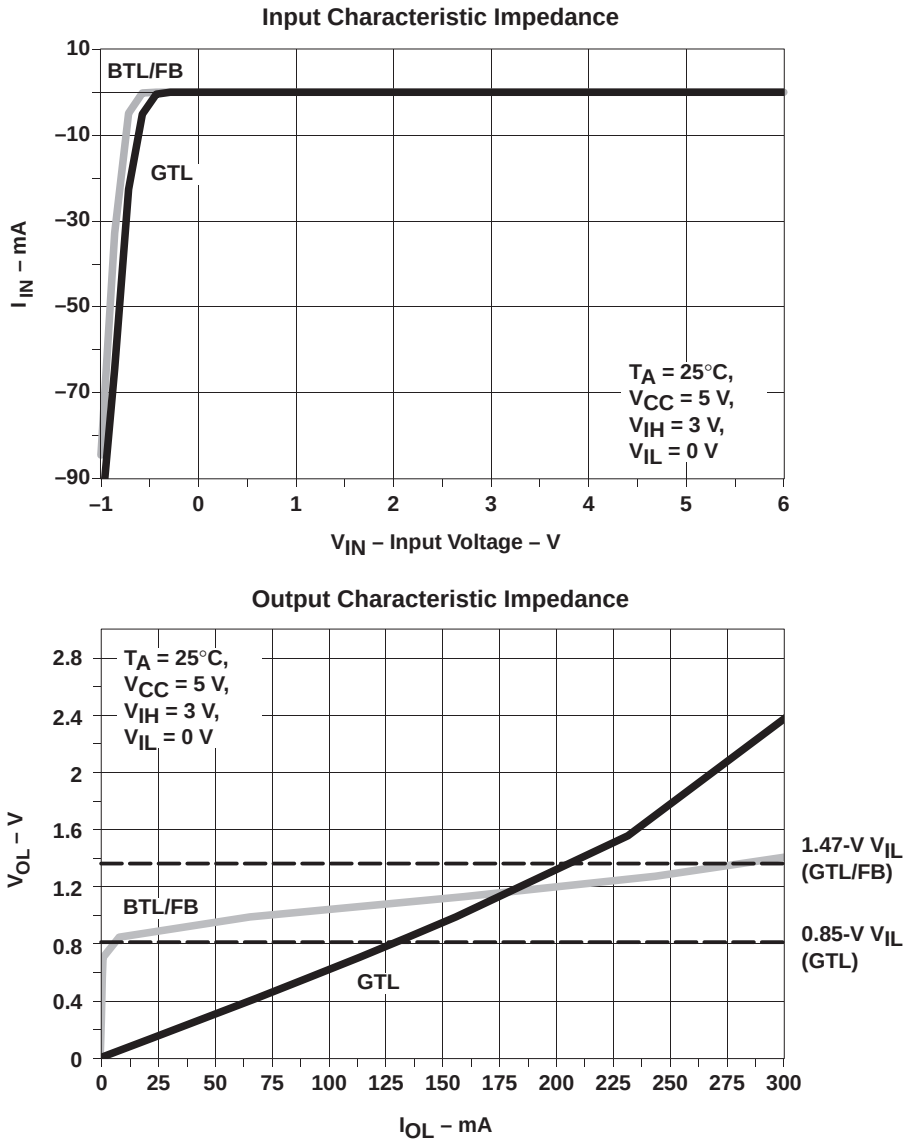
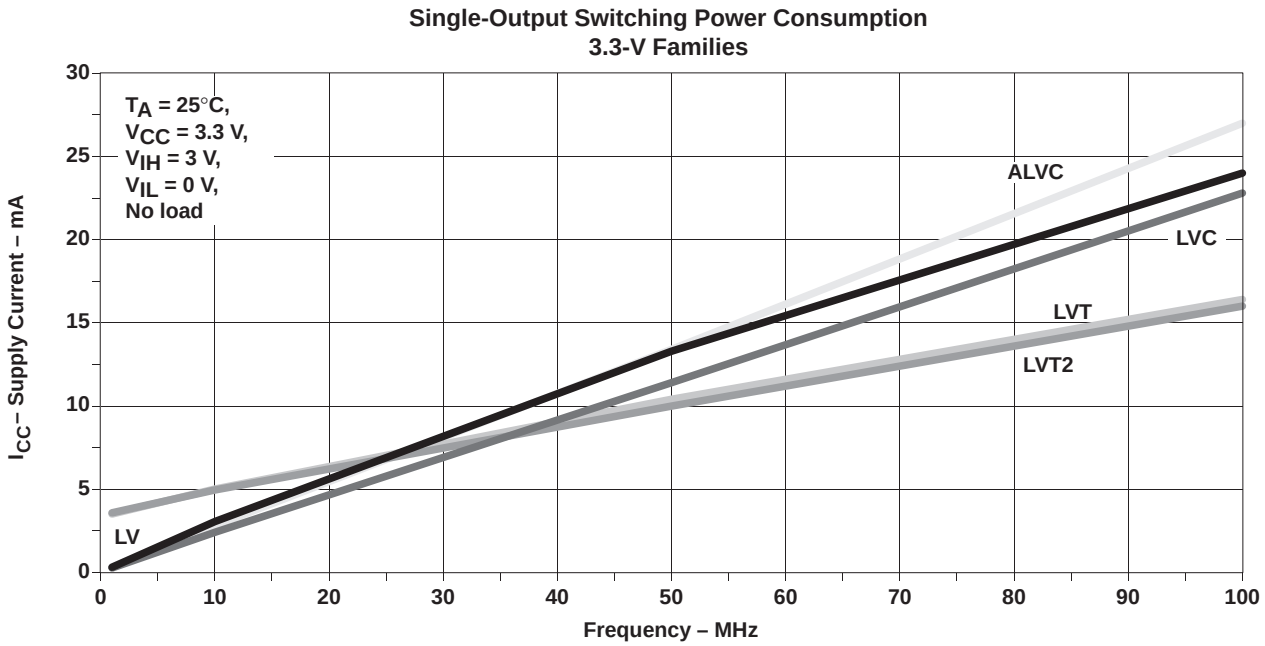


Figure 12. GTL and BTL/FB Input and Output Characteristic Impedance

The BTL input receiver is a differential amplifier, with one side connected to an internal reference voltage. The threshold is designed with a narrow window (V_{IH} = 1.62 V and V_{IL} = 1.47 V). Unlike GTL, BTL requires a separate supply voltage for the threshold circuit. It eliminates any noise generated by the switching outputs. The output driver is an open-collector output with a termination resistor selected to match the bus impedance. When the device is turned off, the output is pulled up to output supply voltage (V_{TT} = 2.1-V typ). The I/Os work independently of the device's V_{CC}; they communicate with devices designed for 5-V or 3.3-V V_{CC}. The TTL input is a 5-V CMOS inverter and the output is a bipolar output similar to the ABT output structure. BTL requires three power supplies: the main power supply (V_{CC}), the bias generator supply (BG V_{CC}), and the bias supply voltage (BIAS V_{CC}) that establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected. The recommended frequency at which the family runs is in the 30-MHz to 75-MHz range, depending on the application as well as the board layout. Figure 11 shows a typical BTL input and output circuit and Figure 12 shows their characteristic impedance. Since BTL has an open-collector output, only the I_{OL}/V_{OL} curve is displayed.

Power Consumption

Several factors influence the power consumption of a device: frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance of the device. The maximum operating frequency is limited by the thermal characteristics of the package. TI provides package power-dissipation information in data sheets under “absolute maximum ratings”. These numbers are calculated using a junction temperature of 150°C and a board trace length of 750 mils (no airflow). Refer to the *Package Thermal Considerations* application report in the ABT data book for the relationship between junction temperature and reliability. Traces, power planes, connectors, and cooling fans play an important role in improving the heat dissipation. Figures 13 through 15 show the typical power consumption with single- or all-outputs switching. Figure 16 also shows the maximum frequency at which a family can operate and still meet the V_{OH} and V_{OL} specifications. No frequency beyond the maximum number is acceptable. Note that all registered devices were tested based on the clock frequency, and the nonregistered devices were tested based on the input frequency.



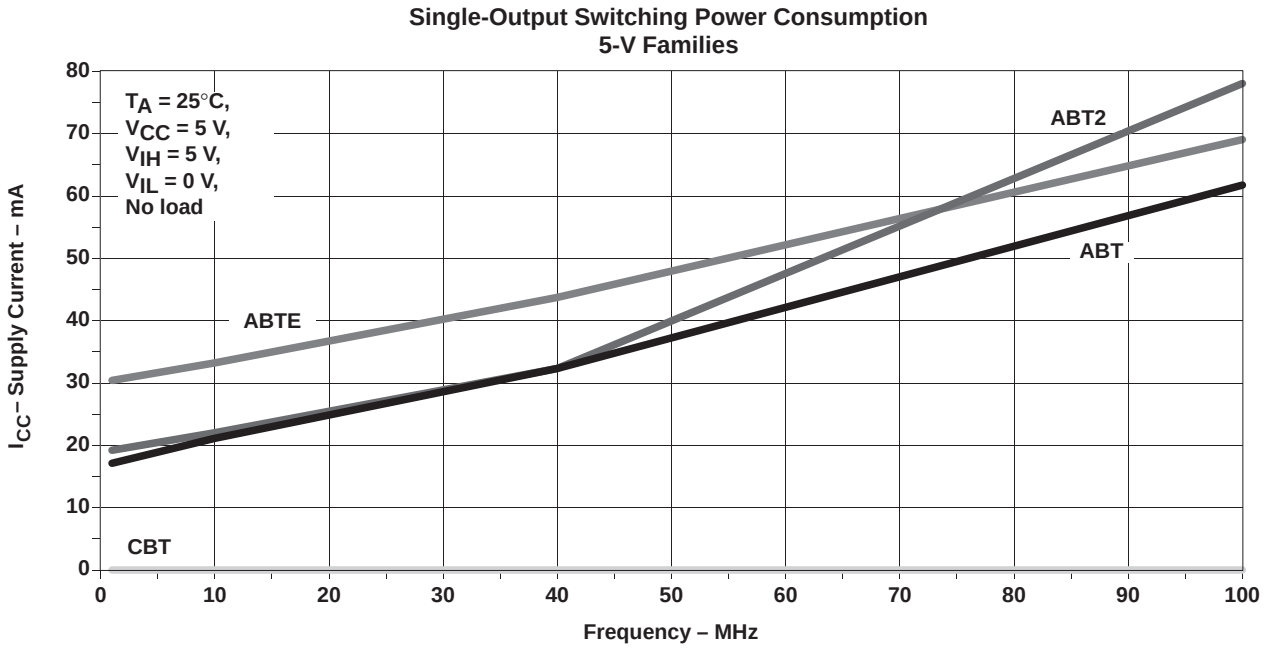
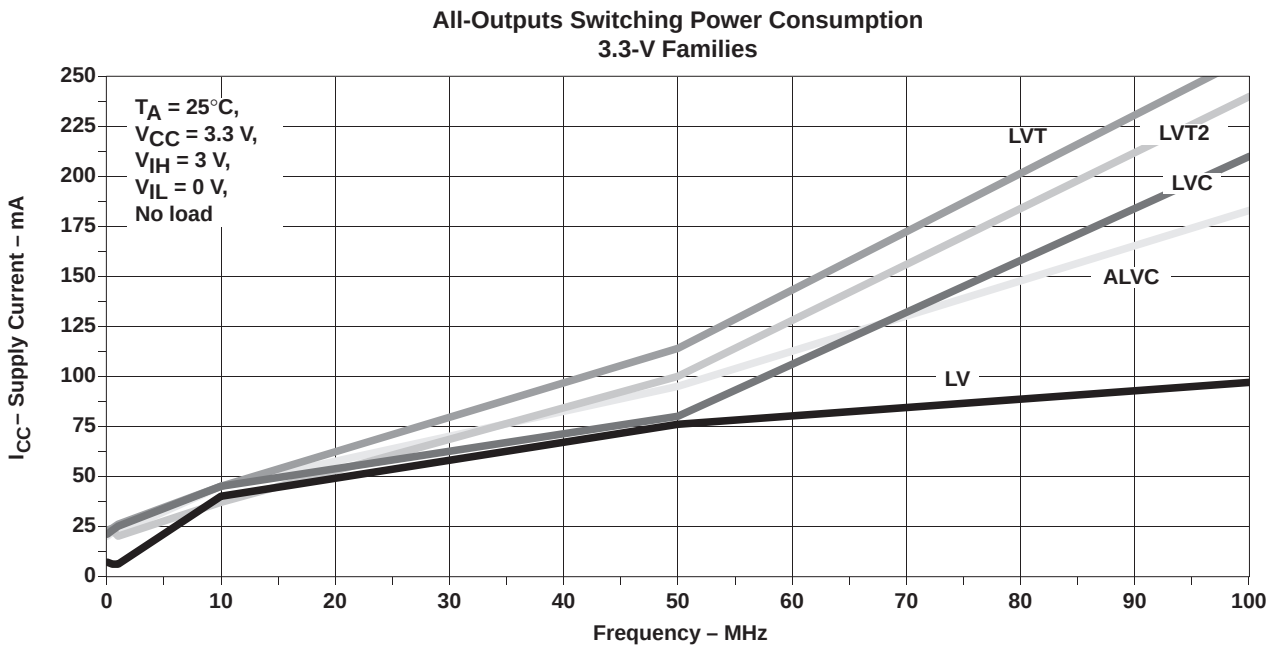


Figure 13. Power Consumption With Single-Output Switching



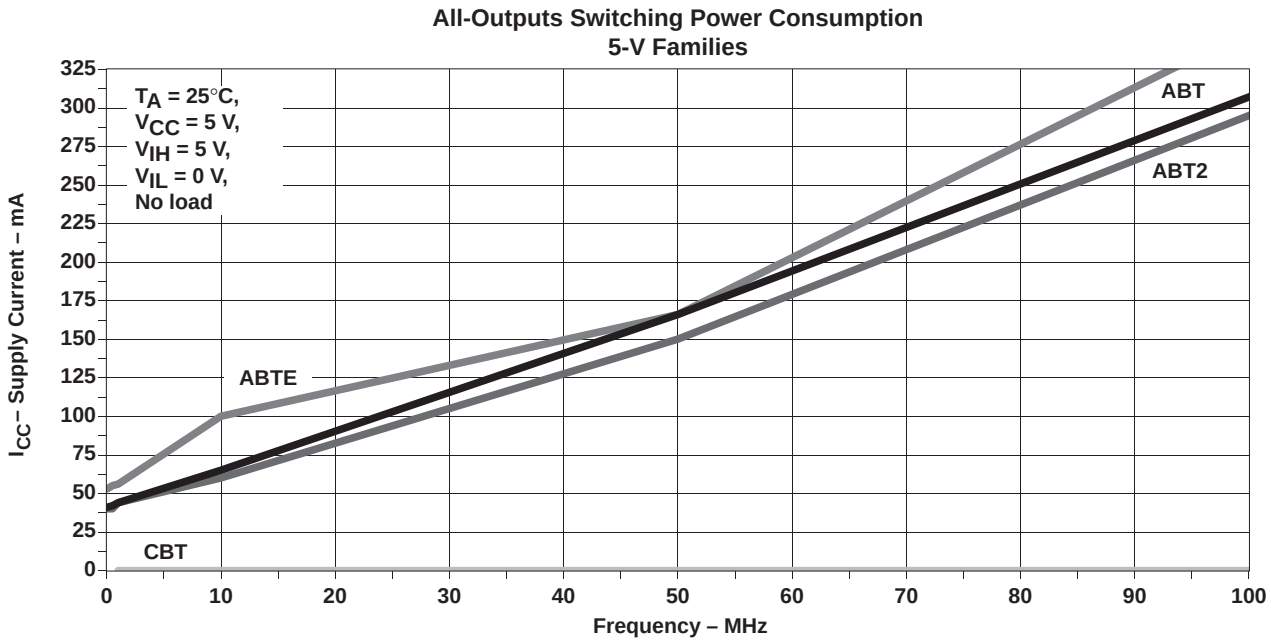


Figure 14. Power Consumption With All-Outputs Switching

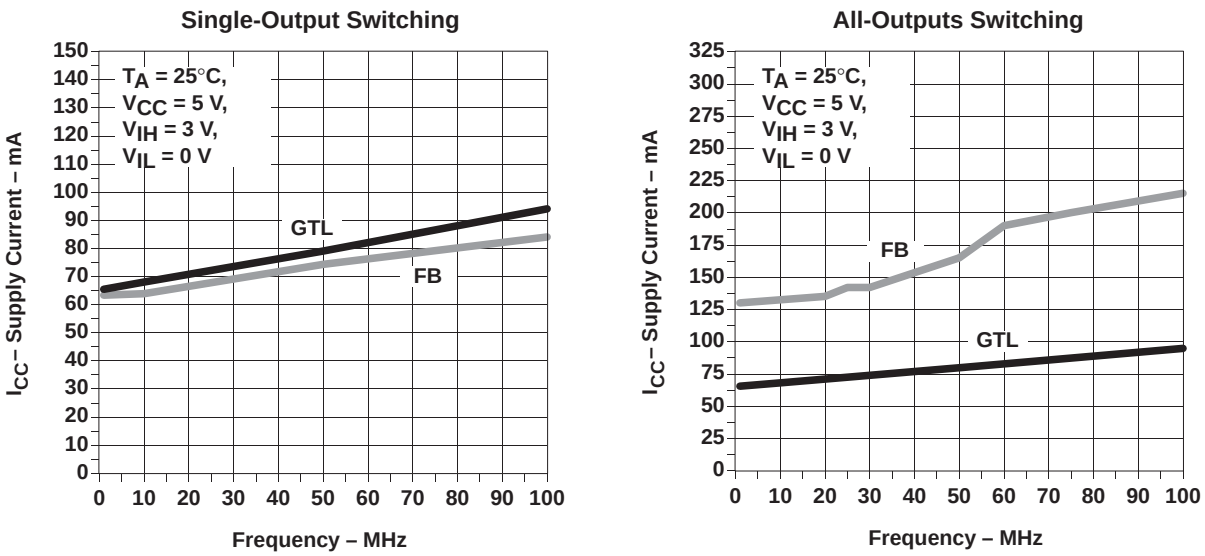
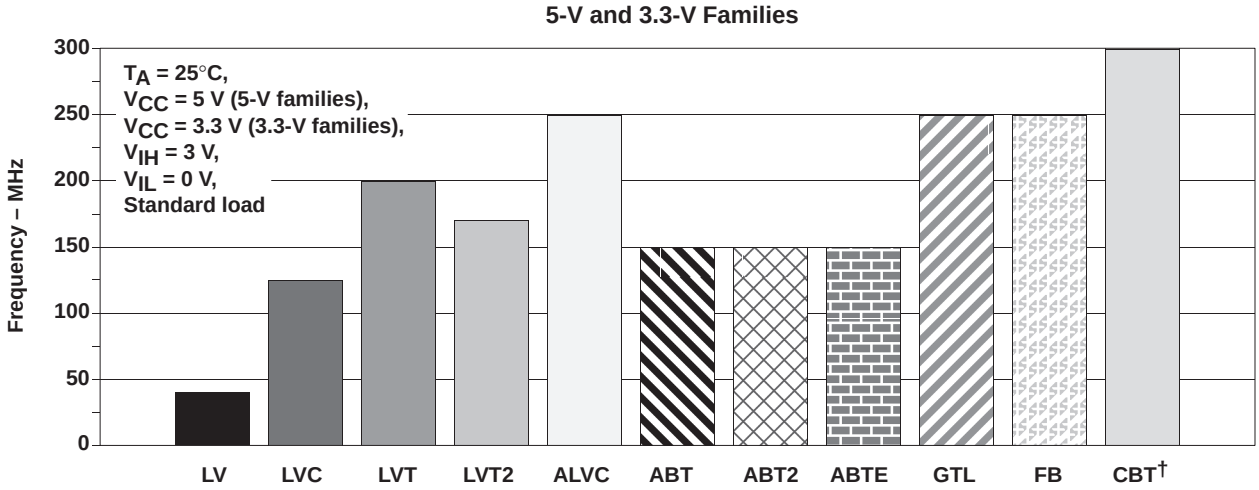


Figure 15. FB1650 and GTL16612 Power Consumption With Single- and All-Outputs Switching



† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 16. Functional Frequency Using Standard Load Specified in Data Sheets

Power Calculation

When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values are given in the individual data sheets. All inputs or I/Os (except GTL or BTL I/Os), when driven at TTL levels, consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not completely turned off. This value is known as ΔI_{CC} and is provided in the data sheet.

Dynamic power consumption results from charging and discharging both internal parasitic capacitances and external load capacitance. The parameter for CMOS devices that accounts for the parasitic capacitances is known as C_{pd}. It is obtained using equation 2 and is found in the data sheet.

$$C_{pd} = \frac{I_{CC}(\text{dynamic})}{V_{CC} \times f_i} - C_L \quad \textbf{(3)}$$

Where:

f_i = Input frequency (Hz)
V_{CC} = Supply voltage (V)
C_L = Load capacitance (F)
I_{CC} = Measured value of current into the device (A)

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC}-versus-frequency curves display essentially the same information (see Figures 13 through 15). The slope of the curve provides a value in the form of mA/(MHz × bit) that, when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current.

Equations 4 through 7 are used to calculate total power for CMOS or BiCMOS devices:

$$P_T = P_{S(tatic)} + P_{D(ynamic)} \quad \textbf{(4)}$$

CMOS

CMOS-level inputs

$$P_S = V_{CC} \times I_{CC} \quad \textbf{(5)}$$

$$P_D = \left(C_{pd} \times f_i + C_L \times f_o\right) \times V_{CC}^2 \times N_{sw} \quad \textbf{(6)}$$

TTL-level inputs

$$P_S = [I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad \textbf{(7)}$$

$$P_D = \left(C_{pd} \times f_i + C_L \times f_o\right) \times V_{CC}^2 \times N_{sw} \quad \textbf{(8)}$$

BiCMOS

Note: $\Delta I_{CC} = 0$ for bipolar devices.

$$P_S = V_{CC}\left[DC_{en}\left(N_H \times \frac{I_{CCH}}{N_T} + N_L \times \frac{I_{CCL}}{N_T}\right) + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right] \quad \textbf{(9)}$$

$$P_D = [DC_{en} \times N_{sw} \times V_{CC} \times f_i \times (V_{OH} - V_{OL}) \times C_L] + [DC_{en} \times N_{sw} \times V_{CC} \times f_2 \times I_{CCD}] \times 10^{-3} \quad \textbf{(10)}$$

Where:

V_{CC} = Supply voltage (V)
I_{CC} = Power supply current (A) (from the data sheet)
I_{CCL} = Power supply current (A) when outputs are in low state (from the data sheet)
I_{CCH} = Power supply current (A) when outputs are in high state (from the data sheet)
I_{CCZ} = Power supply current (A) when outputs are in high-impedance state (from the data sheet)
ΔI_{CC} = Power supply current (A) when one input is at a TTL level (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)
DC_d = % duty cycle of the data (50% = 0.5)
N_H = Number of outputs in high state
N_L = Number of outputs in low state
N_{sw} = Total number of outputs switching
N_T = Total number of outputs
N_{TTL} = Number of inputs driven at TTL levels

f_i = Input frequency (Hz)
f_o = Ouput frequency (Hz)
f_1 = Operating frequency (Hz)
f_2 = Operating frequency (MHz)
V_{OH} = Output voltage (V) in high state
V_{OL} = Output voltage (V) in low state
C_L = External load capacitance (F)
I_{CCD} = Slope of the I_{CC}-versus-frequency curve (mA/MHz × bit)

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device, with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

Package Power Dissipation

Thermal awareness became an industry concern when surface-mount technology (SMT) packages began replacing through-hole (DIP) packages in PCB designs. Circuits operating at the same power enclosed in a smaller package meant higher power density. To add to the issue, systems required increased throughput, which resulted in higher frequencies, increasing the power density even further. Not only do these same issues concern designers today, they are getting progressively more severe.

Figure 17 explains part of the reason for increased attention to thermal issues. As a baseline for comparison, the 24-pin small-outline integrated circuit (SOIC) is shown, along with several fine-pitch packages supplied by TI, including the 24- and 48-pin SSOP, 24- and 48-pin TSSOP, and 100-pin thin quad flat pack (TQFP). The 24-pin TSSOP (8, 9, and 10 bits) allows for the same circuit functionality of the 24-pin SOIC to be packaged in less than a third of the area, while the 48-pin TSSOP (16, 18, and 20 bits) occupies less area and has twice the functionality of the 24-pin SOIC. This same phenomenon is expanded even further with the 100-pin TQFP (32 and 36 bits), which is the functional equivalent of four 24-pin or two 48-pin devices, with additional board savings over that of the SSOP packages. As the trend in packaging technology moves toward smaller packages, attention must be focused on the thermal issues that are created.

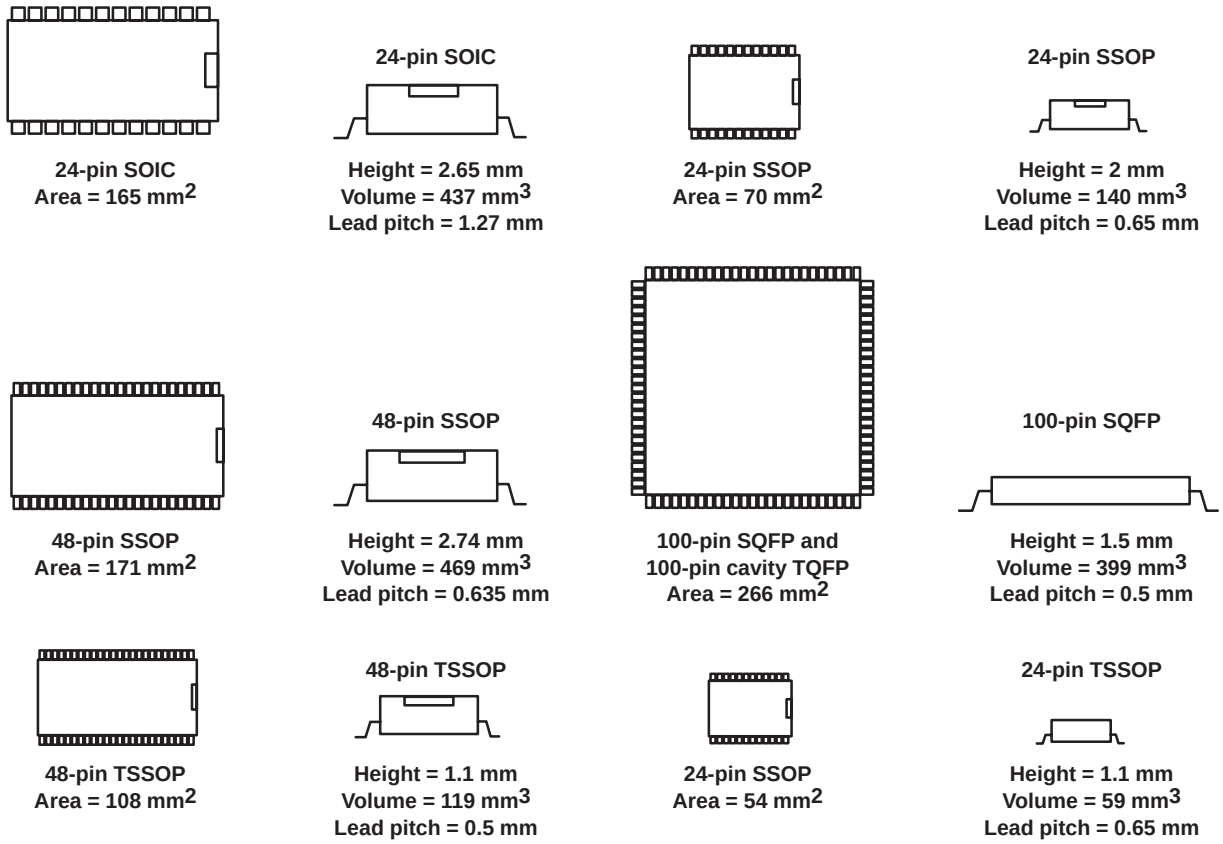


Figure 17. Advanced Packages

A better understanding of the factors that contribute to junction temperature (T_J) provides a system designer with more flexibility when attempting to solve thermal issues. Device junction temperature is determined by equation 7:

$$T_J = T_A + (\Theta_{JA} \times P_T) \tag{11}$$

Where:

T_J = Junction (die) temperature (°C)
T_A = Ambient temperature (°C)
Θ_{JA} = Thermal resistance of the package from the junction to the ambient (°C/W)
P_T = Total power of the device (W)

Junction temperature is altered by lower chip power consumption, longer trace length, heatsinks, forced air flow, package mold compound, lead-frame size and material, surface area, and die size. Some of these are mechanically inherent in a particular package, while others are controlled by the designer and are application specific. Understanding which variables can be influenced by practicing good thermal-design techniques requires a more detailed investigation of power considerations as well as thermal-resistance measurements. The package power dissipation is calculated using a junction temperature (T_J) of 150°C and an ambient temperature (T_A) of 55°C. Θ_{JA} is calculated using a board trace length of 750 mils and no airflow. Table 2 provides the different Θ_{JA} for different packages. Refer to the *Package Thermal Considerations* application report in the ABT data book for the relationship between junction temperature and reliability.

Table 2. Θ_{JA} for Different Packages

NO. OF PINS		14	16	20	24	48	52	56	64	80	100
SOIC	Package	D	D	DW	DW	—	—	—	—	—	—
	ΘJA	76	73	59	56	—	—	—	—	—	—
SSOP	Package	DB	DB	DB	DB	DL		DL			
	ΘJA	185	175	164	152	80		68			
TSSOP	Package	PW	PW	PW	PW	DGG		DGG			
	ΘJA	195	187	143	140	115		92			
QFP	Package						RC			PH	
	ΘJA						69			84	
TQFP	Package								PM	PN	PZ
	ΘJA								96	89	79
TQFP–HP	Package										PCA
	ΘJA										52.4

Advanced Packaging

In addition to its strong commitment to provide fast, low-power, high-drive integrated circuits, TI is the clear-cut leader in logic packaging advancements. The development of the SSOP in 1989 provided system designers the opportunity to reduce the amount of board space required for bus-interface devices by 50 percent. Several 24-pin solutions, including the familiar SOIC, SSOP, and TSSOP are widely used, as well.

The 48-/56-pin SSOP/TSSOP packages allow twice the functionality (16-, 18-, and 20-bit functions) in approximately the same or less board area as a standard SOIC. This is accomplished by using a 25-mil (0.635-mm) lead pitch, as opposed to 50 mil (1.27 mm) in SOIC. Figure 18 shows a typical pinout structure for the 48-pin SSOP/TSSOP. The flow-through architecture is standard for all Widebus™ devices, making signal routing easier during board layout. Also, note the distributed GND and V_{CC} pins, which improve simultaneous switching performance, as discussed in the signal integrity section of this report.

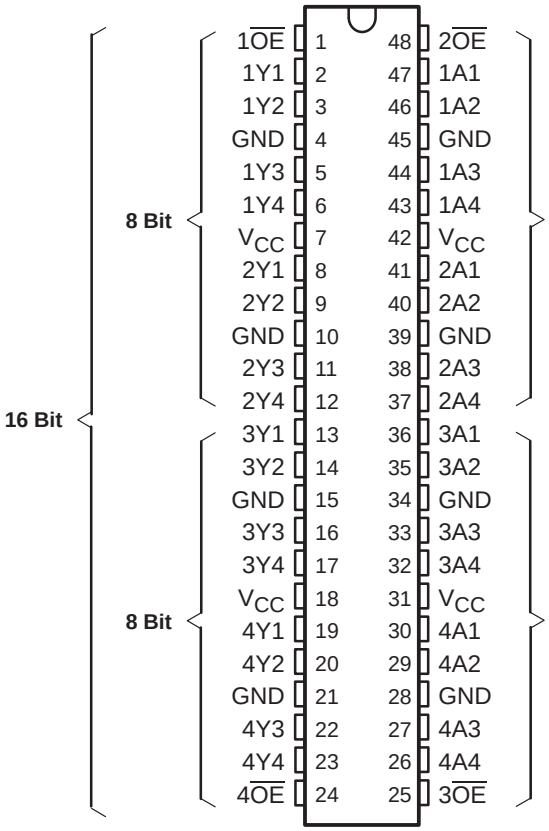


Figure 18. Distributed Pinout of ’ABT16244A

When using the small-pin-count SSOPs (8-, 9-, and 10-bit functions), the same functionality will occupy less than half the board area of an SOIC (70 mm^2 vs 165 mm^2). There is also a height improvement over the SOIC that is beneficial when the spacing between boards is a consideration. For very dense memory arrays, the packaging evolution has gone one step further with the TSSOP. The TSSOP thickness of 1.1 mm gives a 58-percent height improvement over the SOIC. Another packaging evolution is the EIAJ standard 100-pin TQFP package (0.5-mm lead pitch), which was developed for both the Widebus+™ family (32-bit ABT) and the 18-bit FB+/BTL universal bus transceivers (UBT™). The FB version is a high-power package. A package cross-section, as shown in Figure 19, reveals a metal heatsink that facilitates the excellent thermal performance of the package.

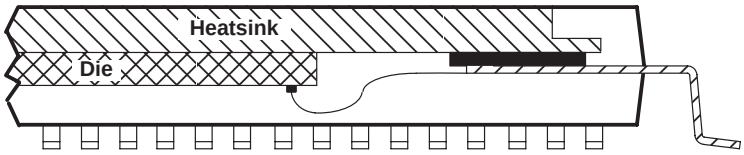
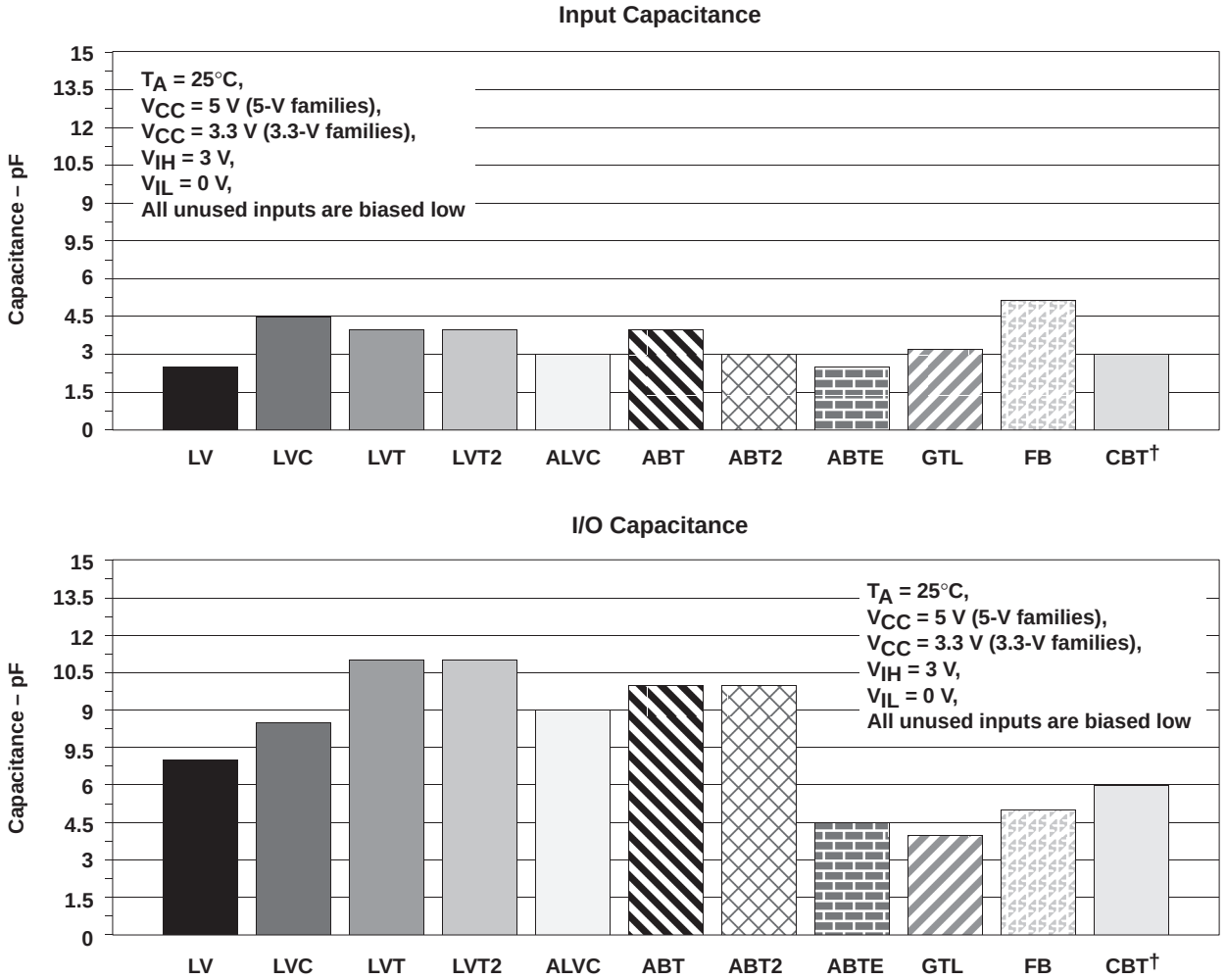


Figure 19. Cross-Section of Thermally Enhanced EIAJ 100-Pin TQFP

For more information about the various packages used with the Advanced Bus-Interface families, refer to the Mechanical Data section in the ABT or LVT data book.

Output Capacitance

TI designed both the CMOS and BiCMOS logic families for the lowest capacitance possible. GTL and BTL/FB, however, were designed to meet a 5-pF I/O capacitance on the B port. Figure 20 shows the typical input, I/O, and output capacitance of these families.



† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 20. Capacitance Variation Between Families

ac Performance

Simultaneous-Switching Phenomenon

System designers are frequently concerned with the performance degradation of ICs when outputs are switched. TI's priority, when designing the bus-interface families, is to minimize signal-integrity concerns and reduce the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of these families for both octals and Widebus™ devices.

Figure 21 shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor (V_L) is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly, as shown in Figure 22. The voltage output low, peak or valley (V_{OLP}, V_{OLV}), is measured on one quiet output when all others are switched from high to low.

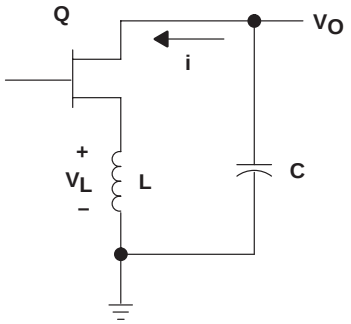


Figure 21. Simultaneous-Switching Output Model

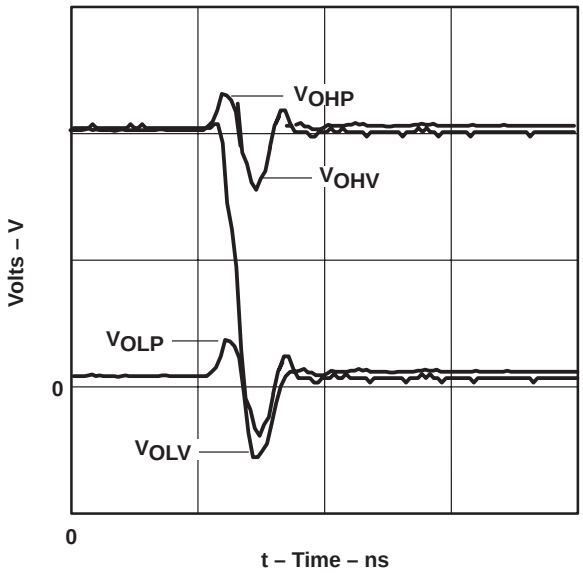


Figure 22. Simultaneous-Switching-Noise Waveform

A similar phenomenon occurs with respect to the V_{CC} plane on a low-to-high transition, known as voltage output high, peak or valley (V_{OHP}, V_{OHV}). Most problems are associated with a large V_{OLP} because, in most cases, the range for a logic 0 is much less than the range for a logic 1 (see Figure 23). For a comprehensive discussion of simultaneous switching, see the *Simultaneous Switching Evaluation and Testing* application report or the *Advanced CMOS Logic Designer's Handbook* from TI.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to the ac performance section of this report.

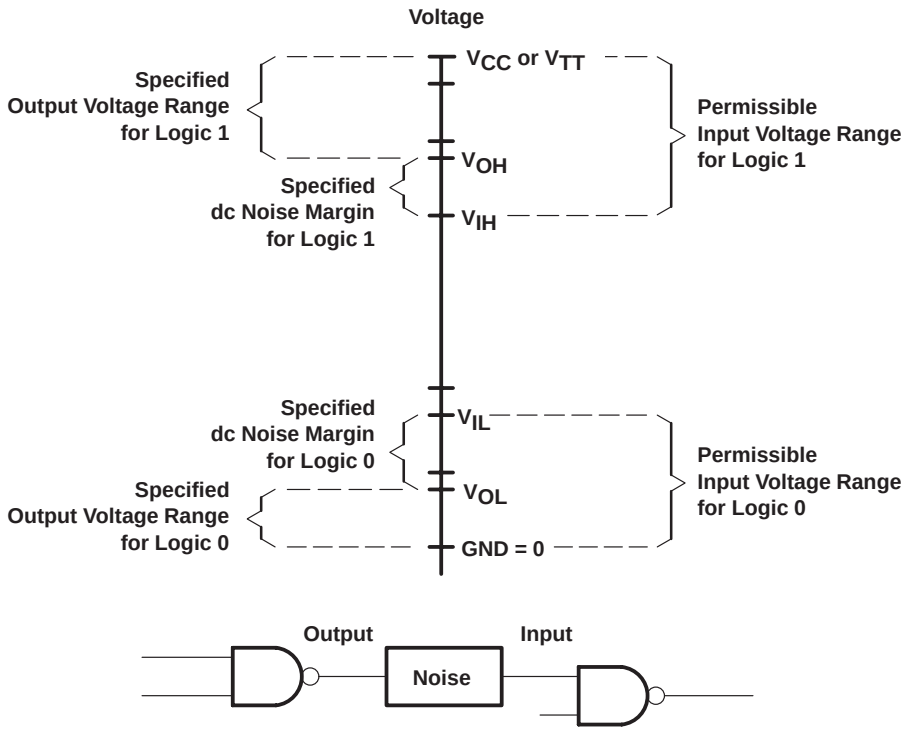


Figure 23. dc Noise Margin

Simultaneous-Switching Solutions

IC manufacturers can reduce the effects of simultaneous switching by decreasing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in detail in the 1988 Texas Instruments *Advanced CMOS Logic (ACL) Designer's Handbook*.

Octal devices employ the standard end-pin GND and V_{CC} configuration while maintaining acceptable simultaneous switching performance. Widebus™ series (16-, 18-, and 20-bit functions), on the other hand, are offered in an SSOP package (see the packaging section of this report) that was developed by TI to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with 16 outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is normally a GND pin for every two outputs and a V_{CC} pin for every four outputs. This allows the transient current to be distributed across multiple power pins and decreases the overall current range of change (di/dt) effect.

From basic circuit analysis, the induced voltage across an inductor is defined as:

$$v = L(di/dt) \tag{12}$$

Where:

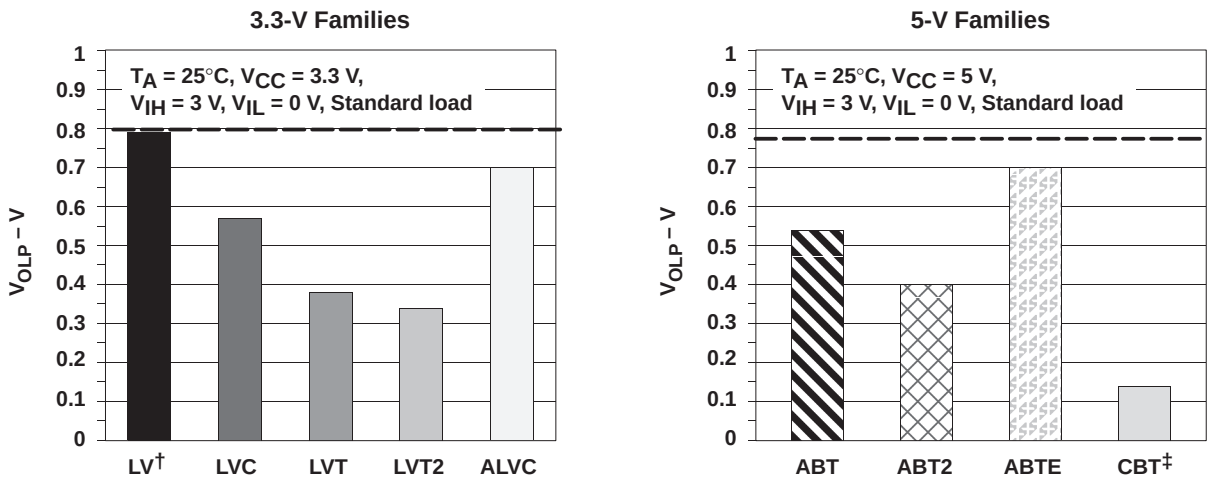
L = Inductance
di/dt = Rate of change of the current

The current through an output is dependent on the voltage level and the load seen at the output. This can be expressed mathematically as:

$$i = C(dv_{out}/dt) \tag{13}$$

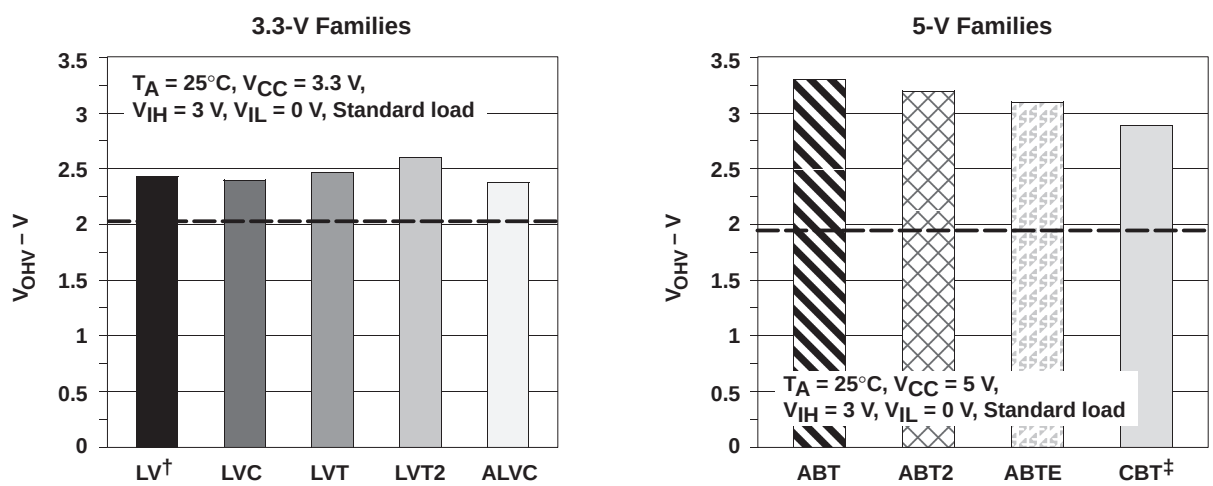
Analysis of equations 12 and 13 clearly shows that the more V_{CC} and ground pins there are, the lower the lead inductance, resulting in less noise.

As the speed of today's circuits increases, di/dt increases and so does the generation of simultaneous-switching noise.The standard methodology devised by the industry to measure voltage bounce is to keep one output at either logic high (V_{OH}) or logic low (V_{OL}) and to switch all other outputs at a predefined frequency. Figures 24 through 26 show a comparison of the noise generation as (N – 1) outputs are switched simultaneously while the Nth output is held high or low. Refer to Figure 1 for the guaranteed V_{IL}(max) and V_{IH}(min) specification for various families.



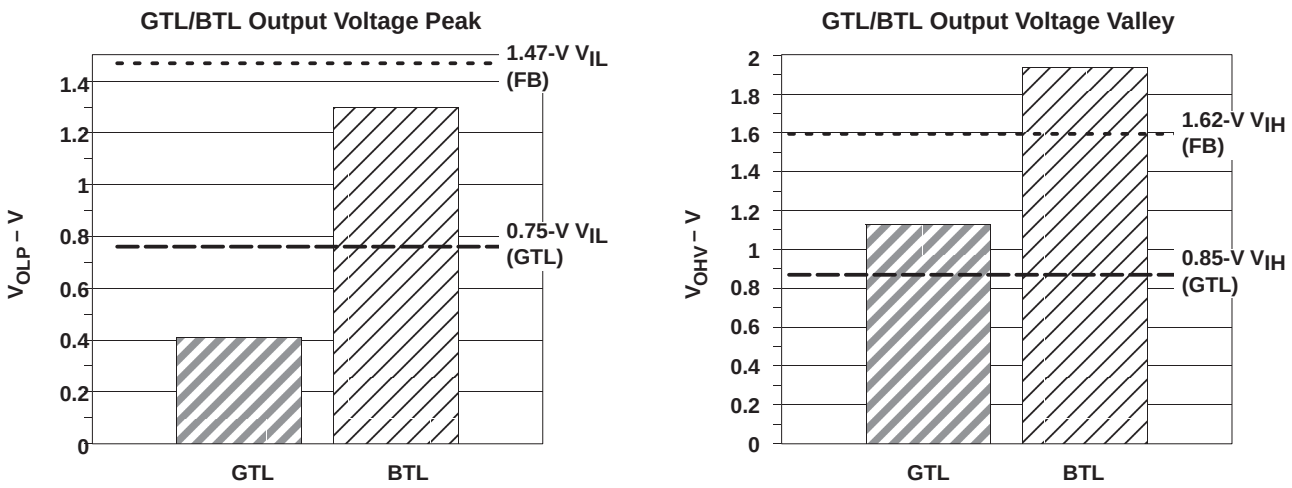
† LV is tested using octal packages only.
‡ Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 24. Typical Output Low-Voltage Peak (V_{OLP}) on 3.3-V and 5-V Families



† LV is tested using octal packages only.
‡ Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 25. Typical Output High-Voltage Valley (V_{OHV}) on 3.3-V and 5-V Families

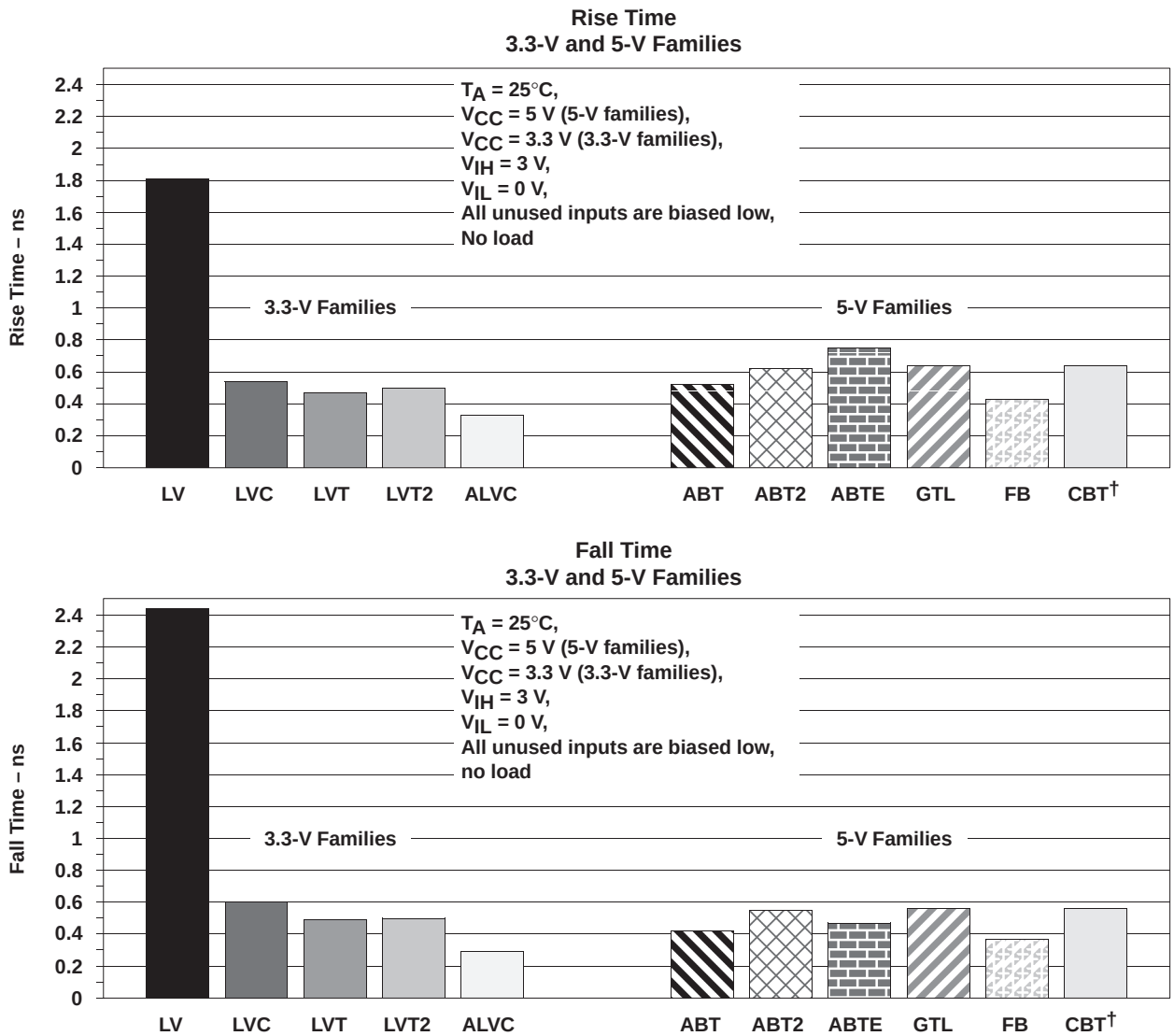


T_A = 25°C, V_{CC} = 5 V (BTL, GTL), V_{CC} = 3.3 V (GTL), V_{IH} = 3 V, V_{IL} = 0 V, Standard load

Figure 26. Typical Output Voltage Peak (V_{OLP}) and Valley (V_{OHV}) on GTL and BTL

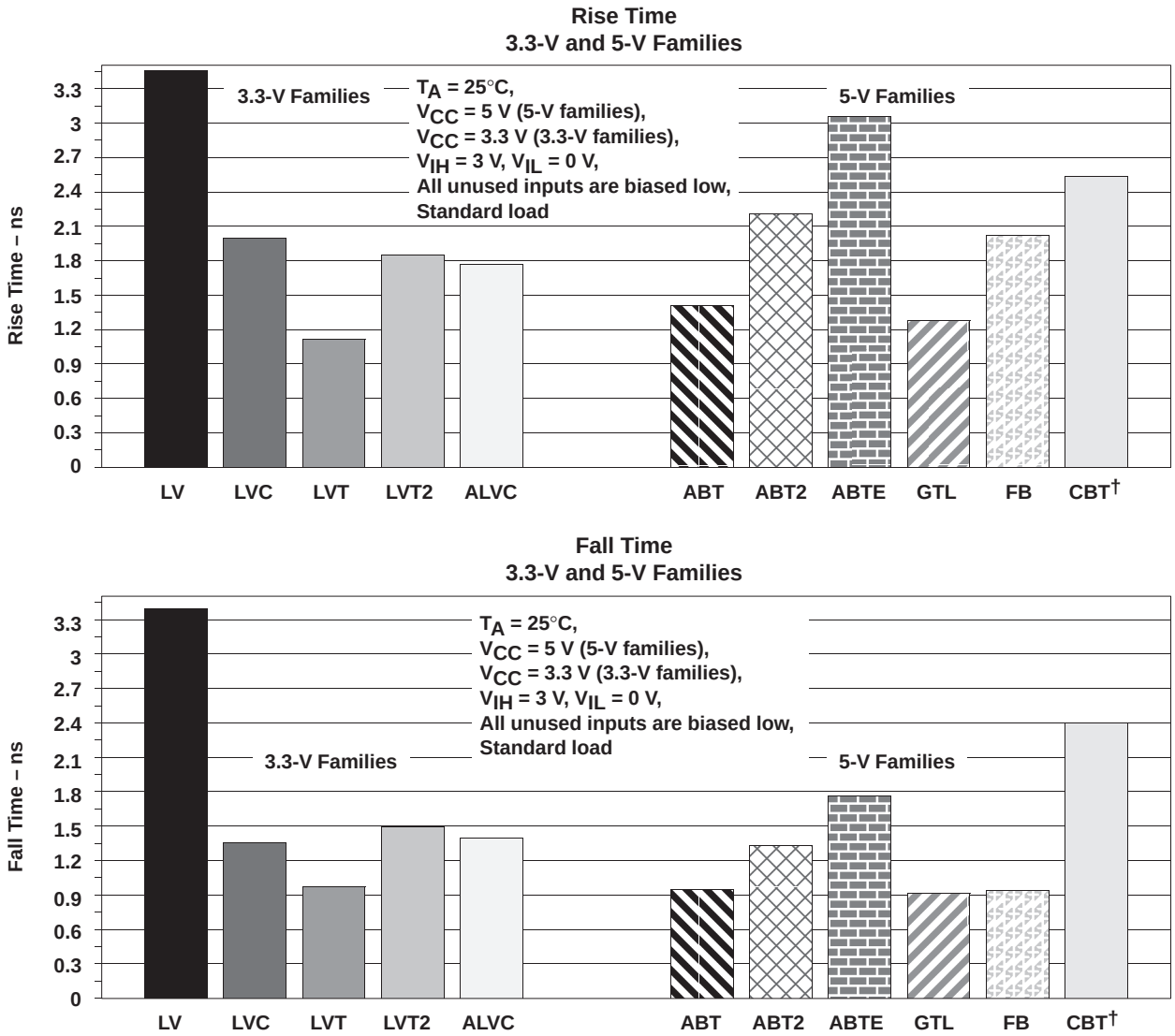
Slew Rate

Slew rate plays an important role in backplane or point-to-point application designs. The slower the output slew rate of a device, the less susceptible the signal is to reflections and noise. Based on this data, a designer knows how to terminate a bus or backplane. Using the characterization laboratory boards, the output slew rate (t_{rise} and t_{fall}) was taken with and without the standard output load. Figures 27 and 28 show the output rise and fall times of each output taken between 10% and 90% for TTL, 0.5 V and 1 V for GTL, and 1.3 V and 1.8 V for BTL. Figures 29 and 30 show the rise and fall time as the number of outputs switching increases. The curves in both plots look almost flat between one output switching and all outputs switching.



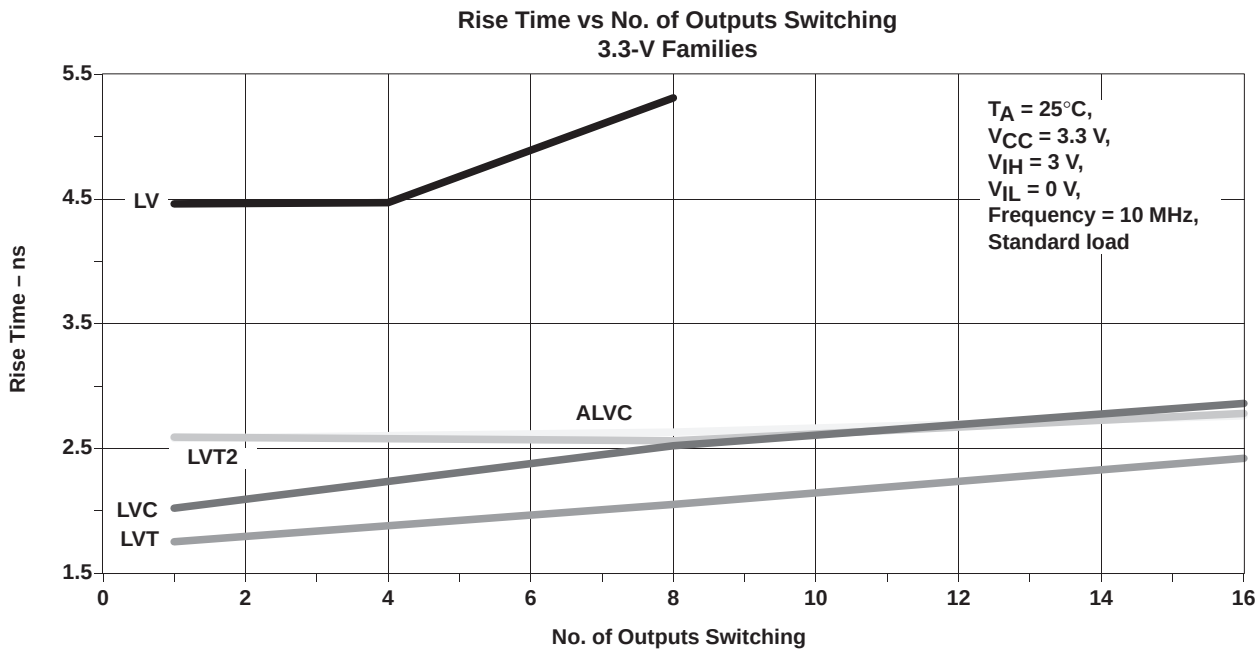
† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

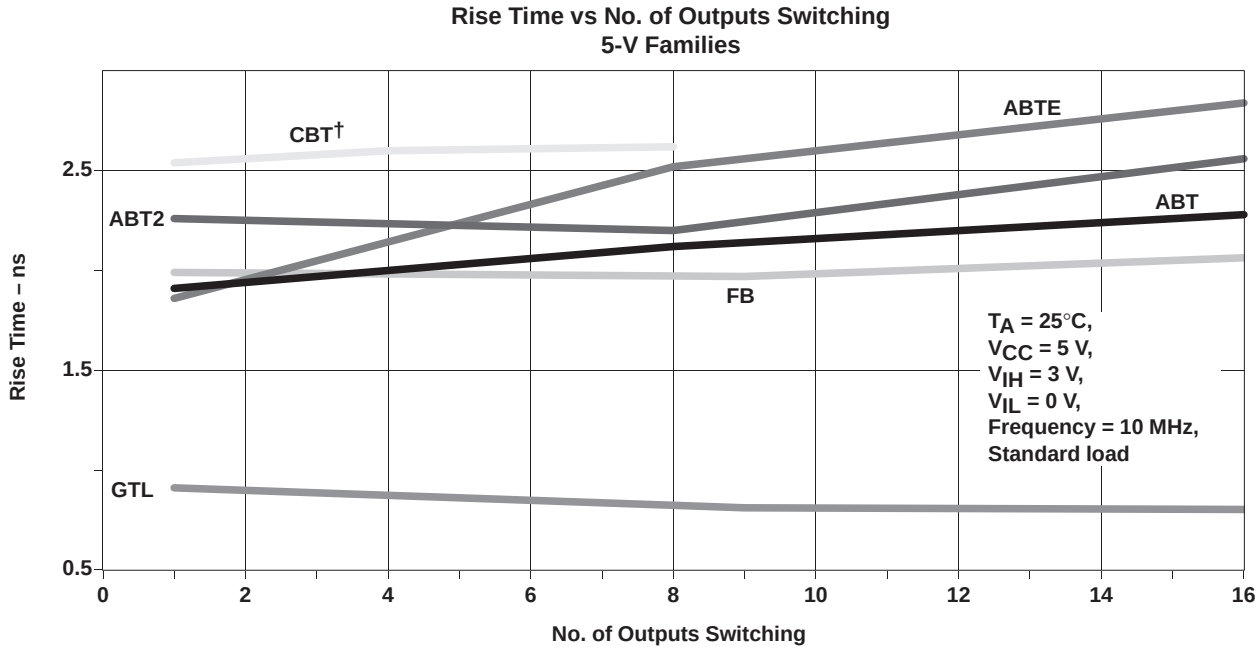
Figure 27. Typical Output Rise and Fall Time Measured Between Specified Levels or Voltages



† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

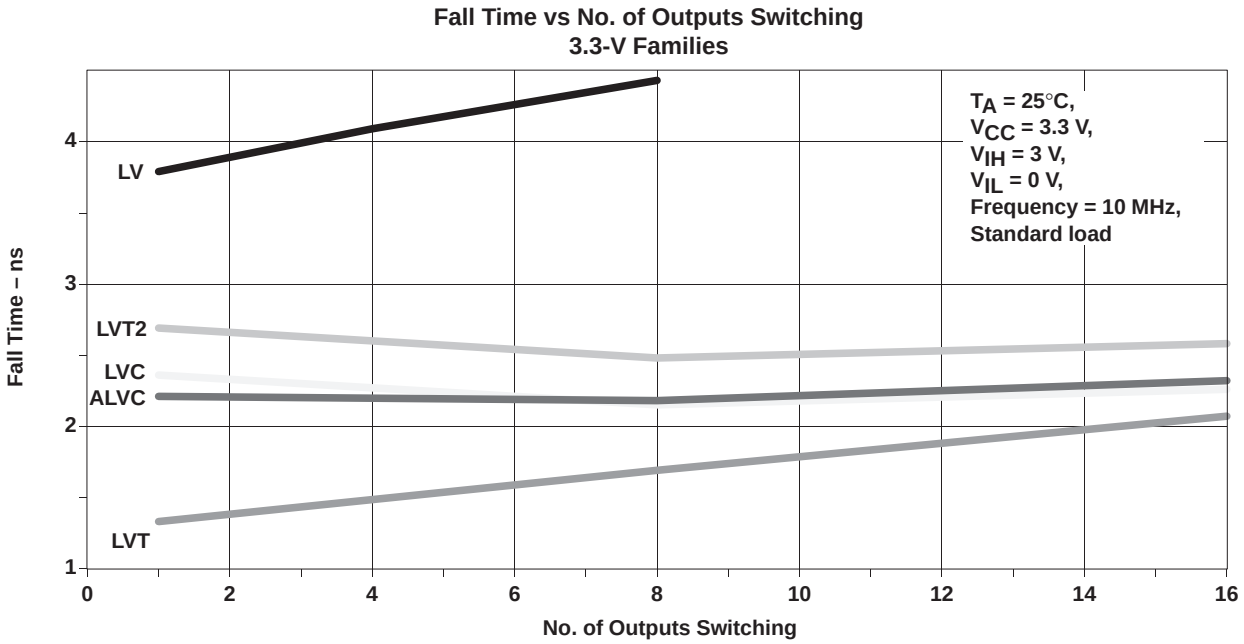
Figure 28. Typical Output Rise and Fall Time Measured Between Specified Levels or Voltages

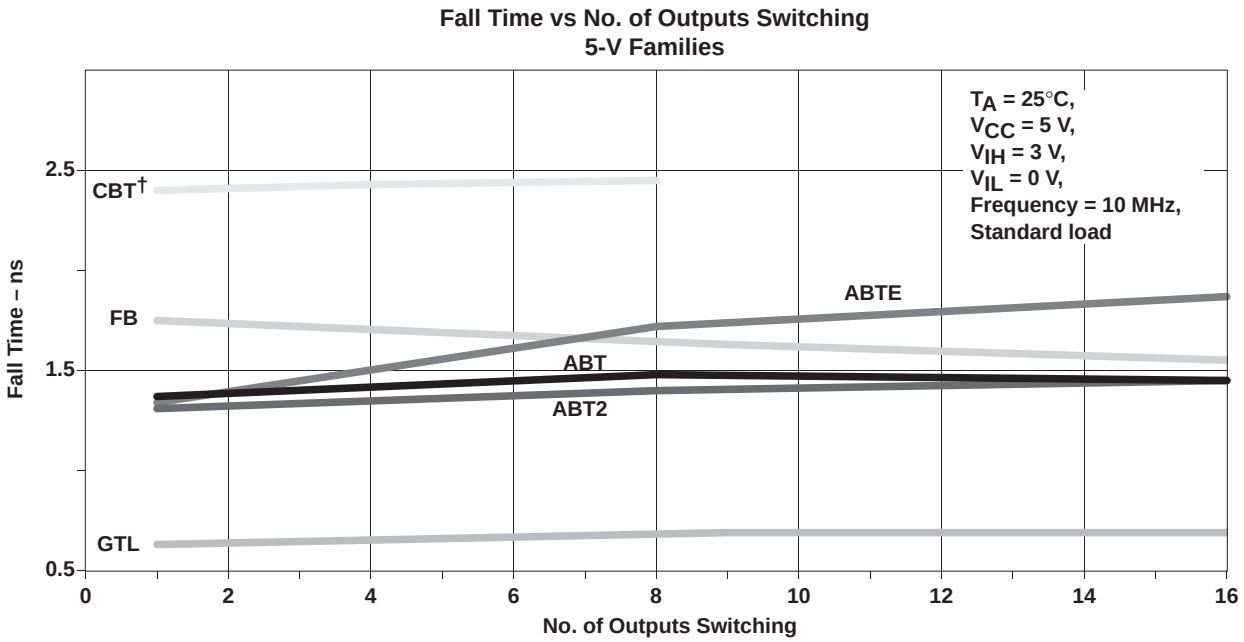




† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 29. Typical Output Rise Time as the Number of Outputs Switching Increases



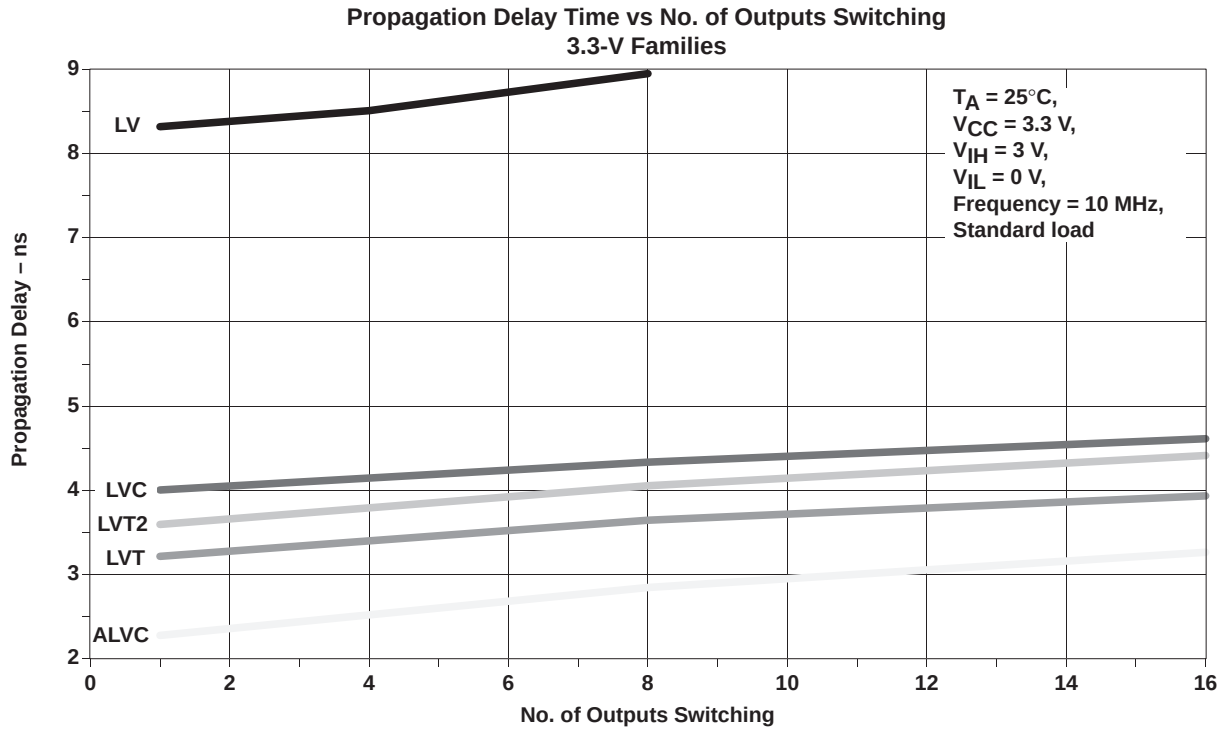


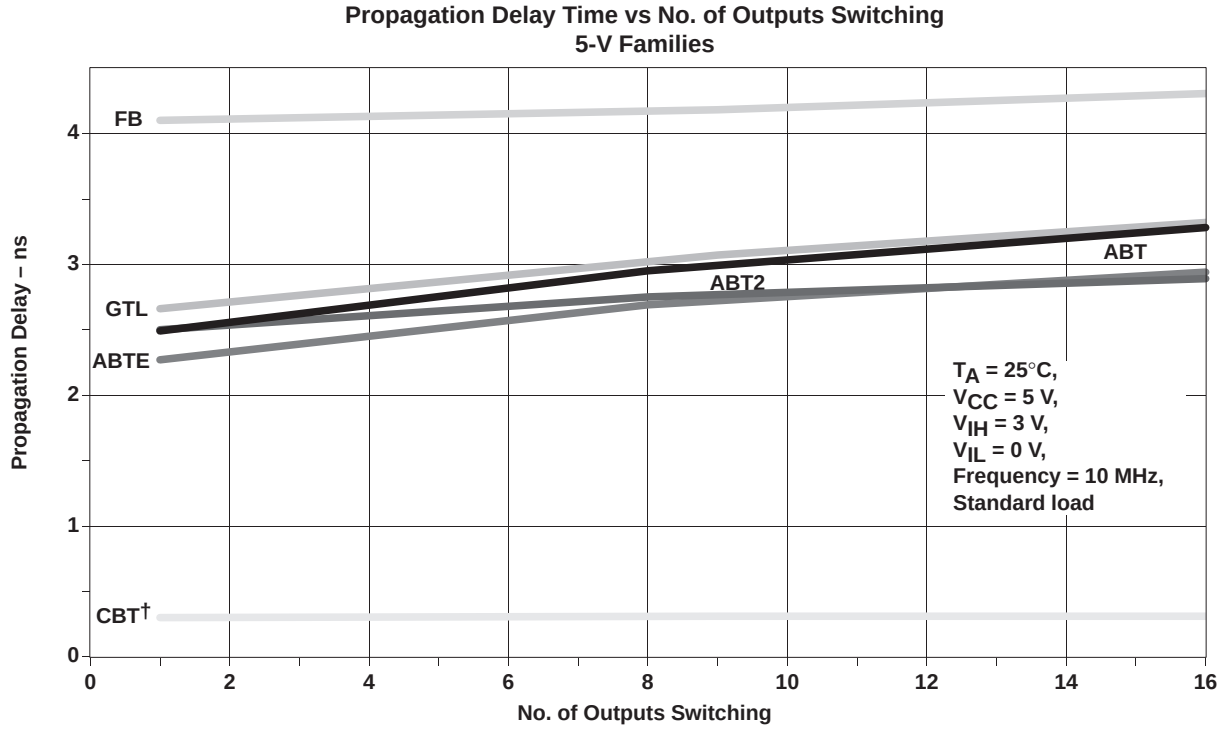
† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 30. Typical Output Fall Time as the Number of Outputs Switching Increases

Effects of Simultaneous Switching and Capacitive Loading on Propagation Delay

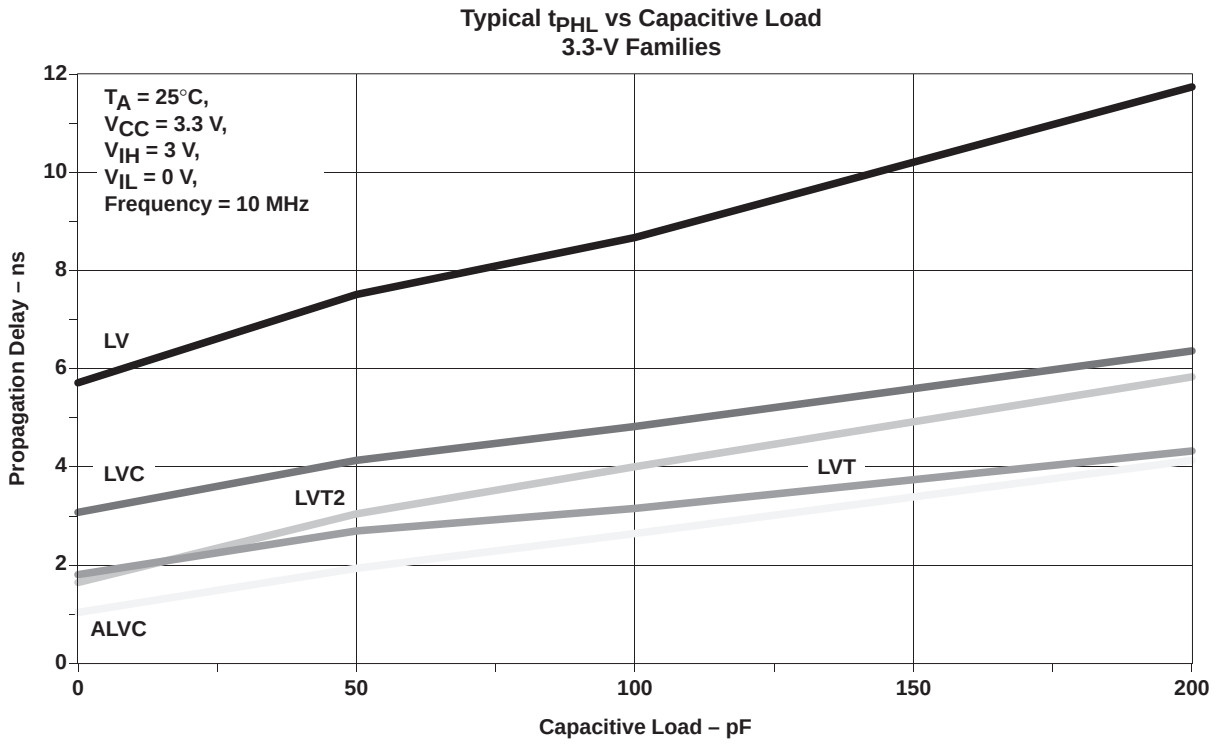
Another factor that may be of concern to a designer is the change in propagation delay when more outputs are switching or when the output capacitive load is varying. This data is very useful, since a typical application would use all outputs simultaneously. In addition, it usually requires different loading conditions than the data sheet specifies. Data sheets do not show the performance of the device with different loads; they only use the standard load specified in data sheets. Figure 31 shows the propagation delay of a device as the number of outputs switching increases. Figures 32 and 33 show the increase in propagation delays (t_{PHL} and t_{PLH}) as the output capacitive load increases from 0 pF to 200 pF.

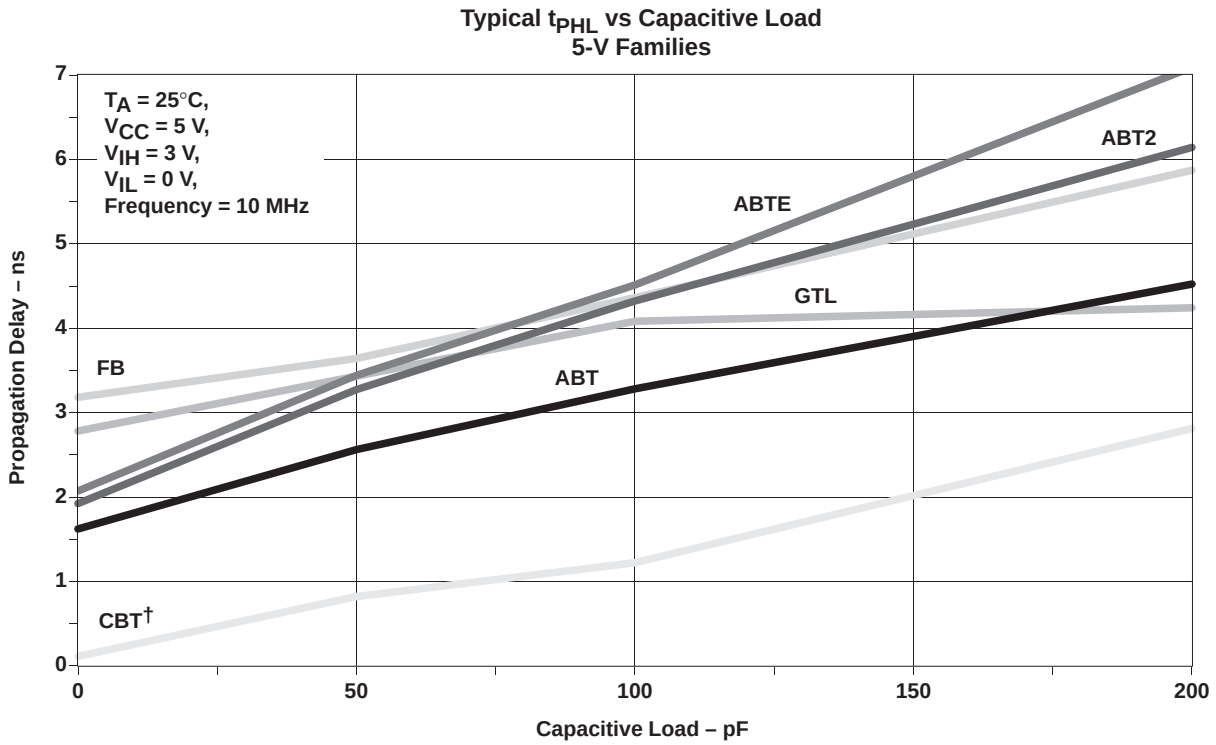




† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

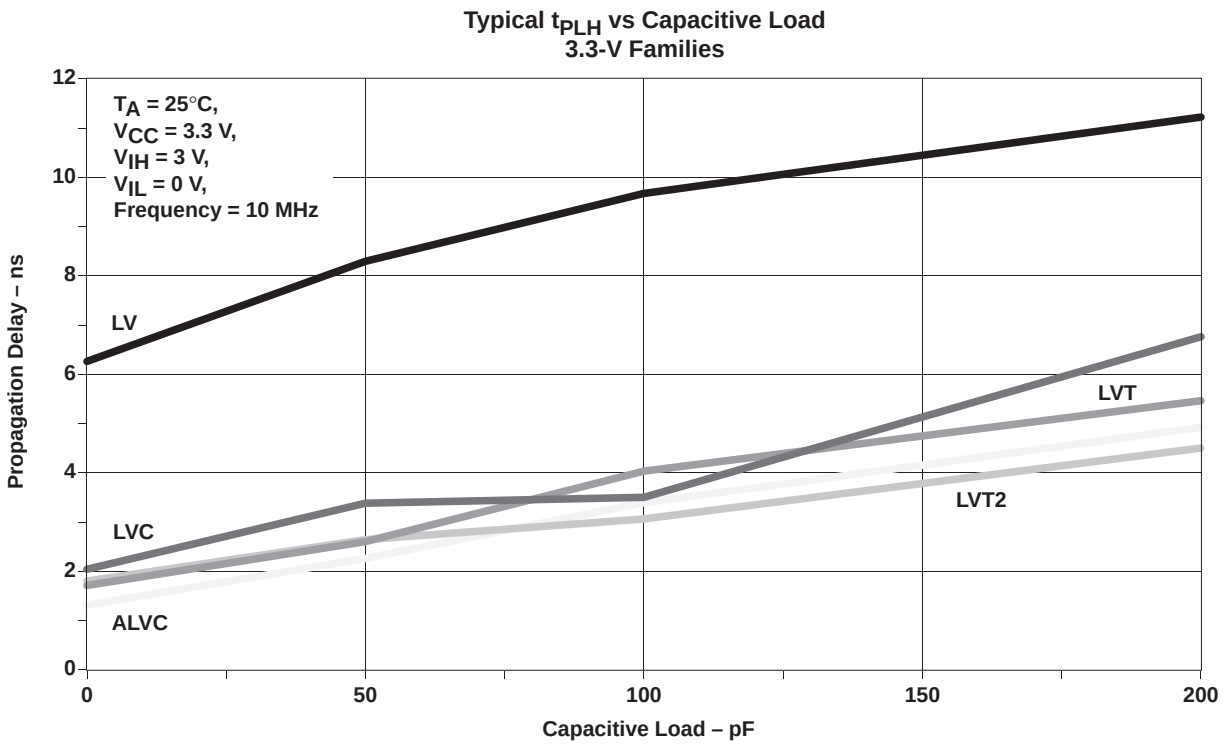
Figure 31. Typical Propagation Delay vs Number of Outputs Switching (Standard Load)

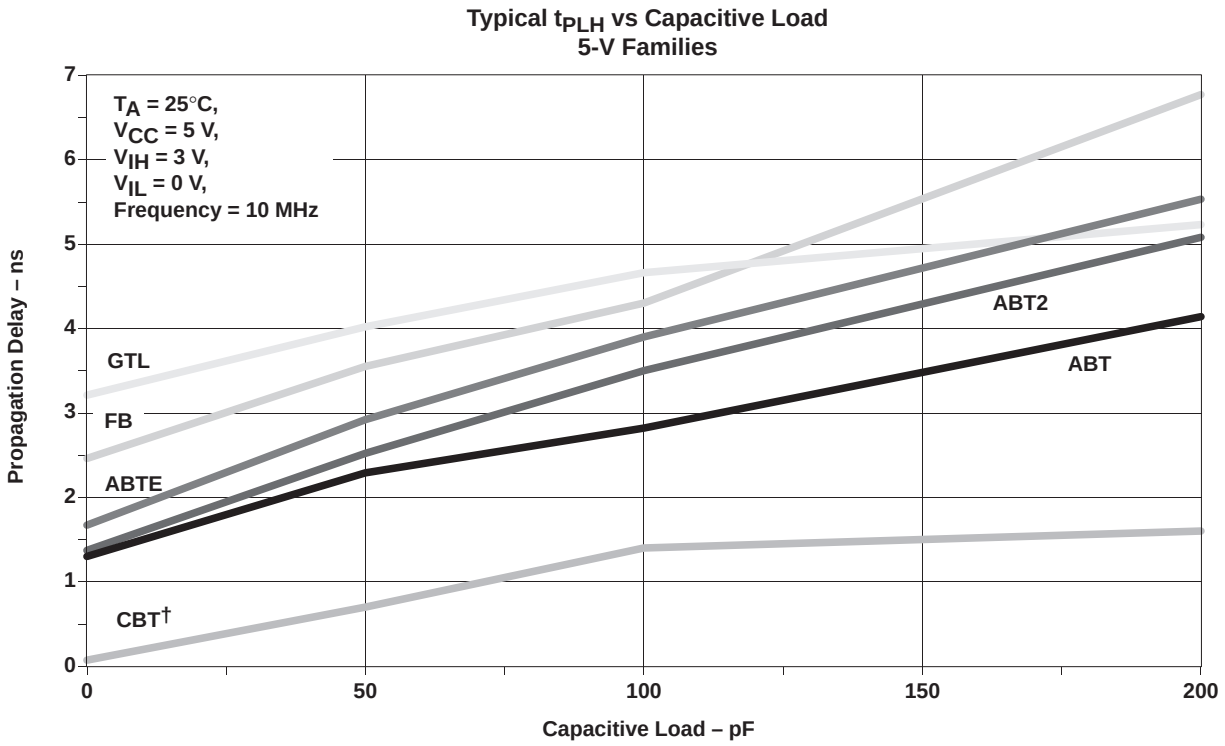




† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 32. Typical t_{PHL} vs Capacitive Load





† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 33. Typical t_{PLH} vs Capacitive Load

Skew

Skew is a term that is used to define the difference in time between two different signal edges. There are several different types of skew currently being used; however, the skew discussed here is the skew of propagation delays across the outputs of a device. More specifically, it is the difference between the largest value obtained for a propagation delay and the smallest value across all of the outputs. For example, if output 3 has the largest propagation delay (t_{PLH}) and output 14 has the smallest, the output skew for this device would be the difference between the propagation delays for output 3 and output 14 (see Figure 34).

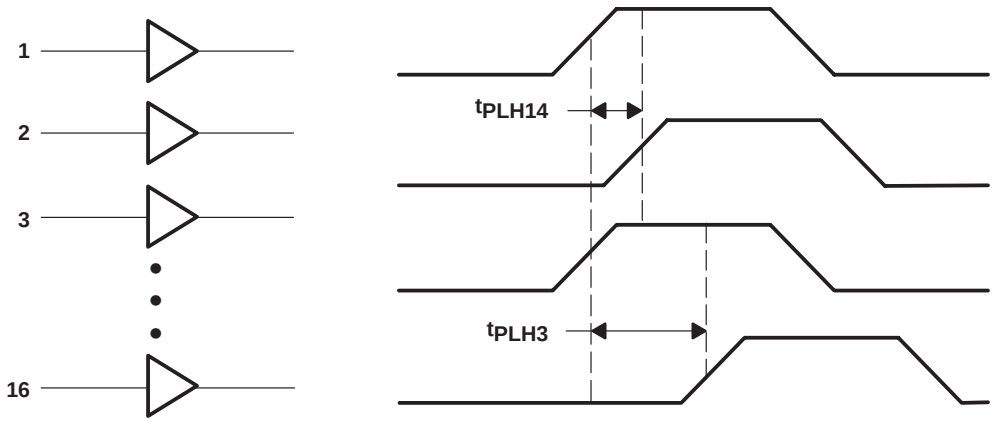
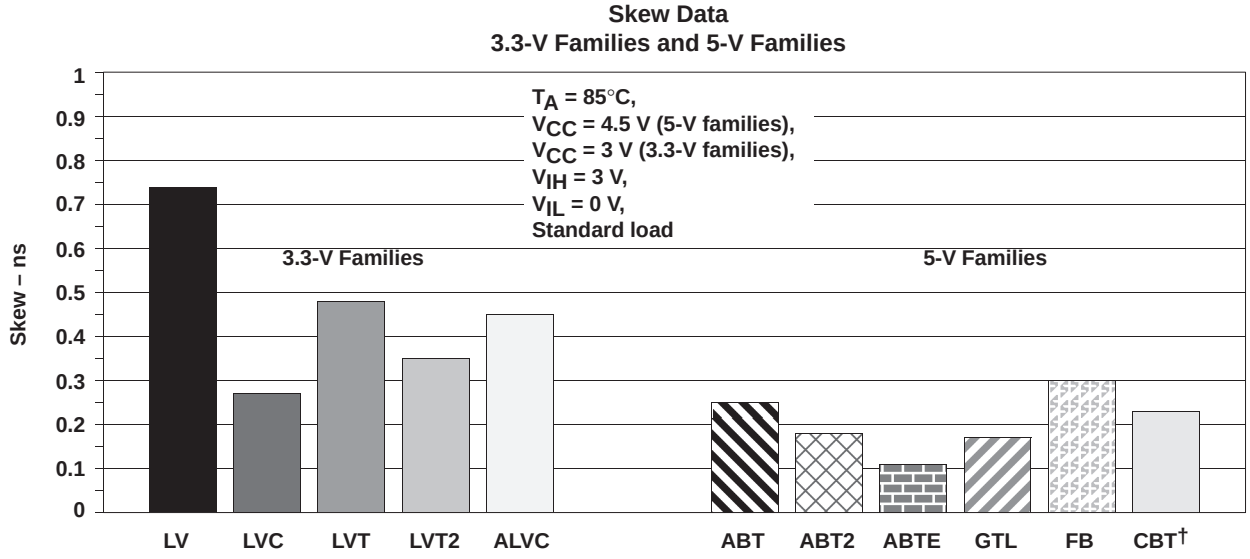


Figure 34. Skew = $|t_{PLH3} - t_{PLH4}|$

The data presented in this report is taken from devices that have one output switching at a time (V_{CC} = MIN and T_A = 85°C). This data represents the average worst-case condition skew. Figure 35 shows the skew of the different families using the standard load specified in data sheets.



† Data is based on the input signal characteristics: V_{IL} = 0 V, V_{IH} = 3 V, t_r/t_f = 2 ns.

Figure 35. Typical Skew Between Outputs

Bus-Hold Circuit

The most effective method to provide defined levels for a floating bus is to use TI's *bus hold* as a built-in feature on selected families (see Table 3).

Table 3. List of Devices With Bus Hold

FAMILY	BUS HOLD
ABT WIdebus+™ (32- and 36-bit)	All devices
ABT Octals and Widebus™	Selected devices
Low Voltage (LVT and ALVC)	All devices
LVC Octals and Widebus™	Selected devices
GTL	A port only

Bus hold is a circuit used in TI's selected families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. It consists of two back-to-back inverters, with the output fed back to the input via a resistor (see Figure 36). To understand how the bus-hold cell operates, let's assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes in the high-impedance state and the bus-hold circuit holds the high level via the feedback resistor. The current requirement of the bus hold is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

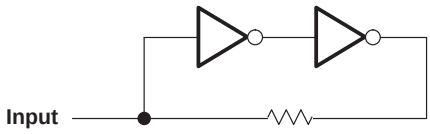


Figure 36. Typical Bus-Hold Cell

Table 4 shows the data-sheet dc specifications for bus hold. The first specification is the minimum available current to hold the bus at 0.8 V or 2 V. These voltages are the guaranteed low and high levels for TTL inputs. The second specification is the maximum current that the bus hold sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input approaches the rails. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold since a true leakage test cannot be achieved due to the existence of the bus-hold circuit. Since bus hold behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with bus hold only and does not apply to buffers. Note that all LVT, ABT Widebus+™, selected ABT and LVC octals, and Widebus™ devices have the bus-hold feature. Refer to Table 4 or the manufacturer for more information.

Table 4. Data-Sheet Specification for Bus Hold

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold features)

PARAMETER	TEST CONDITIONS				MIN	MAX	UNIT
$I_{I(hold)}$	LVT, LVC, ALVC	Data inputs or I/Os	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	–75		
			V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
$I_{I(hold)}$	ABT Widebus+™ and selected ABT Widebus™	Data inputs or I/Os	V_{CC} = 4.5 V	V_I = 0.8 V	100		µA
				V_I = 2 V	–100		
			V_{CC} = 5.5 V,	V_I = 0 to 5.5 V		±500	
I_{OZH}/I_{OZL}	ABT	Transceivers with bus hold	This test is not a true I_{OZ} test since bus hold is always active on an I/O pin. It tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
	LVT, LVC, ALVC					±1	
I_{OZH}/I_{OZL}	ABT	Buffers with bus hold	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	µA
	LVT, LVC, ALVC					±5	

Partial Power Down

Partial power down and live insertion are becoming a major issue in today's system designs. Many new standards have included this as part of their specification. The plug-and-play feature is beginning to dominate the PC market and the telecom industry has been using it for a long time. When a system is partially down, the unpowered device is expected to go into a high-impedance state so the device does not disturb or disrupt the data on the bus. When using standard CMOS devices, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as hot-card insertion without adding current-limiting components. This is not the case with ABT, LVT, LVC, GTL, and BTL, as these paths have been eliminated with the use of either blocking diodes or current-blocking circuitries. Figure 37 shows functionally-equivalent schematics of the input and output structures for these families. Refer to Figures 5 and 10 for more detail on the input and output behavior under these conditions.

Consider the situation shown in Figure 38. The driving device is powered with V_{CC} = 5 V while the receiving device is powered down (V_{CC} = 0). If these devices are either LV, ALVC, or ALB, the receiver can be powered up through the diode, D2 and D3, when the driver is in a high state. ABT, LVT, LVC, GTL, and BTL devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application. The electrical characteristics table in the data sheet has a specification called I_{off}. This specification shows the test condition and the maximum leakage a device can source or sink when V_{CC} is off. Refer to the individual data sheets for more details.

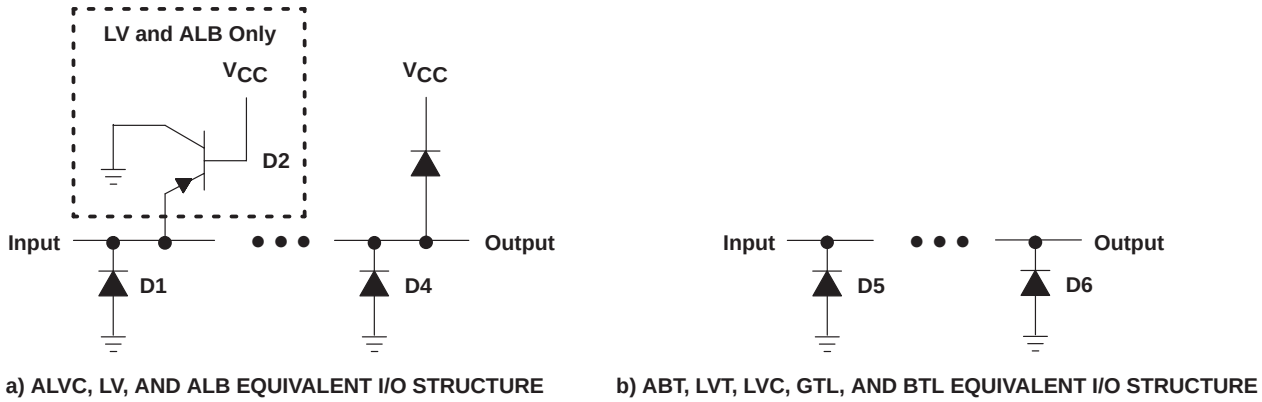


Figure 37. Simplified Input Structures for CMOS and ABT Devices

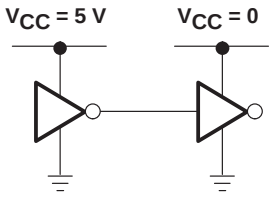


Figure 38. Example of Partial-System Power Down

Power-Up or Power-Down High Impedance

Power-up 3-state circuitry is another feature that TI offers on selected LVT, ABT, and FB. This feature keeps the output in a high-impedance state during power up or power down, regardless of the output-enable control pin's state (V_{CC} = 0 V to 2.1 V for ABT and FB, and V_{CC} = 0 V to 1.5 V for LVT). After V_{CC} reaches the specified value, the output-enable control takes over and puts the device in the required state (see Figure 39). The electrical characteristics table in the data sheet has both the power-up and power-down specifications (I_{OZPU} and I_{OZPD}). These specifications show the test condition and the maximum leakage an output can source or sink when V_{CC} is between 0 V and 2.1 V for ABT and FB or between 0 V and 1.5 V for LVT (the nomenclature for the selected LVT devices that offer this feature is LVTZ). Refer to the LVT data book for more details. Power-up or power-down high impedance can also be achieved with other families by adding an external pullup or pulldown resistor (typically 1 kΩ) from the output-enable pin to V_{CC} (active-low devices) or to GND (active-high devices) (see Figure 40). This ensures the high-impedance state during the full V_{CC} ramp. As long as the output-enable pin is not driven to an active state by the controlling device, an ASIC, FPGA, or PAL, the output remains disabled.

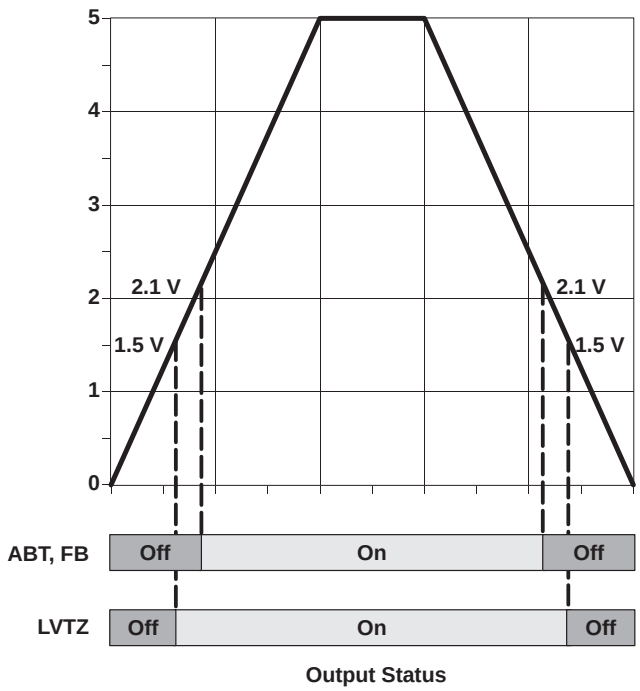
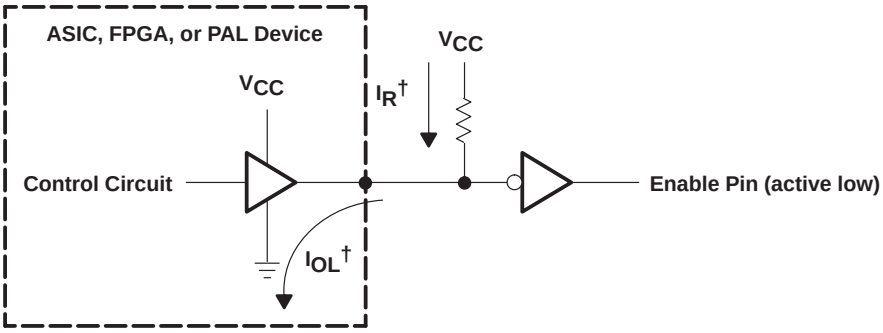


Figure 39. Power-Up and Power-Down High Impedance Up to 2.1 V (ABT, FB) and 1.5 V (LVTZ)



† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 40. Power-Up High Impedance With Active-Low Control Pin

ABTE, FB, and CBT (CBT6800 only) have an added feature called BIAS V_{CC}. This feature is used to precharge the output, trace, and connector capacitance during power up. This circuit prevents the device from spiking the backplane and disrupting the data during hot-card insertion. For this feature to work, both ground and BIAS V_{CC} pins must make contact before V_{CC} does (both pins should be the longest on the card).

Additional Design Considerations for GTL and BTL/FB

GTL

To successfully design with the GTL family, several rules and techniques with regard to voltage generation and proper termination must be followed. First, both 3.3-V and 5 V-V_{CC} are needed in the current generation of GTL devices (only the 3.3-V V_{CC} will be needed in the next-generation GTL). Second, the termination voltage (V_{TT} = 1.2 V) should be regulated from the 5-V- V_{CC}, keeping in mind the current requirements of the outputs (40 mA per output). There are several linear regulators that are capable of performing this function. Depending on the design, the regulator could be either on the backplane itself or on the individual cards. Third, the reference voltage (V_{REF} = 0.8 V) must be generated from V_{TT}. The V_{REF} voltage can be generated using a simple voltage-divider circuit with an appropriate bypass capacitor (0.01 µF or 0.1 µF) placed as close as possible to the V_{REF} pin. The V_{REF} input circuitry consumes very little power (1-µA max). This enables several devices to have their V_{REF} pin connected to the same voltage-divider circuit, thus eliminating the need for multiple voltage-divider circuits (see Figure 41).

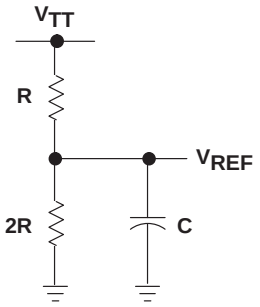


Figure 41. Proposed Circuit to Generate V_{REF}

BTL/FB

For the BTL family, there are four power supplies and two grounds to be connected. For live-insertion applications, the power-up scheme should be as follows: the GND lead should make contact first, followed by BIAS V_{CC}. This sequence precharges the board and the device capacitance and establishes a voltage between 1.62 V and 2.1 V on the BTL outputs. Next, V_{CC} makes contact and, as it ramps up, the BIAS-V_{CC} circuitry starts to turn off. When V_{CC} reaches its final value, the BIAS V_{CC} circuitry is completely isolated and does not interfere with the device functionality. BG-V_{CC} and BG-GND pins are used to supply power to the bias-generator input circuitry. Both signals must be isolated from the rest of the power supplies. This ensures the signal integrity at the BTL input. The 2.1-V V_{TT} should be regulated from a higher voltage and should supply enough current to switch all 18 outputs (100 mA per output). V_{TT} variation should not exceed ±2% and it is recommended that proper bypass capacitors (0.01 µF or 0.1 µF) be used. The termination resistor should not exceed ±1% of its resistance value.

Conclusion

Today's high-speed bus and point-to-point applications require devices that can provide high performance, excellent signal integrity, and cost effectiveness. TI's Advanced System Logic (ASL) group offers the widest selection of logic families that meet these requirements, from low drive (6 mA) to high drive (180 mA) and from low performance (16 ns) to high performance (sub 2 ns) propagation delay. These families are leading the industry and are used extensively in almost every application (PCs, workstations, telecom, networking, etc.). ASL also offers a wide variety of packaging options, including advanced packaging such as the plastic TQFP, SSOP, and TSSOP. The product offerings, coupled with the information provided in this application report, enable the designer to have a complete understanding of these products and their behavior. Table 5 summarizes the various circuit features and characteristics that were discussed in this application report. It can be used as a reference guide to help select the appropriate device for any application.

Table 5. Summary of the Various Features and Characteristics of the Device Families

	$\Delta t/\Delta$† (ns/V)	Drive I_{OL}/I_{OH} (mA)	I_{CCD} (mA/MHz Bit)	TYP V_{OLP}/V_{OHV} (V)	TYP Output Rise/Fall (ns)	TYP t_{PD} vs Cap. (ns/pF)	TYP t_{PD} vs SS (ns/Nsw)	MAX t_{PD} (ns)	TYP Skew (ns)	MAX I_{CC} CMOS (mA)	MAX $I_{CCH}/I_{CCL}/I_{CCZ}$ BiCMOS (mA)	5-V Tol.	PU3S	Bus Hold	25-Ω Output Series Resistor	TYP Control/I/O Cap. (pF)
LV	100	8/–8†	0.22	0.70/2.4	1.81/2.44	0.028	0.11	16	0.74	0.02						2.5/2.5/7
LVC	10	24/–24	0.23	0.57/2.4	0.54/0.6	0.014	0.04	5.2	0.27	0.02		√†		√‡	√‡	3.3/5.5/9
LVT	10	64/–32	0.12	0.38/2.47	0.47/0.49	0.01	0.04	4.1	0.48		0.12/5/0.12†	√		√		3.5/4/10
LVTZ	10	64/–32	0.12	0.38/2.47	0.47/0.49	0.01	0.04	4.1	0.48		0.12/5/0.12†	√	√	√		3.5/4/8
LVT2	10	12/–12	0.12	0.34/2.6	0.5/0.5	0.018	0.05	4.9	0.35		0.12/5/0.12†	√		√	√	3.5/4/10
ALVC	10	24/–24	0.27	0.70/2.38	0.33/0.29	0.014	0.05	3.4	0.45	0.04				√	√‡	3.5/6/7.5
ABT	10	64/–32	0.49	0.54/3.3	0.52/0.42	0.013	0.04	4.2	0.25		2/30/2†		√‡	√‡		3/3/6
ABT2	10	12/–12†	0.49	0.40/3.3	0.62/0.55	0.019	0.04	4.2	0.18		2/30/2†		√‡	√‡	√	3/3/6
ABTE	10	90/–60	0.42	0.70/3.1	0.75/0.47	0.024	0.04	5.2	0.11		36/48/32			√		2.5/2.5/4.5
GTL	10	40§	0.30	0.40/1.1	0.64/0.56	0.0054	0.04	4	0.17		120	√		√		3.5/3.5/4
FB	5	100§	0.20	1.3/1.9	0.43/0.37	0.014	0.04	5.6	0.30		60†		√			5/5/4
CBT	–	0/0	0	0.14/2.89	0.64/0.56	0.013	0.02	0.25	0.23	0.003†						3/6/6

† Unless otherwise noted in data sheets
‡ Selected devices only
§ Open-drain/open-collector devices

Acknowledgment

The author of this document is Ramzi Ammar.

References

1 Texas Instruments *Advanced BiCMOS Data Book 1994*, SCBD002B.

2 Gunning, Bill; Yuan, Leo; Nguyen, Trung; Wong, Tony, GTL: “A Low-Voltage Swing Transmission-Line Transceiver”, March 15, 1991.

3 Texas Instruments, “Package Thermal Considerations”, *Advanced BiCMOS Data Book 1994*, SCBD002B, page 13-97.

Implications of Slow or Floating CMOS Inputs

SCBA004C
February 1998

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Contents

List of Illustrations

Introduction

In recent years, CMOS (AC/ACT, AHC/AHCT, ALVC, CBT, CBTLV, HC/HCT, LVC, LV/LV-A) and BiCMOS (ABT, ALVT, BCT, FB, GTL, and LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application report explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with issues when designing with families in which floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

Characteristics of Slow or Floating CMOS Inputs

Both CMOS and BiCMOS families have a CMOS input structure. This structure is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on, the p-channel is off, and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5-V V_I (see Figure 2). This is not a problem when switching states within the data-sheet-specified input transition time limit specified in the recommended operating conditions table for the specific devices. Examples are shown in Figure 3.

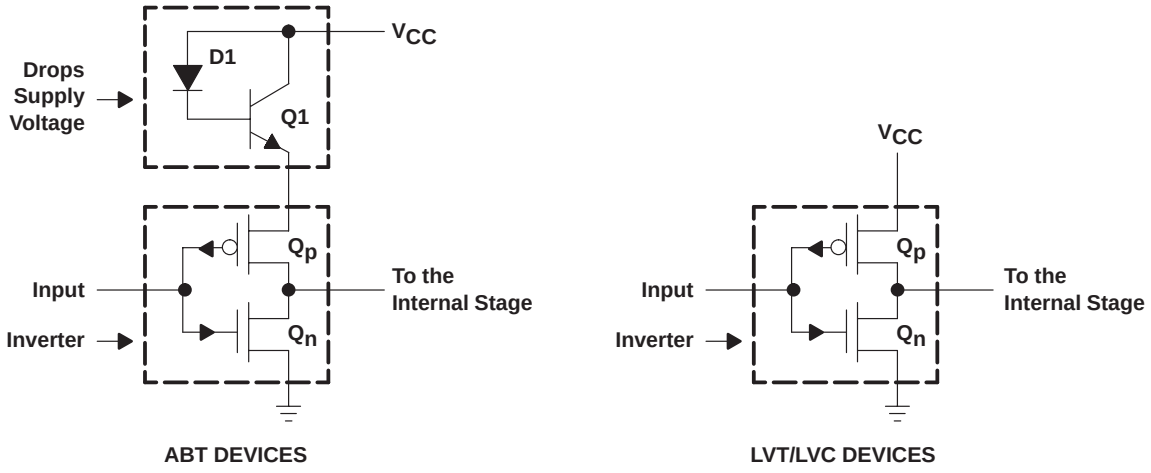

Figure 1. Input Structures of ABT and LVT/LVC Devices

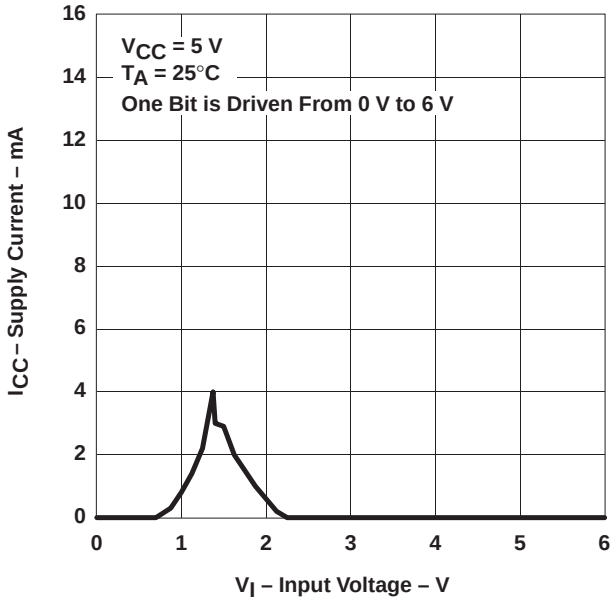

Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions†

				MIN MAX	UNIT
Δt/Δv	Input transition rise or fall rate	ABT octals		5	ns/V
		ABT Widebus™ and Widebus+™		10	
		AHC, AHCT		20	
		FB		10	
		LVT, LVC, ALVC, ALVT		10	
		LV		100	
		LV-A	V_{CC} = 2.3 V to 2.7 V	200	
			V_{CC} = 3 V to 3.6 V	100	
			V_{CC} = 4.5 V to 5.5 V	20	
t_t	Input transition (rise and fall) time	HC, HCT	V_{CC} = 2 V	1000	ns
			V_{CC} = 4.5 V	500	
			V_{CC} = 6 V	400	

† Refer to the latest TI data sheets for device specifications.

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package occurs.

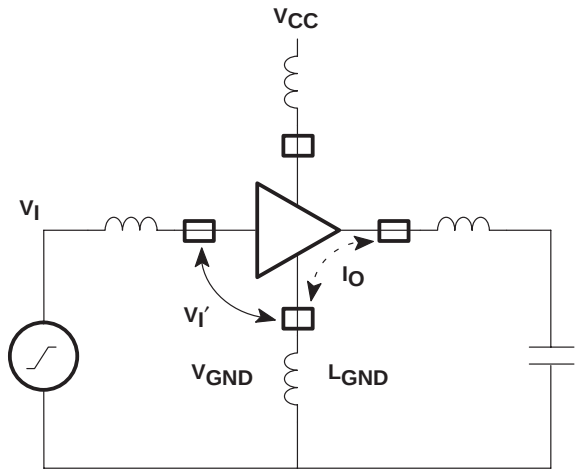

Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver has 36 I/O pins floating at the threshold, the current from V_{CC} can be as high as 150 mA to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT V_I = 3.4 V, ΔI_{CC} = 1.5 mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as shown in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

For CBT or CBTLV devices, this applies to the control inputs. For FB and GTL devices, this applies to the control inputs and the TTL ports only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
ΔI_{CC}‡	ABT, AHCT	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		1.5	mA
	CBT Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	
ΔI_{CC}‡	CBTLV Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND		750	µA
ΔI_{CC}‡	LVT	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND		0.2	mA
	LVC, ALVC, LV					0.5	

† Refer to the latest TI data sheets for device specifications.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Examples of Supply-Current Change of the Input at TTL Level as Specified in Data Sheets

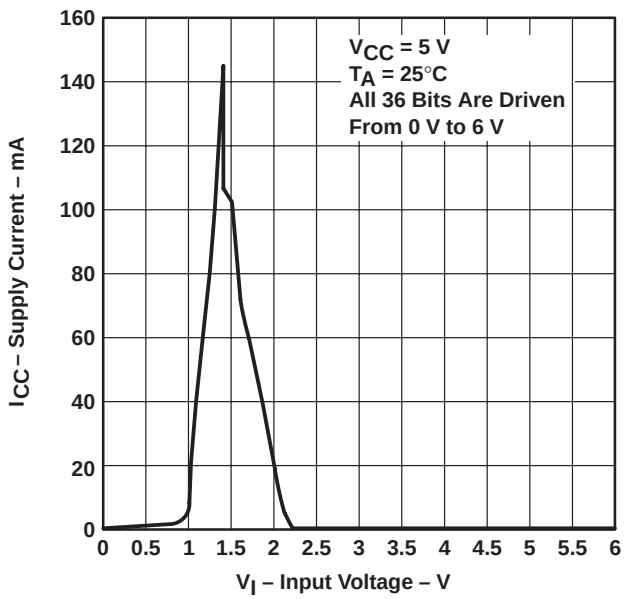

Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

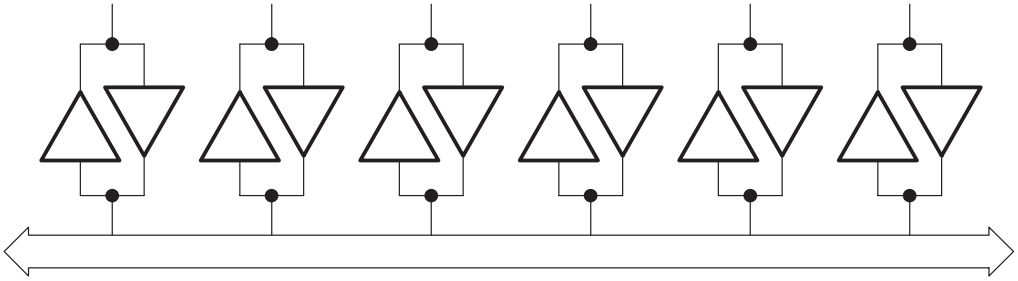

Figure 7. Typical Bidirectional Bus

Recommendations for Designing More-Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus always is either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is $I_{OZ} = 50\ \mu A$ and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as shown in equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \qquad (1)$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus does not exceed the 0.8-V level specified. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components may oscillate, or device reliability may be affected.

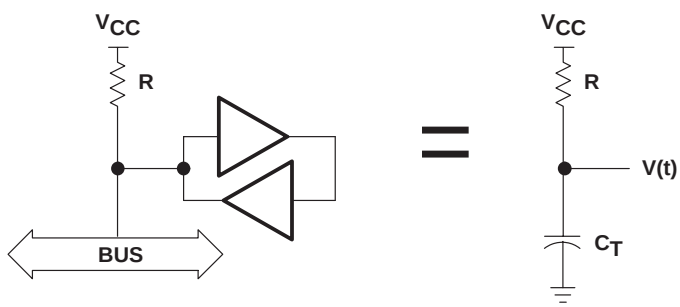

Figure 8. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C_T represents the device plus the bus-line capacitance and R is a pullup resistor to V_{CC}. The value of the required resistor can be calculated as shown in equation 2.

$$V(t) = V_{CC} - [e^{-t/RC_T}\ (V_{CC} - V_i)] \qquad (2)$$

Where:

V(t)	=	2 V, minimum voltage at time t
V_i	=	0.5 V, initial voltage
V_{CC}	=	5 V
C_T	=	total capacitance
R	=	pullup resistor
t	=	maximum input rise time as specified in the data sheets (see Figure 3).

Solving for R, the equation becomes:

$$R = \frac{t}{0.4 \times C_T} \quad (3)$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.4 \times C \times N} \quad (4)$$

Where:

C = individual component and trace capacitance
N = number of components connected to the bus

Assuming that there are two components connected to the bus, each with a capacitance C = 15 pF, requiring a maximum rise time of 10 ns/V and t = 15-ns total rise time for the input (2 V), the maximum resistor size can be calculated:

$$R = \frac{15\ \text{ns}}{0.4 \times 15\ \text{pF} \times 2} = 1.25\ \text{k}\Omega \quad (5)$$

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI™) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

Table 1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+ (32 and 36 bit)	All devices
ABT Octals and Widebus	Selected devices only
AHC/AHCT Widebus	TBA (Selected devices only)
Low Voltage (LVT and ALVC)	All devices
LVC Widebus	All devices

Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

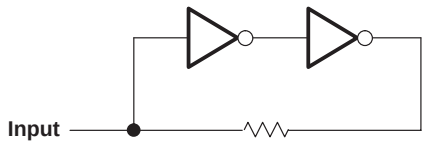

Figure 9. Typical Bus-Hold Circuit

As mentioned previously in this section, TI offers the bus-hold capability as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n-channel and a p-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the n-channel is on. Both channels have a relatively small surface area — the on-state resistance from drain to source, R_{dson}, is about 5 kΩ.

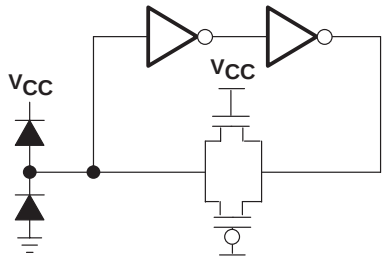

Figure 10. Stand-Alone Bus-Hold Circuit (SN74ACT107x)

Assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 µA and the voltage drop across the 5-kΩ resistance is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus-hold circuit can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ V}{10\ \mu A \times 5\ k\Omega} = 16\ \text{components} \quad (6)$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus-hold circuit. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At V_I = –1V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.

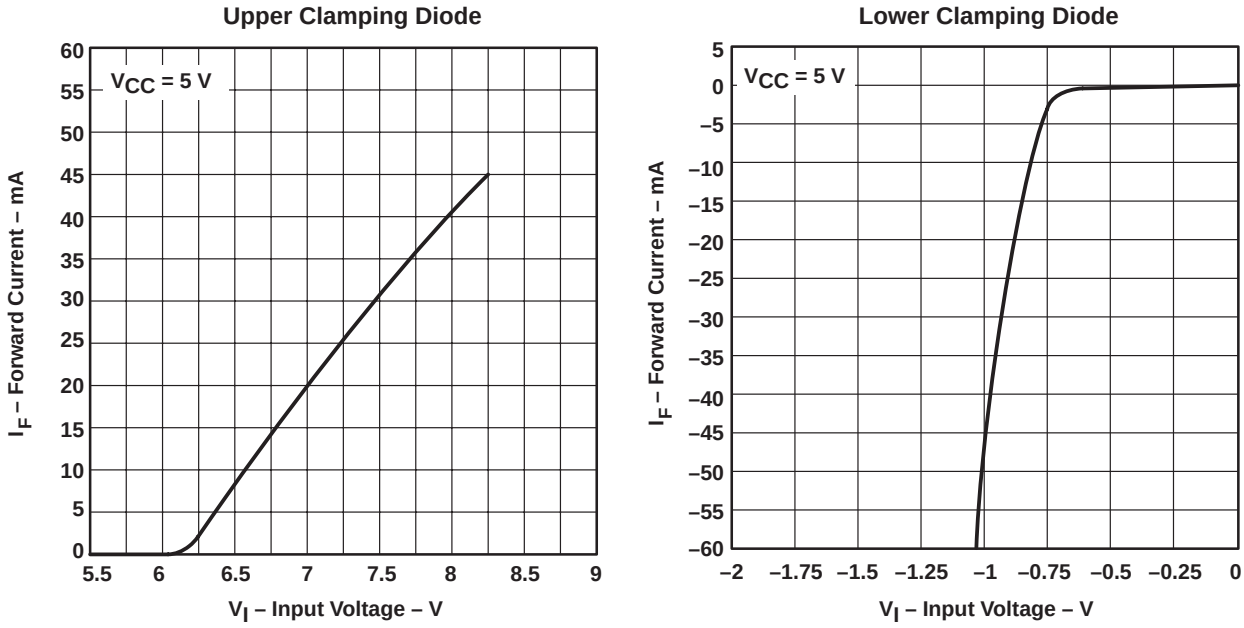

Figure 11. Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit, with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus-hold circuit can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus-hold circuit is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).

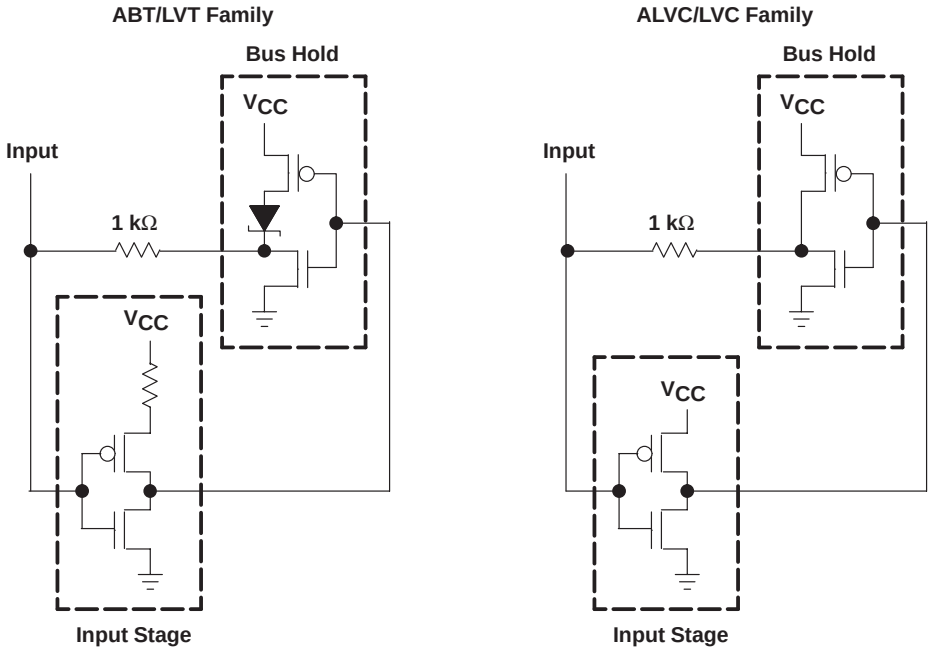

Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus-Hold Circuit

Figure 13 shows the input characteristics of the bus-hold circuit at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 µA for 3.3-V input and 400 µA for 5-V input.

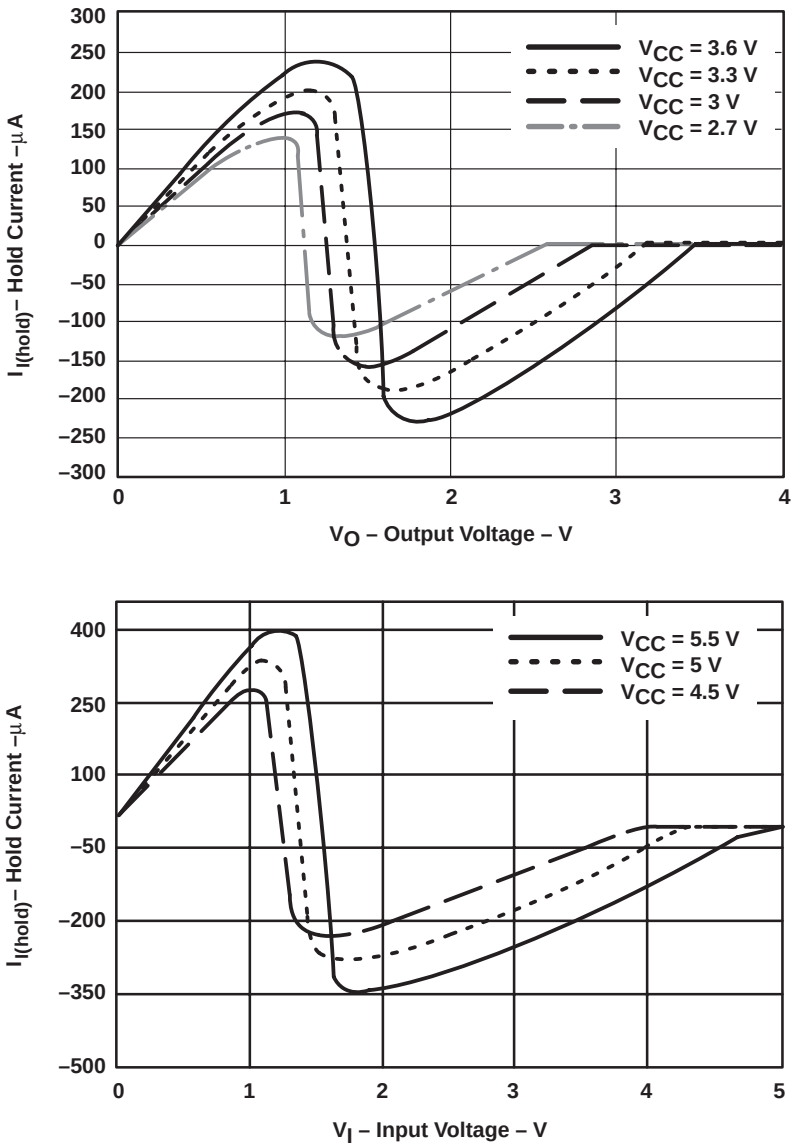

Figure 13. Bus-Hold Input Characteristics

When multiple devices with bus-hold circuits are driven by a single driver, there may be some concern about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold circuits require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1cm, with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus-hold circuit disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus-hold circuit tries to counteract the driver, causing the rise or fall time to increase. Then, the bus-hold circuit changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

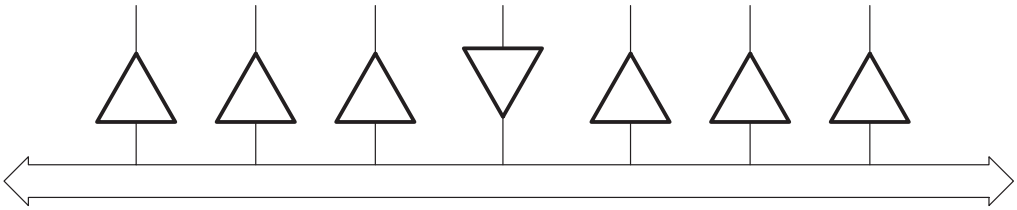

Figure 14. Driver and Receiver System

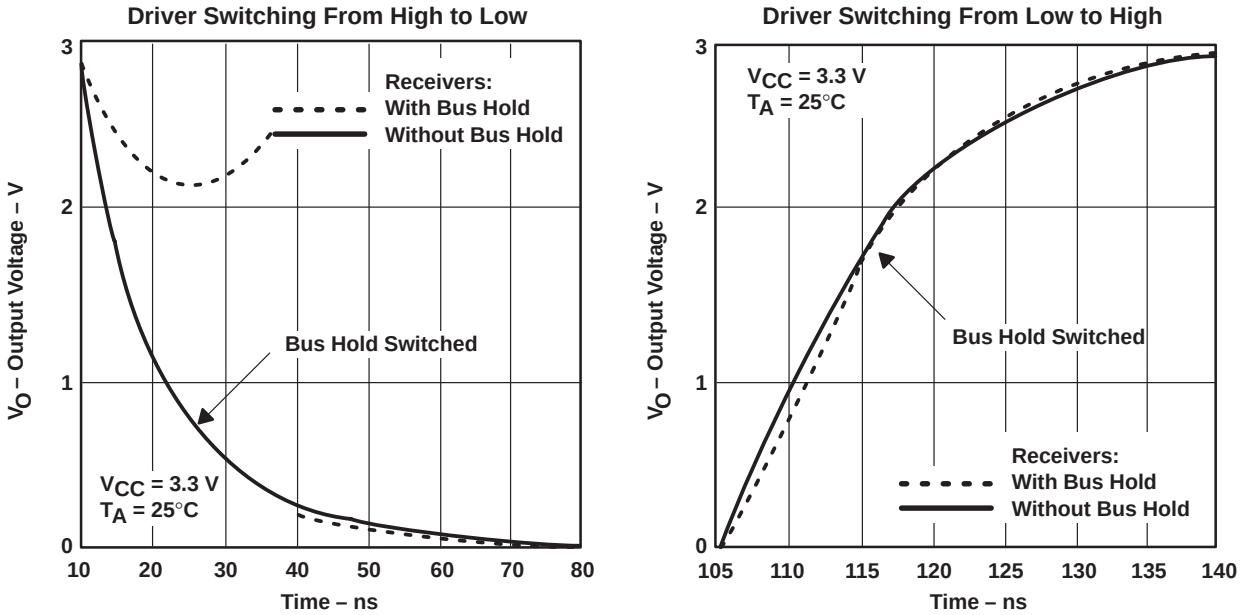

Figure 15. Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. The spike at about 1.5-V V_I is due to both the n-channel and the p-channel conducting simultaneously. This is one of the CMOS transistor characteristics.

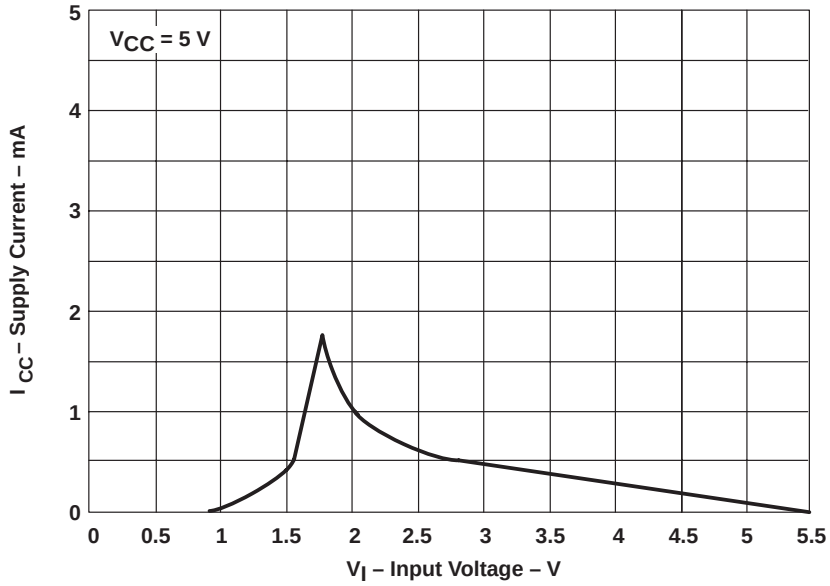

Figure 16. Bus-Hold Circuit Supply Current Versus Input Voltage

The power consumption of the bus-hold circuit is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies, with or without bus hold. The increase in power consumption of the bus-hold circuit at higher frequencies is not significant enough to be considered in power calculations.

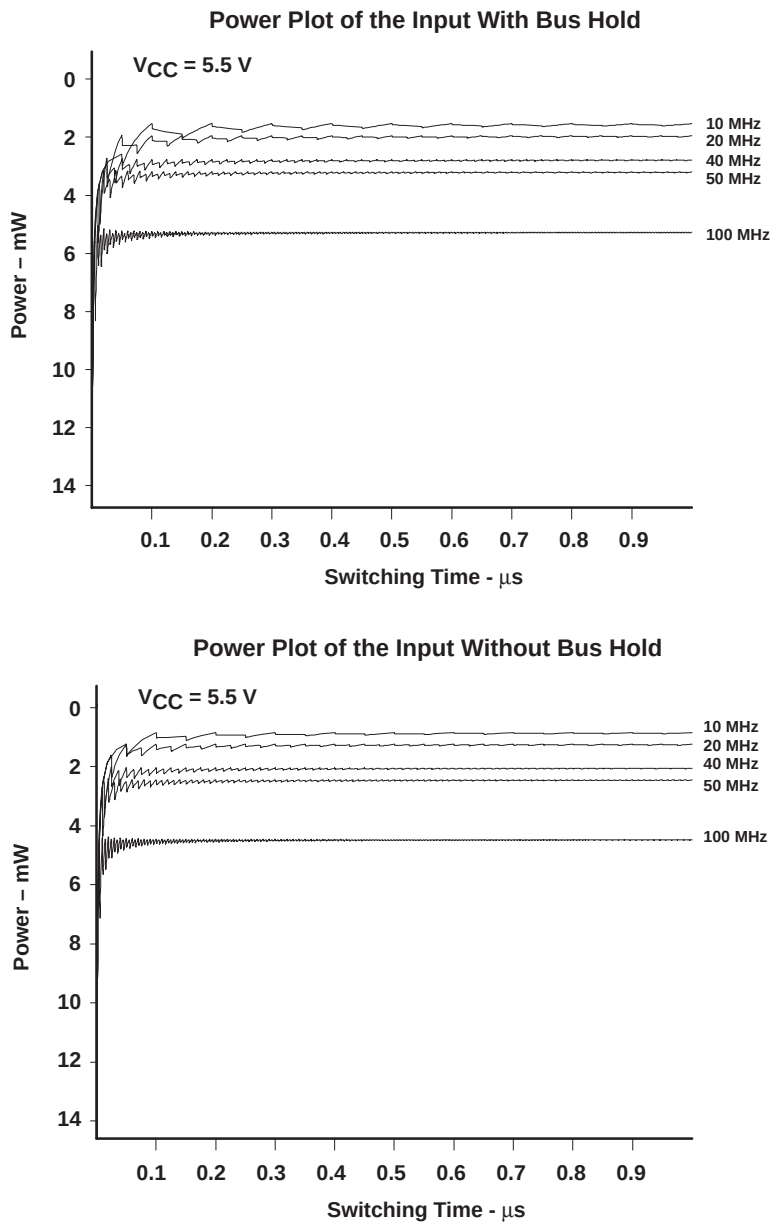

Figure 17. Input Power With and Without Bus Hold at Different Frequencies

Figure 18 shows the data-sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus-hold circuit sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because the bus-hold circuit behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with the bus-hold feature only and does not apply to buffers. All LVT, ABT Widebus+, and selected ABT octal and Widebus devices have the bus-hold feature (refer to Table 1 or contact the local TI sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature)†

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	–75		
		LVC, ALVC	V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
		ABT Widebus+ and selected ABT	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	–100		
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test because bus hold always is active on an I/O pin. Bus hold tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

† Refer to the latest TI data sheets for device specifications.

Figure 18. Example of Data-Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. The three methods recommended in this application report should be considered. If it is not possible to control the bus directly, and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic

SCEA003A
March 1997

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Contents

List of Illustrations

Introduction

This application report examines the requirements for a low-swing interface in high-speed digital systems and how well this need is addressed by two interface standards: backplane Transceiver Logic (BTL) and Gunning Transceiver Logic (GTL). Both interface standards attempt to improve the performance of high-speed digital systems by reducing the difference between the logic high-voltage level and the logic low-voltage level.

A comparison of various performance criteria, such as power consumption, noise immunity, capacitive loading, speed, and packaging, shows that GTL and BTL provide a compelling solution in both point-to-point and backplane environments. Guidelines for system designs using Texas Instruments (TI) GTL and BTL products are addressed, including associated voltage supplies and proper termination techniques.

Test Setup

The TI GTL16612 and FB1650 were used to study the various performance levels. A backplane-like design has been established to perform the laboratory work supporting this application report. Four boards with 2-in. stubs and 50-Ω interconnecting transmission lines were used to simulate the backplane environment. A 50-MHz frequency was used unless otherwise noted. The output supply voltage (V_{TT}) was supplied through a resistor at each end of the backplane (50-Ω to 1.2 V for GTL and 33-Ω to 2.1 V for BTL) for both families as specified in both IEEE (BTL) and JEDEC (GTL) standards. Figure 1 shows the backplane model with all four boards connected.

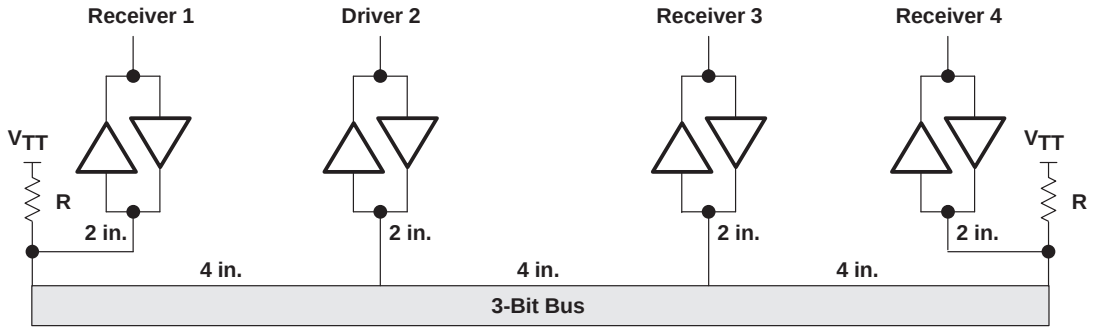

Figure 1. Backplane Model With All Four Boards Connected

Another design has been used to simulate the transmission-environment effect when transferring data across a longer point-to-point transmission line. Figure 2 shows the same backplane model with only one driver and one receiver used to transfer the data across 12-in., 28-in., and 48-in. transmission lines.

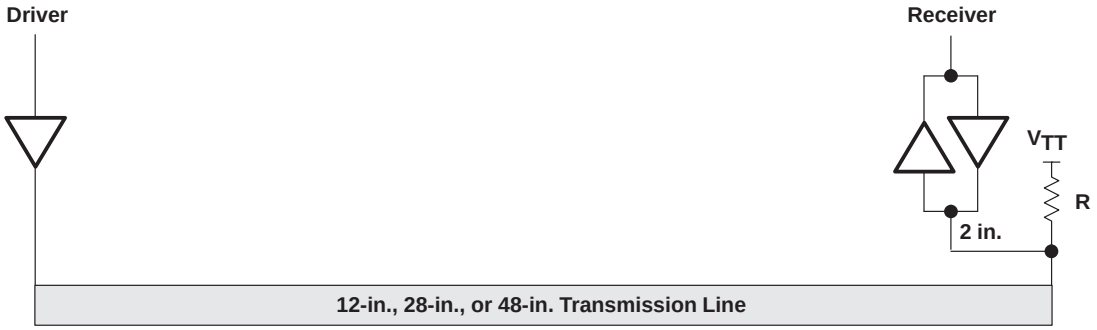

Figure 2. Point-to-Point Model With Only One Driver and One Receiver Connected

Advantages of GTL or BTL Over CMOS/TTL

BTL and GTL were developed to solve the bus-driving problem associated with TTL and to enhance the performance of point-to-point and backplane applications. BTL and GTL also eliminate the need for the extra time required for the TTL signal to settle due to reflection and noise generated when switching. The 1-V swing of both signals versus the 3-V to 5-V swing of TTL and CMOS signals helps reduce the noise generated on the bus when the outputs are switching simultaneously. Table 1 shows the minimum high-level output voltage (V_{OH}) and the maximum low-level output voltage (V_{OL}) of CMOS, TTL, BTL, and GTL signals.

Table 1. V_{OH} and V_{OL} Levels for Various Families

LOGIC LEVEL	V_{OH}min (V)	V_{OL}max (V)
CMOS	3.8	0.44
TTL	2.4	0.55
BTL	2.1	1
GTL	1.2	0.4
GTL+	1.5	0.4

BTL and GTL buffers are designed with minimal output capacitance (5 pF maximum) compared to a TTL output buffer (8 pF to 15 pF typical). A TTL or CMOS output capacitance, coupled with the capacitance of the connectors, traces, and vias reduces the characteristic impedance of the backplane. For high-frequency operation, this phenomenon makes it difficult for the TTL or CMOS driver to switch the signal on the incident wave. A TTL or CMOS device needs a higher drive current than presently available to be able to switch the signal under these conditions. However, increasing the output drive clearly increases the output capacitance. This scenario again reduces the characteristic impedance even more. That is why a lower signal-swing family with reduced output capacitance, such as BTL or GTL, is recommended when designing high-speed backplanes.

GTL Family Input and Output Structure

The GTL input receiver is a differential comparator with one side connected to the externally provided reference voltage, V_{REF}. The threshold is designed with a precise window for maximum noise immunity ($V_{IH} = V_{REF} + 50$ mV and $V_{IL} = V_{REF} - 50$ mV). The output driver is an open-drain n-channel device which, when turned off, is pulled up to the output supply voltage (V_{TT}). When turned on, the device can sink up to 40 mA of current (I_{OL}) at a maximum output voltage (V_{OL}) of 0.4 V. The output is designed for a 50-Ω transmission line terminated at both ends (25-Ω total load). The inputs and outputs are designed to work independently of the device's V_{CC}. They can communicate with devices designed for 5-V, 3.3-V, or even 2.5-V V_{CC}. The TTL input is a 5-V tolerant 3.3-V CMOS inverter that can interface with 5-V TTL signals. Bus hold is also provided on the TTL port to eliminate the need for external resistors when the inputs and outputs are unused or floating. The TTL output is a bipolar output. It is similar to the LVT output structure.[1] At this time, the GTL16612 and GTL16616 devices require two power supplies to function: a 5-V supply ($V_{CC(5)}$) for the GTL and a 3.3-V supply ($V_{CC(3.3)}$) for the LVTTL. The maximum operating frequency of the family is 95 MHz (GTL16612 and GTL16616). The GTL16622 and GTL16923 will operate up to 200 MHz in both directions (GTL to TTL or TTL to GTL) and will have a single 3.3-V power supply.[1] Figure 3 shows a typical GTL input and output circuit.

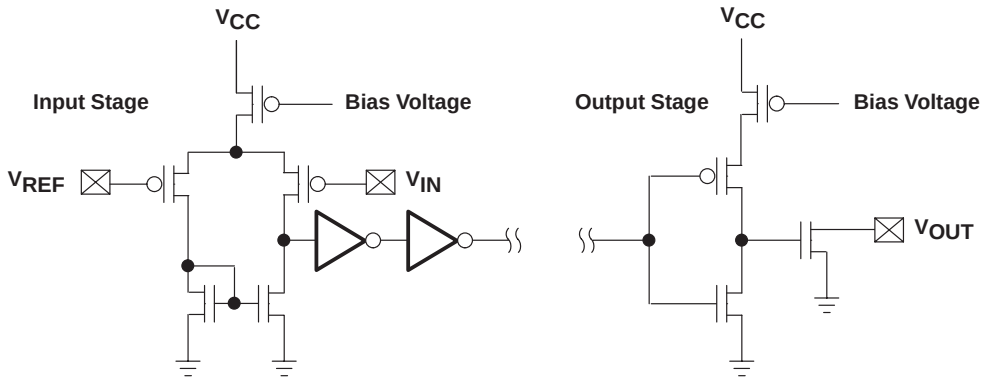

Figure 3. Typical GTL Input and Output Cells

BTL Family Input and Output Structure

The BTL input receiver is a differential amplifier with one side connected to an internal reference voltage. The threshold is designed with a narrow window (V_{IH} = 1.62 V and V_{IL} = 1.47 V). Unlike GTL, BTL requires a separate supply voltage for the threshold circuit to eliminate any noise generated by the switching outputs. The output driver is an open-collector output with a termination resistor selected to match the bus impedance. When the device is turned off, the output is pulled up to the output supply voltage (V_{TT} = 2.1 V typical). The inputs and outputs work independently of the device's V_{CC}. They can communicate with devices designed for 5-V or 3.3-V V_{CC}. The TTL input is a 5-V CMOS inverter, and the output is a bipolar output similar to the ABT output structure.[1] BTL requires three power supplies: the main power supply (V_{CC}), the bias generator supply (BG V_{CC}), and the bias supply voltage (BIAS V_{CC}) that establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected. The maximum operating frequency of the BTL family is 75 MHz, depending on the application as well as the board layout. Figure 4 shows a typical BTL input and output circuit.

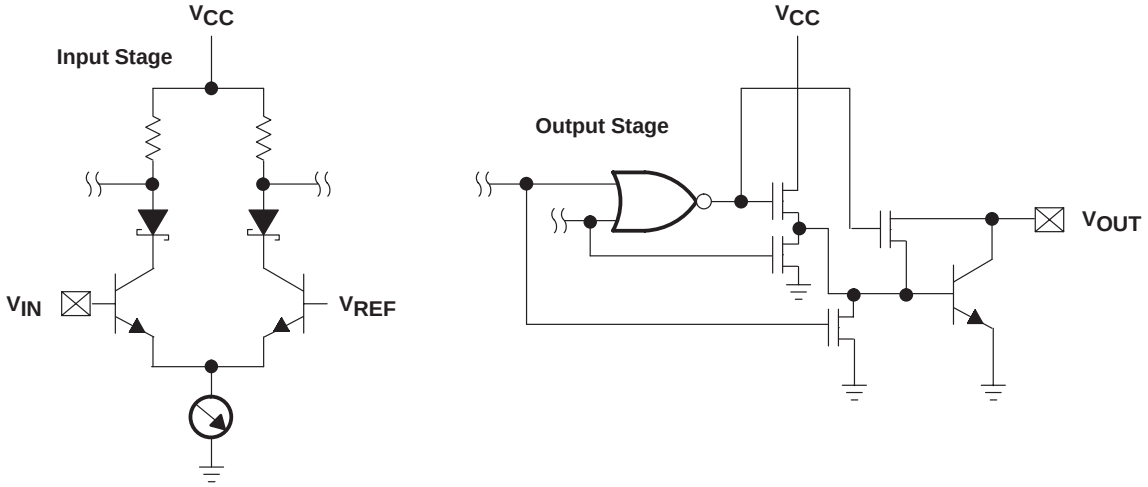

Figure 4. Typical BTL Input and Output Cells

Power Consumption

Several factors influence the power consumption of a device: frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance of the device. For BTL and GTL devices, the output power is supplied externally by the output voltage supply (V_{TT}). The maximum operating frequency is limited by the thermal characteristics of the package. TI provides package power-dissipation information in data sheets under “absolute maximum ratings”. These values are calculated using a junction temperature of 150°C and a board trace length of 750 mils (no airflow).[2] Traces, power planes, connectors, and cooling fans play an important role in improving heat dissipation. Figure 5 shows the power consumption of BTL and GTL devices driving the backplane described above. As the frequency increases, GTL16612 power consumption does not increase as fast as the FB1650. This characteristic is due to the predominant use of CMOS technology, the lower drive current, and the lower voltage swing of GTL (0.8-V swing for GTL versus 1-V swing for BTL). Lower drive current and lower voltage swing are two of the benefits that GTL provides over BTL drivers. A power-consumption comparison (see Table 2) illustrates the advantage of GTL over BTL when 160 active inputs and outputs are switching.[3] Another benefit GTL offers is that the family uses the common 56-pin SSOP and TSSOP packages rather than the 100-pin thin quad flat package (TQFP) with a heat slug mounted above the die in BTL parts. The pin count on the TQFP package is almost twice the pin count of the SSOP or TSSOP packages.

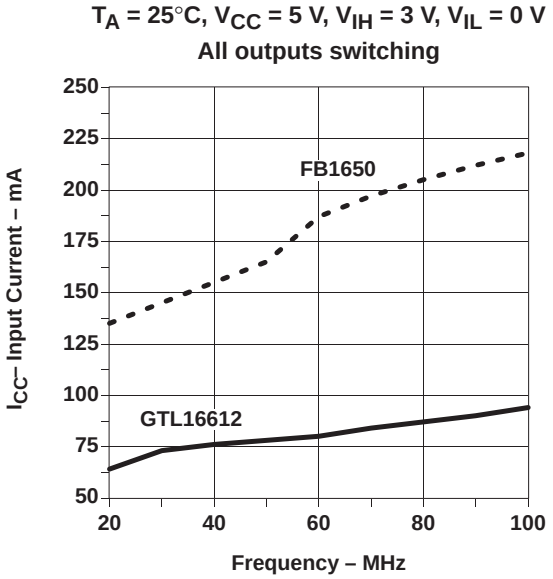

Figure 5. FB1650 and GTL16612 Power Consumption With All Outputs Switching

Table 2. Power Comparison (160 Active Inputs and Outputs)

TECHNOLOGY	POWER (W)	TERMINATION (BOTH ENDS)
BTL	11	33 Ω to 2.1 V
GTL	2	50 Ω to 1.2 V

Simultaneous Switching

In a given digital circuit, there is a large change in current over a very short time when multiple outputs switch simultaneously. As this increased current flows through the bond wires and the leadframe, it develops a voltage across the wire's inductance. This feedback mechanism is known as simultaneous switching noise (SSN). This noise manifests itself as V_{OL} or V_{OH} voltage bounce at the package pin(s).

From basic circuit analysis, the induced voltage across an inductor is defined as:

$$v = L\frac{di}{dt} \quad (1)$$

Where:

L = Inductance
di/dt = Rate of change of the current

The current through an output is dependent on the voltage level and the load at the output, which can be expressed mathematically as:

$$i = C\frac{dv_{out}}{dt} \quad (2)$$

Analysis of equations (1) and (2) clearly shows that because of the lower voltage swing, GTL and BTL offer better noise immunity compared to TTL or CMOS outputs.

As the speed of today's circuits increases, the current rate of change (di/dt) increases and so does the susceptibility to SSN, i.e., voltage bounce (GND and V_{CC}). The standard methodology devised by the industry to measure voltage bounce is to keep one output at either logic high (V_{OH}) or logic low (V_{OL}) and to switch all other outputs at a predefined frequency. Figures 6 through 9 compare both GTL and BTL for noise immunity as 17 outputs are switching simultaneously.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

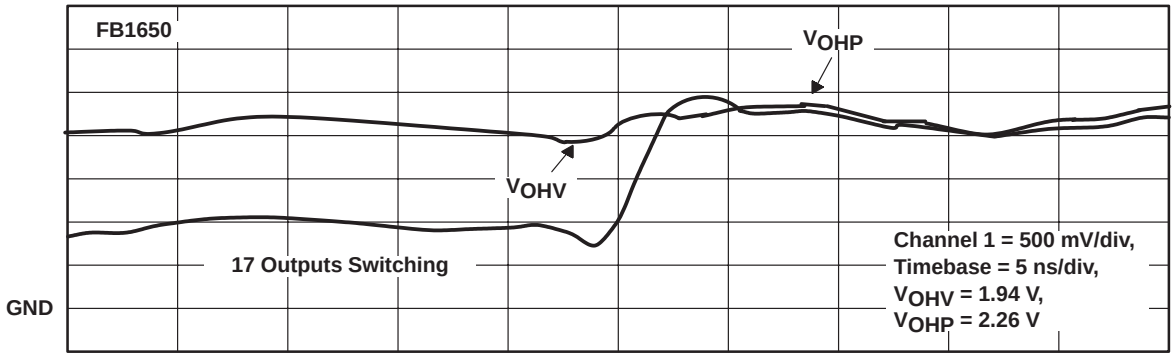

Figure 6. FB1650 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω

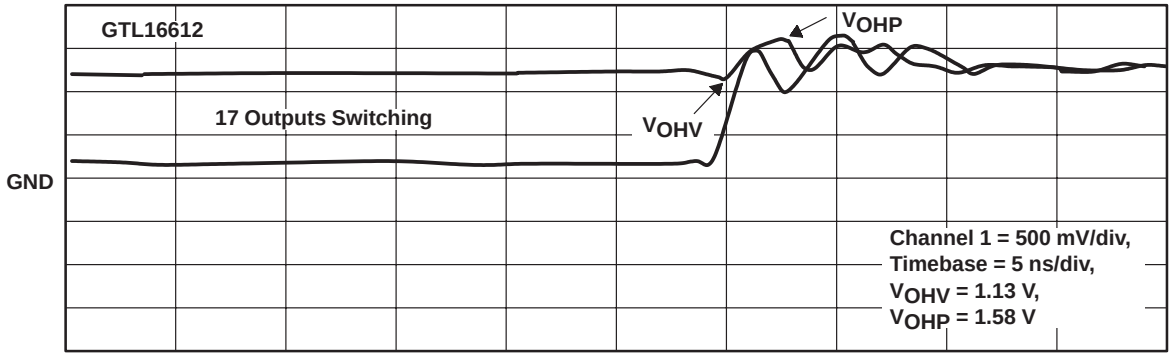

Figure 7. GTL16612 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

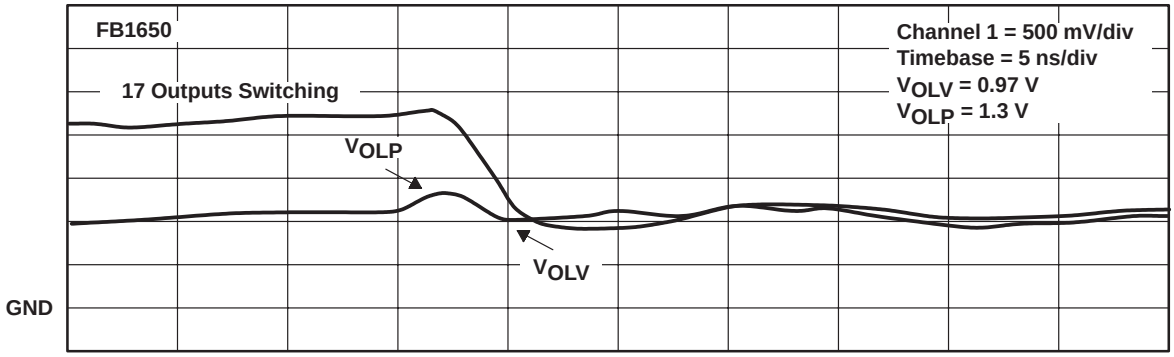

Figure 8. FB1650 Low Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω

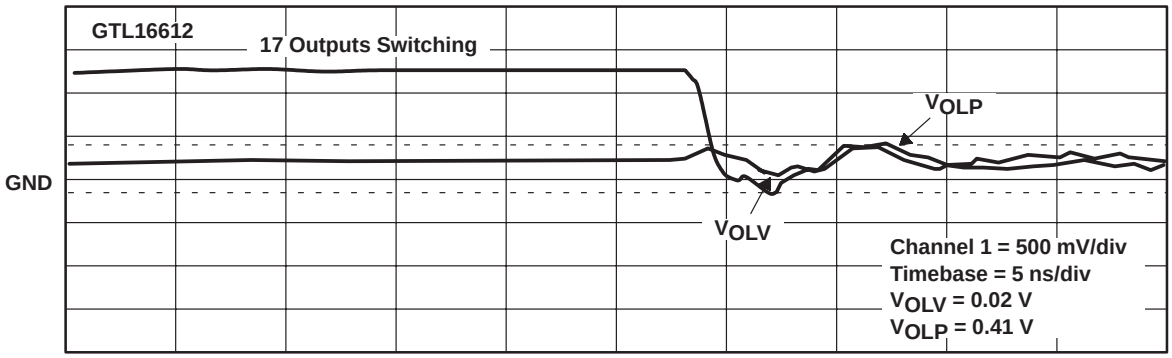

Figure 9. GTL16612 Low Output Voltage Peak and Valley Noise on an Unswitched Output

Output Capacitance

GTL and BTL devices are designed to meet a 5-pF capacitance on their input and output ports (B port). Figure 10 shows the variation of the output capacitance across both processes.

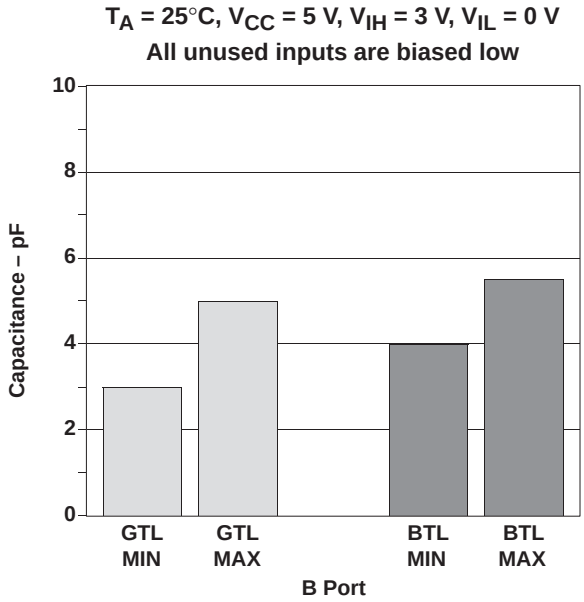

Figure 10. Capacitance Variation Across Process

Slew Rate

Slew rate plays an important role in backplane or point-to-point application designs. The slower the output slew rate of a device, the less susceptible the signal is to reflections and noise. Using the backplane model (see Figures 1 and 2), the output slew rate (t_r and t_f) of the driving device was taken under the following conditions: a 10-in., 50-Ω transmission line and a single termination to V_{TT} at the receiver end. Figures 11 through 14 show the rise and fall times of both devices taken between the two specified voltages of 0.5 V to 1 V for GTL and 1.3 V to 1.8 V for BTL. Both the BTL and GTL slew rates are acceptable.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

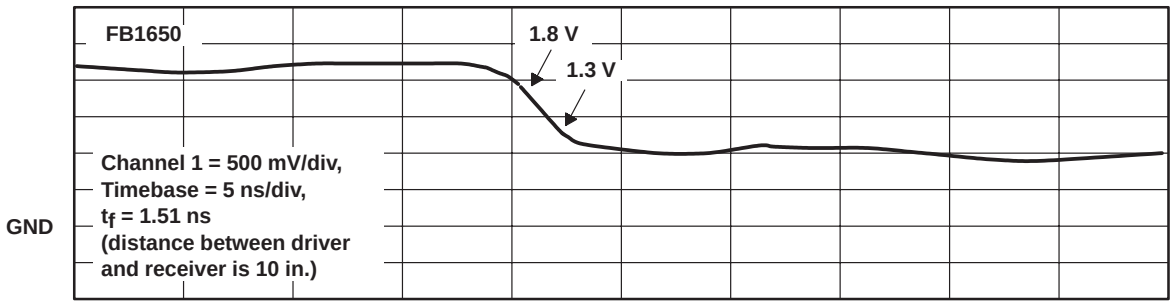

Figure 11. FB1650 Fall Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

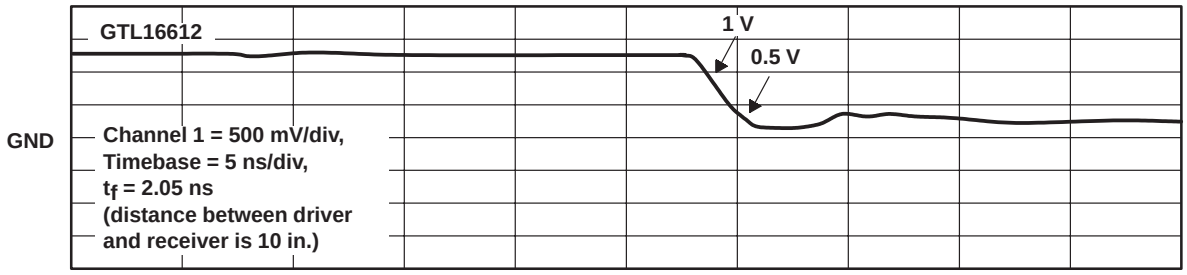

Figure 12. GTL16612 Fall Time Measured Between 0.5 V and 1 V

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

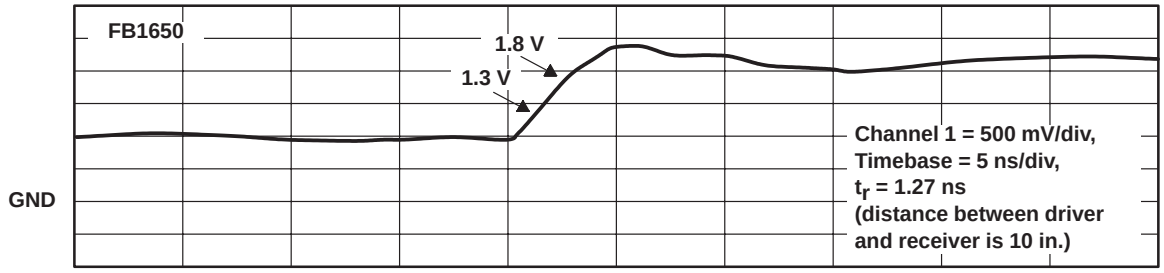

Figure 13. FB1650 Rise Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

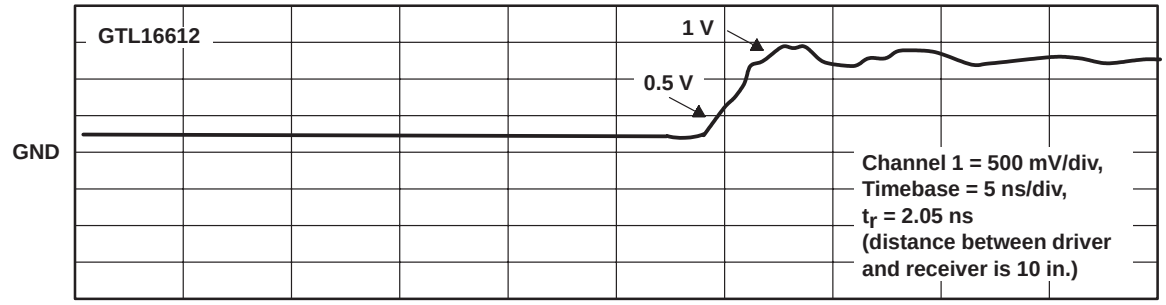

Figure 14. GTL16612 Rise Time Measured Between 0.5 V and 1 V

Signal Integrity

Figures 15 and 16 show the signal integrity of data propagating across the 50-Ω transmission line using three cable lengths (A = 12 in., B = 28 in., and C = 46 in.). The clock frequency is 75 MHz. The measurement was taken at the receiver end of the cable. The GTL output waveform has kept its input square-wave shape better than the BTL waveform has. The cable and the termination resistors used in this laboratory are not precisely matched; that is why a small reflection can be seen on the GTL outputs when switching low to high. In real systems, where both the termination resistor and the traces are matched, these reflections will be reduced.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 75 MHz

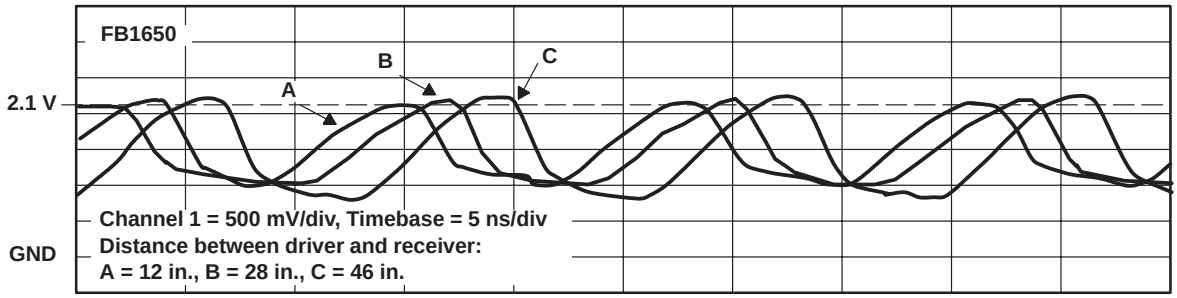

Figure 15. FB1650 Signal Integrity at the Receiver Input Using Different-Length Cables

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 75 MHz

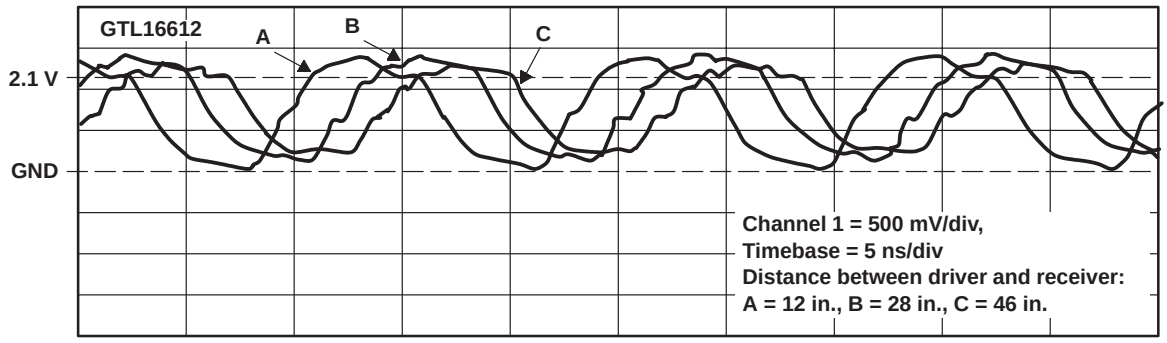

Figure 16. GTL16612 Signal Integrity at the Receiver Input Using Different-Length Cables

Design Considerations

To successfully design with the GTL family, several rules and techniques with regard to voltage generation and proper termination must be followed. First, both 3.3-V and 5-V V_{CC} are needed in the present generation of GTL devices (only the 3.3-V V_{CC} will be needed in the next-generation GTL). Second, the termination voltage (V_{TT}) should be regulated from the 5-V V_{CC}, keeping in mind the current requirements of the outputs (40 mA per output). There are several linear regulators that are capable of performing this function. Depending on the design, the regulator could be either on the backplane itself or on the individual cards. Third, the reference voltage (V_{REF}) must be generated from V_{TT}. The V_{REF} voltage can be generated using a simple voltage-divider circuit with an appropriate bypass capacitor (0.01 µF or 0.1 µF) placed as close as possible to the V_{REF} pin. The V_{REF} input circuitry consumes very little power (1 µA maximum). This enables several devices to have their V_{REF} pin connected to the same voltage-divider circuit, thus eliminating the need for multiple voltage-divider circuits (see Figure 17).

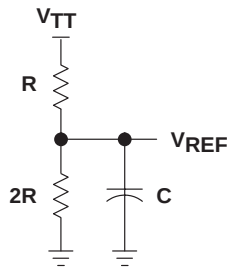

Figure 17. Proposed Circuit to Generate V_{REF}

For the BTL family, four power supplies and two grounds are connected. For live-insertion applications, the power-up sequence should be: the GND pin should make contact first, followed by BIAS V_{CC}. This sequence will precharge the board and the device capacitance and will establish a voltage between 1.62 V and 2.1 V on the BTL outputs. Next, the V_{CC} pin makes contact and, as V_{CC} ramps up, the BIAS V_{CC} circuitry starts to turn off. When V_{CC} reaches its final value, the BIAS V_{CC} circuitry is completely isolated and does not interfere with the device functionality. BG V_{CC} and BG GND pins supply power to the bias generator input circuitry. BG V_{CC} and BG GND must be isolated from the other power supplies to ensure signal integrity at the BTL input. The 2.1-V V_{TT} should be regulated from a higher voltage and should supply enough current to switch all 18 outputs (100 mA per output). V_{TT} variation should not exceed ±2% and it is recommended that proper bypass capacitors (0.01 µF or 0.1 µF) be used. The termination resistor should not exceed ±1% of its resistance value.

Table 3 gives the designer an estimate of the maximum number of loads allowed when designing with GTL and BTL families.[4] Note that crosstalk and poor board layout can degrade the overall quality of the backplane, thereby affecting the number of loads.

Using the formula:

$$t_r,\ t_f = 2.2 \times Z_S \times [(L \times C_O) + (N \times C_N)] \quad \textbf{(3)}$$

and assuming $t_r,\ t_f = t_p = \frac{1}{2f}$ (for worst-case condition), the maximum number of loads on the backplane (N) can be calculated as follows:

$$N = \frac{1}{4.4 \times f \times Z_S \times C_N \times 10^{-6}} - \frac{L \times C_O}{C_N} \quad \textbf{(4)}$$

Where:

t_r = Rise time of the device (ns)
t_f = Fall time of the device (ns)
Z_S = Output impedance of the source (Ω), 25 Ω for GTL, 16.5 Ω for BTL
C_O = Characteristic capacitance per unit length of the transmission line (pF/in.) (see Table 3)
L = Length of the backplane (in.)
N = Maximum number of loads on the backplane
C_N = Capacitance for each load (pF), 5 pF for the device, 5 pF for the connector
t_p = Pulse width of the signal (ns)
f = Frequency of the signal on the backplane (MHz)

Table 3. Typical Strip-Line Characteristics†

DIMENSIONS (mils)			LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in.)	t_{pd} (ns/in.)	MAXIMUM NUMBER OF LOADS		
						GTL		BTL
T	H	W				L = 12 in.	L = 16 in.	L = 24 in.
1.5	6	20	27	6.67	0.18	10	8	12
1.5	6	15	32	5.83	0.186	11	9	14
1.5	10	20	34	5.58	0.189	11	9	14
1.5	12	20	37	4.75	0.176	12	11	16
1.5	10	15	40	4.67	0.187	13	11	16
1.5	12	15	43	4	0.172	13	12	18
1.5	20	20	44	4	0.176	13	12	18
1.5	20	15	51	3.5	0.179	14	13	19
1.5	30	20	55	3.25	0.179	14	13	20
1.5	30	15	61	2.92	0.178	15	14	21

† The characteristic impedance of the strip line is based on the following:
er = 5, relative dielectric constant of the board material (G10 glass epoxy)
H = thickness of the insulation dielectric
T = cross-sectional length of the strip line
W = cross-sectional width of the strip line
Frequency of the signal on the backplane is 50 MHz.

Summary

Today's high-speed backplane and point-to-point applications require devices that can provide high performance, excellent signal integrity, and cost effectiveness. GTL and BTL transceivers are designed to meet these characteristics. Both transceiver families show similar skew, slew rate, and SSN performance. BTL is generally used for heavily loaded backplanes (100-mA I_{OL}) and for frequencies less than 75 MHz. However, the laboratory data presented in this report show that GTL is more suitable for designs that require high performance (up to 100 MHz for the GTL16612 and GTL16616 and 200 MHz for the GTL16622 and GTL16923) and low power consumption at low cost and minimum board space.

References

1. Texas Instruments Incorporated, *ABT Advanced BiCMOS Technology Data Book*, 1994, literature number SCBD002B.
2. Texas Instruments Incorporated, "Package Thermal Considerations", *ABT Advanced BiCMOS Technology Data Book*, 1994, literature number SCBD002B, pg. 13–97.
3. Gunning, Bill; Yuan, Leo; Nguyen, Trung; Wong, Tony, *GTL: A Low-Voltage Swing Transmission Line Transceiver*, March 15, 1991.
4. Texas Instruments Incorporated, *Advanced Schottky Load Management*, 1987, literature number SDAA006.

Next-Generation BTL/Futurebus Transceivers Allow Single-Sided SMT Manufacturing

SCBA003C
March 1997

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Contents

List of Illustrations

Introduction

BTL (IEEE 1194.1-1991) and Futurebus designs offer significant performance advantages over conventional TTL backplane implementations, but these advantages come with trade-offs. Switching noise in the form of ground bounce and EMI must be controlled, and proper termination schemes must be employed to ensure signal integrity in this high-speed switching environment. Trade-offs for price in the form of total system solution versus overall system performance are also of concern. This paper begins with the historical perspective on signal-integrity issues addressed by the IEEE and follows with new pioneering bus-interface solutions to help reduce overall BTL or Futurebus system costs and design complexities.

Current Generation of BTL/Futurebus Transceivers

A number of suppliers have developed BTL and Futurebus transceiver solutions that comply with IEEE 1194.1. These devices share the same reduced output swing and tight switching thresholds shown in Figure 1 and a slew-rate control (see Figure 2). The various devices differ considerably in wafer-fab process technology, propagation-delay performance, and other performance metrics (see Table 1).

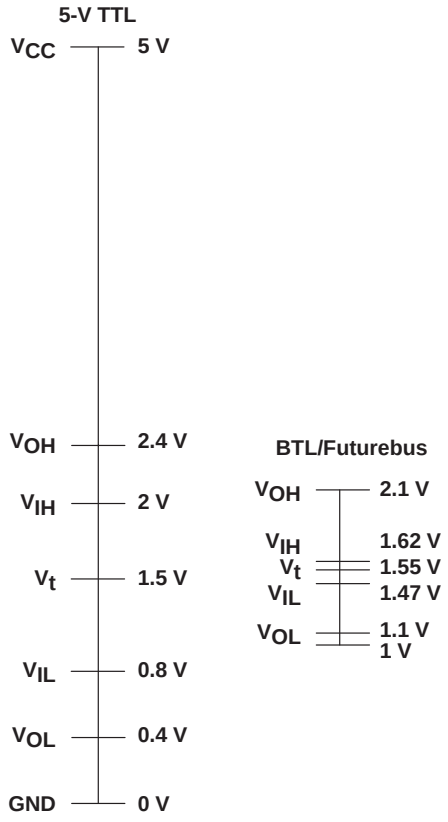


Figure 1. Comparison of TTL and BTL Switching Standards

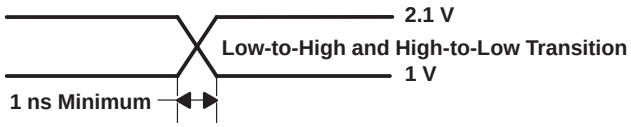


Figure 2. Slew-Rate Control (OEC™) Diagram

Table 1 shows an evolutionary progression in bipolar wafer-fab technology and improved propagation-delay performance. Bipolar fab technologies are chosen for this class of device for their high drive capability, low switching noise, and relative ease of designing (relative to pure CMOS) the analog circuitry required to meet the slew-rate control requirement (see Figure 2). Bipolar circuits have the disadvantage of relatively high power dissipation. The heat generated by this high power dissipation, coupled with the large switching currents coming from the bus termination, place a thermal limitation on the numbers of bits that can be integrated into a single, standard integrated-circuit package (typically, only four bits).

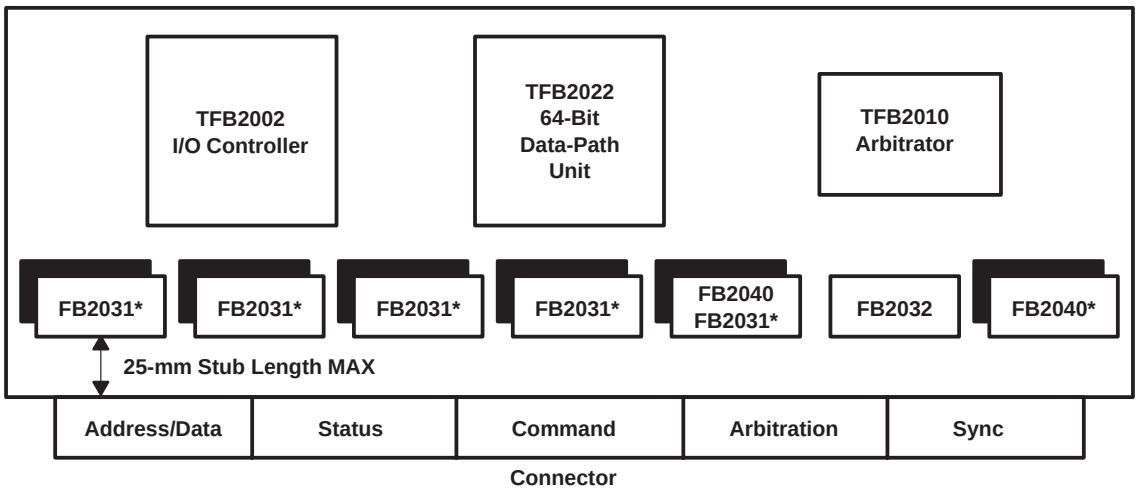
Table 1. BTL/Futurebus Transceiver Offering Available Today

TRANSCEIVER	SUPPLIER	TECHNOLOGY	BITS/PACKAGE	t_{pd} (ns)
ALS056/057	TI, NSC	3-µm Bipolar	4/8	20
DS3890	NSC	2-µm Bipolar	8†	15
DS3896/7	NSC	1.5-µm Bipolar	4/8	12
DS3893A	NSC	1.2-µm Bipolar	4	7
FB1650	TI	0.8-µm BiCMOS	18	7.2
FB1651	TI	0.8-µm BiCMOS	17	7.2
FB1653	TI	0.8-µm BiCMOS	17	6.6
FB2032	TI	0.8-µm BiCMOS	9	8.3
FB2033A	TI	0.8-µm BiCMOS	8	5.6
FB2031	TI, Philips	0.8-µm BiCMOS	9	6.6
FB2040	TI, Philips	0.8-µm BiCMOS	8	6.5
FB2041A	TI, Philips	0.8-µm BiCMOS	7	5.6

† Unidirectional driver only; not a true bidirectional transceiver

The newer class of BiCMOS transceivers employs a bipolar output structure to achieve the desired drive, noise, and slew-rate control of previous-generation products. They also offer higher performance, much lower power dissipation, and take the next step toward higher integration.

Futurebus adds an additional constraint to board layout by mandating that all compliant cards have a maximum stub length of 25 mm to reduce loading and minimize reflections. This is also a wise rule of thumb for non-BTL/Futurebus designs. As data paths have increased in width from 32 to 64 bits (128 bits in the future), this stub-length requirement has forced system designers to wrestle with the manufacturing problems of double-sided surface mounting of the transceivers on boards as large as 12 Standard Units (12SU). Even with the relatively dense packaging of today's fastest and most integrated transceivers, this can be a formidable design problem that adds significantly to the overall manufacturing cost of a board (see Figure 3).



NOTE: The second-part type descriptor (*) indicates that a second transceiver is mounted on the opposite side of the board.

Figure 3. Uncached 64-Bit Futurebus Layout With Texas Instruments Controller Chipset and Today's Most Integrated Transceivers

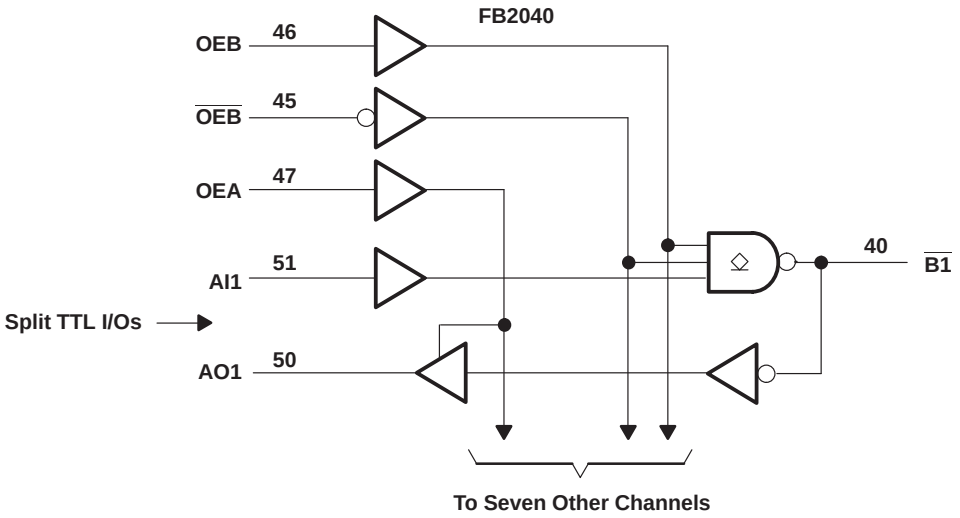
Another problem with the present generation of transceivers is the purchasing requirement for multiple transceiver types. Continuing with the above example, the common 64-bit uncached solution requires three different transceiver types for a complete distributed arbitration Futurebus implementation (see Table 2).

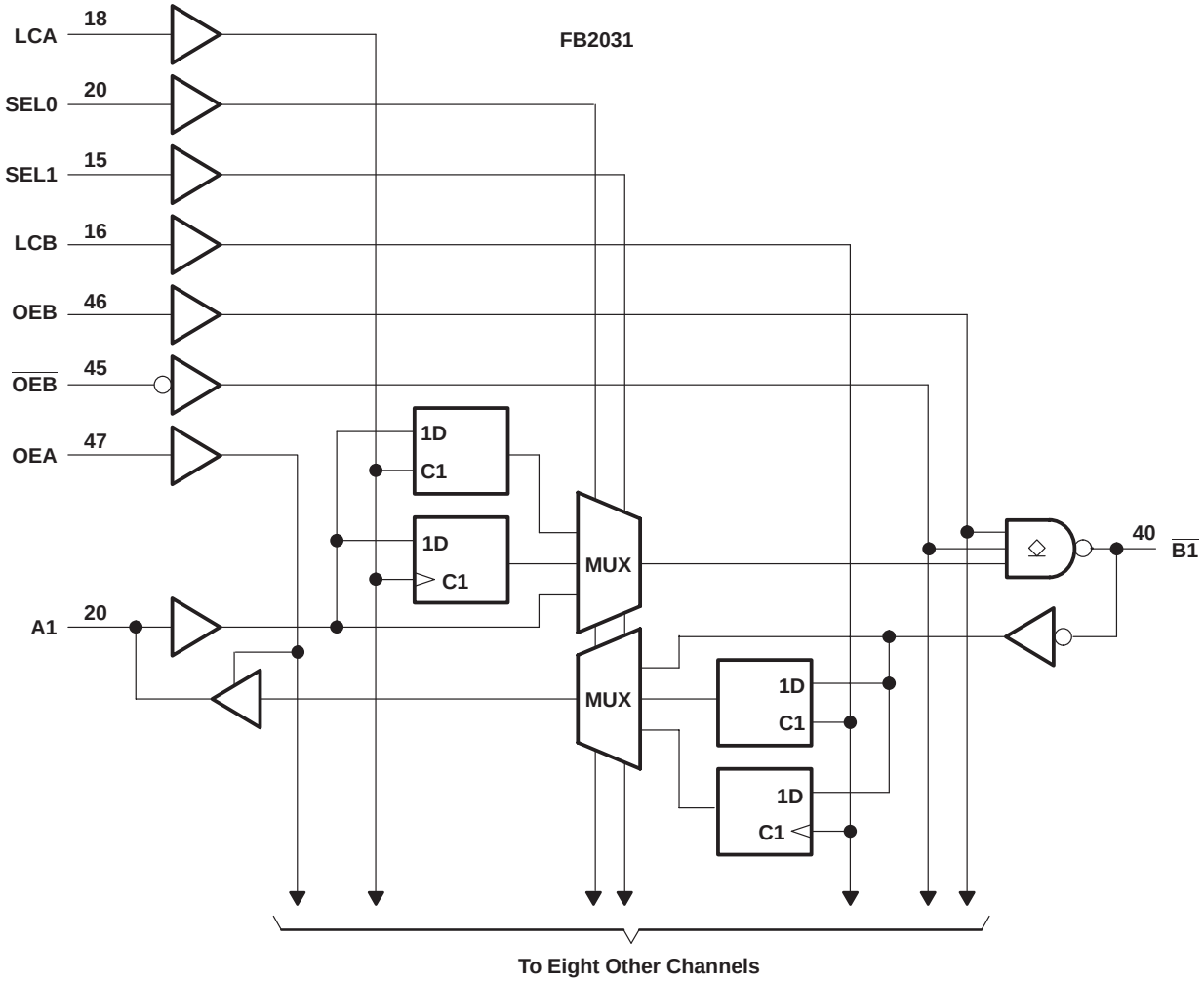
Table 2. Transceiver Descriptions for 64-Bit Uncached Futurebus Boards Using FB20xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD
FB2031	9-Bit Data/Address Transceiver With Clock and Latch	9
FB2032†	Arbitration Contest Transceiver	1
FB2040	8-Bit Status/Sync Transceiver With Split TTL I/O	3
	Total Part Count	13

† Optional for distributed arbitration only

These transceivers were designed quite differently from one another due to the specific functions they perform in the system (data/address, sync, arbitration, status, or command). Figure 4 highlights the functional differences between the FB2040 (status and sync transceiver) and the FB2031 (address/data transceiver). The main distinctions are the universal storage modes (transparent, latched, or clocked) of the FB2031 and the separate, or split, TTL I/O pins of the FB2040. As previously noted, until recently, efforts to develop any sort of true universal BTL/Futurebus transceiver have not been practical due to the absence of a viable, high-power, fine-pitch package with more than 56 pins.





Pin numbers shown are for the RC package.

Figure 4. Functional Differences Between FB2040 Control Transceiver and FB2031 Address/Data Transceiver

A New Generation of BTL/Futurebus Transceivers

In response to the need for single-sided surface mounting and simplified transceiver architectures, Texas Instruments has developed both a high-power package and a series of 18-channel BTL/Futurebus universal bus transceivers (UBT™). These new devices, designated as the FB16xx series, are packaged in a high-power version of the EIAJ standard 100-pin TQFP package (0.5-mm lead pitch). A package cross section, as shown in Figure 5, reveals a metal heatsink that facilitates the excellent thermal performance of the package. Refer to *Thermal Characteristics of SLL Packages and Devices*, literature number SCZA005, for θ_{JA} and reliability issues.

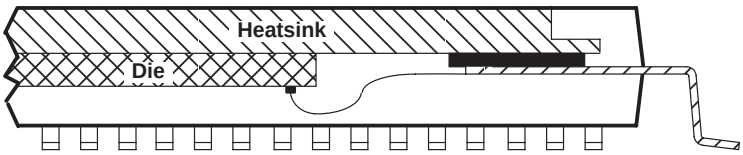
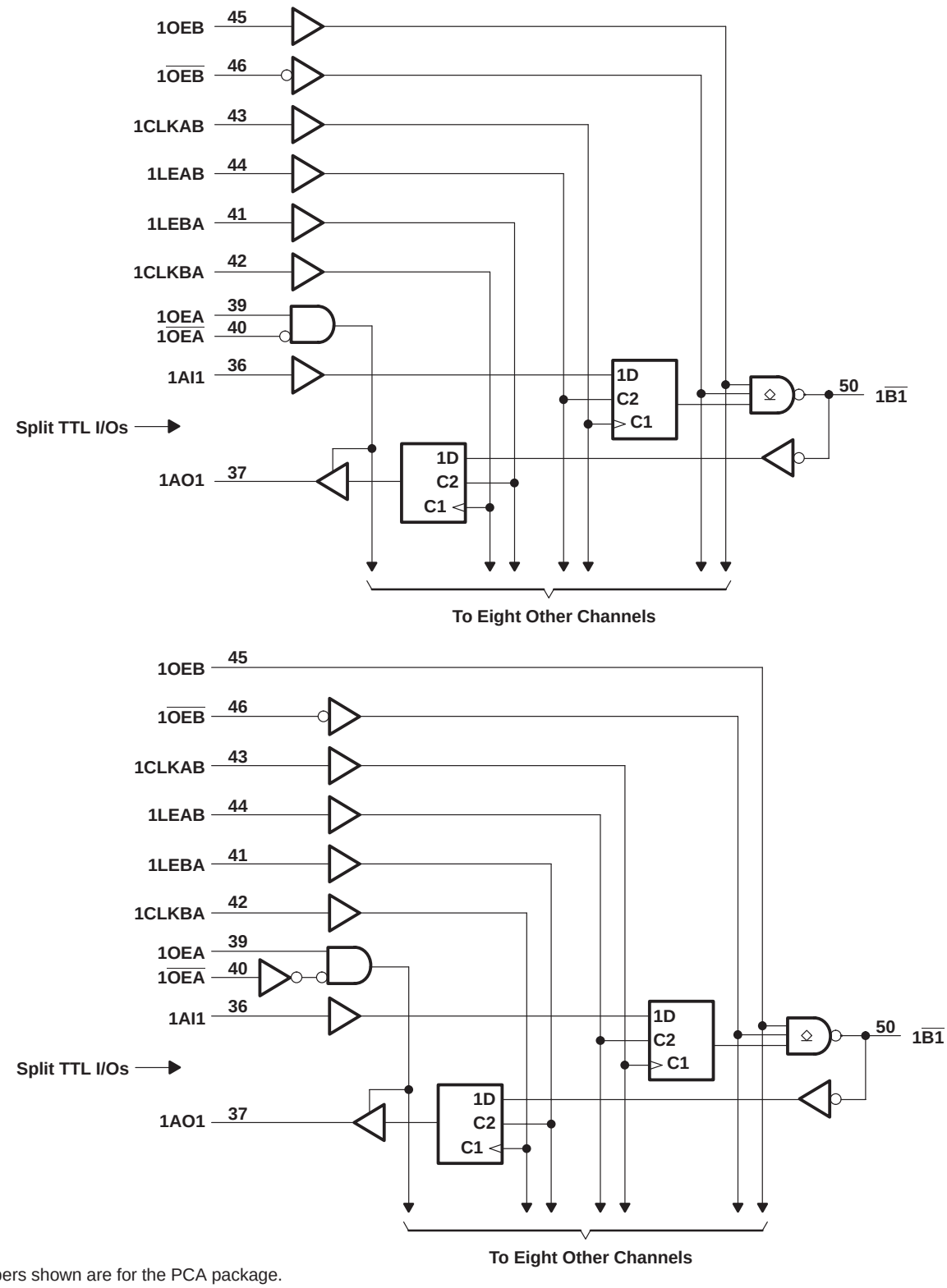


Figure 5. Cross Section of Thermally Enhanced EIAJ 100-Pin TQFP

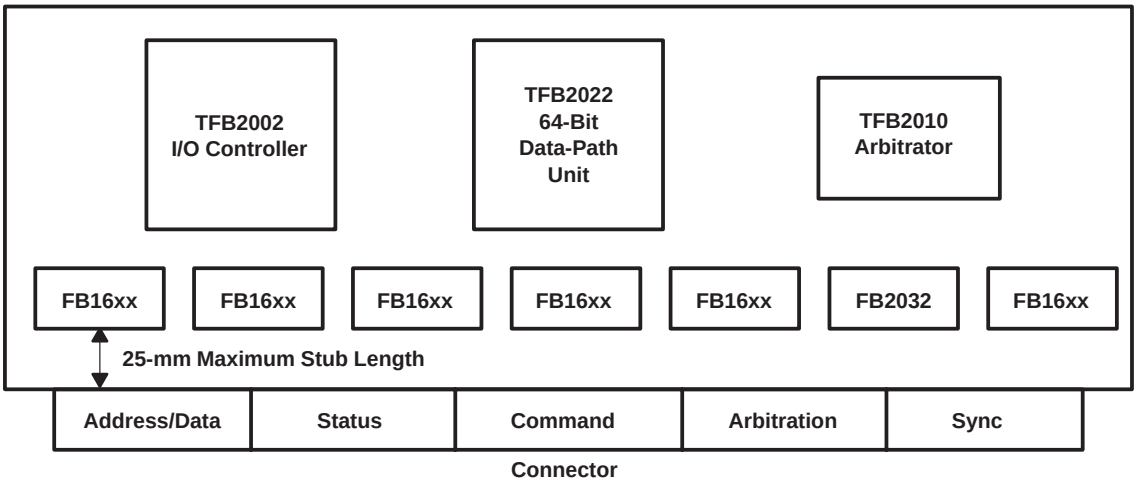
The FB16xx series devices are designed with both the universal data-storage capabilities of the FB2031 address/data transceiver and the separate TTL I/O of the FB2040 control transceiver. This series of devices can be configured as two independent 9-channel transceivers (see Figure 6) or one coherent 18-channel transceiver.



Pin numbers shown are for the PCA package.

Figure 6. Functional Circuit Diagram of FB1650

This flexible design approach eliminates the need for double-sided surface mounting, along with all of the associated manufacturing costs, and still meets the IEEE 896.2-1991 25-mm maximum-stub-length requirement (see Figure 7).



NOTE: There is no double-sided SMT requirement.

Figure 7. Uncached 64-Bit Futurebus Layout With Texas Instruments Chipset and FB16xx Transceivers

In addition, the 18-channel architecture lends itself naturally to reduced pin-to-pin signal skew. Advanced BiCMOS circuit design techniques have improved propagation-delay performance over the previous generation of BiCMOS transceivers. Table 3 shows a transceiver description for the same 64-bit uncached Futurebus example considered previously (see Table 2).

Table 3. Transceiver Descriptions for 64-Bit Uncached Futurebus Board Using FB16xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD
FB16xx	18-Bit TTL/BTL UBT With Split TTL I/O	6
FB2032†	Arbitration Contest Transceiver	1
	Total Part Count	7

† Optional for distributed arbitration only

This is nearly a 50% reduction in component count and approximately 15% in cost savings on the transceivers alone. Significant savings (tens of dollars per board) in manufacturing costs also are realized by moving to single-sided SMT manufacturing. Other members of the FB16xx family include system clock-distribution features that lend themselves to more specific end-system applications such as ATM hubs and routers (see Table 4).

Table 4. Transceiver Descriptions for Other Members of the FB16xx Series

DEVICE	DESCRIPTION
FB1650	18-Bit TTL/BTL UBT With Split TTL I/O
FB1651	17-Channel UBT With Separate Buffered and Delayed Clock Bit
FB1653	17-Channel UBT With Separate Buffered Clock Bit (variable delay lines)

Summary

The high-speed data-communication requirements of today's fastest board-level computers and telecommunications and network switching equipments can be met with BTL- and Futurebus-compatible transceivers and switching levels. Stub-length constraints and ever-increasing data-path widths have made it difficult to control signal integrity and manufacturing and procurement costs in these high-performance systems. The next generation of 18-channel BTL/Futurebus universal bus transceivers meets this market need by facilitating low-cost single-sided surface-mount manufacturing, and single-device-type procurement, characterization, qualification, and specification.

Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices

SCBA006A
December 1996

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Contents

List of Illustrations

Introduction

The data in this application report demonstrates the skew between the outputs of a sample of Texas Instruments Advanced BiCMOS (ABT) devices. This report explains which output skew is being examined, where the data comes from, and how the data is analyzed. Some of the errors that may be present in the data are discussed.

Skews

Skew is a term that defines the difference in time between two signal edges. Several different types of skew being used are defined in JEDEC 99 clause 2.3.5.

Output Skew [$t_{sk(o)}$] – The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminating at different outputs.

Input Skew [$t_{sk(i)}$] – The difference between two propagation delay times that originate at different inputs and terminate at a single output.

Pulse Skew [$t_{sk(p)}$] – The difference between the propagation delay times t_{PLH} and t_{PHL} when a single switching input causes one or more outputs to switch.

Process Skew [$t_{sk(pr)}$] – The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions.

Limit Skew [$t_{sk(l)}$] – The difference between: 1) The greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) The lesser of the minimum specified values of t_{PLH} and t_{PHL}.

The skew discussed here is the skew of propagation delays across the outputs of a device. More specifically, it is the difference between the largest value obtained for a propagation delay and the smallest value across all of the outputs. For example, if output 3 has the largest propagation delay t_{PLH} and output 14 has the smallest, the output skew for this device would be the difference between the propagation delays for output 3 and output 14 (see Figure 1).

The majority of the curves presented in this paper consist of data taken on devices that have one output switching at a time. This produces a skew that should not be confused with the defined data-sheet skew $t_{sk(o)}$. The data-sheet value for $t_{sk(o)}$ is found by switching all of the outputs simultaneously. Two of the devices examined in this paper ('ABT16240 and 'ABT16500A) include curves that present $t_{sk(o)}$ data.

Source of Data

The data used to produce the curves presented in this paper was extracted from the characterization data bases used to prepare the data sheets for the devices presented. The sample size of the data base is approximately 30 devices for each characterization lot (wafer) used.

The data was sorted so that the maximum skew for each device at a particular V_{CC} and temperature combination could be determined. Next, the maximum skew values were averaged to produce a data point for each transition. Further statistical analysis of this data was performed to calculate a standard deviation of the maximum skew across the devices. This value was then used to produce a three-standard-deviation data point for each V_{CC} and temperature combination. The data is presented as a family of curves across V_{CC}, with each member of the family being an output skew versus temperature curve. The curves for each device are broken out by output transition (i.e., t_{PLH}, t_{PHL}). Each transition is further separated into a set of curves depicting the average skew across the devices and a set representing the average skew, plus three standard deviations.

For those devices (’ABT16952 and ’ABT16500A) that have registers, the data path chosen for each device was the path that put the device in a transparent mode. Also, for the bidirectional devices (’ABT16245, ’ABT16952, and ’ABT16500A), the A-to-B direction was used.

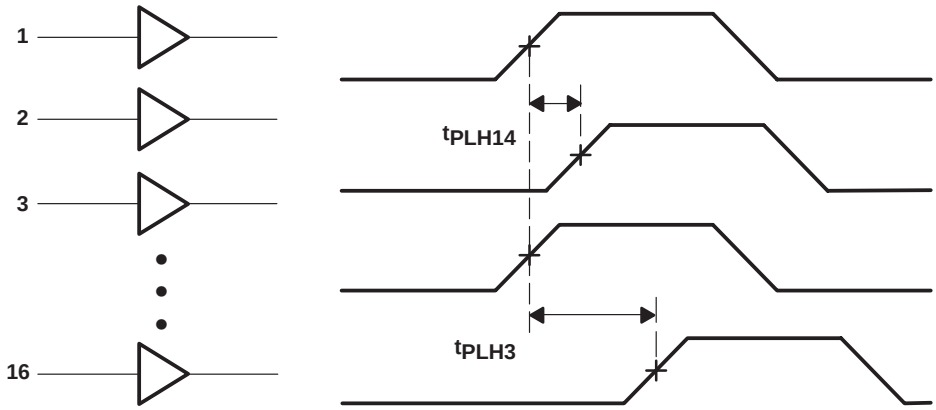


Figure 1. Skew = $|t_{PLH14} - t_{PLH3}|$

Sources of Error in Data

The data in this report was taken on an IMPACT tester, which is automatic test equipment used to characterize integrated circuits. The tester is offset using a golden unit that has had data taken on a laboratory bench setup. The offsetting process is the main source of error in the data.

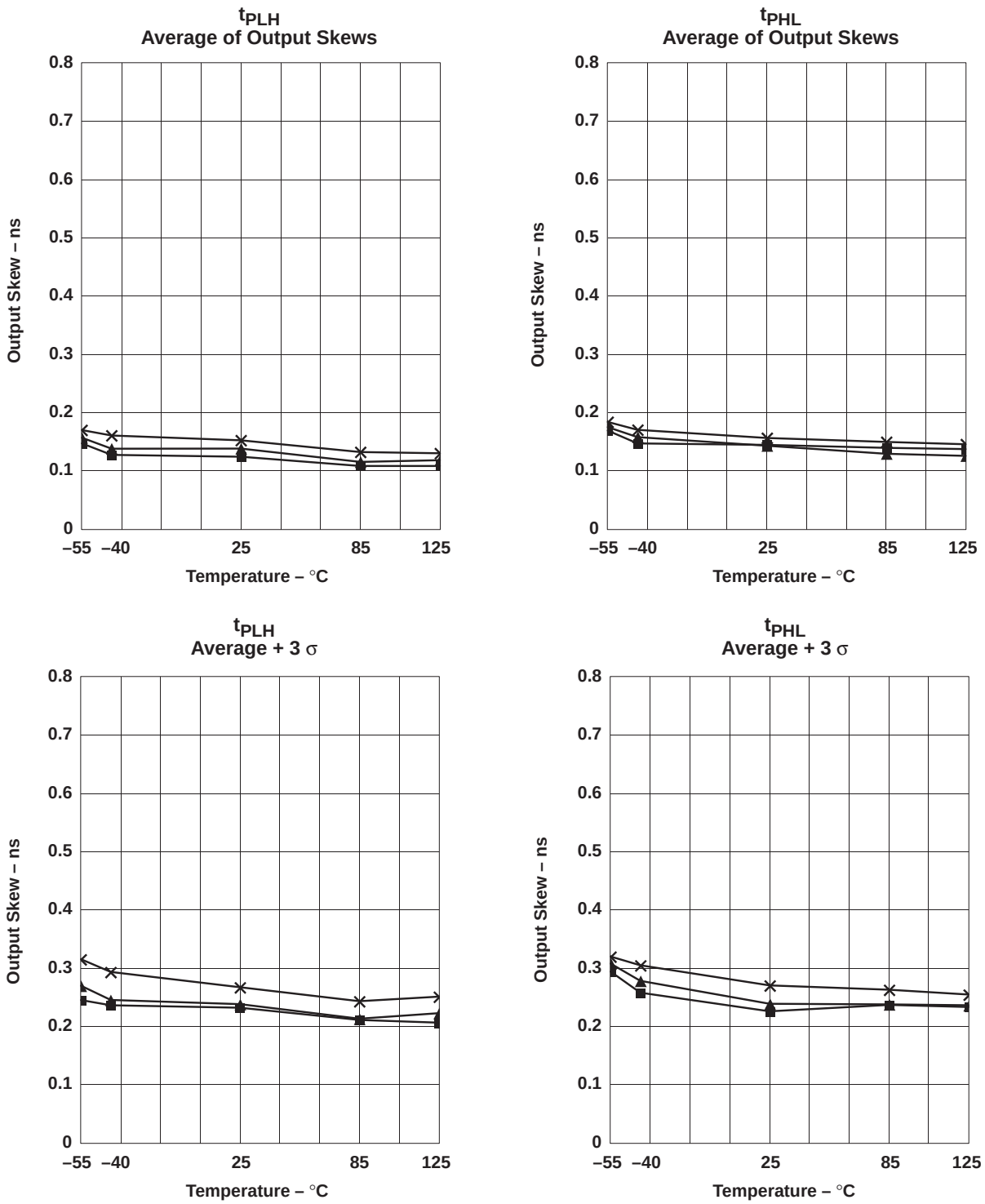
Briefly, the tester is offset in the following manner. The golden unit has its propagation delay measurements taken at 25°C and 85°C using a pulse generator as the source and an oscilloscope as the measurement device. The golden unit is then placed on the IMPACT and the data is again taken. The difference between the two values is the offset. The 25°C offsets are used for the data taken at –55°C, –40°C, and 25°C, while the 85°C offsets are used at 85°C and 125°C.

Great care is taken during this process to ensure that the induced error is kept to a minimum. For example, the boards are checked before use to ensure the output loads are correct, the oscilloscope is calibrated each day, and the input signals are closely monitored to ensure that the intended signal is delivered to the golden unit.

This reduction in error is quite important in this application because the average skews for the devices are about 200 ps. A 20-ps error in offsets translates into an approximate error of 10% in the output skew data. However, it can be seen in the curves presented here that the error has been kept to a minimum and that the curves are fairly well behaved.

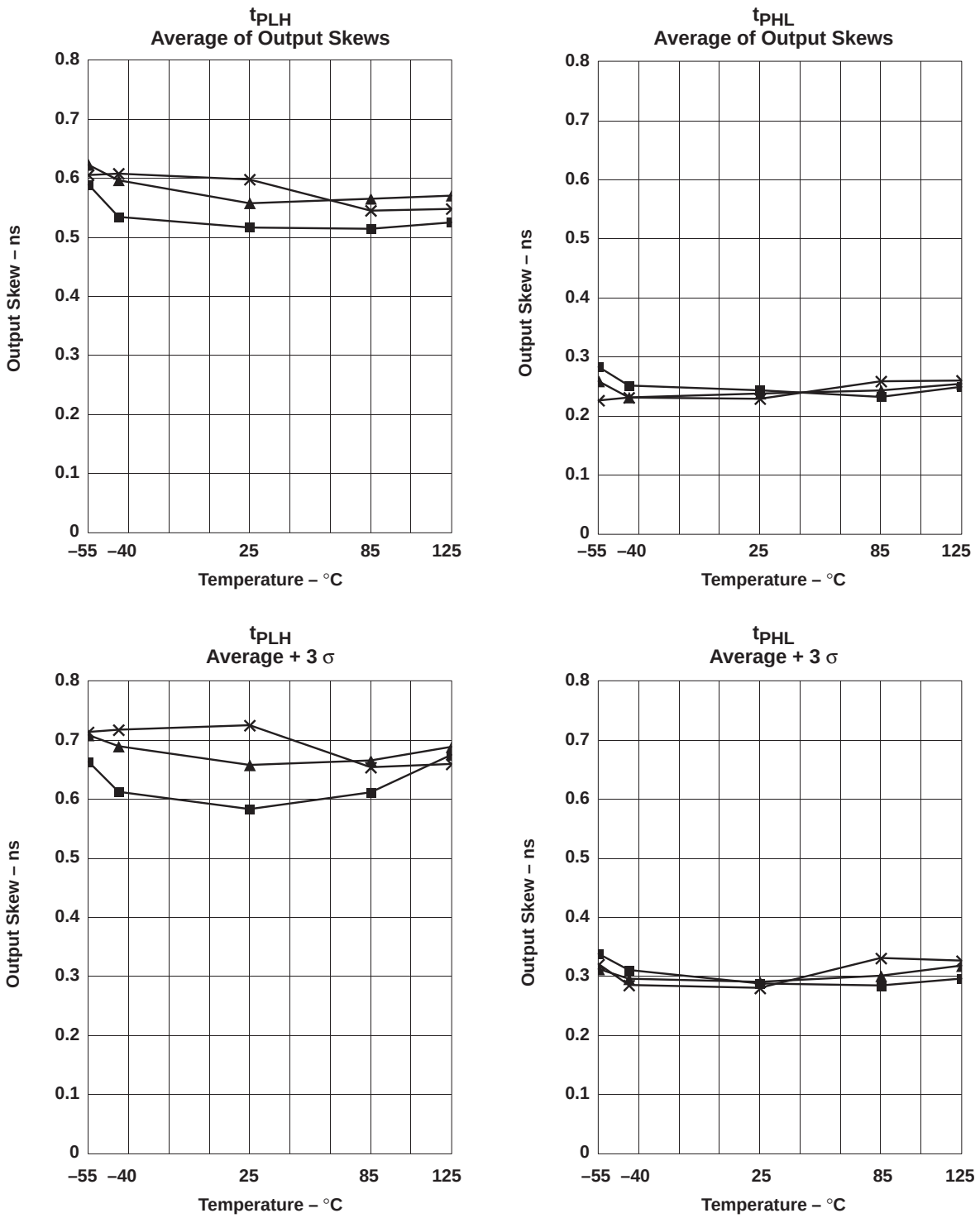
Summary

The family of curves presented in Figures 2 through 9 demonstrates that the Texas Instruments Advanced BiCMOS family of devices can be expected to produce an average skew between outputs that remain below 400 ps for devices with single switching outputs. Also, when a device’s outputs switch simultaneously, the average skew across the outputs can be expected to remain below 700 ps.



X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 2. ’ABT16240 – Single Switching



X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 3. ’ABT16240 – Simultaneous Switching

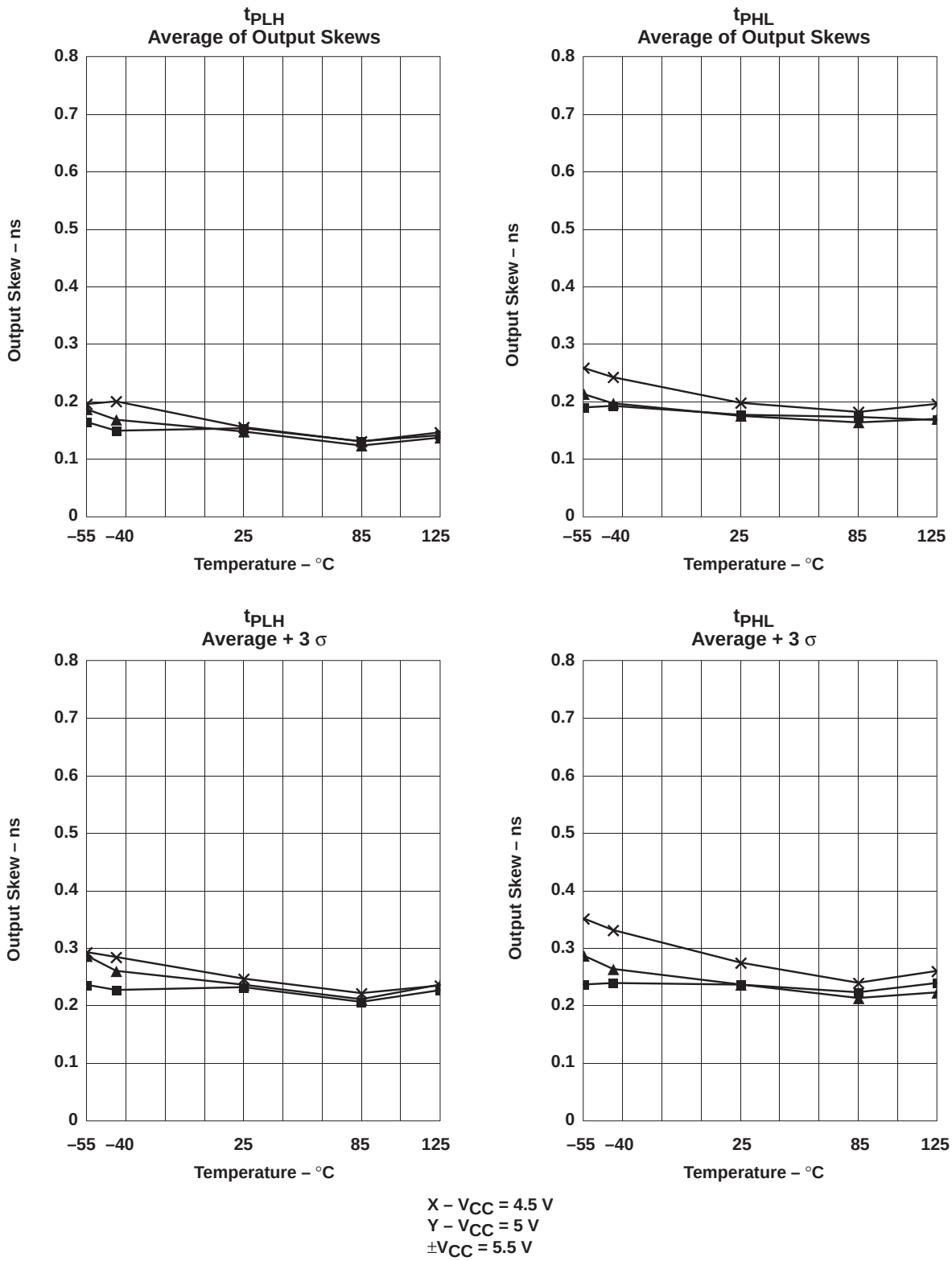
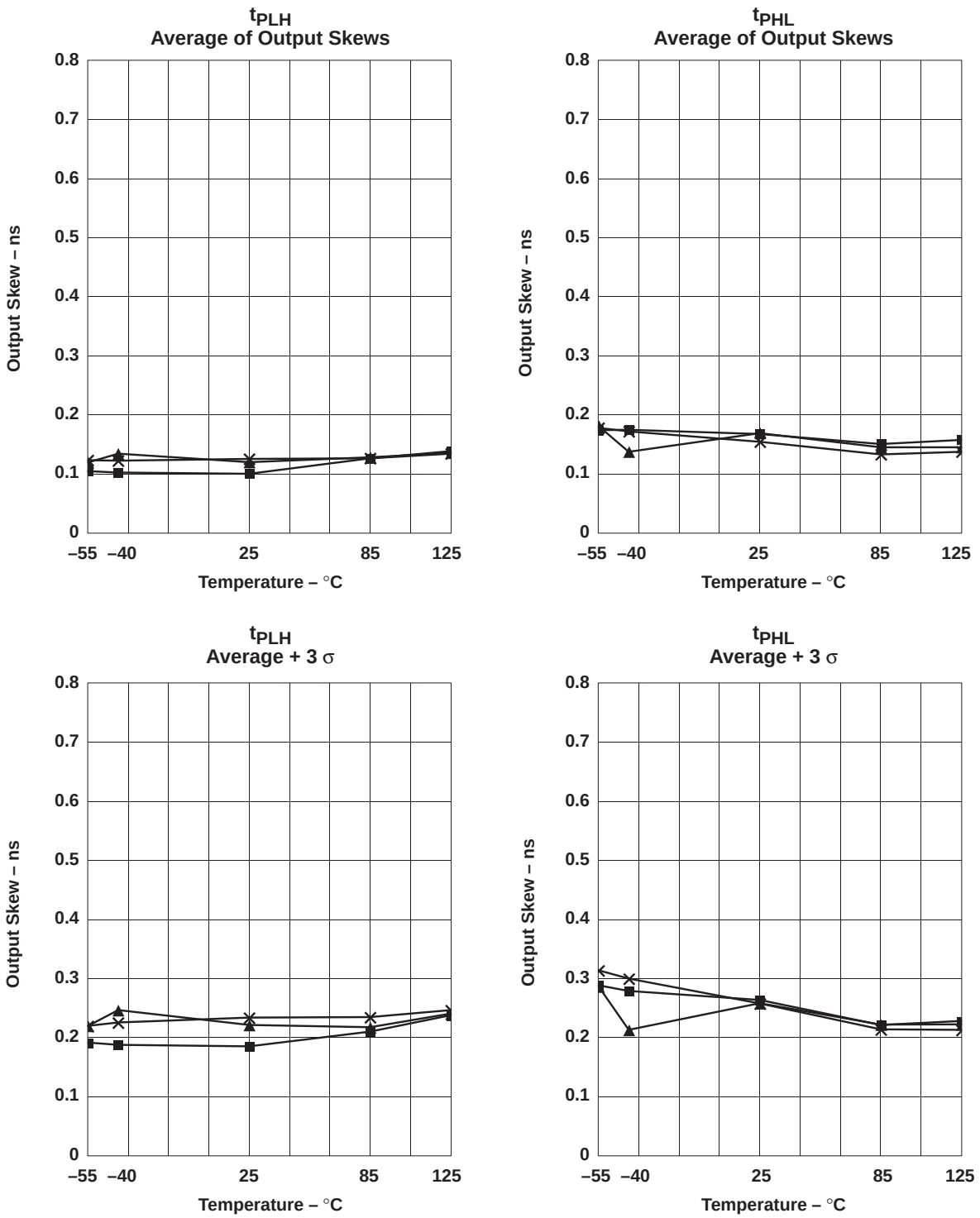
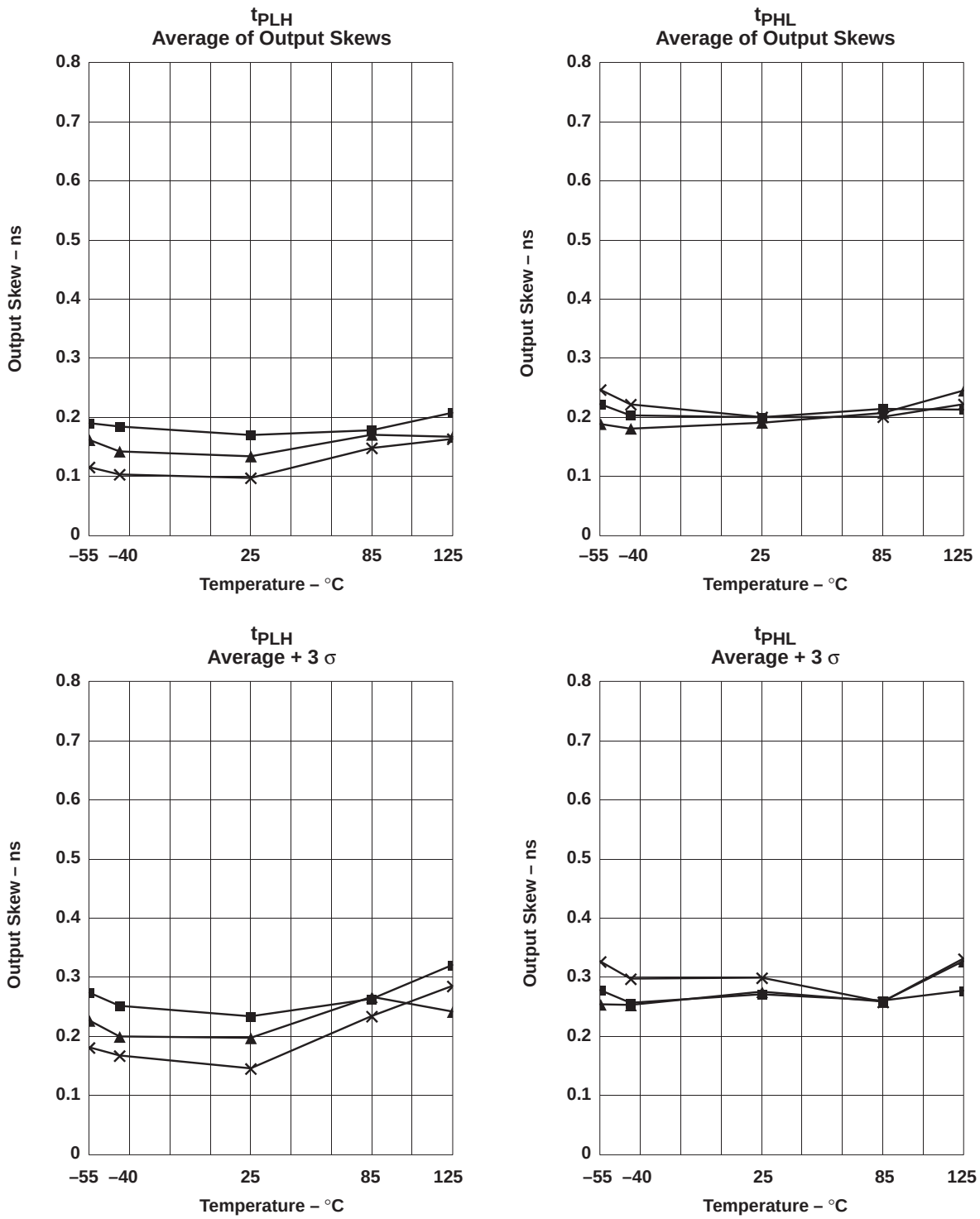


Figure 4. ’ABT16245 – Single Switching



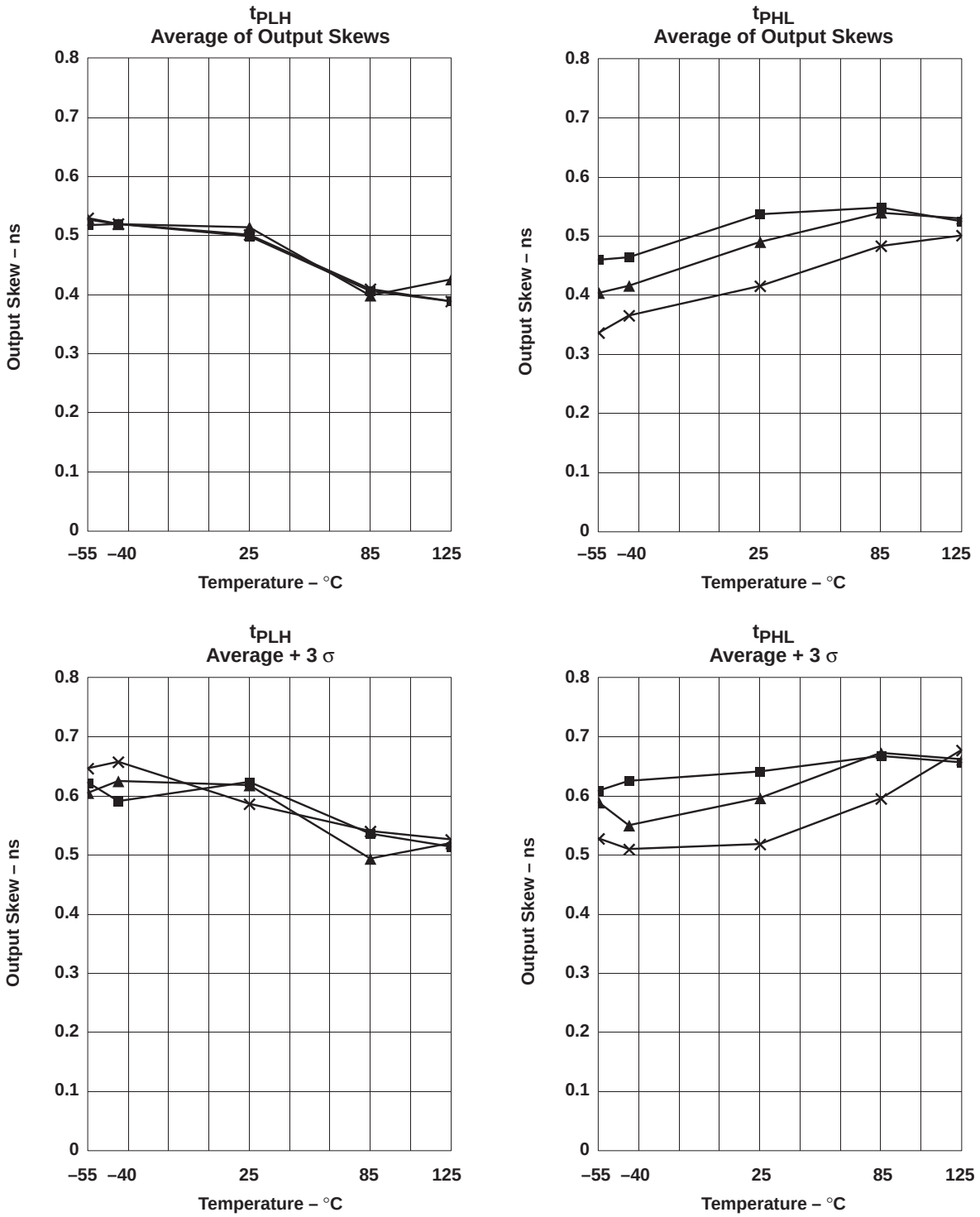
X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 5. ’ABT16952 – Single Switching



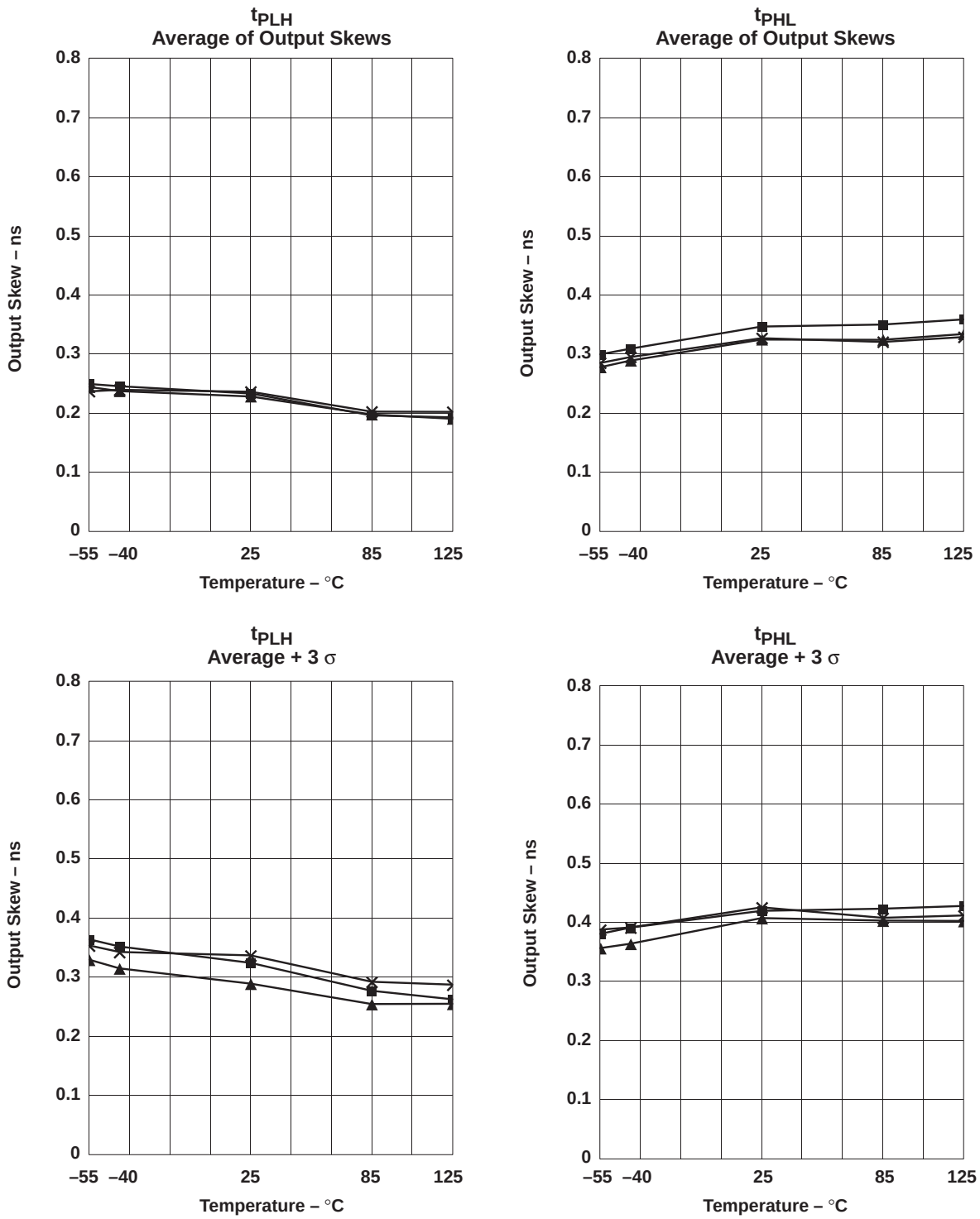
X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 6. ’ABT16500A – Single Switching



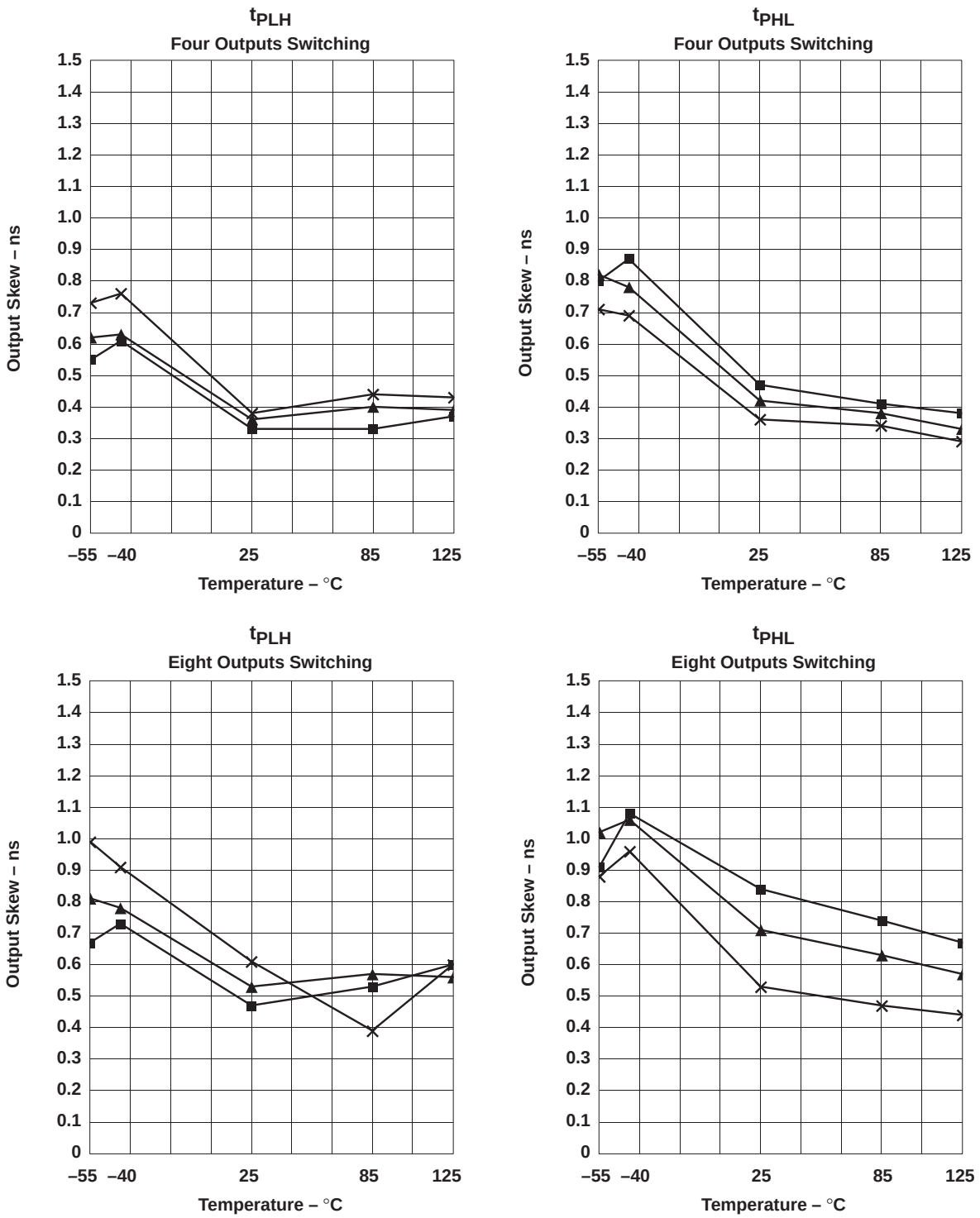
X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 7. ’ABT16500A – Simultaneous Switching



X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 8. ’ABT244 – Single Switching



X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 9. ’ABT244 – Multiple-Output Switching

Application Report
SZZA016B - June 2001

Basic Design Considerations for Backplanes

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Ernest Cox, Steve Blozis, and Jose M. Soltero

Standard Linear & Logic

ABSTRACT

This application report describes design issues relevant to the parallel backplanes typically used in the wireless, datacom, telecom, and networking markets. Designing a high-performance backplane is extremely complex, because issues such as distributed capacitance, stub lengths, noise margin, rise time (slew rate), flight time, and propagation delay must be defined and optimized to achieve good signal integrity along the transmission line.

This application report uses a GTLP backplane driver to study the effects of these factors in an actual backplane application. Guidelines that enable the design engineer to successfully design a high-performance backplane with GTLP or other single-ended open-drain devices, such as BTL, are provided.

This application report is a revision of the original *Basic Design Considerations for Backplanes*, literature number SZZA016, published June 1999. The theory text was rewritten to make it clearer, and the theory-to-practice section was added, based on work done with the GTLP evaluation module (EVM).

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Introduction

Since the beginning, most equipment makers have used parallel-backplane architectures to deliver large amounts of data across one shared bus. The parallel backplane provides a physical and electrical interconnect between various modules in a system. Each module in the backplane communicates with other modules through the backplane bus. Typically, this bus is driven by a backplane transceiver, primarily as the point-of-contact between backplane cards. The basic backplane is a parallel data-transfer topology used in a multipoint transfer scheme. For example, the TDM bus in a wireless base-station unit operates in a multipoint fashion, with high-speed data communicating between different regions across the backplane.

With the expansion of the internet and wireless/telecom infrastructures, new end-equipment markets have emerged that deliver faster data, integrated voice and data, or a little of both, and need higher performance backplanes. The constant pressure to increase bandwidth requires design engineers to choose between higher performance, more expensive backplane-optimized transceivers to maximize the frequency, increase the bit width using older technology, or a combination of these goals. This application report addresses some of the basic design issues encountered in higher performance backplanes. The effects of distributed capacitance on termination resistance and flight time are examined and the various effects of stubs and connectors are discussed.

Backplane Design Topology – Point-to-Point vs Multipoint

Figure 1 is an example of a simple point-to-point data transfer. A driving device at point A drives a 51-Ω transmission line. A termination resistor (R_{TT}) that matches the line impedance is placed at point B, along with a receiving device. All calculated values for the termination resistance are ideal. The designer must use actual values that best match, or are lower than, calculated values. In this example, the transmitter is an open-drain device that pulls the line low when turned on, but requires the termination resistor to pull the line high when turned off.

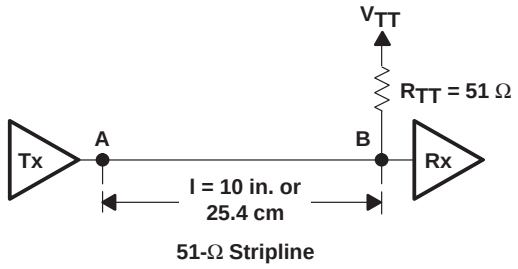


Figure 1. Point-to-Point Application

When the output transistor drives the line low, a constant dc current flows from the termination voltage, V_{TT}, to ground. Too small a termination resistance can damage the driver due to excessive currents. Assuming V_{TT} = 1.5 V, V_{OL} = 0.4 V, and R_{TT} = 51 Ω, the constant dc current is about 21.6 mA ($I_{OL(max)} = (V_{TT} – V_{OL})/R_{TT}$). However, this current increases linearly with V_{TT} and should not exceed the recommended current rating of the output driver.

In this, and the following multipoint example, the transmission line is assumed to be a stripline trace that is 10 in. (25.4 cm) long with a natural impedance (Z_0) of 51 Ω, which corresponds to a characteristic capacitance (C_0) of 3.5 pF/in. (138 pF/m).

The propagation delay (t_{pd}) is the time delay through the transmission line per unit length and is a function of the natural impedance and characteristic capacitance.

Use equation 1 to calculate propagation delay (t_{pd}).

$$t_{pd} = Z_o \times C_o \tag{1}$$

In this example, t_{pd} = 51 Ω × 3.5 pF/in. (138 pF/m) yields 178.5 ps/in. (7038 ps/m or 7.03 ns/m).

The total flight time (t_{flight}) is the time required for the signal to propagate down the transmission line from driver to receiver (time from A to B) and is a function of t_{pd} and length of the line.

Use equation 2 to calculate t_{flight}.

$$\begin{aligned} t_{flight} = t_{pd} \times \text{length of line} &= 178.5\ \text{ps/in.} \times 10\ \text{in.} \\ &\text{or } 7.03\ \text{ns/m} \times 0.254\ \text{m} \\ &= 1.784\ \text{ns} \end{aligned} \tag{2}$$

In Figure 2, the point-to-point configuration has been changed to a multipoint layout. Eleven transceivers are placed on the 10-in. transmission line, with 1-in. spacing (d) between each transceiver. One transceiver is configured as a transmitter (Tx); the other ten are configured as receivers (Rx). In a multipoint system, any position can assume the role of transmitter, with the remaining positions acting as receivers, as shown by the transceiver symbol. The 51-Ω stripline transmission line must be terminated at both ends because the transceiver at either end could be the driver. The optimum termination resistance (R_{TT}) for the multipoint system is less than the natural transmission-line impedance of 51 Ω, due to the effects of distributed capacitance. Procedures to calculate the optimum R_{TT} and the effects of mismatched R_{TT} on signal integrity are the main focus of this application report.

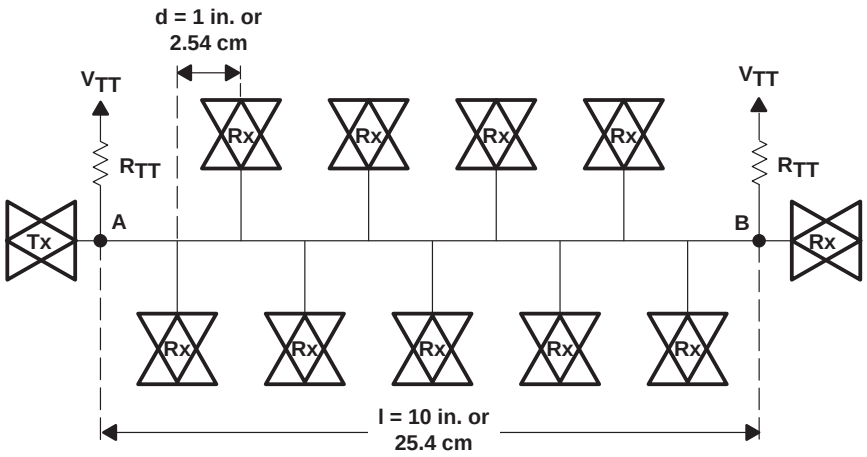


Figure 2. Multipoint Application

Distributed Capacitance

Figure 3 is a simplified version of Figure 2, where an equivalent capacitive load (12-pF capacitor) replaces the receivers. It is assumed that the spacing between card slots is within the rise and fall time of the driver signal, and that all slots are populated with cards.

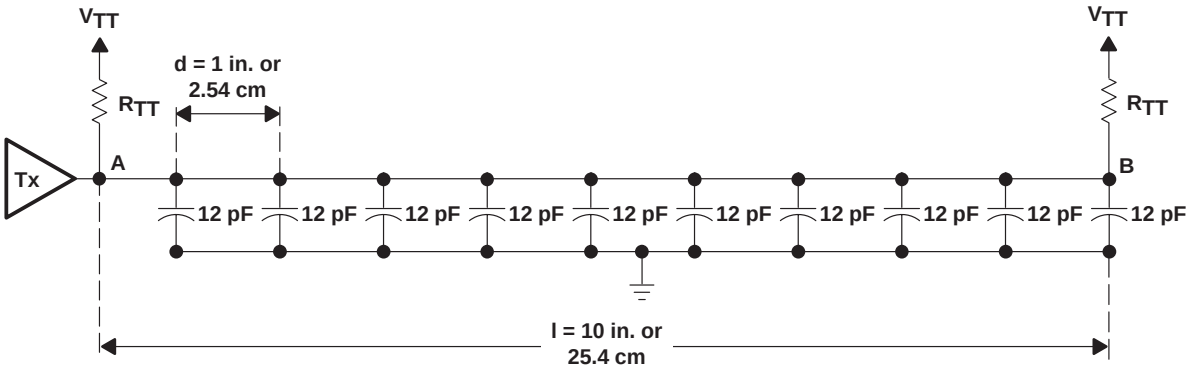


Figure 3. Equivalent Multipoint Application

Total capacitance (C_t) is calculated by summing all the capacitive components associated with the transceiver and the connection to the backplane. Figure 4 shows a typical connection scheme between the backplane stripline and the driving/receiving device on the daughter card. Point C is the connection to the backplane stripline, while point D is the connection to a transceiver integrated circuit. Total capacitance (C_t) at point C is the sum of each of the elements in the connection chain. Total capacitance then can be distributed uniformly across the transmission line at an equivalent rate of capacitance per inch (C_d).

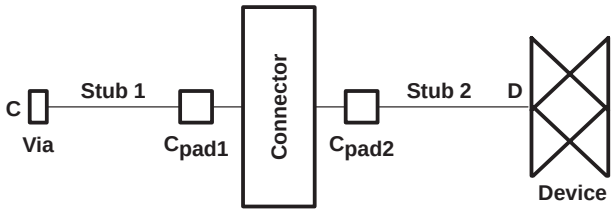


Figure 4. Typical Connection Scheme to Backplane

The stub lines (stub 1 and stub 2) are 51-Ω microstrip construction with a characteristic capacitance of 2.6 pF/in. (102 pF/m). The connection via connects stub 1 to the backplane trace and has an approximate capacitance of 0.5 pF. Stub 1 is 1/16 in. in length and is connected on the other end to the surface-mount pad for the connector (C_{pad1}), which has a capacitance of approximately 0.5 pF.

The HSPICE model for the connector used in this example has a connector capacitance (C_{con}) of 0.74 pF. C_{pad2} has the same value as C_{pad1} and is the surface-mount pad for the connector on the daughter-card side that connects the connector to the daughter-card stub (stub 2). Stub 2 is 1 in. long and is attached to the other end of the transceiver input/output pin, which has a typical capacitance (C_{io}) of 7 pF.

Two different printed circuit board (PCB) transmission lines are shown in Figure 5. Basically, microstrip resides on the top of the PCB, whereas the stripline is imbedded within the PCB layers. A microstrip is faster due to the less inherent capacitance, but a stripline exhibits better signal integrity because the reference planes shield the conductor from damaging EMI fields. Other performance differences are discussed later in this application report.

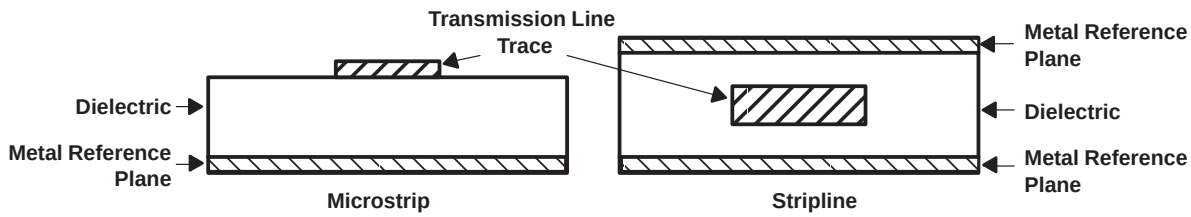


Figure 5. Typical PCB Transmission Lines

The capacitance of the via, pads, and stubs can be calculated based on the dimensions and type of traces. www.ultracad.com provides an excellent capacitance calculator with background information. The C_{io} of the transceiver and the connector capacitance can be obtained from the manufacturer's specification sheet.

The capacitance in this chain is summed as:

$$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io} \qquad (3)$$
$$C_t = 12\ \text{pF}$$

Where:

C_{via} = capacitance of via = 0.5 pF
C_{stub1} = capacitance of stub 1 = 0.0625 × 2.6 = 0.16 pF
C_{cpad1} = capacitance of C_{pad1} = C_{pad2} = 0.5 pF
C_{cpad2} = capacitance of C_{pad2} = C_{pad2} = 0.5 pF
C_{stub2} = capacitance of stub 2 = 1 × 2.6 = 2.6 pF
C_{con} = capacitance of connector = 0.74 pF
C_{io} = input/output capacitance of device = 7 pF

The total capacitance (C_t) of 12 pF is placed at point C on the backplane for every transceiver. More than half of C_t is the transceiver typical input/output pin capacitance. This is why backplane designers require low-capacitive ICs to optimize performance in high-frequency backplanes.

With all the slots filled, the 10-in. transmission line has 11 12-pF capacitors distributed at 1-in. intervals. The distributed capacitance (C_d) affects both the propagation delay and the characteristic impedance of the stripline transmission line, which results in a new effective impedance, $Z_{o(eff)}$, and a new effective propagation delay, $t_{pd(eff)}$. The distributed capacitance equals the total capacitance divided by the separation, or $C_d = C_t/d$. In our example, C_d = 12 pF/1 in. or 12 pF/in. (472 pF/m). The new effective impedance, $Z_{o(eff)}$, and effective propagation delay, $t_{pd(eff)}$, can be calculated using equations 4 and 5.

$$Z_{o(eff)} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \qquad (4)$$

$$t_{pd(eff)} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \qquad (5)$$

Figures 6 and 7 show the effects of the term $\sqrt{1 + (C_d/C_o)}$ on Z_o and t_{pd} by plotting the normalized effective impedance and t_{pd} in terms of distributed capacitance divided by the characteristic capacitance, C_d/C_o.

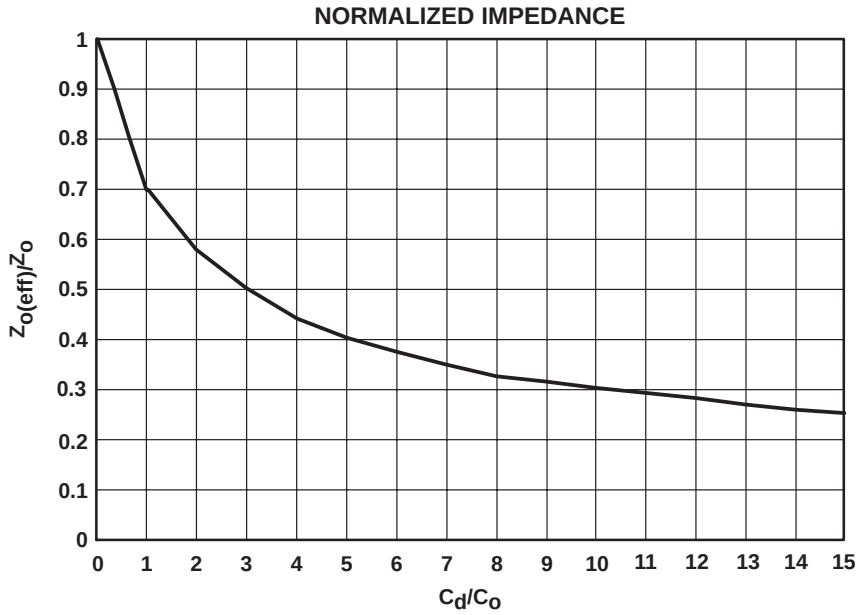


Figure 6. Effective Impedance vs C_d/C_o

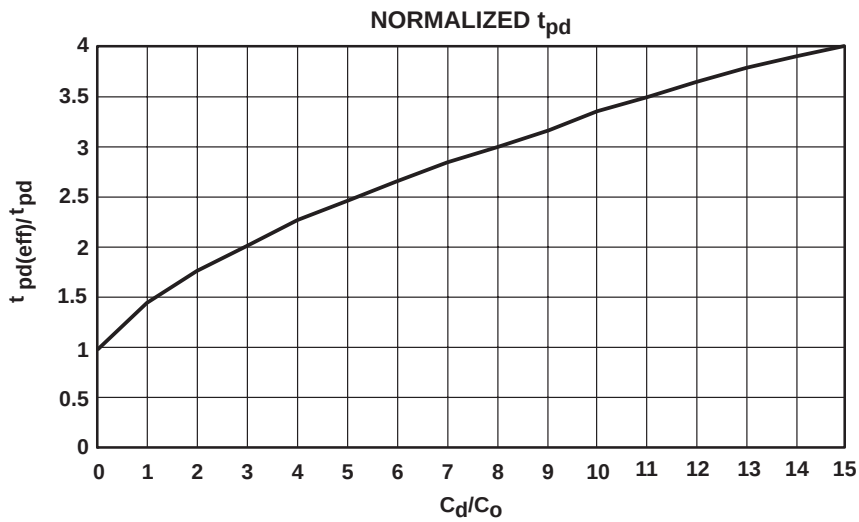


Figure 7. Effective t_{pd} vs C_d/C_o

An easy-to-follow calculation using Figures 6 and 7 is based on a 50-Ω line (Z_o) with a t_{pd} of 180 ps/in. (7.09 ns/m) used in a system where the C_d/C_o ratio is 3. From Figure 6, the C_d/C_o of 3 yields an effective impedance of 0.5 times the characteristic impedance, or $Z_{o(eff)} = 0.5 \times 50 = 25\ \Omega$. Figure 7 shows that for the same C_d/C_o ratio of 3, the transmission-line effective propagation delay has doubled and $t_{pd(eff)} = 2 \times 180 = 360$ ps/in. (14.18 ns/m).

In a previous example (capacitors in Figure 3), C_d = 12 pF/in. (472 pF/m) and C_o = 3.5 pF/in. (138 pF/m) make the C_d/C_o ratio = 3.43 and the term $\sqrt{1 + (C_d/C_o)}$ = 2.1. Figures 6 and 7 reflect the changes in the effective values of the transmission line to be 0.48 times the normal impedance and 2.1 times the normal propagation delay.

Another way to calculate the new effective impedance and propagation delay is to use equations 4 and 5 instead of Figures 6 and 7.

The value of the effective impedance is:

$$Z_{o(eff)} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} = \frac{51}{2.1} = 24.2\ \Omega \tag{6}$$

The value of the effective t_{pd} is:

$$t_{pd(eff)} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} = 178.5(2.1) = 375.6\ \text{ps/in.} \tag{7}$$

Using equation 2, the new flight time between points A and B in Figure 3 is:

$$t_{flight} = t_{pd} \times \text{length of line} = 375.6\ \text{ps/in.} \times 10\ \text{in.} = 3.76\ \text{ns} \tag{8}$$

Note that the propagation delay was 1.785 ns in the point-to-point example.

As discussed previously, the optimum termination resistance is equal to the effective impedance, $Z_{o(eff)}$, of the system so, in this case, the optimum termination resistance, R_{TT}, is the same as $Z_{o(eff)}$ which is 24.2 Ω. The optimum termination resistance ensures incident-wave switching without undershoot or overshoot.

Figure 8 shows the effect on signal integrity in different-terminated conditions. R_{TT} should be less than or equal to $Z_{o(eff)}$ for incident-wave switching, optimum signal integrity, and the best upper noise margin.

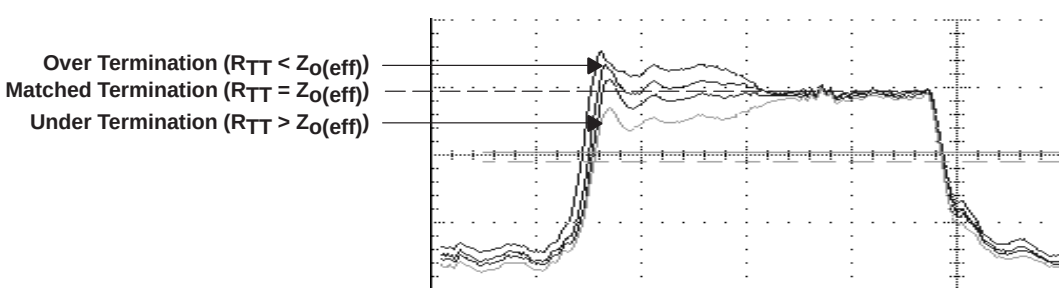


Figure 8. Termination Resistance vs $Z_{o(eff)}$

Equation 9 provides all parameters needed to calculate an optimum termination value:

$$R_{TT} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} = \frac{Z_o}{\sqrt{1 + \frac{C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io}}{dC_o}}} \tag{9}$$

Optimum Termination Simulation

Figure 9 is the result of HSPICE simulation of the circuit in Figure 3, with 51 Ω used for the pullup terminations (R_{TT}) to 1.5 V. Figure 3 did not show the L-C-R values inherent in transmission lines, but they are included in the HSPICE simulations. The transmitter (driver) is a high-drive GTLP device operating at 50-MHz clock frequency. Because the device is operating in the latched mode, the data signal shown is only one-half clock frequency, or 25 MHz.

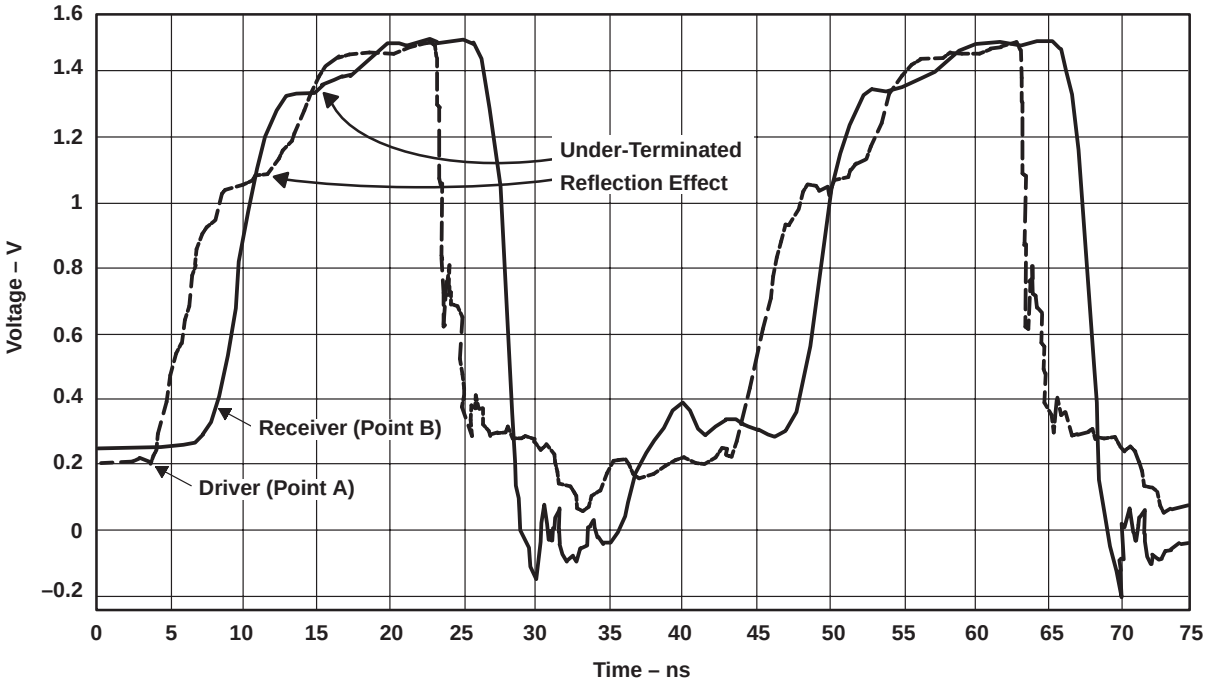


Figure 9. Mismatched Line Termination

One signal in Figure 9 is the driver output at point A of the fully loaded transmission line, and the other signal is the receiver input at point B of the fully loaded transmission line that is farthest from the driver. The effects of the reflections due to termination mismatch can be seen clearly.

Figure 10 shows the same waveforms when the termination resistors are changed to the calculated value of 24.2 Ω. The improvement in signal integrity is due to matching the termination resistors to the loaded impedance of the stripline transmission line. The delay between the two signals is measured at the 1-V threshold level for the GTLP device.

The HSPICE simulation produces the same flight time from point A to point B, as calculated previously.

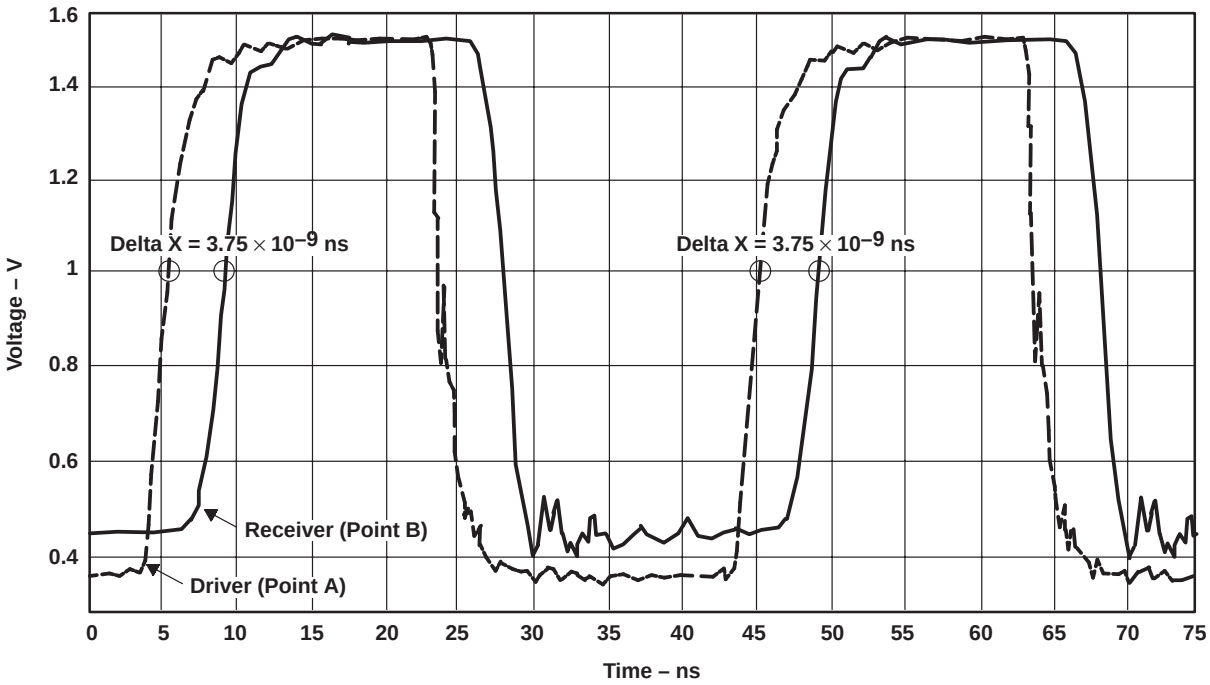


Figure 10. Matched Line Termination

Stripline vs Microstrip Tradeoffs

Table 1 demonstrates the effects of distributed capacitance on various microstrip and stripline transmission lines used in backplane designs. Er is the dielectric constant and depends on the material used in the multilayer-backplane printed circuit board. For Table 1 discussion purposes, the distributed capacitance is fixed at 12 pF/in. Results in the table differ if the distributed capacitance value is changed. The highlighted stripline Z_O 50-Ω line is closest to the multipoint distributed-capacitance example discussed previously.

Table 1. Comparison of Backplane Lines (Loaded Backplane, C_d = 12 pF/in.)

TYPE LINE Er = 4.5	C_O (pF/in.)	Z_O (Ω)	$Z_{O(eff)}$ (Ω)	t_{pd} (ps/in.)	$t_{pd(eff)}$ (ps/in.)
Microstrip	1	140	38.8	140	505
Microstrip	2	70	26.5	140	370
Microstrip	2.8	50	21.7	140	322
Microstrip	4.67	30	15.9	140	265
Stripline	1.29	140	43.6	180	578
Stripline	2.58	70	29.5	180	428
Stripline	3.6	50	24	180	375
Stripline	6	30	17.3	180	312

Using the same impedance (Z_o) in a loaded backplane, microstrip lines (on the surface of the backplane board) have a faster effective t_{pd} than striplines (embedded in the backplane board), but the microstrips have a lower effective impedance than the stripline. This lower effective impedance requires a lower termination resistance to properly terminate the backplane. The designer must balance the required signal propagation time with the driver capabilities when deciding which type of line to use and what characteristic impedance to choose. In general, it is recommended that stripline be used for the backplane transmission line and microstrip be used for the daughter-card stub lines, because stripline has better signal integrity and does not require a lower termination resistance. The microstrip adds less to the total capacitive load for each card, is faster, and is easier to implement on the daughter card.

Backplane DC Effects

Figure 11 is the dc-equivalent circuit of Figure 2 when the driver is turned on and is in the low state. The driver is replaced by its on resistance (R_{device}), and the transmission line is replaced by its dc resistance (R_{line}). The current (I3) is the sum of currents I1 and I2. When the output is low at the driver, V_{OL1} is the product of R_{device} and I3. The voltage (V_{OL2}) is the low level seen at the receiver farthest from the driver and is equal to $V_{TT} - (R_{TT} \times I2)$.

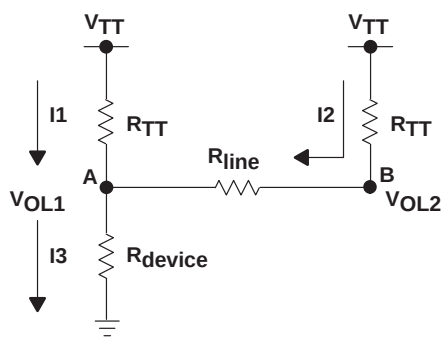


Figure 11. DC Equivalent of Single Backplane Line

In our example, R_{TT} = 24.2 Ω, R_{line} = 2.2 Ω, and V_{TT} = 1.5 V. The basic equation starts with:

$I3 = V_{TT}/[R_{TT}//(R_{TT} + R_{line}) + R_{device}]$

Where:

$R_{TT}//(R_t + R_{line})$ is the parallel resistance of the upper branch.

From this expression, the following equations can be derived:

$$V_{OL1} = \frac{(V_{TT})(R_{device})(2R_{TT} + R_{line})}{\left[(R_{TT})(R_{TT} + R_{line}) + (R_{device})(2R_{TT} + R_{line})\right]} \quad (10)$$

$$V_{OL2} = V_{OL1} + \frac{(R_{line})(V_{TT} - V_{OL1})}{R_{TT} + R_{line}} \quad (11)$$

$$R_{device} = \frac{(R_{TT})(V_{OL1})(R_{TT} + R_{line})}{(V_{TT} - V_{OL1})(2R_{TT} + R_{line})} \quad (12)$$

For the device model in Figure 10, the R_{device} value was estimated to be 4 Ω. Using equation 10, V_{OL1} = 0.361 V and, using equation 11, V_{OL2} = 0.456 V, which matches well with the results observed in Figure 10.

The dc analysis can help provide the designer with best-case low-level voltage (V_{OL1}) and worst-case (V_{OL2}) signal levels expected at the receivers on a backplane when the termination resistance has been determined.

The V_{OL} levels affect the noise margins at all receivers as shown in Figure 10. The signal at point B is at the last receiver at the end of a 10-in.-long transmission line. The low level of this signal is higher than that of point A (less lower noise margin). Smaller values of R_{TT} or longer backplanes (higher values of R_{line}) will reduce point-B noise margin even more. The drive capability (characterized by R_{device}) of the transmitter also will affect the waveforms V_{OL}.

Effect of Changing Stub Length on Backplane Signal Characteristics

The effects of changing stub length are most noticeable in the stub associated with the transceiver that drives the signal and, to a lesser extent, on the stubs at the transceivers that are receiving the signal. These effects are in two categories:

- Flight time – The longer the stub, the longer it takes for a signal to propagate through it, and results in increased flight time from the driver to the backplane line (stub delay).
- Rise time [also known as slew rate (V/ns)] – One of the interesting effects of the stub is the faster rise time observed at the driver circuit as stub Z_o, or stub length, increases.

The inductance of the stub and connector form an L-C-R network between the driver and the load (backplane). Figure 12 shows a simplified equivalent circuit.

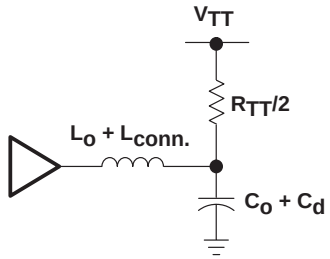


Figure 12. Thevenin Equivalent of Load

The longer the stub length, or the higher the stub Z_o, the larger is the inductance seen by the driver [the sum of the stub line inductance (L_o) and the connector inductance ($L_{conn.}$)] and, thus, the faster the rise time of the driving waveform. The faster rise time causes increased ringback (increased reflections) and worsens the signal integrity of the system. Therefore, it is best to use a low stub Z_o and keep the length as short as possible, preferably less than 1 in.

The following analyses are based on HSPICE simulations of the backplane model (see Figure 2). Figure 13 shows the results of simulation data taken on rise time when only the stub Z_o was changed. The termination resistance used in the calculation was also changed with each new value of stub impedance, because this changes the effective characteristic impedance on the backplane. S1 is the rise time at the driver measured from 20% to 80% steady-state low and high levels. S2 is the rise time measured at the beginning of the backplane. S3 is the measured rise time when the signal leaves the backplane at the last receiver slot. S4 is the measured rise time at the last receiver.

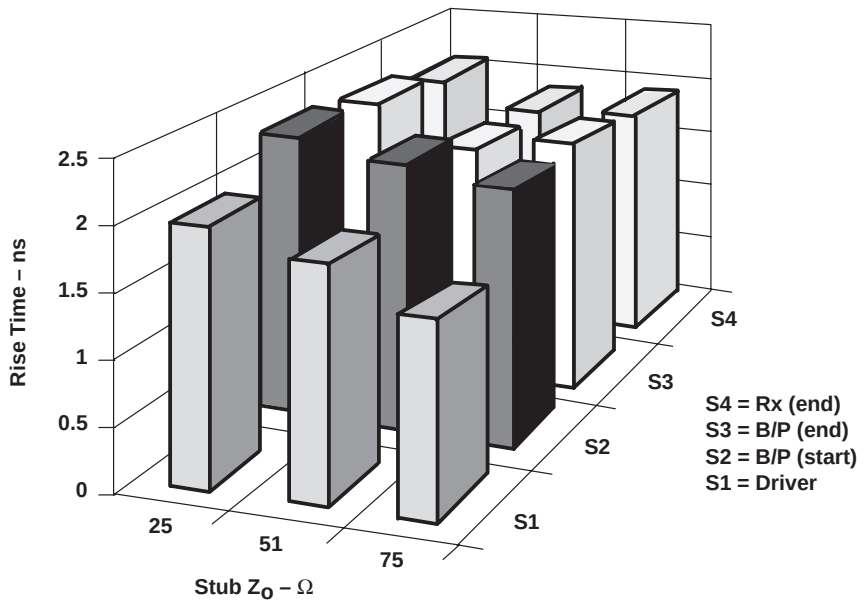


Figure 13. Rise Time vs Stub Z_O at Various Points on the Backplane

The higher-impedance stubs (higher inductance) produce a faster driver rise time (higher slew rate) and, therefore, faster rise times at all points along the backplane. This shows that system slew rate is dependent on both the device slew rate and the stub impedance. If the system rings, a lower stub Z_O can alleviate the problem, because it would slow the rise time to a more manageable value. Figure 14 shows the effects of stub length on stub delay and driver rise time. Stub impedance is fixed at 51 Ω, and only stub lengths and R_{TT} were changed.

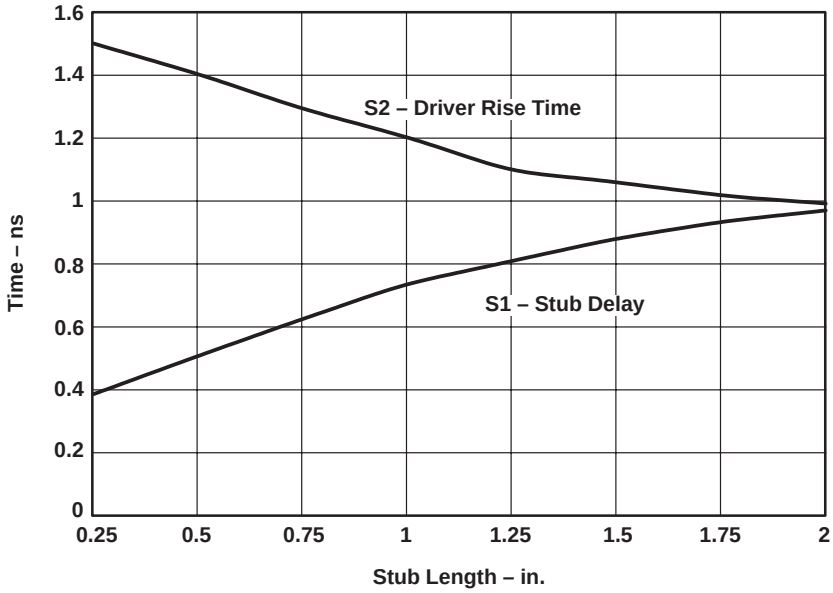


Figure 14. Effects of Stub Length on Stub Delay and Rise Time

The termination was calculated for each stub length, using equation 9. The capacitance of the different stub lengths changed the distributed capacitance on the backplane. Figure 14 shows that as stub length increases, stub delay increases and driver rise time (slew rate) decreases.

Figure 15 shows the effect of stub length on termination resistance, and demonstrates that longer stub lengths result in a lower optimum R_{TT} when everything else is held constant.

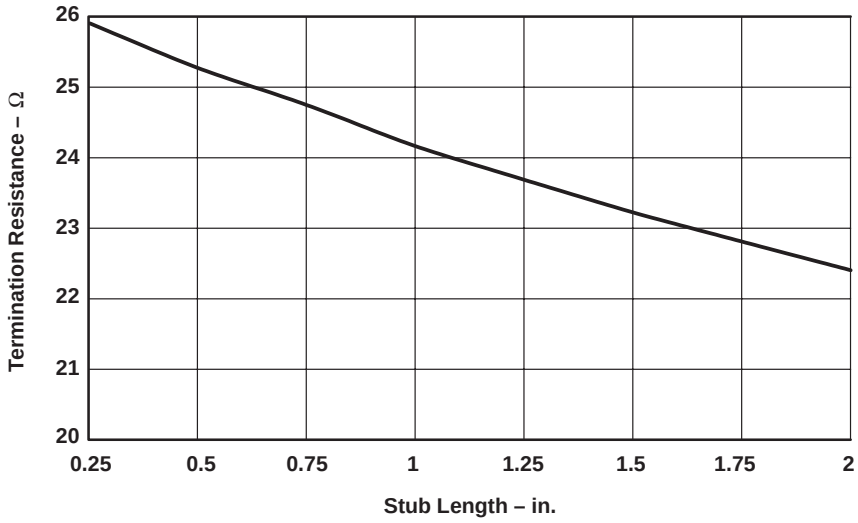


Figure 15. Effect of Stub Length on Termination Resistance at S1

In all three cases, minimum stub lengths are desired because they result in the best stub propagation delay, rise time, and termination resistance. A stub-length design goal is 1 in., or less.

Figure 16 shows the results of simulations of flight time in a backplane. Various stub impedances with fixed stub lengths of 1 in., coupled with a fixed 25-Ω or 50-Ω connector and termination resistors fixed at 24 Ω, or calculated based on stub impedance, were modeled into the system shown in Figure 2. The driver's rise time (20% to 80%) was set to 1.5 ns. The measurements show the delay between the driver and the receiver located at opposite ends of the 10-in. transmission line.

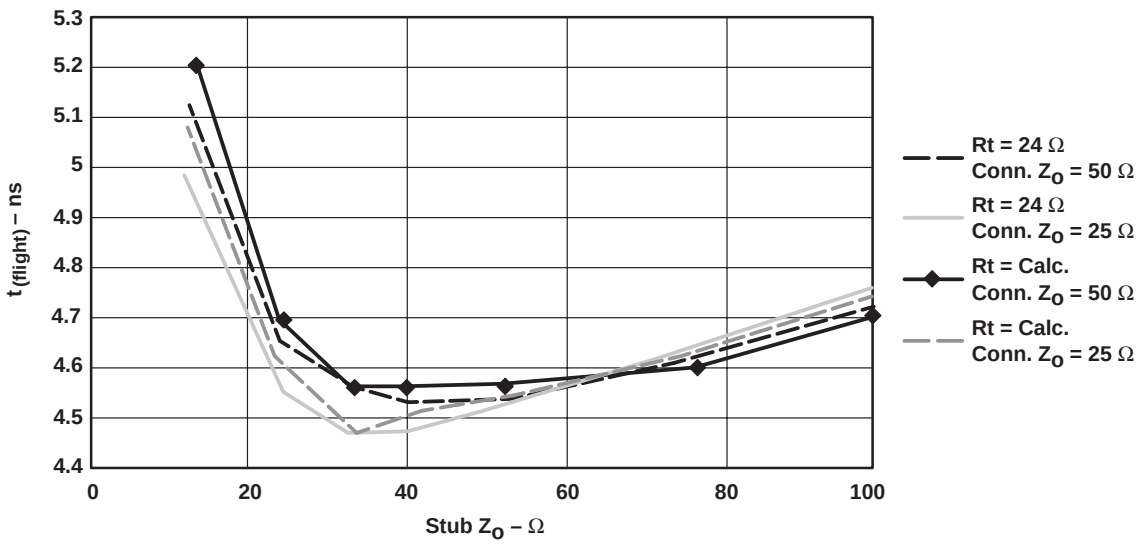


Figure 16. System Flight Time vs Stub Impedance

Figure 16 indicates that a range of stub impedances produces a minimum system flight time. Lowest flight times are observed between 35 Ω and 50 Ω.

Higher-impedance stubs have a larger value of inductance that results in gradually longer stub delays and flight times.

Lower-impedance stubs have larger values of capacitance that result in increased distributed capacitance on the backplane. This increases the effective propagation delay and also increases flight time much more dramatically than the higher-impedance stubs.

A design goal would be to have the stub Z_O between 35 Ω and 65 Ω for optimum performance.

Distributed Capacitance – Theory to Practice

The effect of distributed capacitance was observed in the GTLP evaluation module (EVM). The EVM is a 17.9-in., 48-bit, 20-slot stripline backplane with slot-to-slot spacing (slot pitch) of 0.94 in. and removable terminations. The backplane is divided into six groups, with each group having eight traces. Group 1 is 20 slots long, while group 6 is only 2 slots long. The other groups are 16, 12, 8, and 4 slots long. Group 1, bit 1 was used for this theory-to-practice evaluation. The natural trace impedance (Z_O) was planned to be 55 Ω for all, but two traces in group 1, including the trace used for this experiment, were higher due to missing reference planes between them. Available termination-resistor values are 25 Ω, 33 Ω, 38 Ω, and 50 Ω. Data was taken at 23-MHz, 50-MHz, and 87-MHz clock frequencies. The SN74GTLPH1655 high-drive transceiver was used for this experiment and was operated in the latched mode where data frequency is one-half of clock frequency. The data waveforms are shown. The driver in all cases is in slot 1; the waveforms shown were obtained directly from the backplane connector pin of the receiver slot under test.

Fully Loaded Backplane

Figure 17 clearly shows the effect of the different termination resistors on signal integrity in the fully loaded EVM. All waveforms show incident-wave switching, with upper noise margin gained with lower termination-resistor values. The 50-Ω termination value is unacceptable. The 43.5-MHz and 11.5-MHz data waveforms are included for comparison.

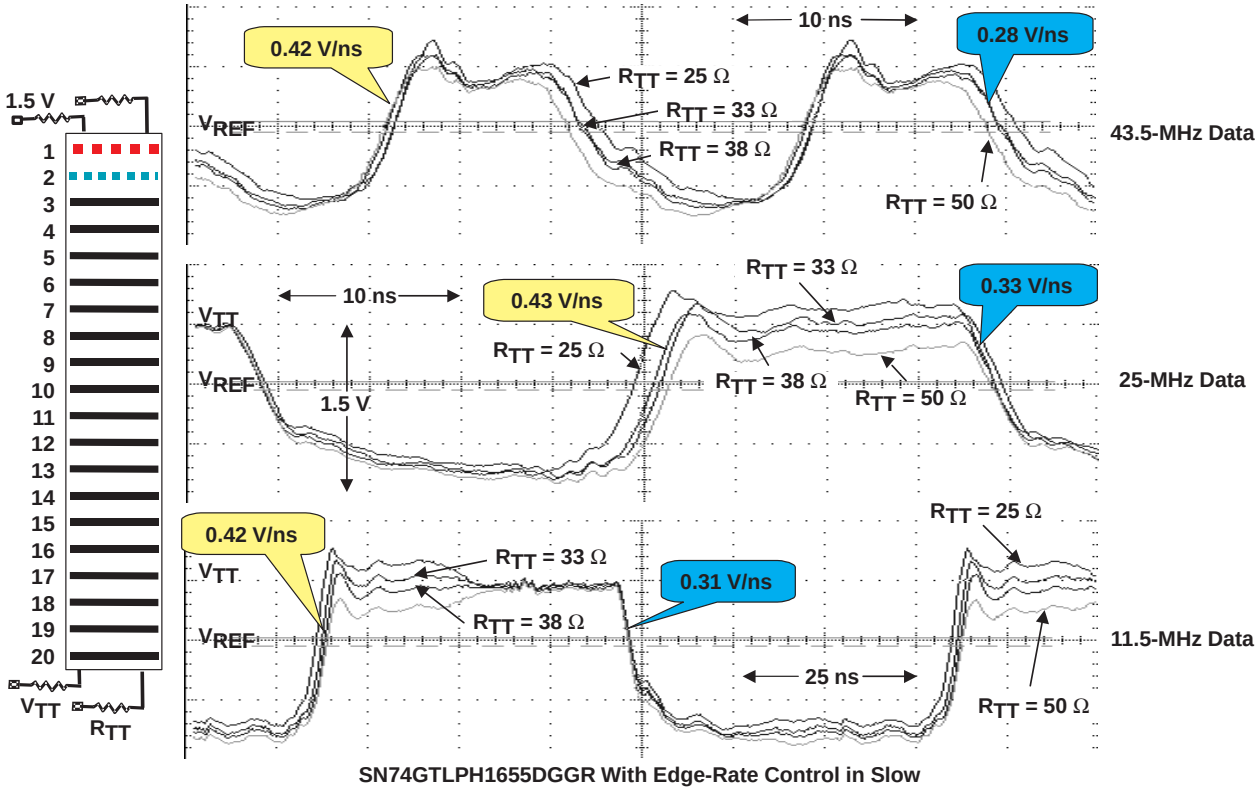


Figure 17. Fully Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 2)

The V_{OH} voltages at both 25-MHz and 43.5-MHz data rates never converge to the termination voltage of 1.5 V as with 11.5-MHz data. The reason is that the reflections have not had enough time to settle, which typically takes one round trip on the bus.

Additionally, slew rates of the optimum termination line are included for the rising and falling edges. Typical TTL slew rates in lumped loads are from 1 V/ns to 1.4 V/ns, depending on the capacitive load. The significantly slower GTLP edge rates result in a larger device t_{pd}, but allow for higher system frequencies because limited ringing improves signal integrity. The observed slew rate should increase as the load is reduced.

C_t can be calculated using the information known about the EVM and the observed $Z_{o(eff)}$. Assuming stripline construction with Z_o = 95 Ω and C_o = 2.40 pF/in, solve for C_d using equation 9 and assuming that the optimum $R_{TT} = Z_{o(eff)}$ = 35 Ω. An interpolated R_{TT} value of 35 Ω was chosen because it produces the best incident-wave switching performance. Then, solve for C_t by multiplying C_d by the separation between two transceivers which, in this case, is 0.94 in.

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1\right) \times C_o = \left(\frac{95^2}{35^2} - 1\right) \times 2.40 \text{ pF/in.} = 15.28 \text{ pF/in.} \tag{13}$$

$$C_t = C_d \times d = 15.28 \text{ pF/in.} \times 0.94 \text{ in.} = 14.36 \text{ pF} \tag{14}$$

Using C_d and C_o, the effective t_{pd} and flight time can be calculated.

t_{pd} for our EVM transmission line with a Z_o of 95 Ω = 230 ps/in.

$t_{pd(eff)} = t_{pd} \times \sqrt{1 + (C_d/C_o)}$ = 230 ps/in. × 2.71 = 624.3 ps/in.

The total distance traveled from slot 2 to the termination load is:

18 slots × 0.94 in. + termination stub length of 1 in. = 17.92 in.

Therefore, flight time is 17.92 in. × 624.3 ps/in., or 11.2 ns.

Round-trip flight time from slot 2 to the load, and back, is 22.4 ns.

The observed settling time is 20.8 ns.

Lightly Loaded Backplane

Figure 18 clearly shows the effect of the different termination resistors on signal integrity when every other card is removed from the EVM and the distributed capacitive load is reduced by a factor of two. There is still some capacitive loading (about 0.7 pF) at the empty slot position, but the majority is removed with the female connector, stub, and device C_{io}.

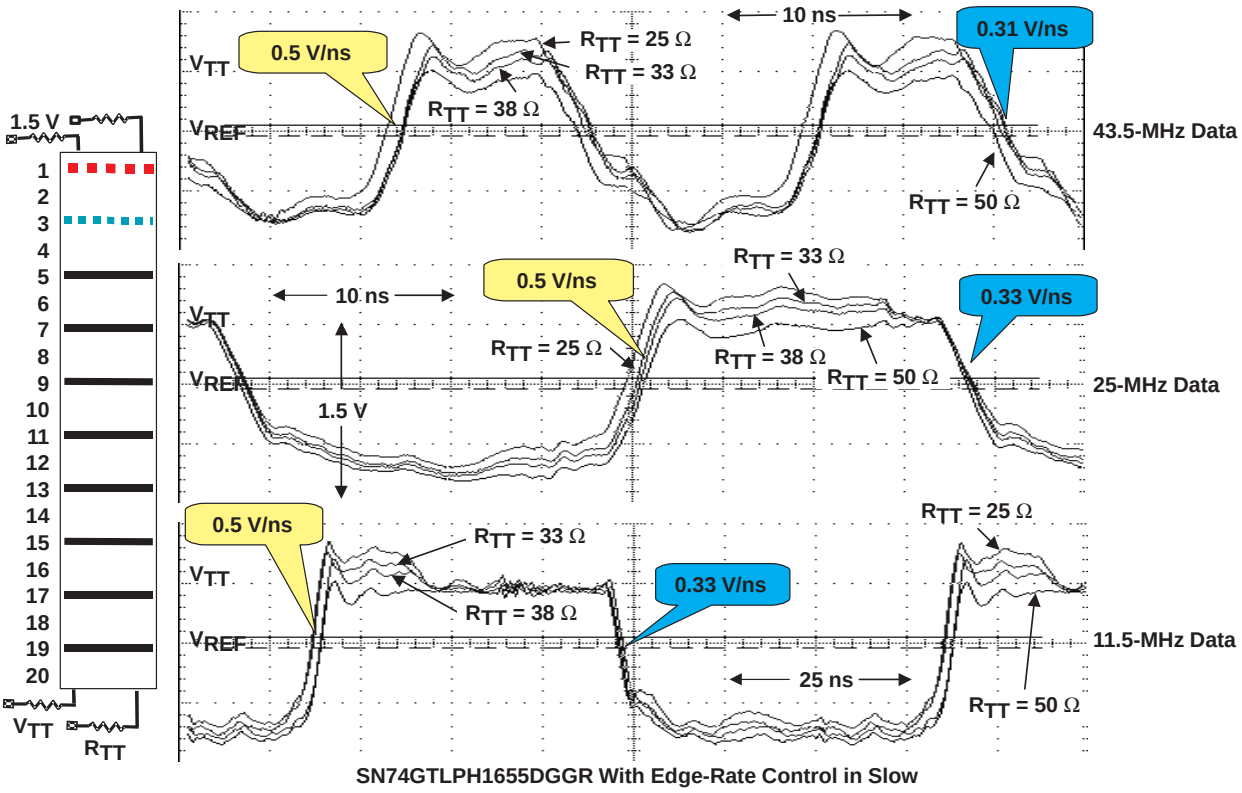


Figure 18. Lightly Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 3)

All termination resistances again show incident-wave switching, with noise margin gained as the termination-resistor value is reduced, but all resistances are within acceptable noise-margin limits. This shows a very important point; reducing C_t by increasing slot spacing, reducing stub length, using devices with a lower C_{io}, or a combination of all three reduces the loaded backplane capacitance, allowing a higher termination-resistor value to be used.

C_t can be calculated again, and should be the same value as obtained for the fully loaded case. Optimum R_{TT}, in this case, is 46 Ω (interpolated from Figure 18).

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1\right) \times C_o = \left(\frac{95^2}{46^2} - 1\right) \times 2.40 \text{ pF/in.} = 7.84 \text{ pF/in.} \tag{15}$$

$$C_t = C_d \times d = 7.84 \text{ pF/in.} \times 1.88 \text{ in.} = 14.73 \text{ pF} \tag{16}$$

The fully loaded and lightly loaded C_t values agree closely, as expected.

$$t_{pd(eff)} = t_{pd} \times \sqrt{1 + (C_d/C_o)} = 230 \text{ ps/in.} \times 2.07 = 475.1 \text{ ps/in.}$$

Therefore, flight time is 16.98 in. (17 slots × 0.94 in. + 1 in.) × 475.1 ps/in. or 8.1 ns.

Round-trip flight time from slot 3 to the load, and back, is 16.2 ns.

The observed settling time is 15.5 ns.

Very Lightly Loaded Backplane

Figure 19 clearly shows the effect of the different termination resistors on signal integrity when every other three cards are removed from the EVM and the distributed capacitive load is reduced by a factor of four.

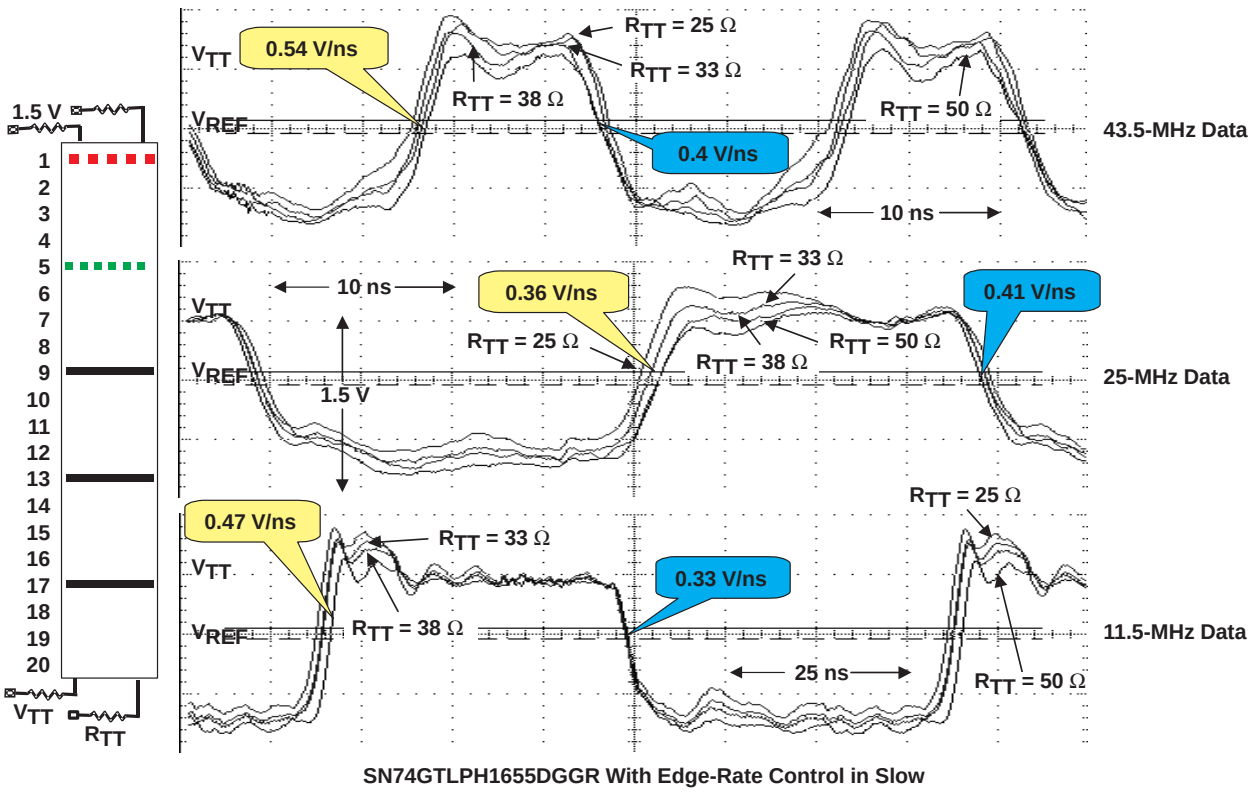


Figure 19. Very Lightly Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 5)

C_t can be calculated and should be the same values as obtained in the other cases. Optimum R_{TT}, in this case, is 60 Ω (extrapolated from Figure 19).

$$C_d = \left(\frac{Z_o^2}{R_{TT}^2} - 1\right) \times C_o = \left(\frac{95^2}{60^2} - 1\right) \times 2.40\ \text{pF/in.} = 3.62\ \text{pF/in.} \tag{17}$$

$$C_t = C_d \times d = 3.62\ \text{pF/in.} \times 3.76\ \text{in.} = 13.6\ \text{pF} \tag{18}$$

In all cases, the C_t values agree closely (within ±5%).

$$t_{pd(eff)} = t_{pd} \times \sqrt{1 + (C_d/C_o)} = 230\ \text{ps/in.} \times 1.58 = 364.3\ \text{ps/in.}$$

Therefore, flight time is 15.1 in. (15 slots × 0.94 in. + 1 in.) × 364.3 ps/in. or 5.5 ns.

Round-trip flight time from slot 5 to the load, and back, is 11.0 ns.

The observed settling time is about 10 ns. Some oscillations are evident to about 25 ns.

In all cases (i.e., fully, lightly, and very lightly loaded) observed vs calculated flight times are within 10%.

The total capacitance in all the above cases was calculated to be about 14 pF, based on the observed optimum R_{TT}. Analyzing each component in the capacitance chain on the daughter card is summed below, with the results close to observed and measured. The daughter-card construction use for the GTLP EVM is different from the original assumptions. The via and stub 1 add no capacitance to the line. Through-hole connectors, instead of surface mount, were used for increased reliability, but at the expense of additional capacitance. C_{cpad3} was added and is required to connect the device to stub 2.

$$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{cpad3} + C_{io} \quad (19)$$
$$= 0 + 0 + 0.5 + 2.0 + 0.5 + 3.3 + 0.5 + 7 = 14.5 \text{ pF}$$

Where:

C_{via} = capacitance of via = 0 pF
C_{stub1} = capacitance of stub 1 = 0 pF
C_{cpad1} = capacitance of C_{pad1} = 0.5 pF
C_{cpad2} = capacitance of C_{pad2} = 0.5 pF
C_{stub2} = capacitance of stub 2 = 1 in. × 3.3 pF/in. = 3.3 pF
C_{con} = capacitance of connector = 2.0 pF
C_{cpad3} = capacitance of C_{pad3} = 0.3 pF
C_{io} = typical input/output capacitance of device (SN74GTL1655) = 7 pF

The procedure to determine the actual backplane natural trace impedance (Z_o) was to measure the daughter-card C_t directly (13.8 pF). Then, flight time, with only slot 1 occupied, was measured and divided by backplane length to determine that t_{pd} unloaded was 230 ps/in. The same procedure was used in a fully loaded condition, and the resulting t_{pd} was 616 ps/in. Using the backplane calculator set to the new C_t, Z_o was adjusted to match the measured t_{pd}. The new Z_o was 96 Ω, C_o = 2.4 pF/in., and $Z_{o(eff)}$ = 36 Ω.

Table 2 provides the results of additional investigation using different equipment (i.e., TDR) on each of the eight traces in the 20-slot group (group 1) on the GTLP EVM. Z_o is calculated and is our best estimate. The backplane trace impedance with only the connector pins attached (i.e., all cards removed) (Z_o') and the backplane trace impedance in a fully loaded backplane (i.e., 20 cards inserted) (Z_o'') are measured. Group 1, bit 1, Z_o is closer to 91 Ω and, in the fully loaded case, the t_{pd} is 564 ps/in. vs our assumption of 624.3 ps/in. This makes round-trip flight time 20.2 ns, which is much closer to the observed time of 20.8 ns.

Table 2. GTLP EVM Group 1 Trace Impedance

GROUP 1 TRACE	D1	D2	D3	D4	D5	D6	D7	D8
Natural Trace Impedance								
Z_o (Ω)	91	47.5	47	47	48	47.5	83	47.5
t_{pd} (ps/in.)	165	140	138	139	141	148	147	142
C_o (pf/in.)	1.81	2.95	2.94	2.96	2.94	3.12	1.77	2.99
Trace Impedance With Only Connectors								
Zo′ (Ω)	62.7	37.5	37	36.3	37.1	37.9	58.5	36.8
t_{pd}' (ps/in.)	240	177	175	180	183	185	208	183
Trace Impedance Under Full Load								
Z_o'' (Ω)	26.6	17.7	17.9	17.5	17.9	18	24.8	17.7
t_{pd}'' (ps/in.)	564	377	362	373	377	390	493	382

Note the difference in the fully loaded trace impedance between trace D1/D7 and the other traces. Using the lower natural trace impedance offers the advantage of a smaller t_{pd} and shorter time of flight, but at the expense of terminating with a lower-value termination resistor and the subsequent increase in power consumption. Texas Instruments offers both medium-drive (50 mA) and high-drive (100 mA) GTLP devices to allow the designer to match the device with backplane loading. The termination resistor (R_{TT}) should match the fully loaded trace impedance (i.e., Z_o'') of the backplane for optimal signal integrity.

Table 3 provides the stackup used on the GTLP EVM backplane. Additional information on the GTLP EVM can be found in the *GTLP EVM User's Guide* (SCEA023).

Table 3. GTLP EVM Backplane Stackup

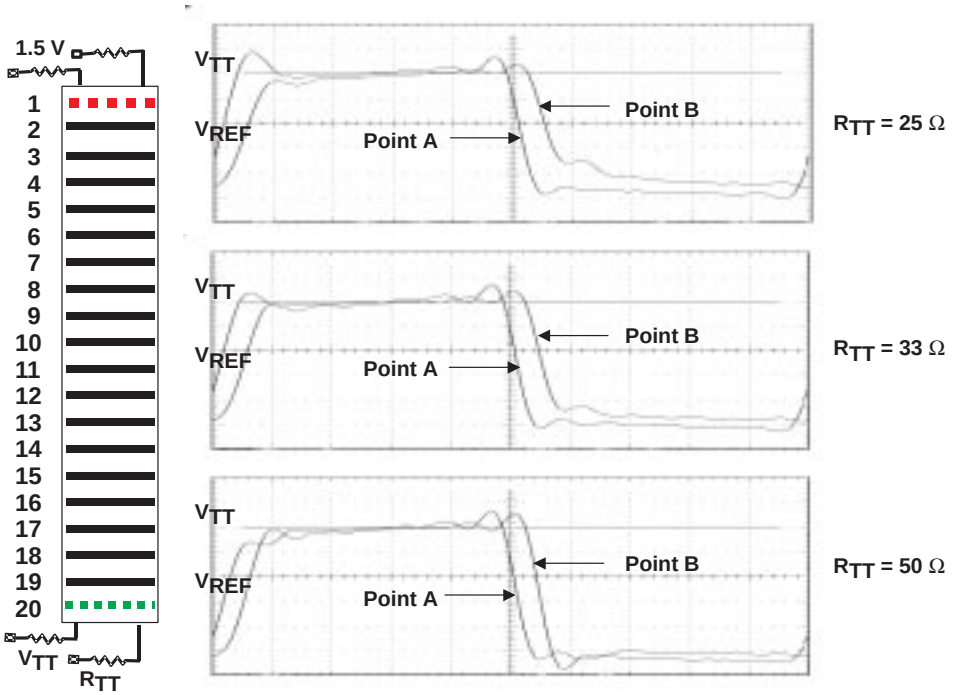
TRACE NAME	USE	LAYER	COPPER WEIGHT (oz)	PHYSICAL REPRESENTATION	DIELECTRIC HEIGHT (in.)	DIELECTRIC NAME
Top	Regulator power/ bypass capacitor/termination	1	0.5			
					0.004	B stage
Internal signal 2	Clock distribution/signal	2	1			
					0.004	Core
Ground plane	Ground plane	3	1			
					0.004	B stage
Internal signal 3	Data signal	4	1			
					0.058	Core
Internal signal 4	Data signal	5	1			
					0.004	B stage
V_{CC}	V_{CC}	6	1			
					0.004	Core
Internal signal 5	Data signal	7	1			
					0.004	B stage
Bottom	Termination	8	0.5			

High-drive (100 mA) devices, such as the SN74GTLPH1655, can drive the transmission line down to $R_{TT} \approx 22\ \Omega$, without exceeding the recommended maximum I_{OL}, while medium-drive (50 mA) GTLP devices can drive the transmission line down to $R_{TT} \approx 38\ \Omega$. Both drives can be used with higher values of R_{TT} (i.e., 60 Ω), if required. Medium-drive GTLP devices cost less, have a smaller pin count (fewer GND and V_{CC} pins), and have slightly less maximum B-port C_{io} (medium drive is 9.5 pF vs 10.5 pF for high drive), so the designer must balance and optimize backplane construction with device capability to ensure optimum system signal integrity.

The driver card on the GTLP EVM used initial engineering samples of the SN74GTLPH1655. All receiver cards used production SN74GTL1655 devices because they were more readily available and were operated only in the receive mode. The newer GTLP devices were designed specifically to drive transmission lines and have slower backplane-optimized slew rates for better signal integrity. GTL devices have faster edge rates and are better for point-to-point applications.

Backplane DC Effects – Theory to Practice

Figure 20 shows the dc effects previously described in the *Backplane DC Effects* section on a fully loaded backplane with waveforms plotted at different terminations. V_{OL} information is taken with an 8-MHz clock frequency (4-MHz data), which is the slowest crystal oscillator we had on hand, in order to eliminate as much ac switching effects from the V_{OL} measurement as possible. Each set of waveforms represents measurements taken at each end of the GTLP EVM (or points A and B as described in Figure 11). As expected, V_{OL} decreases as the termination voltage increases because the GTLP driver is able to drive the line lower with a higher resistance load.



SN74GTLPH1655 With Edge-Rate Control in Fast and Frequency = 100 MHz

Figure 20. Fully Loaded Backplane vs R_{TT} (Driver in Slot 1, Receiver in Slot 20)

Assuming the line resistance from one end of the GTLP EVM to the other (slot 2 to slot 20) to be about 2.7 Ω, an on resistance of the SN74GTLPH1655 output driver to be 2.75 Ω (measured value), and V_{TT} = 1.5 V, and using equations 10 and 11, theoretical values vs actual test measurements were obtained (see Table 4). V_{TT} voltage source cause V_{OL} (and V_{OH}) to fluctuate; the difference in the two levels was plotted (not shown) and measured. This voltage difference was then compared to the calculated values, and the data shows that a very good correlation exists. Thus, validity of equations 10 and 11 is verified.

Table 4. Theoretical vs Actual V_{OL} Measurements

R_{TT} (Ω)	THEORETICAL VALUES			ACTUAL VALUES
	V_{OL} SLOT 2 (V)	V_{OL} SLOT 20 (V)	DIFFERENCE (mV)	DIFFERENCE (mV)
25	0.260	0.380	121	120
33	0.207	0.305	98	96
38	0.184	0.271	87	
50	0.145	0.215	69	72

Data from Table 4 also implies that there is a theoretical maximum length of a backplane. As the length increases, the V_{OL} difference increases and reaches a point where the highest V_{OL} value is within the predetermined noise margin allotted to the system by the designer.

Conclusion

Good backplane designs should follow the design rules in this application report and account for the capacitive loading effects on a backplane transmission line to obtain better signal integrity and achieve incident-wave switching. Minimizing the distributed capacitance on the backplane transmission line is desirable and can be accomplished by using transceiver devices with low C_{io}, selecting connectors with low capacitance, using higher natural trace impedance (balanced against backplane time of flight), and by keeping stub lengths short.

The backplane integrated-circuit drive strength must be selected based on the fully loaded characteristic impedance of the backplane and should be able to maintain the minimum required V_{OL} levels along the entire length of the backplane without exceeding the recommended maximum low-level output current limitations.

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Glossary

C_{io}	Input/output capacitance of the transceiver
C_o	Characteristic capacitance – capacitance per unit length of a transmission line in free space
GTL	Gunning transceiver logic– operates at signal levels of V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{OL} = 0.4 V. GTL+ is a derivative of GTL that operates at higher noise-margin signal levels of V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{OL} = 0.55 V, and moves V_{REF} from the normal ground-bounce area.
GTLP	Gunning transceiver logic plus – normally associated with slower edge-rate devices optimized for distributed loads that allow higher-frequency operation in heavily loaded backplane applications
L_o	Characteristic inductance – inductance per unit length of a transmission line in free space
R_{TT}	Termination resistance – resistance used to match the effective impedance of a transmission line in order to minimize reflections. $R_{TT} = Z_{o(eff)}$
$t_{(flight)}$	Flight time – time it takes a signal to propagate between two points on a transmission line. $t_{(flight)}$ = length $\times$ t_{pd}
t_{pd}	Propagation delay – delay per unit length of a signal traveling down a transmission line, expressed by the formula $t_{pd} = Z_o \times C_o$
Z_o	Characteristic impedance – impedance of a transmission line, as defined by $Z_o = \sqrt{L_o/C_o}$
$Z_{o(eff)}$	Effective impedance – impedance of a transmission line when external capacitance is added at fixed intervals along the line. $Z_{o(eff)} = \sqrt{L_o/(C_o + C_d)}$

Application Report
SCEA022 - April 2001

Achieving Maximum Speed on Parallel Buses With Gunning Transceiver Logic (GTLP)

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Standard Linear & Logic

ABSTRACT

This application report compares two approaches for synchronous bus-system designs. The focus of the report is the comparison of a system using central-synchronous system clock (CSSC) with a system operated with a source-synchronous system clock (SSSC).

The basic characteristics of lines, key factors that influence the bus line delay, and the impedance of bus lines are described.

The theoretical advantages of an SSSC system over a CSSC system are based on a comparison of timing budget calculations. Theoretical results are confirmed by measurements, using the GTLP demonstration backplane.

In the SSSC mode, the system-clock frequency is, with a clock frequency of 120 MHz, about 2.4 times higher than in the CSSC mode.

Contents

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1 Introduction

Driver modules that are set up for a modern-wiring backplane have many complex requirements. The drivers must switch fast, with the smallest possible propagation time and the greatest possible number of bits in one driver, to provide the necessary data throughput over the bus.

In addition, the driver should have a sufficiently high driver capacity to generate the required logic levels, even in the case of a full backplane with many interconnected receive and transmit modules. Also, the drivers should have a small noise potential and a large noise margin. The optimum driver should use little power and have the live-insertion with precharge property, which allows exchanging modules during operation without impairing the function of the overall system.

In many electronic systems, shutdown to change a defective system part is not possible without severe adverse consequences for the complete application. Examples are electronic telecommunications systems, the control center in an electrical power-supply company, or computers used by air-traffic controllers.

The GTLP bus drivers address all the above points: minimum propagation time, high-drive capability, and the capability of being inserted into, or removed from, the system during operation, and have been developed especially for this type of application.

This application report emphasizes system speed, which is achieved by the appropriate architecture, using GTLP devices.

Section 2 describes physical basics of backplanes. Influences of the number of modules and the distance between modules on the properties of transfer speed and line impedance are explained.

Section 3 discusses two setups, both of which are based on a synchronous system design using GTLP devices:

- Central-synchronous system clock (CSSC) – All system cards use the same clock as base for the data.
- Source-synchronous system clock (SSSC) – The transmitter also sends the clock signal, via an additional line, along with the data.

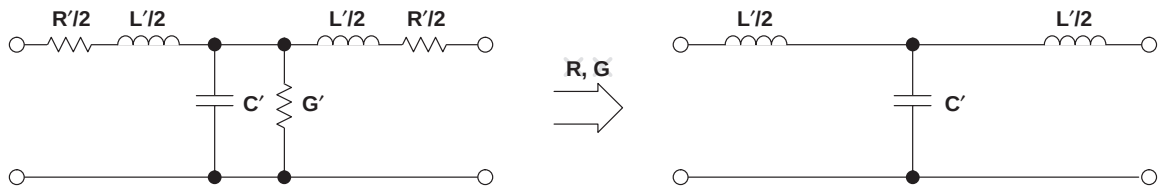
The theoretical considerations are confirmed by measurements using the GTLP demonstration board.

In principle, both systems can be set up using technologies other than GTLP. However, the combination of the advantages of high-driver capability, live-insertion capability, and flexible edge steepness that can be modified during operation, is found only with the GTLP bus-driver solution.

2 Physical Properties and Limitations of Bus Lines

The basic composition of a line consisting of capacitive and inductive replacement components is shown in Figure 1. In the case of static conditions, line impedance primarily is determined by the ohmic resistance and/or the parallel conductance of C′ of the line. These are not of any consequence at a frequency of just a few kilohertz, because the frequency is in the term $\omega = 2 \times \pi \times f$.

At high frequencies, transmission-line losses on printed circuit boards in digital systems can be neglected.



L′ = Characteristic Inductance Per Unit Length (nH/cm)
C′ = Characteristic Capacitance Per Unit Length (pF/cm)
R′ = Characteristic Resistance Per Unit Length (Ω/cm)
G′ = Characteristic Conductance Per Unit Length (S/cm)

Complex Line Impedance

$$\vec{Z}_0 = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

With R′ << jωL′ and G′ << jωC′:

Line Impedance $Z_0 = \sqrt{\frac{L'}{C'}}$ **(real number !)**

Propagation Time $\tau = \sqrt{L' \times C'}$

Figure 1. Ideal Transmission Line With Negligible Conductance and Resistance

Comparing the apparent impedance for a specified frequency (e.g., 1 MHz) with the parallel conductance G′ and the series resistance R′ shows that G′ and R′ are negligible compared with the line impedance Z_O.

The simplified formulae for line impedance and the propagation delay time per unit length are dependent only on the inductive and capacitive layer of the line. In practice, calculations are easy to handle. In the case of a homogeneous line, which represents a connection between a transmitter and a receiver, its capacitive and inductive layers determine the line property.

However, if we look at bus lines, such as the one in Figure 2, the line impedance no longer is constant and is dependent on the number of inserted modules.

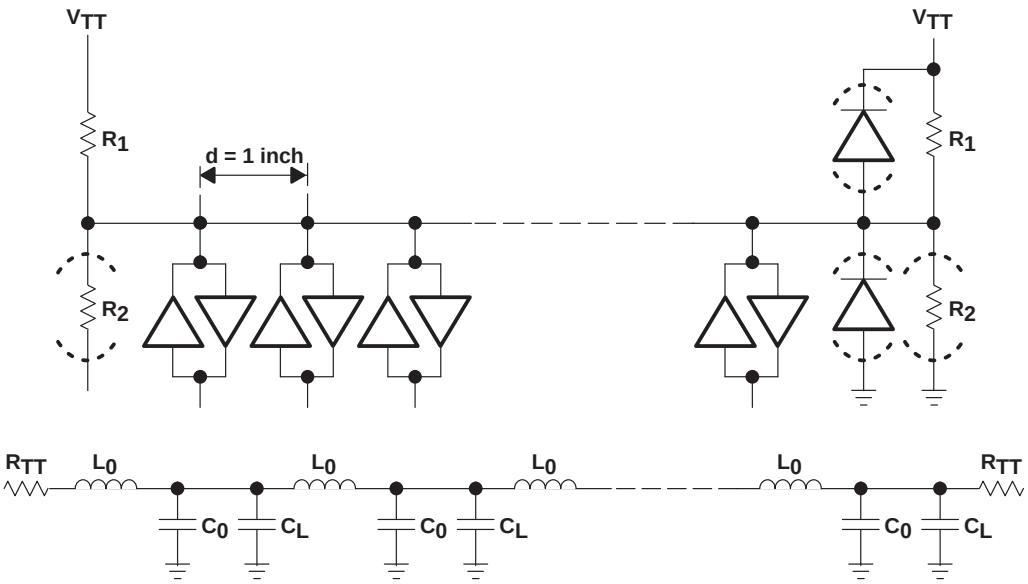


Figure 2. Additional Capacitive Load of Line by Modules

If the distances between the inserted modules remain electrically short, i.e., twice the propagation delay time between two inserted modules is shorter than the rise/fall time of the signal, it is possible to add the capacitive load to the capacitive layer. The influence on the inductive layer is negligible.

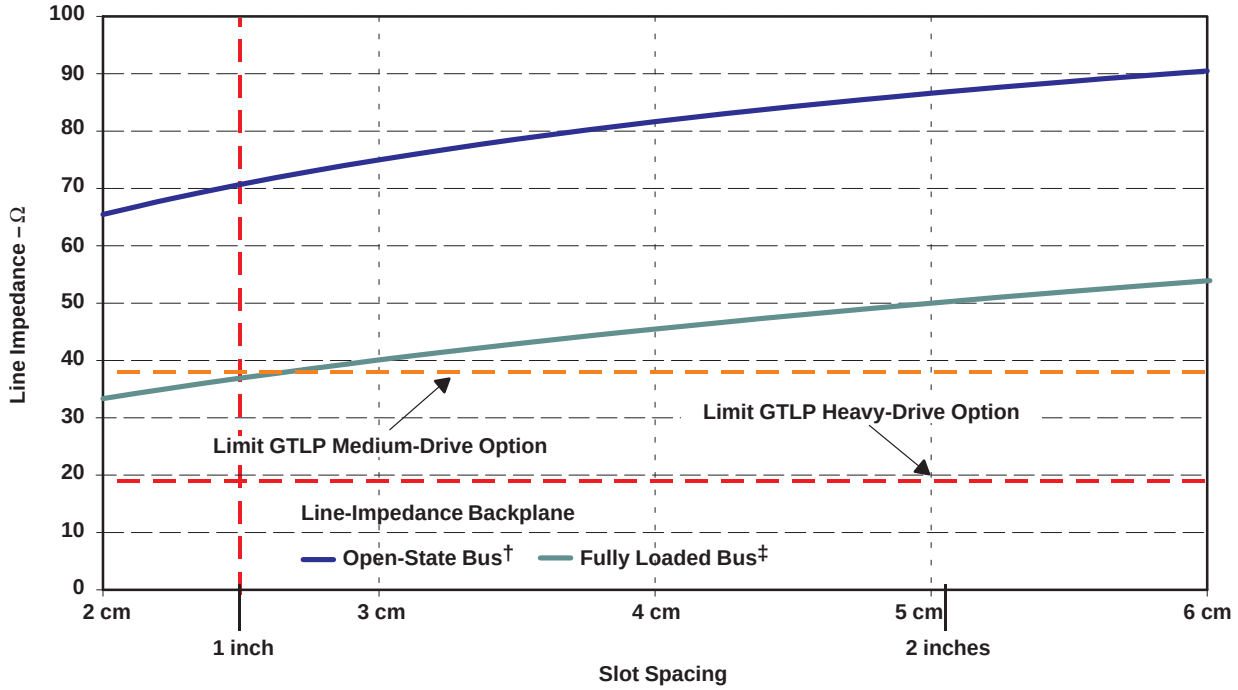
Table 1 shows the comparison between a point-to-point connection on a PCB, an unloaded bus line with the bus connectors only, and a fully loaded bus. The distance between the slots is 1 inch.

Table 1. Comparison of PCB Line and Bus Line (Slot Distance = 1 Inch)

LINE PARAMETER	OPEN LINE		LOADED LINE (BUS)
	PCB	BUS	
Inductive layer, L_0	6.5 nH/cm	6.5 nH/cm	6.5 nH/cm
Capacitive layer, C_0	0.4 pF/cm	0.4 pF/cm	0.4 pF/cm
Connector	Not applicable	2 pF per slide-in module	2 pF per slide-in module
Feed line to backplane side of connector	Not applicable	<<1 pF	<<1 pF
Feed line to module side of connector	Not applicable	Not applicable	~1 pF
Input capacity of receiver	Not applicable	Not applicable	9 pF
Additional capacity load, C_L	Not applicable	2 pF/2.54 cm	10 pF/2.54 cm
Capacitive load per cm	0.4 pF	1.2 pF	4.73 pF
Line impedance, Z_0	127 Ω	74 Ω	37 Ω
Propagation delay time of signal, τ	5.1 ns/m	8.8 ns/m	17.5 ns/m

While the inductive layer remains almost constant in all three cases, the connectors, stub lines to the connector, and driver input and output, as well as the input capacity of the receiver, represent an additional capacitive load for the line. The increased capacitive load reduces the line impedance and starts the demand for higher driver capability for bus-interface logic. However, the signal propagation delay time via the bus increases significantly (by a factor of more than three in the example above)

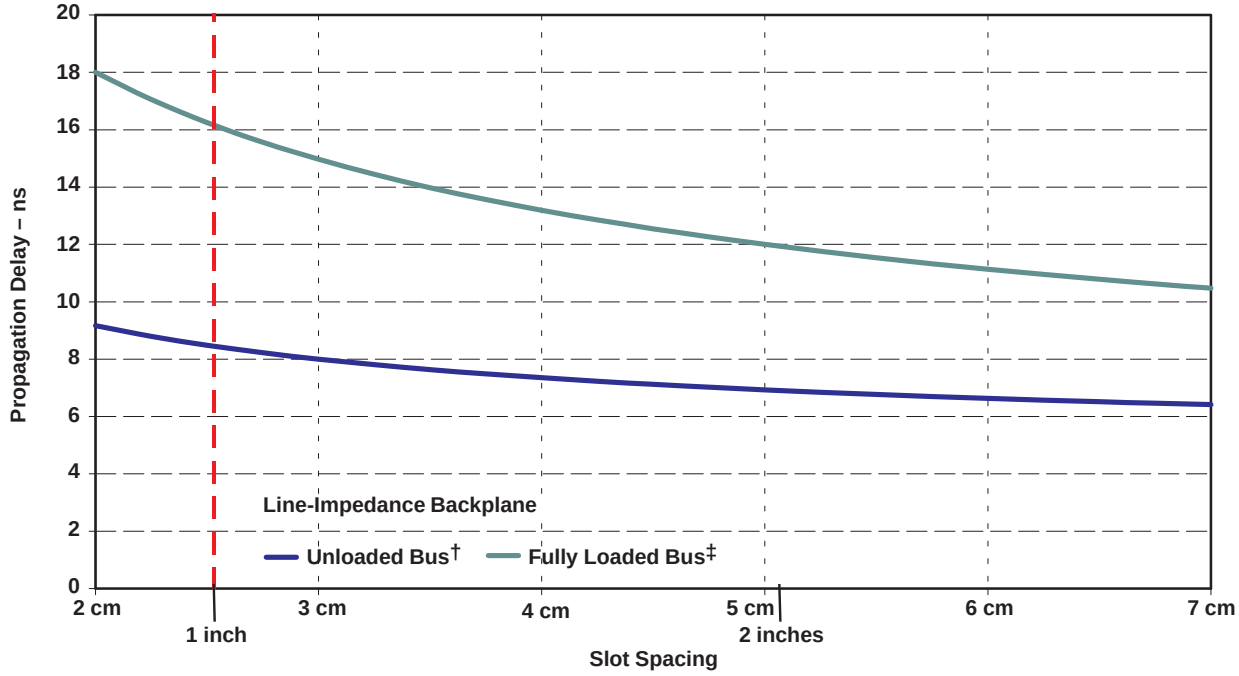
Changing the distances between the modules affects the capacitive layer of the line as shown in Figure 3.



† Assuming a capacitive load of 2 pF per slot (connector only)
‡ Assuming a capacitive load of 10 pF per slot (complete module)

Figure 3. Effect of Slot Spacing on Line Impedance

One curve represents a bus line in the unloaded state, for which the bus-side connectors are the only loads on the line. The other curve represents a fully loaded bus line. The same correlation also is produced with regard to the propagation time of the line, and is shown in Figure 4.



† Assuming a capacitive load of 2 pF per slot (connector only)
‡ Assuming a capacitive load of 10 pF per slot (complete module)

Figure 4. Effect of Slot Spacing on Flight Time

The values from Table 1 for the slot distance of 1 inch in Figures 3 and 4 can be found at intersections with the dashed lines.

The homogeneity of the line impedance cannot be ensured in every case. For a backplane, the modules can be inserted into different positions on the backplane, and some positions can be left empty, so the different bus-line sections have different impedance values.

However, this fact does not significantly affect the quality of the signal.

3 Transfer Modes

For a synchronous system, as the name suggests, it is important for the transferred data to refer to a common system-clock signal. Every participant in the system then gets the active edge of system clock as a reference and a data signal, which refers to the system clock.

In this section, two synchronous transfer modes are described:

- Central-synchronous system clock (CSSC) mode
- Source-synchronous system clock (SSSC) mode

System parameters that have an important role in affecting the maximum clock speed, in conjunction with the calculation of the time budget, are discussed in the following subsections.

3.1 Parameters for the Time Budget

Parameters for the time budget are assigned to different sources (see Figure 5). The transmitter and clock-distribution devices have skew values and additional propagation time as a result of simultaneous switching. Flight time represents the propagation delay time of the signal via the bus. Finally, the setup and hold times of the receiver must be taken into account.

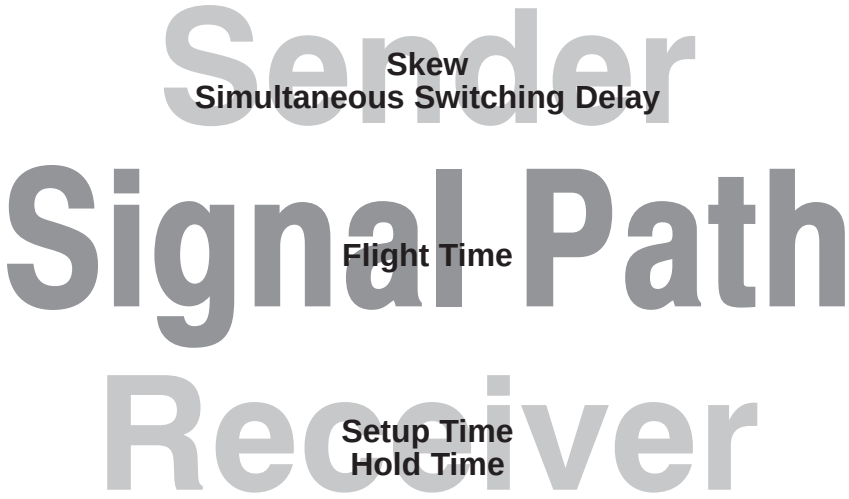


Figure 5. Important Parameters for the Time Budget

3.1.1 Skew

Skew is the small difference that arises from different propagation delays between output stages within a device. These differences, which cannot be prevented, are defined in the EIA/JEDEC standard, *Definition of Skew Specification for Standard Logic Devices* (EIA/JESD 65) (see Figure 6).

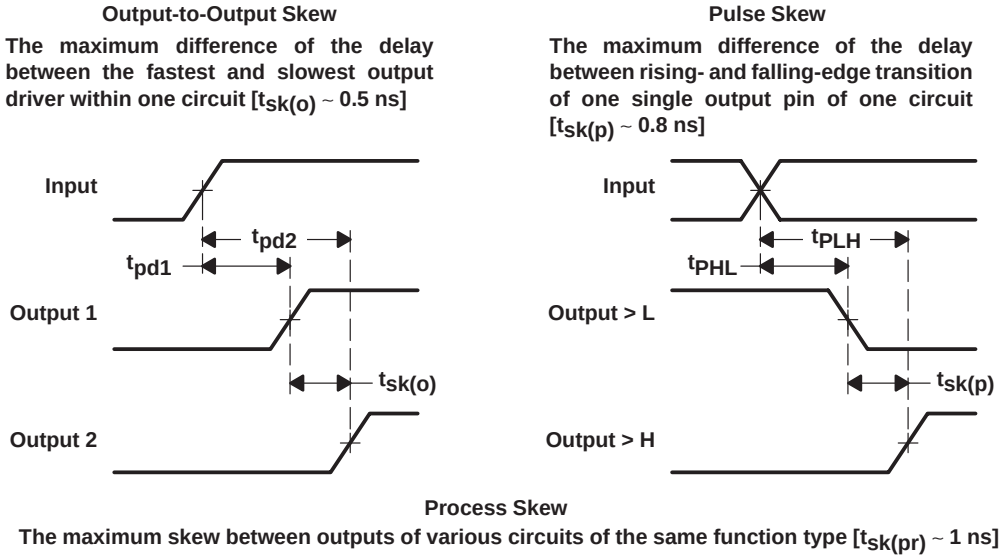


Figure 6. Skew Definitions

Output-to-output skew, $t_{sk(o)}$, is the maximum difference between the slowest and the fastest of the drivers within a package. For clock distribution drivers, $t_{sk(o)}$ is approximately 500 ps. For interface devices, this parameter is not always given, but is typically less than 1 ns.

Pulse skew, $t_{sk(p)}$, describes the difference in propagation delay time between the positive and negative edge, and it is an important definition, if there is a specific duty cycle required.

Should more than one device participate in the clock distribution, process skew (which is the maximum difference in propagation time between drivers of the same function) is defined. Process skew is added to the output-to-output skew.

3.1.2 Propagation Time Due to Simultaneous Switching

The simultaneous switching parameter, Δt_{pd}, is the difference in propagation time that arises from the simultaneous switching of several outputs of the same device.

Data sheets show only the maximum propagation time of one output when it is the only one to be switched. An additional propagation time must be taken into account when multiple outputs are switched simultaneously. The reason for the increase in propagation time is the internal package inductance, which works as a current brake. The more outputs that are switched on, the greater the current and, therefore, the braking effect is greater. Figure 7 shows this correlation for different package options.

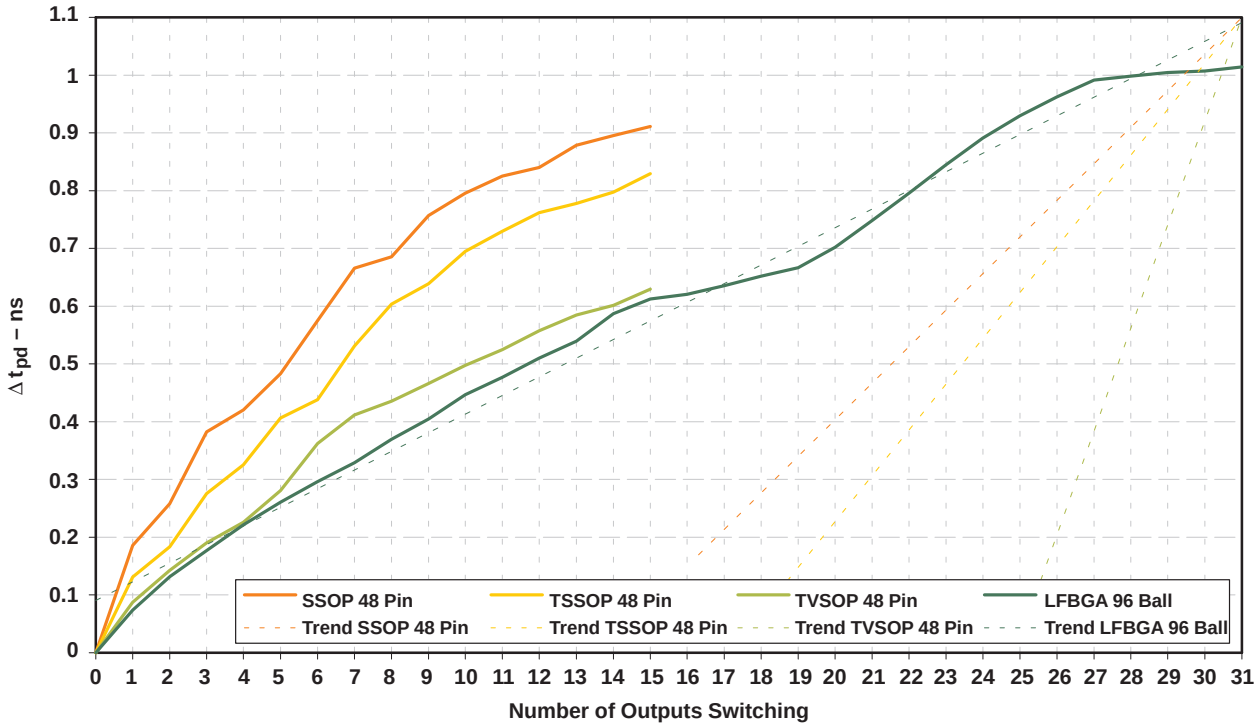
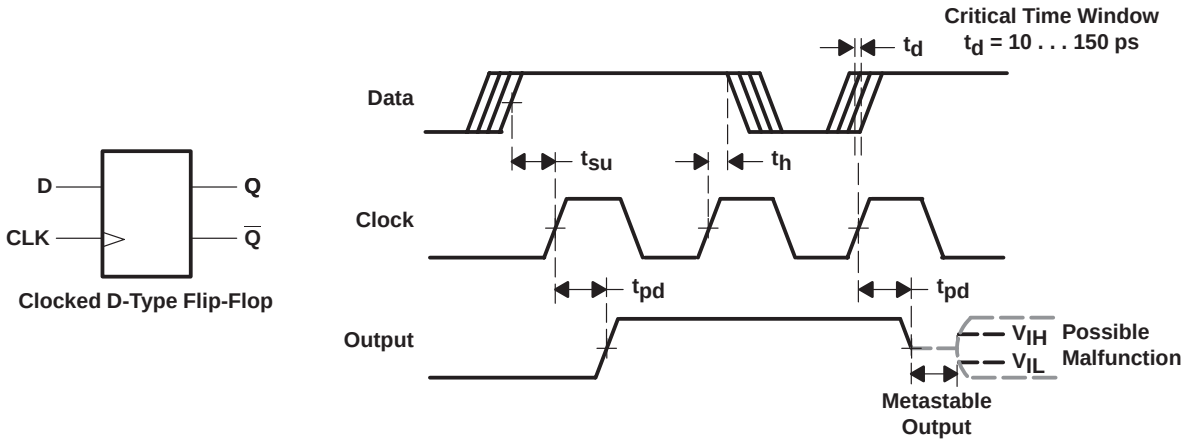


Figure 7. Effect of Simultaneous Switching on Propagation Time

The low-profile fine-pitch BGA (LFBGA) package shows the best skew behavior, when forced by simultaneous switching, in this comparison. Despite having double the number of outputs switched at the same time, the absolute difference of the propagation delay in Figure 7 is not significantly greater than that of other modern 16-bit dual-inline packages.

3.1.3 Setup and Hold Times at Receiver Input

In a synchronous system, a common clock signal, which is synchronous for all the interface devices (e.g., registers or flip-flops) exists. Figure 8 shows the definitions for setup and hold time based on a D flip-flop. Both times are defined around the active edge of the clock signal.



NOTE: The setup and hold times are given in the data sheets. For GTLPH1655, t_{su} is 2.6 ns and t_h is 0.5 ns.

Figure 8. Setup and Hold Times

The setup time is the time during which a data signal must be stable before the active edge of the clock input occurs. The hold time is the time during which a data signal must be stable after the active edge of the clock input occurs. Should either of the two times be violated, it is possible that the output can be in a metastable state in the critical time window. The result can be a state in undefined range or even in the threshold region, that represents neither a logical 1 nor a logical 0. The consequence can be that the subsequent stage can interpret the value as either high or low. Therefore, the probability of malfunctions increases dramatically.

3.2 Central Synchronous Clock Distribution

A basic prerequisite for a synchronous system is that the transferred signals refer to a common clock signal that is transmitted from a central clock distribution circuit. In the layout shown in Figure 9, the active clock edge reaches all parts of the system as simultaneously as possible. For skew adjustment, the line lengths have been chosen to be as close as possible.

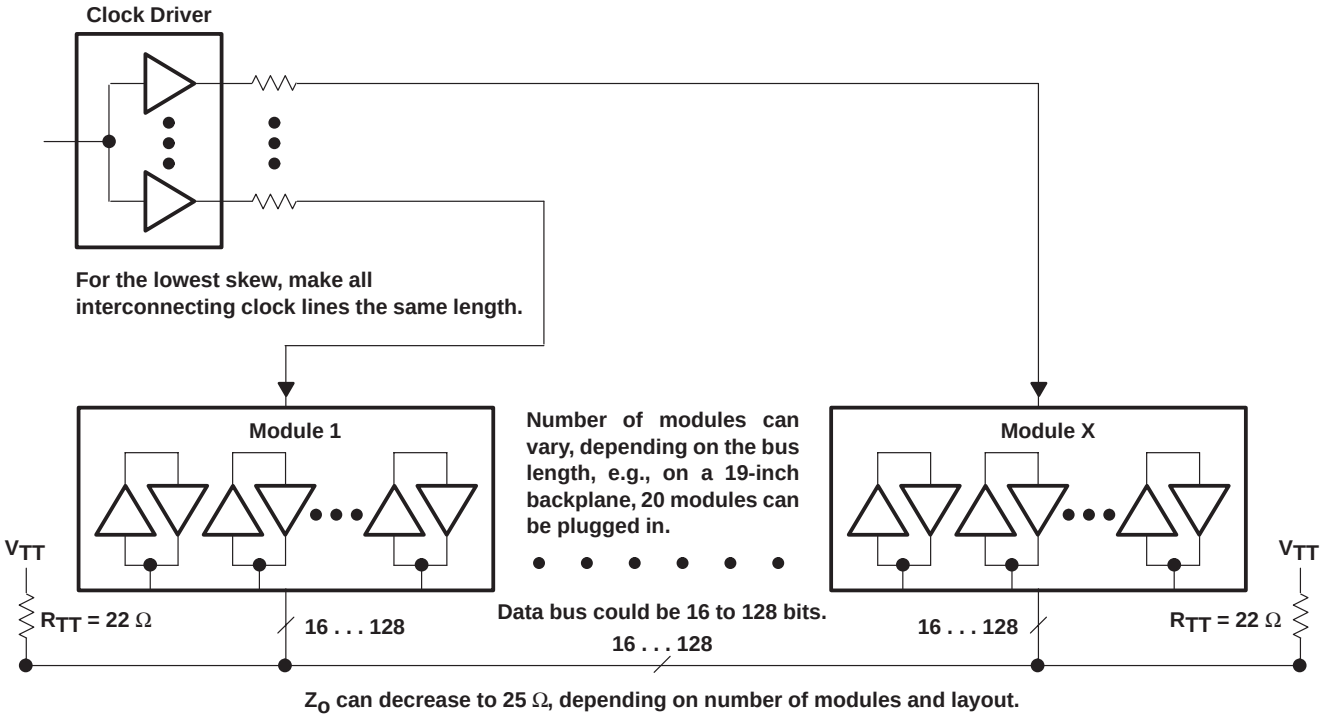
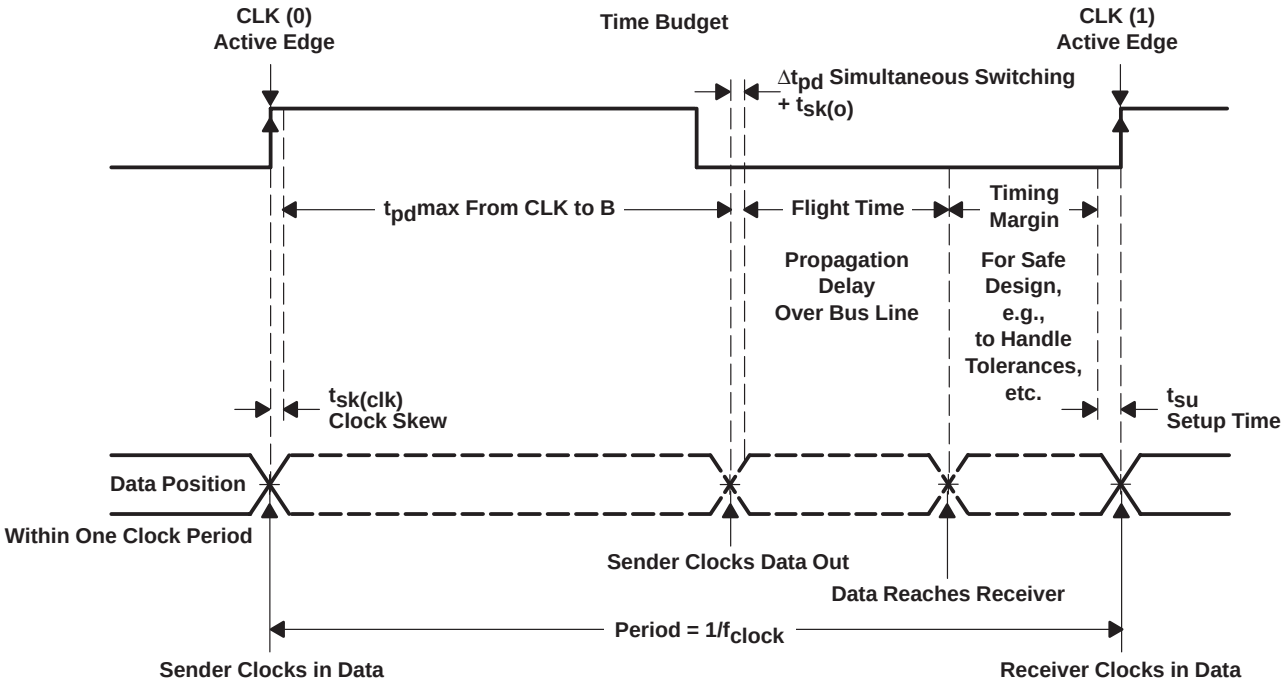


Figure 9. Principle of Central Synchronous Clock Distribution

Figure 10 shows the time budget for the central-clock distribution. All times that must be taken into account are shown. The main contributors of time in the timing budget are the propagation delay time of the device and the propagation delay time over the bus.



NOTE: No additional clock signal line is required because all receivers refer to system clock.

Figure 10. Time Budget for Central Synchronous System Clock Distribution Environment

The need for all system parts to receive the clock at the same time is a disadvantage because the propagation delay time of the data signals via the bus must be taken into account when determining the maximum frequency of the system.

The transmitted data must propagate over the distance from the transmitter to the receiver within a single clock cycle, because the transmitter and the receiver work with exactly the same active edge of the clock signal.

Should the data fail to reach the receiver input within a clock period, the synchronicity of the system no longer can be ensured. In this case, the signal reaches one part of the bus system at the right time (within the same clock period), while another part does not receive the signal until one clock period later. This effect is shown as case 2 of Figure 11.

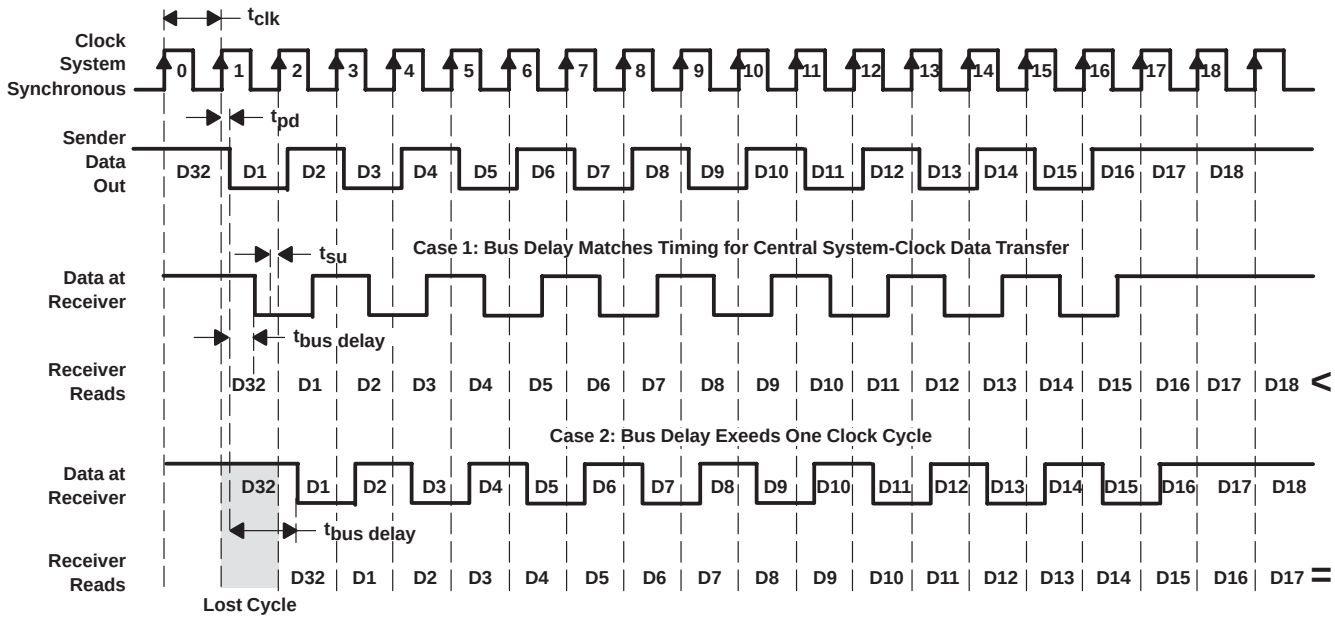


Figure 11. Two Examples for Data Transmission in a Central Synchronous System Clock Distribution Environment

The maximum frequency is calculated from the skew of the clock-distribution circuit [t_{sk}(clk)], the device propagation (t_{pd}), the skew of the driving device, the additional propagation delay time (Δt_{pd}) due to simultaneous switching of several outputs, the transit time via the bus [t_{flight}(bus)], as well as the setup time of the connected receiver [t_{setup}(rec)]. The formula for calculating the maximum frequency is:

$$f_{max}(clk) = \frac{1}{t_{sk}(clk) + t_{pd}(clk\ \text{to}\ B) + \Delta t_{pd}(sim.sw.transm.) + t_{sk(o)} + t_{flight}(bus) + t_{setup}(rec)} \quad (1)$$

With:

$t_{sk(o)}$(clk)	= 0.5 ns
t_{pd}(GTLPH1655)	= 5.8 ns
Δt_{pd}	= 1 ns
$t_{sk(o)}$	= ns
Transit time via the bus t_{flight}(bus)	= 10 ns
Setup time for the receiver t_{setup}(rec)	= 2.6 ns
f_{max}	= 47.8 MHz

Central-synchronous clock distribution propagation delay time via the bus takes a large part of the available clock period. The propagation delay over the bus can be lower if the capacitive load is lower. For example, if only the transmitter and one receiver card are plugged into the bus and no additional modules are inserted, the maximum f_{max}(clk) must be put in the formula for a safe circuit design, i.e., assume that all slots are filled with cards.

3.3 Source-Synchronous Clock Distribution

To eliminate the signal propagation delay time on the bus, the solution illustrated in Figure 12 can be used. An additional line for the source-synchronous clock signal and other lines for the arbitration or transmission of the send/receive status are required. However, propagation delay time over the bus (t_{flight}) is eliminated from the calculation of the maximum clock frequency. Therefore, a significantly higher system speed is possible.

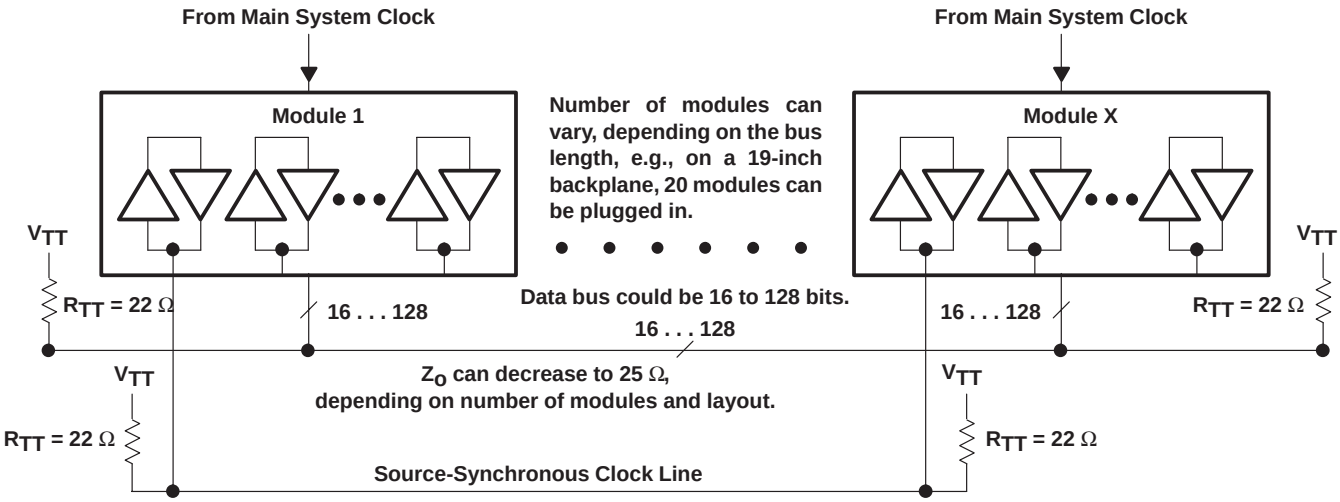


Figure 12. Principle of Source-Synchronous Clock Distribution

The times to be observed refer to two successive clock periods. The first clock period includes times that must be taken into account relative to the transmitter, while the second clock period includes critical times for the receiver. There are two requirements for the maximum clock speed:

$$f_{max}(clk) \leq \frac{1}{t_{sk}(clk) + t_{pd}(clk\ to\ B) + t_{sk(o)} + \Delta t_{pd}(sim.sw.transm.)} \quad (2)$$

$$f_{max}(clk) \leq \frac{1}{t_{hold}(rec) + t_{setup}(rec)} \quad (3)$$

The smaller value for f_{max} from equations 2 and 3 represents the highest possible frequency. Figure 13 shows this correlation graphically.

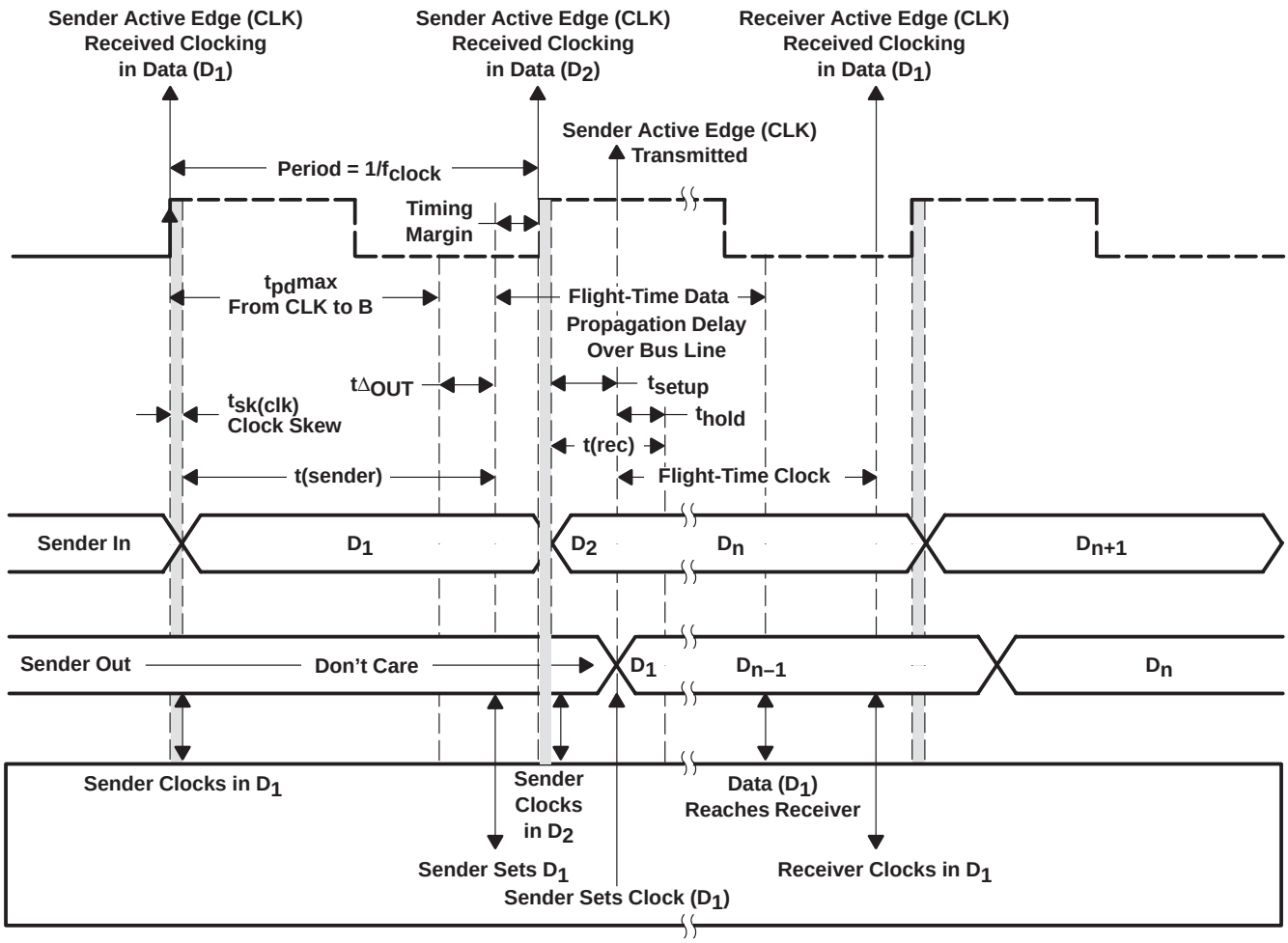


Figure 13. Time Budget for Source-Synchronous Clock Distribution

In this case, error-free synchronous data transfer that is independent of the propagation delay time over the line is possible (see Figure 14). The clock signal – with certain propagation to the data signal – is transferred via a separate clock line.

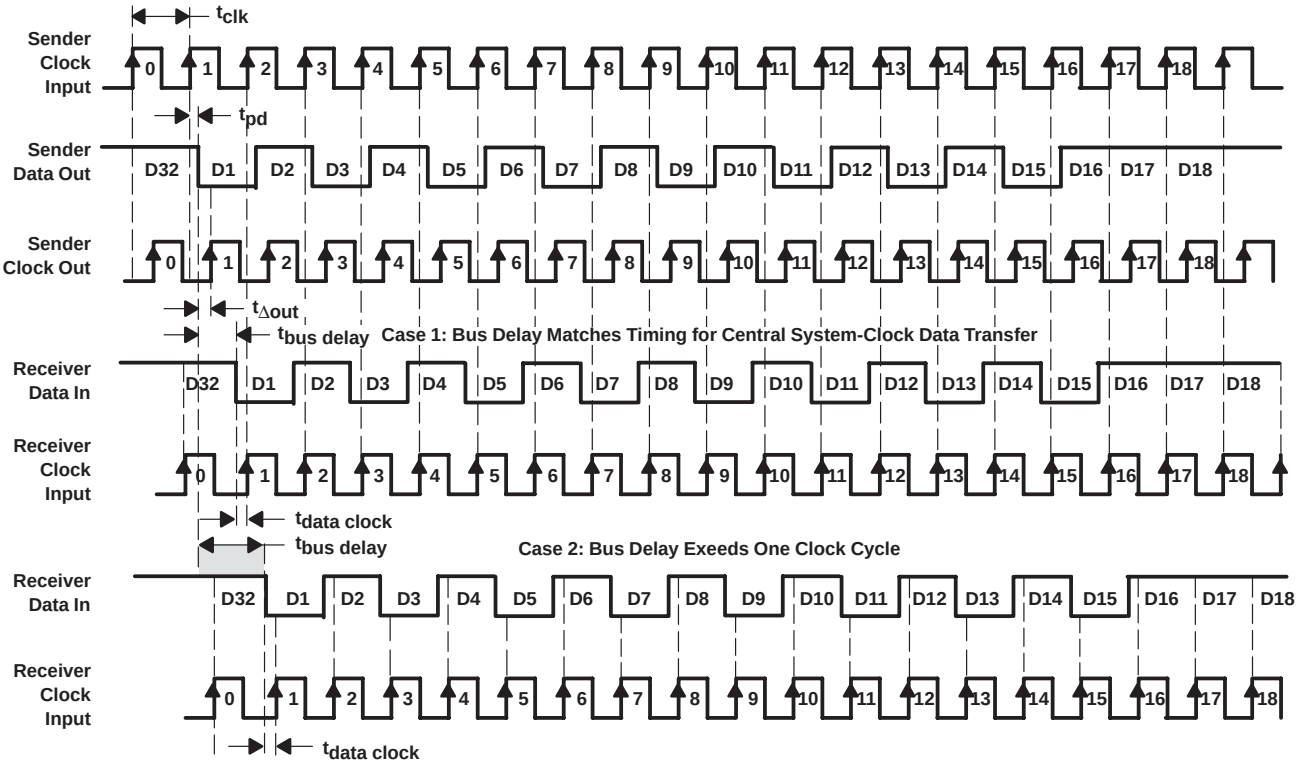


Figure 14. Two Examples of Source-Synchronous Clock Distribution

4 Measurements Using Texas Instruments GTLP Evaluation Module

Theoretical considerations concerning the two transmission modes discussed in the previous sections can be confirmed by measurements, using the GTLP demonstration backplane.

The evaluation module (EVM) (see Figure 15) is a good model for a typical parallel-backplane system as found, for example, in telecom applications.

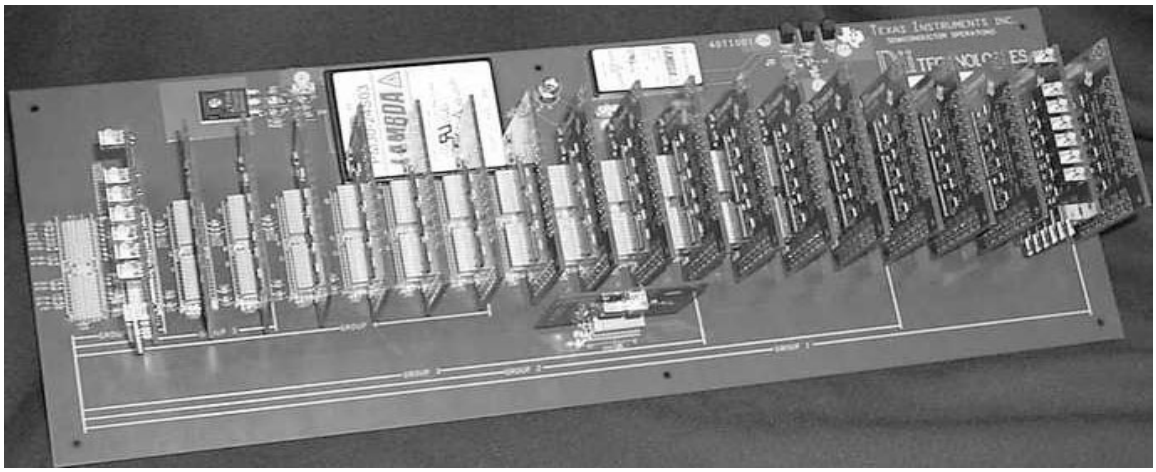


Figure 15. GTLP Demonstration Backplane

Altogether, 48 bits run in parallel over the 19-inch backplane, which has 20 slots, each 1 inch apart. The connectors are fully integrated onto the backplane, while the number of modules can vary. GTLPH1655 devices are used as the interface.

Different bus characteristics can be realized and shown using this EVM.

By using the EVM, it is possible to show the effect of termination resistances on signal quality, as well as different load conditions, due to a different number of modules on the bus. Also, the clock frequency is variable.

Figure 16 shows the layout of the driver card. Using a jumper, the transmitter can be switched from the system-synchronous clock mode to the source-synchronous clock mode.

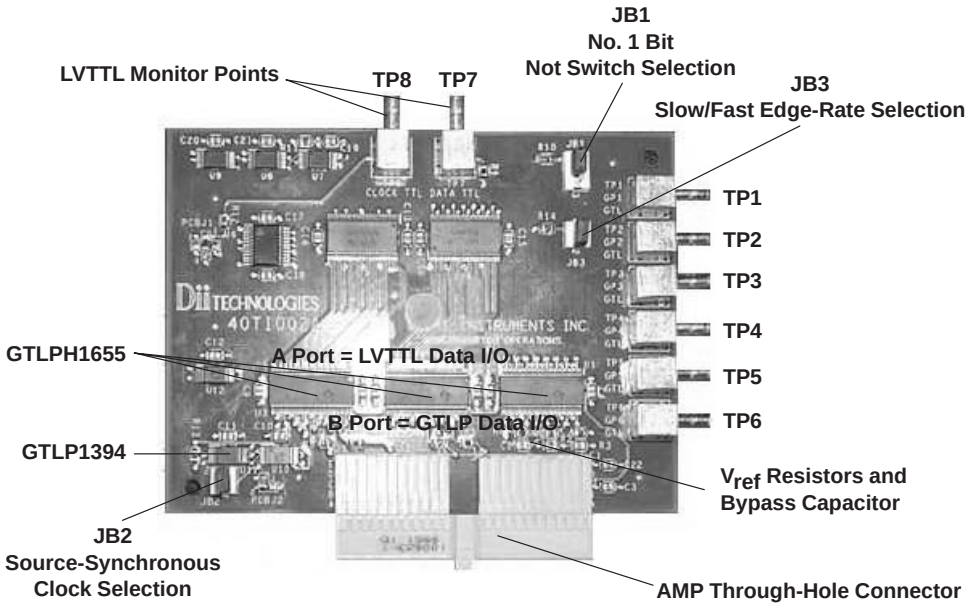


Figure 16. Layout of Driver Card With Monitor Points and Jumpers

Figure 17 shows a receiver card. The receiver card contains GTLPH1655 transceivers that receive data from the GTLP bus and translate it into LVTTL signals.

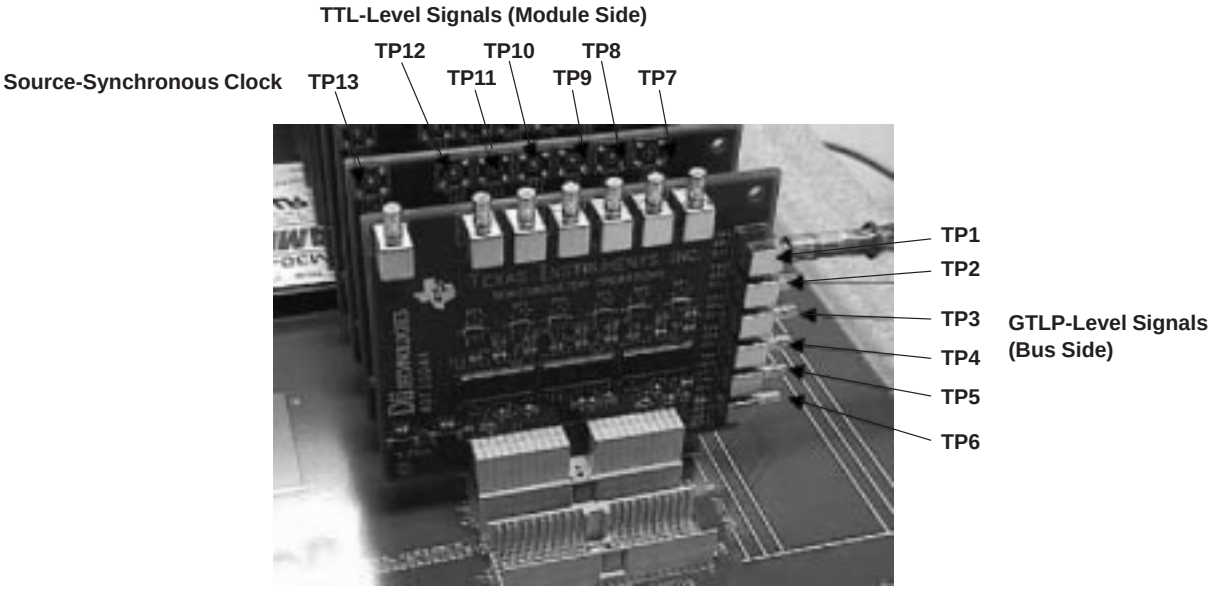


Figure 17. Receiver Card With Monitor Points

Using the receiver card, GTLP bus measurements (GTLP level) and module measurements (LVTTL level) are possible.

The EVM is used to illustrate the difference between system-synchronous data transfer and source-synchronous data transfer. The transmitter is at the beginning of the bus line, and the receiver is at the end of the bus. In both cases, 66 MHz is the clock speed, and gives a clock period of 15.15 ns.

4.1 Data Transfer With System-Synchronous Clock

The propagation time of the signal via the bus amounts to about 4 ns, if all other slots are empty. If the characteristics of the interface modules using GTLPH1655 devices are included, the worst-case scenario for the maximum clock speed is:

$$f_{max}(clk) = \frac{1}{0.5\ ns + 5.8\ ns + 1.1\ ns + 1\ ns + 4\ ns + 2.6\ ns} = \frac{1}{15\ ns} = 66.7\ MHz \quad (4)$$

With no load on the bus, timing already is critical at 66-MHz clock frequency because the timing margin is only 150 ps.

However, GTLPH1655 devices typically have less propagation time (about 3.5 ns compared with data-sheet value of 5.8 ns), thus, the critical frequency increases to about 78.7 Hz (see Figure 18).

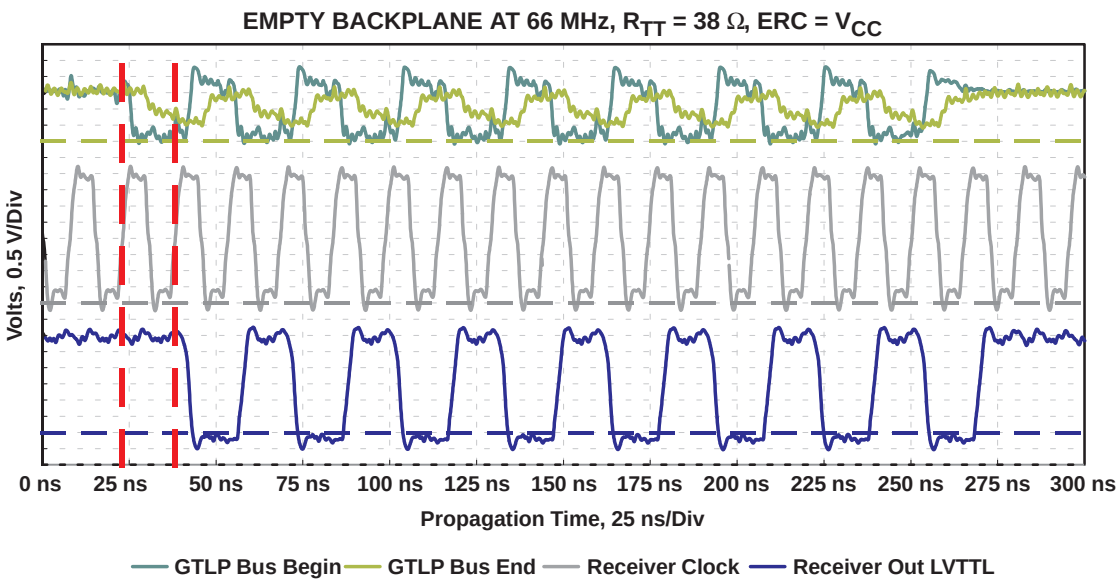


Figure 18. Empty Backplane Transmitter, CSSC in Slot 1, Receiver in Slot 20

However, if additional modules are inserted into the backplane, the capacitive load and, thus, the propagation delay time via the bus, increases significantly. In this case, the propagation delay time via the bus increases to about 10 ns. As a result, the maximum clock speed is significantly lower:

$$f_{max}(clk) = \frac{1}{0.5\ ns + 5.8\ ns + 1.1\ ns + 1\ ns + 10\ ns + 2.6\ ns} = \frac{1}{21\ ns} = 47.6\ MHz \quad (5)$$

Therefore, the required period in this case is 21 ns, increasing the chosen clock period from 66 MHz by 6 ns. The consequence is that not all modules receive the same data with the same clock edge. Some modules receive the data with the active edge of consecutive clock periods, as shown in Figure 19. With an empty backplane (see Figure 18), the data was transmitted with the next active edge of the clock signal at the receiver output. In this case, it takes one more clock period (see Figure 19).

In other words, the system no longer is working synchronously, and errors due to missing synchronicity can result.

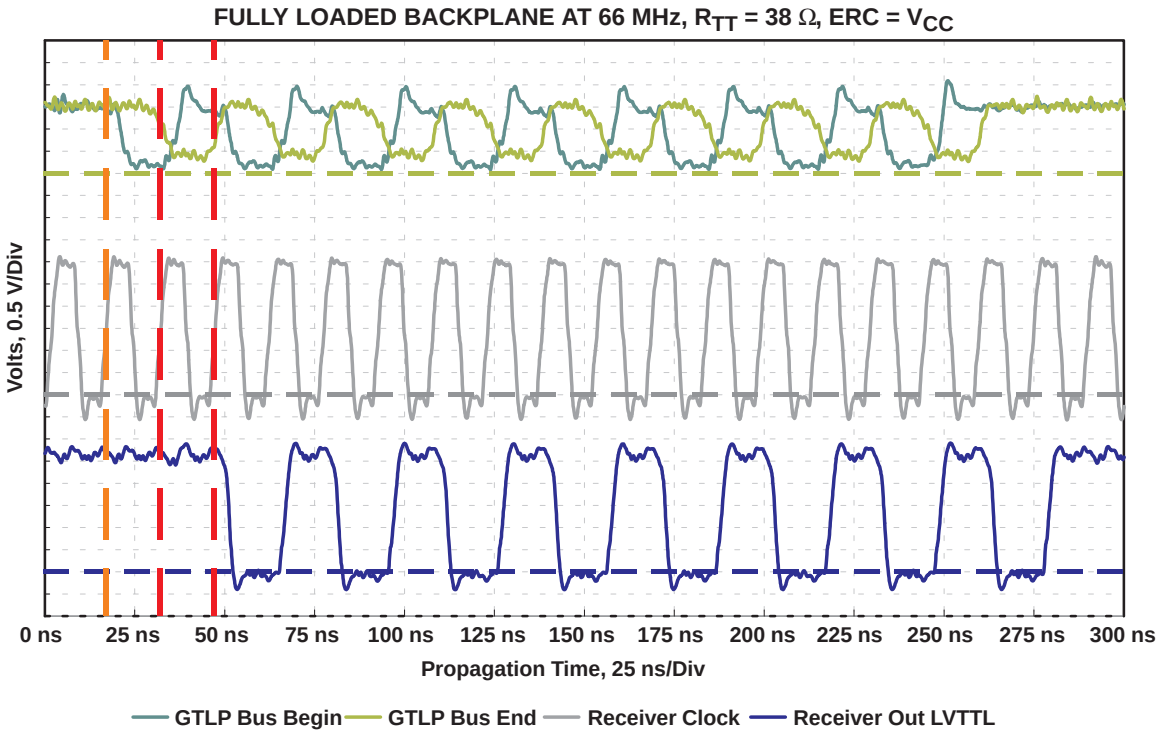


Figure 19. Empty Backplane Transmitter, CSSC in Slot 1, Receiver in Slot 20

4.2 Data Transfer With Source-Synchronous Clock

The sender is switched to source-synchronous clock mode by moving a jumper on the driver card. Comparing the signals on the empty backplane, there is little difference, as similar results are seen in the oscilloscope pictures (see Figure 16).

In the source-synchronous mode, the signal is within the same clock period (see Figure 20). The clock pulse no longer has any relation to the signal on the bus, because the clock pulse is measured at the receiver and, therefore, has a proper relation only to the TTL output signal.

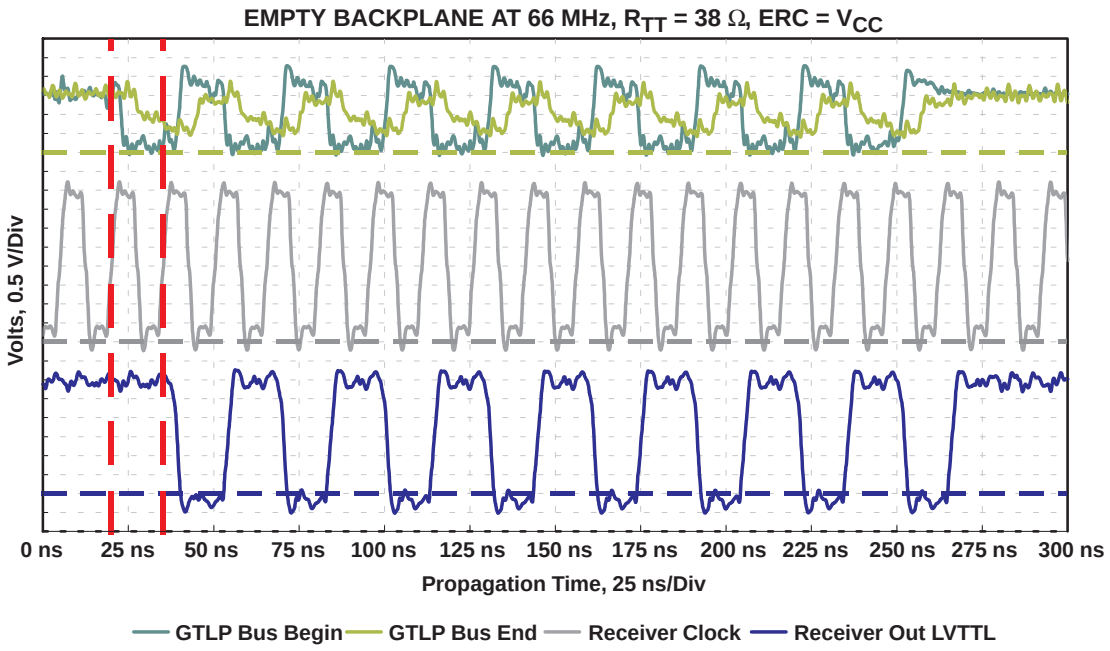


Figure 20. Signals on Empty Backplane, SSSC, Transmitter in Slot 1, Receiver in Slot 20

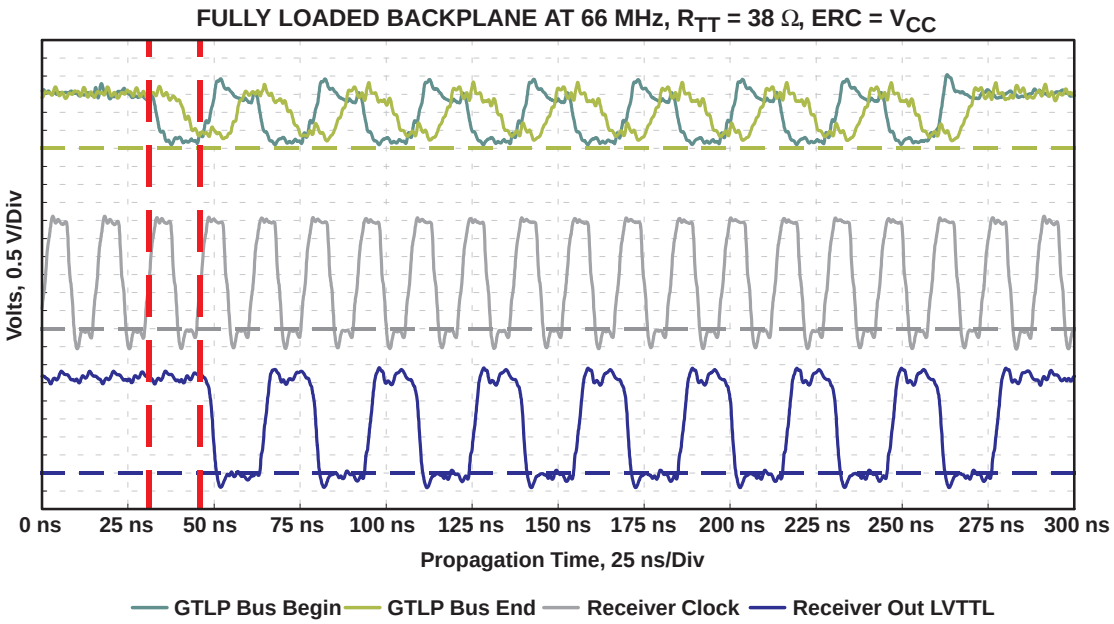


Figure 21. Fully Loaded Backplane, SSSC, Transmitter in Slot 1, Receiver in Slot 20

Even if the bus is fully loaded, a correct signal transfer can be observed. The only drawback is the need for an additional line in the bus layout. The clock signal always is transferred, with a small delay, to the present datum. The increase in propagation delay time via the bus, as a result of the additional input capacitance of the inserted modules, no longer is relevant.

The maximum frequency is calculated using data-sheet values, realistic approximations, and equation 2:

$$f_{max}(CLK) = \frac{1}{0.5\ ns + 5.8\ ns + 1.0 + 1\ ns} = \frac{1}{8.3\ ns} = 120.4\ MHz \qquad (6)$$

5 Summary

With the central-clock-distribution system, the highest possible system pulse rate is about 50 MHz (assuming a 19-inch backplane). With the source-synchronous system, the clock frequency can be increased by a factor of 2.4, to 120 MHz.

Table 2 lists three system solutions, along with relevant parameters that must be taken into account during system design.

Table 2. Comparison of Parallel Bus Systems With Different Pulse Supplies

PARAMETER	SYNCHRONOUS SYSTEM		ASYNCHRONOUS SYSTEM
	CENTRAL-CLOCK DISTRIBUTION	SOURCE-SYNCHRONOUS CLOCK DISTRIBUTION	NO SYSTEM CLOCK PULSE
Pulse skew	Output-to-output pulse driver (to be taken into account)	Output-to-output pulse driver (to be taken into account)	Not applicable
t_{pd} CLKAB	Device dependent (to be taken into account)	Device dependent (to be taken into account)	Not applicable
Δ Data – pulse	–/–	To be fixed	Not applicable
t_{pd} (sim.switch)	Package dependent (to be taken into account)	Package dependent (to be taken into account)	Package dependent (to be taken into account)
$t_{sk(o)}$	Device dependent (to be taken into account)	Device dependent (to be taken into account)	Device dependent (to be taken into account)
Bus propagation delay time	Bus dependent (to be taken into account)	0 ns Not applicable	Bus dependent (to be taken into account)
Setup time	Package dependent (to be taken into account)	0 ns Not applicable	Not applicable

For the central-system-clock solution, a central clock exists for all bus attendees. The maximum clock speed is about 50 MHz and provides a 32-bit data width and a data throughput rate of up to 1.6 Gbit/s. A significant limiting factor for the time budget is the transit time via the bus.

For a system with a source-synchronous system clock, the clock signal, with a slight shift in time to the data, is sent together with the data signal on the bus. The delay between data and clock is constant for all bus members. The maximum clock speed is about 120 MHz. The 32-bit data width results in 3.8 Gbit/s as the maximum data throughput. A significant limiting factor for the time budget in this setup is the propagation time, compared with the clock period.

A further option is asynchronous data transfer, in which an integrated system clock does not exist. All the bus drivers are in transparent mode, and switch the outputs according to their propagation time. Therefore, there is no common clock speed.

The asynchronous data frequencies can be 160 MHz, or more, depending on the technology. However, the effective maximum frequency is reduced significantly by additional requirements, such as the introduction of a bus protocol, which is indispensable in this system. The maximum frequencies that produce the theoretical data rate, which is based on 32 bits of up to 5.12 Gbit/s (at160 MHz), can be reached only for a short time, not continuously.

6 Glossary

BTL	Backplane transceiver logic
CMOS	Complementary symmetry metal-oxide semiconductor
CSSC	Central-synchronous system clock
DUT	Device under test
FB	FutureBus (device identifier for backplane transceiver logic devices)
GND	Ground
GTLP	Gunning transceiver logic plus
I/O	Input/output
LVTTL	Low-voltage transistor-transistor logic with 3.3-V supply, compatible with TTL
PCB	Printed circuit board
Slew rate	Slew rate, which is derived using the following equation: slew rate = $\Delta V/\Delta t = (0.8\ V_{OH} - V_{OL})/t_{r,f}$
SSSC	Source-synchronous system clock
TTL	Transistor-transistor logic
t_{pd}	Propagation delay time
t_f	Time to transit from logical high to logical low, measured between the 90% and 10% values of the steady logical-high level
t_r	Time to transit from logical low to logical high, measured between the 10% and 90% values of the steady logical-high level
Transceiver	Trans(mitter) (re)ceiver, bidirectional device
V_{CC}	Supply voltage

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SCEA017 - April 2001

GTLP in BTL Applications

Steve Blozis
Standard Linear & Logic

ABSTRACT

This application report addresses the issues a designer might face when using a GTLP device in a BTL/FB+ application when a legacy BTL/FB+ bus implementation is still in use. Key BTL/FB+ and GTLP device characteristics are compared, and additional GTLP value-added features are discussed.

To demonstrate that GTLP devices can be used in BTL/FB+ applications, the reference voltage (V_{REF}) and termination voltage (V_{TT}) were modified to BTL/FB+ specifications in TI's 20-slot GTLP EVM and waveforms showing system performance are presented. The experiment has shown GTLP technology is suitable for BTL/FB+ applications if maximum output-current ratings are observed.

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Introduction

In the past, the standard solutions for driving bus lines of backplane systems were transistor-transistor logic (TTL) or 5-V CMOS logic circuits. However, some issues resulted from the large 3.3-V or 5-V voltage swing, such as low system frequency performance and noise generated when the outputs switch simultaneously.

An open-collector backplane transceiver logic (BTL) bus with a reduced output voltage swing (<1V) that mitigates these concerns was introduced in the FutureBus Plus (FB+) family of devices. The falling edge is generated actively by the open-collector driver, and the rising edge is generated by a passive pullup network. A pullup network, with the termination resistance matching the loaded bus line impedance, provides optimum signal integrity and incident-wave switching.

Many BTL/FB+ backplanes are in operation. Engineers looking to the future see open-drain Gunning transceiver logic plus (GTLP) devices as a lower-power, higher-frequency migration path. However, their investment in the existing BTL backplanes and cards must be maintained for at least several more years.

This application report discusses how GTLP devices can be substituted for FB+ devices and operated at BTL signal levels until all the cards have been converted to GTLP, or until the higher system frequencies available from GTLP are needed for increased data throughput. Then, the entire BTL system can be converted easily to GTLP signal levels simply by changing the reference voltage and reducing the backplane termination voltage.

Background

FB+ devices are 5-V V_{CC} BiCMOS translators that operate between TTL logic levels on the card and BTL signal levels on the backplane. The backplane signals are generated by an open collector and a termination network (see Figure 1). The saturation voltage of the pulldown transistor and the forward voltage of the serially connected diode generate the output low-level voltage of 1.1 V. The high level of 2.1 V comes from the termination resistor (R_{TT}) connected to the termination voltage of 2.1 V. R_{TT} should equal the loaded-bus line impedance (Z), but the effective dc resistance, as seen by the driver in a typical double-terminated backplane, is R_{TT} in parallel with R_{TT} or one-half R_{TT}. Matching R_{TT} with Z ensures incident-wave switching and improves signal integrity. FB+ devices can handle a current (I_{OL}) up to 100 mA, which equals a R_{TT} of 20 Ω or an effective line impedance of 10 Ω ($R = (V_{OH} – V_{OL})/I_{OL}$). For safe detection of logic levels, the inputs are designed with differential amplifiers and a fixed threshold at 1.55 V ± 75 mV, exactly in the middle of the voltage swing. FB+ logical-layer specification is, according to IEEE Std 1194.1-1991 (BTL) and IEEE Std 896-1991 (FB+), describing node management, live insertion, and profiles. However, the physical layer can be used stand-alone, without the logical layer.

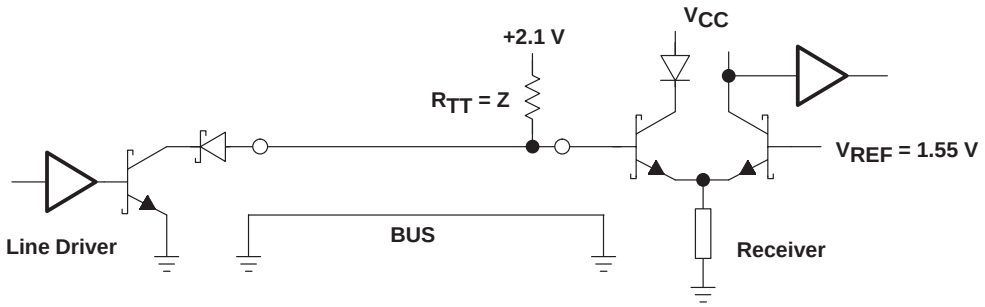


Figure 1. Open-Collector Bus System Using BTL/FB+ Devices

The basic concept of the Gunning transceiver logic (GTL) bus (see Figure 2) is identical to the BTL system, but in a CMOS technology and at a lower voltage level. Because of the missing diode in the open-drain outputs, the low level is 0.4 V. With a high level of 1.2 V, the voltage swing is reduced to only 0.8 V. The threshold is set in the middle of the voltage swing at 0.8 V by the variable V_{REF} input. With a drive capability of 40 mA, GTL devices can drive an effective resistance of around 0.8 V/40 mA = 20 Ω, or a termination resistor R_{TT} of 40 Ω in a double-terminated backplane. As a result of the 0.4-V V_{OL} level and the 40-mA I_{OL} current drive, the maximum output dc power dissipation of one output is 16 mW. These low-power drivers are typically integrated into ASICs for point-to-point applications, and normally are not used in heavily loaded multipoint applications.

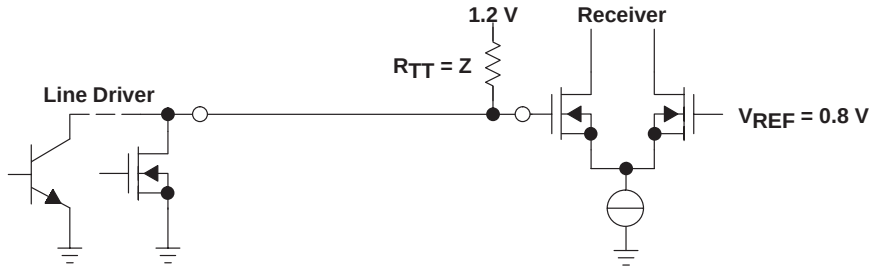


Figure 2. Open-Drain Bus System Using GTL Devices

The GTLP family combines the high-drive benefits of the BTL family, with the reduced power consumption of the GTL family. GTLP specifically is designed and optimized for heavily loaded multipoint backplane applications with a slow, controlled, backplane edge rate, and includes features needed for live insertion and withdrawal.

GTL and GTLP devices support two different signal-level specifications: GTL (JEDEC Standard JESD 8-3) and GTL+ signal levels first used by Intel™ in their Pentium™ processors. GTL voltage swing is from 0.4 V to 1.2 V, with the threshold in the middle of the voltage swing at 0.8 V. GTL+ voltage swing is from 0.55 V to 1.5 V, with the threshold at 1.0 V. GTLP devices, which are optimized for backplane applications and are designated with the SN74GTLP prefix, are optimized for the higher noise-margin GTL+ signal levels to indicate they have a slower slew rate with improved output-edge control, and to differentiate them from point-to-point GTL+-optimized devices.

Both FB+ and GTLP devices are commonly used in multiple-bit, multipoint double-terminated parallel backplanes (see Figure 3). The device turns on to pull the signal low and turns off to allow the termination resistors to pull the signal high, up to the termination voltage. The benefit of this open-collector/open-drain technology is that the output either is sinking current or is in the high-impedance state (3-state), but never sources current. This reduces the power consumption over typical Thevenin or ac terminations. Other benefits include the ability to pick a termination-resistor value that matches the loaded backplane impedance (Z), ensuring incident-wave switching/optimum signal integrity, and no destructive bus-contention issues if multiple devices are on at the same time, which also facilitates a wired-OR arrangement. The loaded backplane impedance, Z, always is lower than the natural bus line impedance (Z_O) and varies from system to system, depending on stub length, slot pitch, device C_{io}, and type of connectors. Surface-mount ceramic-bypass capacitors (0.82 nF) should be connected between V_{TT} and GND on every fourth data bit, to minimize current fluctuations.

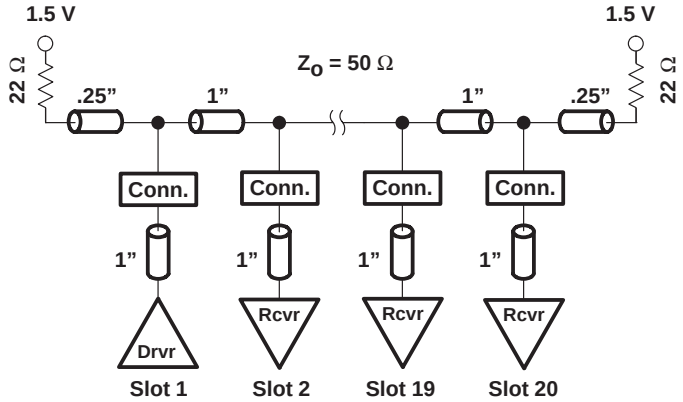


Figure 3. Typical Backplane Physical Representation

FB+ and GTLP Characteristics Comparison

Table 1 compares the FB2033A with the high-drive GTLP2033 device, which is soon to be released. Each characteristic is discussed in general and then in detail if the difference is material to the use of GTLP devices in BTL/FB+ applications. Values of C_{io}, I_{CC}, and t_{pd} are design goals and are subject to change.

Table 1. FB+ and GTLP 8-Bit Registered Transceiver Characteristics Comparison

	CHARACTERISTIC	FB+	GTLP
A-port/daughter card	Logic levels	TTL	LVTTL
	Transistors type – input/output	CMOS/bipolar	CMOS/CMOS
	Drive levels	–32/55 mA	±24 ma
	Bus hold	None	None
	I_{off} and PU3S to support hot insertion	Yes	Yes
B-port/backplane	Signal levels	BTL	GTLP
	Input – differential	±75 mV around fixed threshold of 1.55 V	±50 mV around variable threshold of 1.0 V
	Transistor type – output	Bipolar open collector	CMOS open drain
	Drive levels	100 mA @ 1.1 V	100 mA @ 0.55 V
	Input/output capacitance (C_{io} – max)	6 pF	10.5 pF
	Slew rate – typical rise/fall	0.39/0.33 V/ns	0.5/0.43 V/ns
	I_{off}/PU3S and BIAS V_{CC} to support live insertion	Yes, 1.62 V to 2.1 V	Yes, 0.95 V to 1.05 V
Device	V_{CC}	5 V	3.3 V
	Technology	0.8-µ BiCMOS	0.65-µ CMOS
	I_{CC}	120 mA	40 mA
	Power consumption	100 mW	50 mW
	Transparent mode – maximum propagation delay (GTLP ERC slow or fast for higher/lower values)	A to B 4.6 ns B to A 5.6 ns	A to B 7.7 or 6.3 ns B to A 5.5 ns
	Logic functions	Many – both are exactly the same.	
	ESD	HBM – 2000 V MM – 200 V CDM – 1000 V	HBM – 2000 V MM – 200 V CDM – 1000 V
	Temperature range	0°C to 70°C	–40°C to 85°C
	Package offerings	52-pin TQFP	48-pin TSSOP, TVSOP, or VFBGA
	IEEE Std 1149.1 JTAG	No pins assigned	No pins assigned

A-Port/Daughter-Card Side of the Device

- Logic levels – The logic levels are compatible because the threshold, V_{IH}, V_{OH}, and V_{IL} logic levels are the same. GTLP is 5-V tolerant.
- Transistor types and drive levels – They are not significantly different. Most applications do not require the higher drive and work well with the balanced drive of ±24 mA. Also, GTLP is offered with a series-damping-resistor (SDR) option that reduces the drive to ±12 mA, and provides better signal integrity into smaller lumped loads.
- Bus hold – Neither device has the bus-hold feature. The A port of most GTLP devices that do not feature the split 3-wire A port is featured with bus hold.
- Hot insertion – Both families support hot insertion with the I_{off} and power-up 3-state (PU3S) features.

B-Port/Backplane Side of the Device

- Signal levels – Signal levels are not compatible (see Figure 4). The level of noise margin is about the same; only the input thresholds of operation are different. As discussed in the following paragraphs, GTLP devices can operate at BTL signal levels by changing V_{REF} to 1.55 V and raising V_{TT} to 2.1 V.

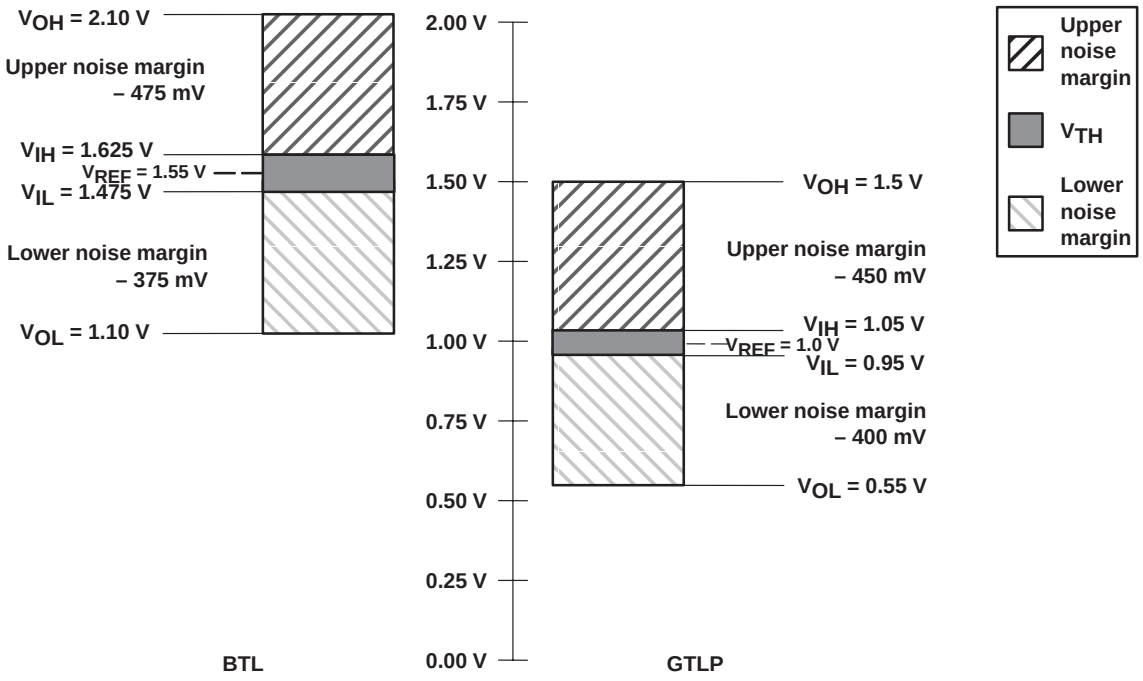


Figure 4. BTL and GTLP Signal-Level Comparison

- Differential input – FB+ devices have a fixed differential input set at 1.55 V, whereas GTLP devices have a variable differential input that is set via the external V_{REF} control pin. Normally, V_{REF} is two-thirds of V_{TT} so that, when V_{TT} is 1.5 V, V_{REF} is 1.0 V. As shown in Figure 5, the GTLP reference level is set by this simple R/2R resistor network, with R typically being a one-fourth-watt resistor in the range of 1 kΩ ± 1%. The advantage of this external V_{REF} and R/2R network is that it maintains the upper and lower noise margin if V_{TT} fluctuates. The maximum input V_{REF} current to a GTLP device is 10 μA. A 0.1-μF to 0.01-μF bypass capacitor should be located as close to the V_{REF} pin as possible to stabilize the voltage.

  When GTLP is used in BTL applications, the resistor network simply is changed to R/3R so that V_{REF} is set at 1.575 V when V_{TT} is changed to 2.1 V. When the card is converted from BTL to GTLP signal levels, simply change the 3R resistor to 2R, and the proper reference voltage is set when V_{TT} is reduced from 2.1 V to 1.5 V.

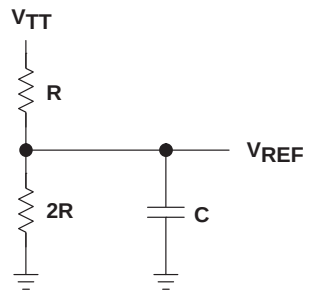


Figure 5. GTLP V_{REF} Resistor Network

- Transistor type – FB+ and GTLP operate the same using only a pulldown transistor on the output, with FB+ bipolar transistors being called open collector and GTLP CMOS transistors being called open drain.
- Drive levels – The drive or current-sinking capability is the same and is 100 mA, to allow termination-resistor R_{TT} values down to 22 Ω (effective termination resistance of 11 Ω) if the voltage swing is limited to 1 V. In actual applications, the GTLP V_{OL} is lower, and higher R_{TT} values are required to avoid exceeding the recommended I_{OL}.
- Input/output capacitance (C_{io} maximum) – The FB+ decoupling diode reduces the maximum output capacitance to about 6 pF. Increased output capacitance of 10.5 pF (8.5 pF typical) is seen in GTLP devices, compared to FB+ devices. This is directly attributable to the GTLP CMOS process, which requires larger-area output structures compared to bipolar output structures used on FB+ devices. This increase in capacitance reduces the loaded-bus line impedance that can be compensated for by lowering R_{TT}. The higher loading reduces t_{pd} and increases the time of flight.
- Live insertion – Both support live insertion through the use of I_{off}, PU3S, and BIAS V_{CC} circuitry. BIAS V_{CC} circuitry precharges the outputs to mid-swing levels to prevent glitching active data on the backplane when cards are inserted or removed, and is disabled when V_{CC} is connected. FB+ BIAS V_{CC} output is fixed at 1.62 V to 2.1 V, whereas the GTLP device BIAS V_{CC} output is fixed at 0.95 V to 1.05 V. If GTLP devices are used at BTL signal levels, the precharge is below the threshold level and may not be as effective in preventing data glitches. However, in the GTLP EVM (a specially designed backplane for customer use), no glitching was noted when GTLP devices were operated at BTL levels.

Device Characteristics

- V_{CC} – FB+ uses 5-V V_{CC}, whereas GTLP uses 3.3-V V_{CC}. The lower V_{CC} is more compatible with newer, higher-performance devices being used in current and future board designs.
- Technology – FB+ uses an older 0.8-μ bipolar process, whereas GTLP uses a newer 0.65-μ CMOS process that has the main advantage of lower power consumption.
- I_{CC} – I_{CC} is the amount of current used by the device and is a factor in computing power consumption. CMOS construction reduces GTLP device I_{CC} to about one-third of FB+ levels.
- Power consumption – Several factors influence power consumption: V_{CC}, I_{CC}, frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance. GTLP power consumption and overall heat dissipated is about one-half of FB+ levels.
- Propagation delay – The A-to-B and B-to-A propagation delays are larger in the GTLP devices due to the slower edge slew rate and the slower CMOS process. High-drive GTLP devices have the option of a smaller t_{pd} by increasing the slew rate through the use of the edge-rate-control (ERC) circuitry. The ERC pin controls slew rate.
- Logic functions – GTLP devices are available in several different functions and package options (see Table 2). FB+ is available in several different functions (see Table 3).
  - Most FB+ devices have split input (AI) and output (AO) buses on the A port, something only the GTLP1394, GTLP1395, and GTLP2033/34 in the GTLP family have. Please contact the GTLP team at gtlp@list.ti.com if you would like a GTLP replacement for your existing FB+ application.
  - The FB1650 emulates the FB2031 and the FB2040.
  - The FB2033A is slightly faster than the FB2033K (custom device released to the general market).

Table 2. High-Drive GTLP Functions

DEVICE	AVAILABILITY	FUNCTION	PINS	PACKAGE
SN74GTLP1394	Now	2-bit bus transceiver with split LVTTL port and feedback path	16	SOIC, TSSOP, and TVSOP
SN74GTLPH1612	Soon	18-bit universal bus transceiver	64	TSSOP
SN74GTLPH1616	Soon	17-bit universal bus transceiver with buffered clock	64	TSSOP
SN74GTLPH1645	Soon	16-bit bus transceiver	56	TSSOP, TVSOP, and VFBGA
SN74GTLPH1655	Soon	16-bit bus transceiver	64	TSSOP
SN74GTLP1395	Soon	2-bit bus transceiver with split LVTTL port and feedback path	20	SOIC, TSSOP, TVSOP, and VFBGA
SN74GTLP21395	Soon	2-bit bus transceiver with split LVTTL port and feedback path	20	SOIC, TSSOP, TVSOP, and VFBGA
SN74GTLP2033	Soon	8-bit inverted registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP22033	Soon	8-bit inverted registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP2034	Soon	8-bit registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLP22034	Soon	8-bit registered bus transceiver with split LVTTL port and feedback path	48	TSSOP, TVSOP, and VFBGA
SN74GTLPH1627	Soon	18-bit bus transceiver with synchronous clock outputs	64	TSSOP

Table 3. FB+ Functions

DEVICE	FUNCTION	PINS	PACKAGE
SN74FB1650	18-bit universal storage transceiver with split TTL I/O	100	PCA
SN74FB1651	17-bit universal storage transceiver with delayed buffered clock with split TTL I/O	100	PCA
SN74FB1653	17-bit universal storage transceiver with delayed buffered clock with split LVTTL I/O (3.3-V and 5-V V_{CC})	100	PCA
SN74FB2031	9-bit address/data transceiver with clock and latch	52	RC
SN74FB2032	9-bit arbitration contest competition transceiver	52	RC
SN74FB2033A	8-bit registered transceiver with split TTL I/O	52	RC
SN74FB2033K	8-bit registered transceiver with split TTL I/O	52	RC
SN74FB2040	8-bit status/sync transceiver with split TTL I/O	52	RC
SN74FB2041A	7-bit transceiver with split TTL I/O	52	RC

- ESD – Both FB+ and GTLP meet the minimum electrostatic discharge (ESD) standards in human-body model (HBM), 2000 V; machine model (MM), 200 V; and charged-device model (CDM), 1000 V. During testing, the GTLP devices pass 4000-V HBM and 3000-V CDM.
- Temperature ranges – FB+ is offered in commercial (0°C to 70°C) and military (–55°C to 125°C) temperature ranges, with some of the newer devices also ac specified for the industrial (–40°C to 85°C) temperature range. GTLP is offered in industrial (–40°C to 85°C) and select devices will be offered in the military (–55°C to 125°C) temperature ranges. Please contact the GTLP team at gtlp@list.ti.com for additional information on the devices in the military temperature range.
- Package offerings – FB+ devices are packaged in older technology, larger, more expensive thin quad flatpack packages that include a thermal heat sink in the 100-pin packages to help dissipate the heat generated by the bipolar outputs. GTLP devices are packaged in modern packages, including the often-requested TSSOP package and, where possible, in the smaller TVSOP packages. Select GTLP devices also are offered in the new very fine-pitch ball grid array (VFBGA) and the dual-die, low-profile, fine-pitch ball grid array (LFBGA) package.
- IEEE Std 1149.1 JTAG – Most FB+ devices have JTAG TAP pins assigned, but no devices with JTAG features have been released. The GTLP team is evaluating JTAG functionality in GTLP devices in VFBGA/LFBGA packages, and solicits your input on the desirability of this feature.
- Price – Comparing suggested resale pricing, the FB2033 is about 85% higher than the GTLP2033. There are similar price differentials for other devices in both families.

Advanced Features of GTLP Devices Not Incorporated in FB+ Devices

- OEC™ circuitry – The low-to-high transition output edge-control circuitry has been improved significantly. The slew rate has been held to about 0.5 V/ns on the rising edge and helps prevent ringing on heavily loaded backplanes, allowing a much higher maximum frequency.
- TI-OPC™ circuitry – GTLP devices feature overshoot-protection circuitry that actively ports backplane energy to GND when the signal level is greater than 0.7 V to 0.8 V above V_{REF}. This prevents large overshoots on improperly terminated or unevenly loaded backplanes during low-to-high signal transition, which limits the subsequent undershoot that would reduce the upper noise margin.
- Edge-rate control (ERC) – This feature allows designers to select either a slow-rising-edge slew rate (about 0.4 V/ns) or a slightly faster slew rate (about 0.45 V/ns). The faster slew rate reduces the maximum propagation delay, allowing a higher system frequency. The maximum frequency with a slow ERC is about 87 MHz, while a fast ERC is about 125 MHz. In BTL applications, the slow ERC should be selected by applying the correct logic level to the external ERC control pin as shown in Table 4. $\overline{ERC}$ is the inverse of ERC and is implemented on some GTLP devices where the control pin replaced a GND pin in the comparable medium-drive GTLP device.

Table 4. B-Port Edge-Rate Control

LOGIC LEVEL		B-PORT OUTPUT EDGE RATE
ERC	$\overline{ERC}$	
H	L	Slow
L	H	Fast

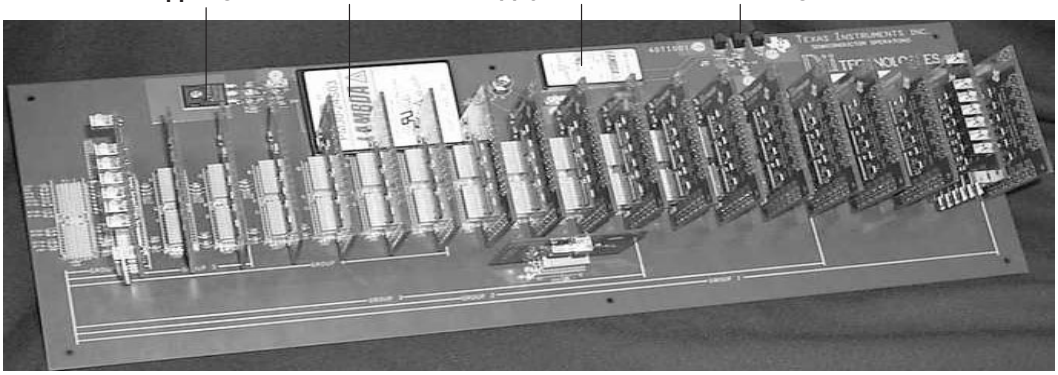
GTLP Data-Sheet Changes Required for BTL/FB+ Applications

Analysis of high-drive GTLP TI-SPICE model data of GTLP and BTL signal levels shows little change in dc specifications, timing requirements, and switching characteristics. This is because the GTLP device always is operated from 3.3-V V_{CC}, even if the B-port output voltage is pulled to 2.1 V. Overall voltage swing is about 0.6 V larger than normal GTLP voltage swings when operated at BTL signal levels.

GTLP Waveforms in BTL Backplane

The GTLP evaluation module (EVM) backplane (see Figure 6) was designed and manufactured to allow factory-trained GTLP Product Marketing Engineers worldwide to have a tool to showcase the GTLP family of products, and to demonstrate how loading and termination affect signal integrity. Currently, there are units in China, Germany, Japan, Korea, and the United States. Demonstrations can be scheduled by contacting your local Texas Instruments Technical Sales Representative or the GTLP team at gtlp@list.ti.com.

1.5-V V_{TT} Regulator **3.3 V – Power Supply – 5 V** **Power-Status Lights**



– Used to investigate how length/board spacing/driver position affects signal integrity
– 48 bits broken into 8-bit widths at increments of 2, 4, 8, 12, 16, and 20 slots
– One bit for source-synchronous clock option
– Clock-frequency options of 23, 50, 66, 75, 87, and 100 MHz
– Termination-resistor options of 25, 33, 38, and 50 Ω in 20-slot length (Group 1)

Figure 6. GTLP EVM Backplane

As shown in Figure 7, the high-drive SN74GTLPH1655DGGR is used on the driver and receiver cards. There is a removable termination card at either end of the backplane to allow performance with different values of R_{TT} to be examined. Two cards (driver and receiver) were modified to operate at BTL signal levels by changing the R/2R V_{REF} resistor network to R/3R. V_{TT} for the entire backplane was changed from 1.5 V to 2.1 V by changing the resistor in the 1.5-V V_{TT} regulator that sets the output voltage.

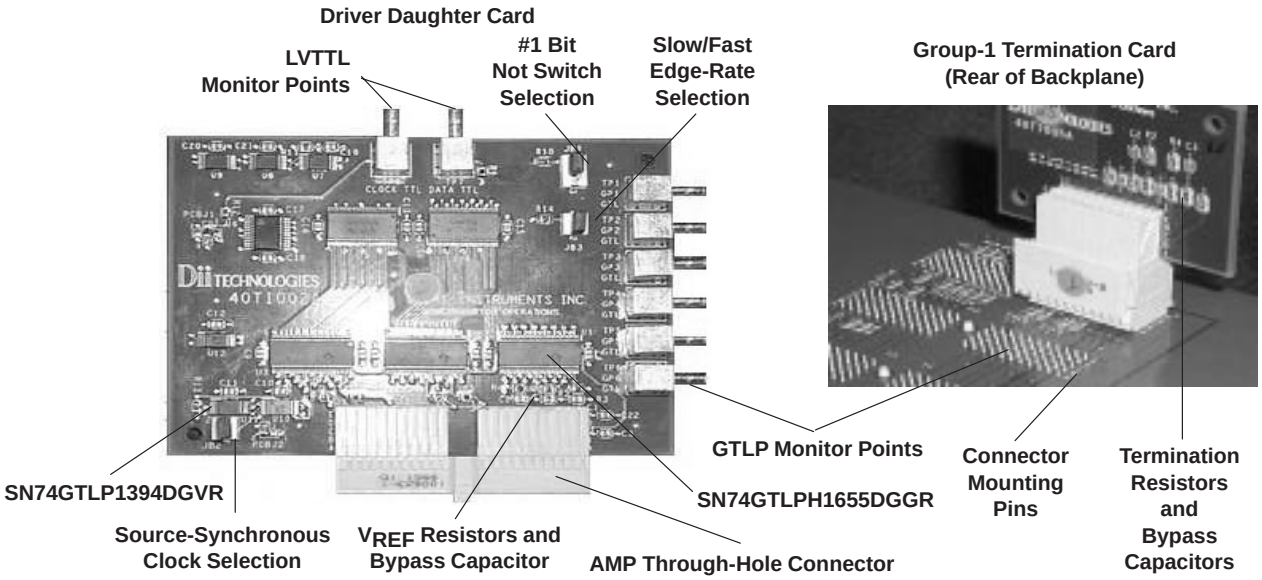
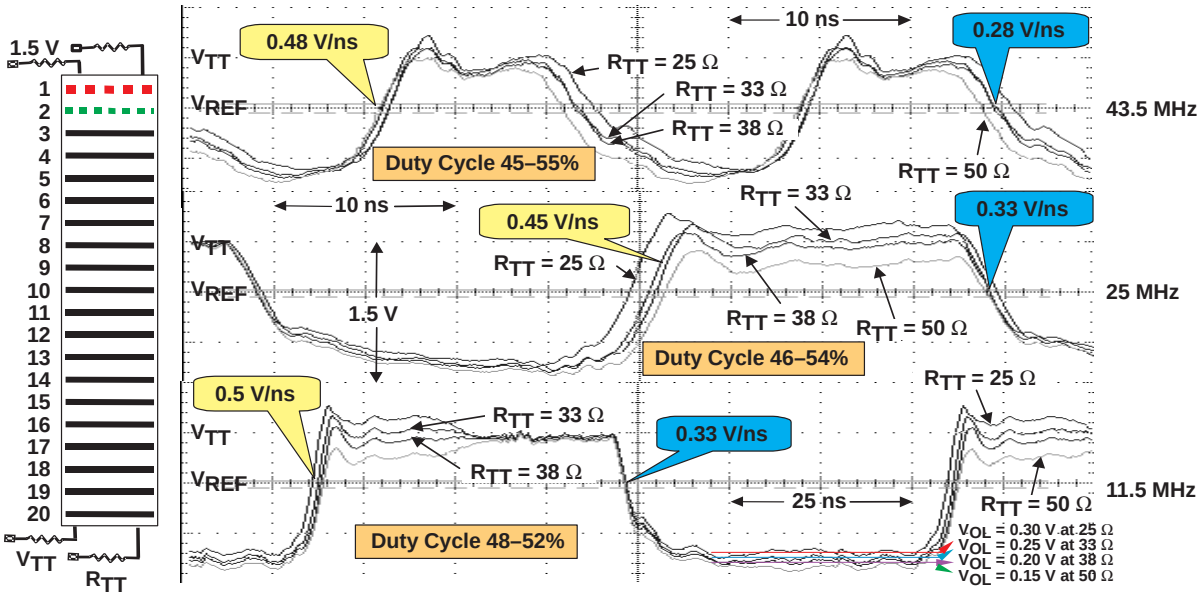


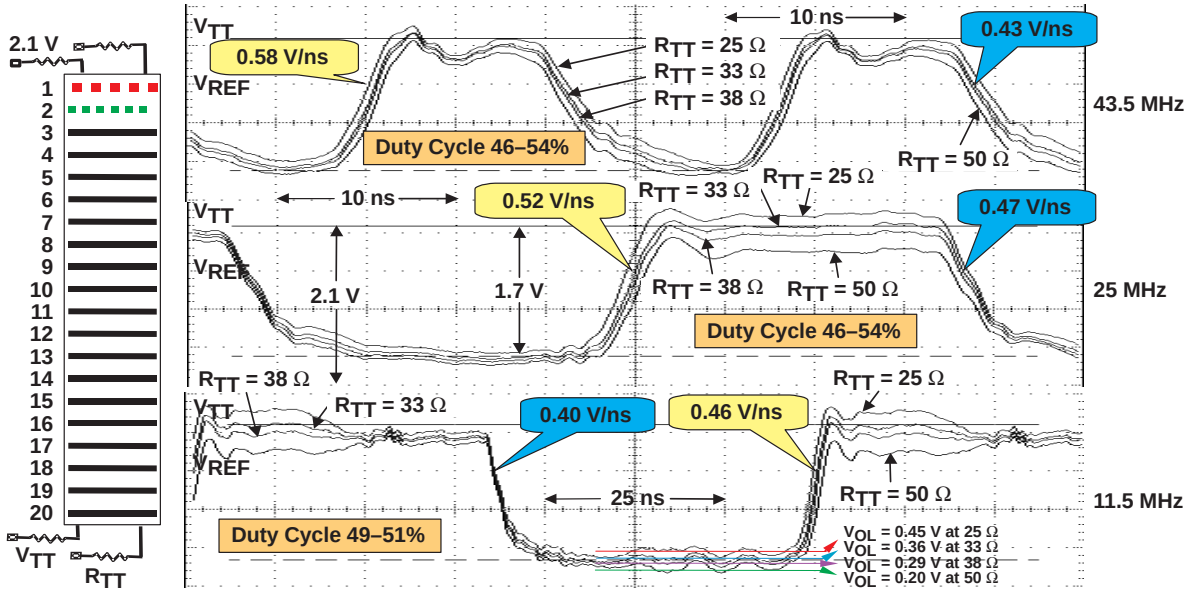
Figure 7. GTLP EVM Driver and Termination Cards

Waveforms using the GTLPH1655 device at both normal GTLP signal levels and BTL signal levels in the fully loaded 17.9-in.-long, 20-slot backplane at various terminations and frequencies are shown in Figures 8 and 9. The GTLP2033 has the same B-port outputs as the GTLPH1655 and other high-drive GTLP devices, so performance is similar. The actual data frequency of the waveform is shown, and is one-half the actual clock frequency. Waveforms were taken at the backplane connector pin. The performance of the GTLP device is excellent at both signal levels. An R_{TT} of 33 Ω most closely matches the loaded-bus line impedance as seen by the well-behaved incident wave. Other high-drive GTLP devices are expected to operate in a similar manner at BTL signal levels.



Fully Loaded Backplane (Driver in Slot 1, Receiver in Slot 2)
SN74GTLPH1655DGGR With Edge-Rate Control in Slow

Figure 8. GTLPH1655 Waveforms at GTLP Signal Levels (Group 1, Bit 1)



Fully Loaded Backplane (Driver in Slot 1, Receiver in Slot 2)
SN74GTLPH1655DGGR With Edge-Rate Control in Slow

Figure 9. GTLPH1655 Waveforms at BTL Signal Levels (Group 1, Bit 1)

Table 5 compares slew rates and duty cycles for Figures 8 and 9. The slew rates and duty cycles were measured at the optimum termination, which is 33 Ω.

Table 5. Waveform Slew Rate and Duty Cycle

LEVEL	MONITOR POINT	DATA FREQUENCY (MHz)	L-H SLEW RATE (V/ns)	H-L SLEW RATE (V/ns)	DUTY CYCLE (%)
GTLP	G1 B1	11.5	0.5	0.33	48–52
GTLP	G1 B1	25	0.45	0.33	46–54
GTLP	G1 B1	43.5	0.48	0.28	45–55
BTL	G1 B1	11.5	0.46	0.40	46–54
BTL	G1 B1	25	0.52	0.47	46–54
BTL	G1 B1	43.5	0.58	0.43	46–54

In Figures 8 and 9, V_{OL} is lower than the specification levels of 0.55 V at GTLP levels and 1.1 V at BTL levels. This larger voltage swing can reduce the maximum possible frequency, increases EMI, and changes the lower end of possible R_{TT} values. Table 6 is a comparison of V_{OH} and V_{OL} at 11.5 MHz with the termination resistance. The I_{OL} was calculated based on $I_{OL} = 2 \times \Delta V/R_{TT}$. The GTLP data sheet lists a recommended maximum device I_{OL} at V_{OL} of 0.4 V and 0.55 V. The lowest termination-resistor value that is possible without exceeding these limits also is calculated, based on $R_{TT} = 2 \times \Delta V/I_{OL}$.

Table 6. V_{OH} and V_{OL} vs I_{OL}

LEVEL	MONITOR POINT	R_{TT} (Ω)	V_{OH} (V)	V_{OL} (V)	ΔV (V)	I_{OL} (mA)	MAXIMUM RECOMMENDED R_{TT} (Ω)	
							I_{OL} 66 mA AT 0.4 V	I_{OL} 100 mA AT 0.55 V
GTLP	G1 B1	25	1.46	0.30	1.16	93	35.2	23.2
GTLP	G1 B1	33	1.45	0.25	1.20	73	36.4	24.0
GTLP	G1 B1	38	1.43	0.20	1.23	65	37.3	24.6
GTLP	G1 B1	50	1.42	0.15	1.27	51	38.5	25.4
BTL	G1 B1	25	2.00	0.45	1.55	124	50.0	31.0
BTL	G1 B1	33	1.93	0.35	1.58	96	47.9	31.6
BTL	G1 B1	38	1.90	0.29	1.61	85	48.8	32.2
BTL	G1 B1	50	1.86	0.20	1.66	66	50.3	33.2

As R_{TT} is reduced, V_{OL} increases because the device has a finite capacity for pulling down the bus voltage. V_{OH} on the monitored bit is reduced at higher levels of R_{TT} because a larger share of V_{TT} is consumed in the fixed 255-Ω test-monitor-point bit resistor. Without this leakage path, which is not found on commercial backplanes, V_{OH} goes to V_{TT}, as shown on the unmonitored bit waveforms.

There are different levels of recommended I_{OL} for the GTLP device at 0.4 V and 0.55 V, because these are points on the voltage vs current (VI) curve that approximate best where the device will be operated. The absolute I_{OL} limit is twice the recommended limit. The device may catastrophically fail at the absolute limit, and the design life of 24,000 hours is degraded on an increasing curve as I_{OL} is operated at the recommended limit, except for brief (<2 ns) time periods where it can be operated at higher levels during ac switching. It is clear that, when using GTLP devices at BTL levels, proper termination must be traded off against natural line impedance without exceeding the maximum recommended I_{OL}.

Frequently Asked Questions

Q: Where can I get more information on GTLP devices?

A: Visit the GTLP internet home page at www.ti.com/sc/gtlp, or e-mail the GTLP team at gtlp@list.ti.com for additional information, data sheets, simulation models, and samples.

Conclusion

GTLP can be used on new BTL/FB+ cards with only a simple modification to the V_{REF} resistor network (R/2R to R/3R) and the shift of V_{TT} (1.5 V to 2.1 V) with limited performance degradation. GTLP allows maximum system frequencies at least comparable to FB+ devices (about 40-MHz clock), while providing advantages that include 3.3-V V_{CC} with 5-V tolerance, smaller TSSOP or BGA surface-mount packages, smaller 2-bit through larger 32-bit functions, lower power consumption, lower cost, and an easy migration path to higher system frequencies (up to 125 MHz) in the future, with a simple reversal of the V_{REF} network to R/2R and reduction of V_{TT} to 1.5 V.

The major disadvantages are that GTLP currently is not offered in exactly the same functionality/control or split A-port inputs and outputs as existing FB+ devices, the output capacitance (C_{io}) is larger, and R_{TT} and the natural bus line impedance must be selected so that the recommend I_{OL} is not exceeded.

The GTLP Team at Texas Instruments should be contacted if there is BTL/FB+ functionality that currently is not offered in the GTLP high-drive family.

Glossary

BiCMOS	Device technology that combines high drive of bipolar outputs with lower power consumption of CMOS inputs
Bipolar	Device technology that has high drive outputs, but has high power consumption
BTL	Backplane transistor logic, which operates at signal levels of V_{TT} = 2.1 V, V_{REF} = 1.55 V, and V_{OL} = 1.1 V
CMOS	Device technology that has balanced drive outputs and low power consumption
FB+	FutureBus Plus devices are designed to operate at BTL signal levels.
GTL	Gunning transceiver logic, which operates at signal levels of V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{OL} = 0.4 V
GTL+	A derivative of GTL that operates at higher-noise-margin signal levels of V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{OL} = 0.55 V and moves V_{REF} from the normal ground-bounce area
GTLP	Gunning transceiver logic plus, which normally is associated with optimized edge-rate devices that allow higher-frequency operation in heavily loaded backplane applications at GTL+ signal levels
R_{TT}	Bus line-termination resistance that should be equal to Z for incident-wave switching and optimum signal integrity
Z	Bus line loaded impedance, taking into account the natural impedance and capacitive loads
Z_o	Bus line natural impedance that is set by type of line construction and dimensions

Acknowledgment

The author of this application report is Steve Blozis, with technical assistance from Susan Curtis and Ernest Cox, and with technical review by Johannes Huchzermeier.

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3. Texas Instruments, *GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic,* application report, March 1997, literature number SCEA003A.
4. Texas Instruments, *GTLP EVM Overview,* presentation, June 2000.
5. Texas Instruments, *GTLP Device Overview,* presentation, June 2000.
6. Texas Instruments, *SN74FB1650, 18-Bit TTL/BTL Universal Storage Transceiver*, data sheet, August 1992 – revised October 1996, literature number SCBS178H.

GTLP Evaluation Module (EVM) User's Guide

SCEA023
June 2001

Texas Instruments

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

Use this manual to set up and use the GTLP evaluation module (EVM) for the SN74GTLPH1655 and other GTLP devices.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – GTLP EVM Board Typical Test and Setup Configuration
- Chapter 3 – Oscilloscope Operation
- Chapter 4 – Waveform Measurement and Interpretation
- Chapter 5 – Troubleshooting
- Appendix A – Bill of Materials, Schematics, Board Layouts, and Suggested Specifications

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case, users, at their own expense, will be required to take whatever measures may be required to correct this interference.

Trademarks

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Contents

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Chapter 1

Introduction

The Texas Instruments (TI) GTLP evaluation module (EVM) board is used to evaluate the SN74GTLPH1655 in multipoint data-transmission applications in a heavily loaded backplane.

The GTLP EVM is a 17.9-in., 20-slot, 0.94-in.-pitch, 8-layer PC backplane board that provides a total of 48 parallel data lines divided into 6 groups of 8 bits staggered into various lengths. The EVM also includes a 1-bit clock along the length of the backplane showing source-synchronous transfer mode. This board allows the designer to connect 50-Ω unloaded parallel buses to the transmitter and receiver connectors in a backplane configuration.

New-design backplane-driver selection criteria are based on drive capability, live-insertion capability, data throughput, noise margin, backward compatibility, and bus configuration. The purpose of the GTLP EVM is to demonstrate the performance of the TI GTLP product portfolio in a best-in-class high-performance backplane. The backplane enables users to observe the effects of different kinds of terminations, changing load conditions due to different spacing and count of daughter cards, and various frequencies, as well as the benefit of source-synchronous clock over system-synchronous clock operations. The backplane also can be used to observe the advantages of edge-rate control and TI-OPC™ overshoot-protection circuitry, and show the performance of TI GTLP devices vs alternate-source devices under different loading conditions.

Topic **Page**

1.1 GTLP EVM Overview

The EVM can be used to evaluate device parameters, while acting as a guide for high-speed board layout. Because GTLP operates over a wide range of frequencies, designers must optimize their designs for the frequency of interest. Additionally, designers can use buried transmission lines and provide additional noise attenuation and EMI suppression to optimize their end product.

The board layout is designed and optimized to support high-speed operation up to 100 MHz. Thus, understanding impedance control and transmission-line effects are crucial when designing high-speed boards.

Some of the advanced features offered by this board include:

- The backplane printed circuit board (PCB) is designed for high-speed signal integrity, while the daughter card is designed with integral measurement points for easily measuring signal integrity.
- Subminiature A connectors (SMA) as specified by MIL-C-39012 coaxial connector specification and parallel fixtures easily are connected to test equipment.
- The first bit of each group of input/output signals is accessible for rapid prototyping.

1.2 GTLP EVM Kit Contents

This EVM kit comprises the following major parts, components of which are listed in Appendix A.1, *GTLP EVM Bill of Materials*:

- ❑ GTLP EVM kit documentation (this document, SCEA023)
- ❑ Backplane
- ❑ Clock driver card
- ❑ Termination card
- ❑ Monitored receiver card
- ❑ Monitored driver card
- ❑ Unmonitored receiver card

1.3 GTLP EVM Kit Availability

The GTLP EVM kit is not available for resale, but can be obtained and used for short periods of time by contacting the GTLP team at GTLP@list.ti.com. There are six locations worldwide where GTLP EVMs can be obtained: Europe, China, Korea, Japan, and the Americas (2).

Chapter 2

GTLP EVM Board Typical Test and Setup Configuration

This chapter describes the GTLP EVM setup and the configurations used to evaluate the SN74GTLPH1655 transceiver. These configurations can be used to evaluate different transceivers that will be available in the future.

Topic **Page**

2.1 GTLP EVM Case

The EVM is stored and transported in a sturdy plastic case with rollers and extensible handle (see Figure 2–1). The handle locks in position and can be extended or retracted by pressing the release on the underside of the handle.

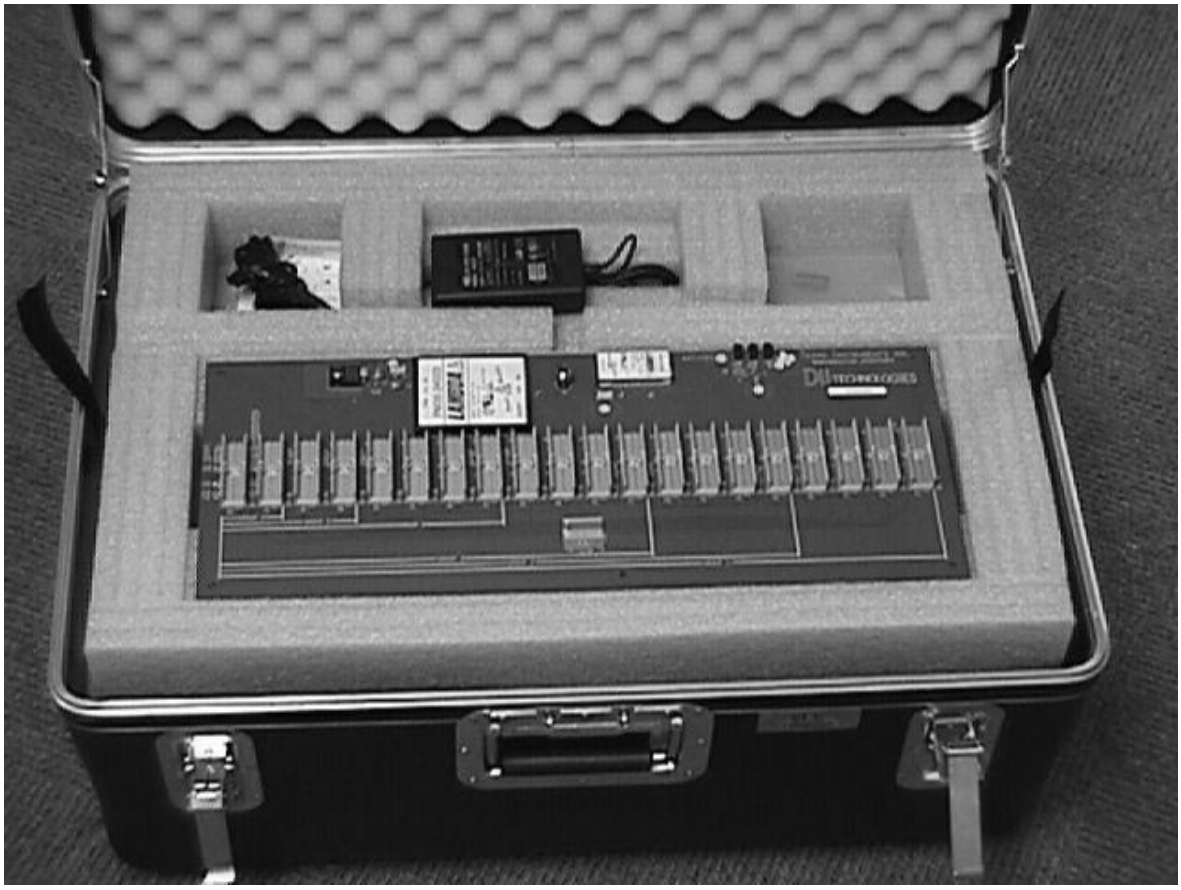
Figure 2–1. GTLP EVM Case

The case is suitable for air transportation and has the combination lock set at 394. To lock the case, rotate one or more of the dials from the opening combination.

2.2 Top Tray

The top tray fits snuggly in the GTLP EVM case (see Figure 2–2) and holds the backplane board, power supply, extra clock crystals, and extra termination cards in place. The tray is electrostatic protective foam that holds the backplane board during demonstrations.

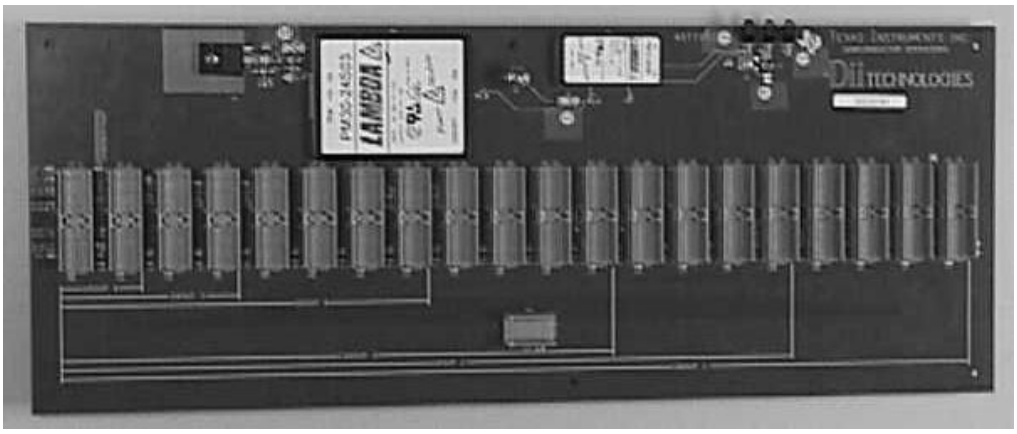
Figure 2–2. GTLP EVM Top Tray



2.3 Backplane Board

The backplane board (see Figure 2–3) is typical of backplanes used in commercial applications, and consists of 20 slots with 0.94-in. pitch and 48 data bits, and 1 clock bit on stripline transmission lines.

Figure 2–3. GTLP EVM Backplane Board



This backplane board is constructed uniquely of six groups of eight data bits each to study the effect of different backplane lengths and driver/receiver placements. Group 1 consists of all 20 slots, but subsequent groups move to the left (see Figure 2–4) and have a reduced number of slots, as listed in Table 2–1.

Figure 2–4. GTLP EVM Backplane Block Diagram

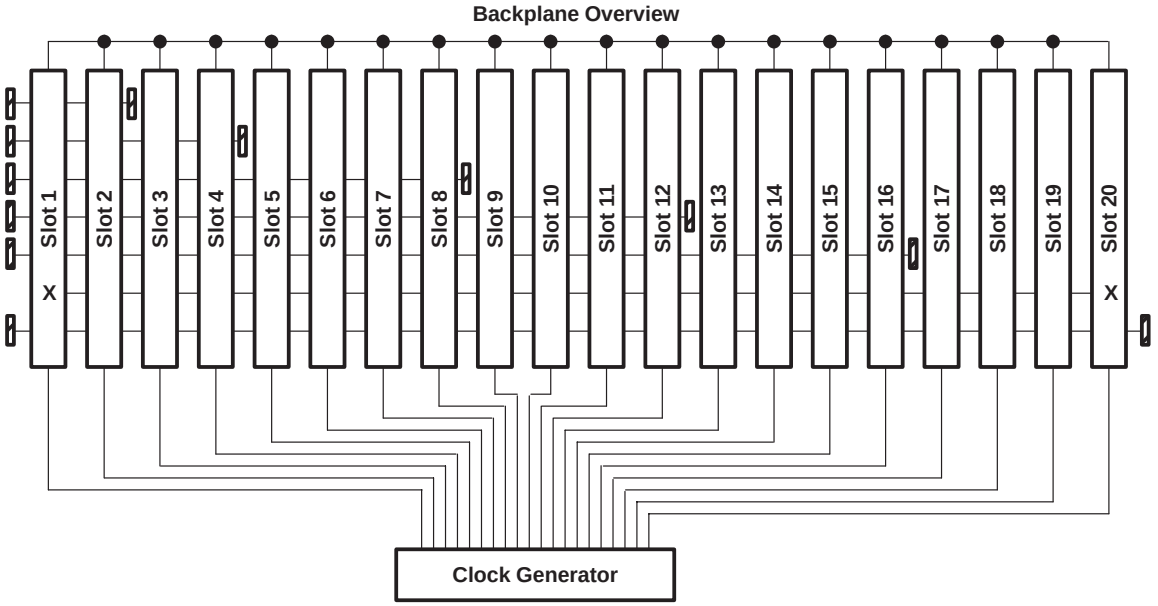


Table 2–1. GTLP EVM Group Assignment

Group 6	Group 5	Group 4	Group 3	Group 2	Group 1
2 slots	4 slots	8 slots	12 slots	16 slots	20 slots
P1-1 to P1-2	P1-1 to P1-4	P1-1 to P1-8	P1-1 to P1-12	P1-1 to P1-16	P1-1 to P1-20

A single GTLP clock line that runs from P1-1 to P1-20 is used in the source-synchronous transfer mode.

The GTLP clock and the data lines from groups 2 through 6 have fixed, on-board, 25-Ω termination resistors. Group 1 data lines terminate on plug-in cards on the back of the backplane board at P1-1B and P1-20B. This provides a way to vary the termination resistance or demonstrate other termination techniques.

The design also uses a system clock that is generated on the clock-driver board plugged into P3. This system clock is distributed to all 20 slots simultaneously and is used as the system master timing in the system-clock mode. Using a separate card for clock generation and distribution is not an industry standard, but it provides flexibility in using this demonstration board.

A logic selection line (MODESEL) connects P1-1 through P1-20. The driver card uses this line to select between source-synchronous and system-clock operation. The demonstration board is an eight-layer board with separate V_{CC} and ground planes. The backplane board stackup is shown in Table 2–2. Embedded microstrip nominal line width is 0.006 in., dielectric material is Nelco N4000-13 with a dielectric constant (50% resin contents) of 3.80 @ 100 MHz.

Table 2–2. GTLP EVM Backplane Eight-Layer Stackup

Trace Name	Use	Layer	Copper Weight (oz)	Physical Representation	Dielectric Height (in.)	Dielectric Name
Top	Regulator power/ bypass capacitor/ termination	1	0.5			
					0.004	B stage
Internal signal 2	Clock distribution/ signal	2	1			
					0.004	Core
Ground plane	Ground plane	3	1			
					0.004	B stage
Internal signal 3	Data signal	4	1			
					0.058	Core
Internal signal 4	Data signal	5	1			
					0.004	B stage
V_{CC}	V_{CC}	6	1			
					0.004	Core
Internal signal 5	Data signal	7	1			
					0.004	B stage
Bottom	Termination	8	0.5			

Targeted, nominal, unloaded line impedance was 50 Ω, but, based on post-manufacturing testing, was not consistent. Results for Group 1, bits 1 through 8 are shown in Table 2–3. The backplane natural trace impedance (Z_o) is calculated and is a best estimate. The backplane trace impedance with only the connector pins attached (i.e., all cards removed) (Z_o') and the backplane trace impedance in a fully loaded backplane (i.e., 20 cards inserted) (Z_o'') are measured.

Table 2–3. GTLP EVM Group 1, Bits 1 Through 8 Trace Impedance

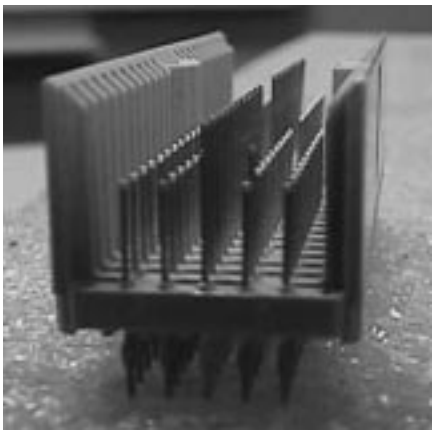
Group 1 Trace	D1	D2	D3	D4	D5	D6	D7	D8
Natural Trace Impedance								
Z_o (Ω)	91	47.5	47	47	48	47.5	83	47.5
t_{pd} (ps/in.)	165	140	138	139	141	148	147	142
C_o (pF/in.)	1.81	2.95	2.94	2.96	2.94	3.12	1.77	2.99
Trace Impedance With Only Connectors								
Z_o' (Ω)	62.7	37.5	37	36.3	37.1	37.9	58.5	36.8
t_{pd}' (ps/in.)	240	177	175	180	183	185	208	183
Trace Impedance Under Full Load								
Z_o'' (Ω)	26.6	17.7	17.9	17.5	17.9	18	24.8	17.7
t_{pd}'' (ps/in.)	564	377	362	373	377	390	493	382

Note the difference in fully loaded trace impedance between trace bit 1 and bit 7 (D1 and D7) and the other traces. Using the lower natural trace impedance offers the advantage of a smaller t_{pd} and shorter flight time, but at the expense of terminating with a lower-value termination resistor and the subsequent increase in power consumption. TI offers both medium-drive (50 mA) and high-drive (100 mA) GTLP devices that allow designers to match the device with backplane loading. The termination resistor (R_{TT}) should match the fully loaded trace impedance (i.e., Z_o'') of the backplane for optimal signal integrity.

2.4 Connectors

An AMP Z-PACK™ 2-mm, 110-pin, hard-metric (HM) male connector is used in slots 1 through 20 (see Figure 2–5) .

Figure 2–5. AMP Z-PACK™ 2-mm, 110-Pin, Hard-Metric (HM) Male Connector

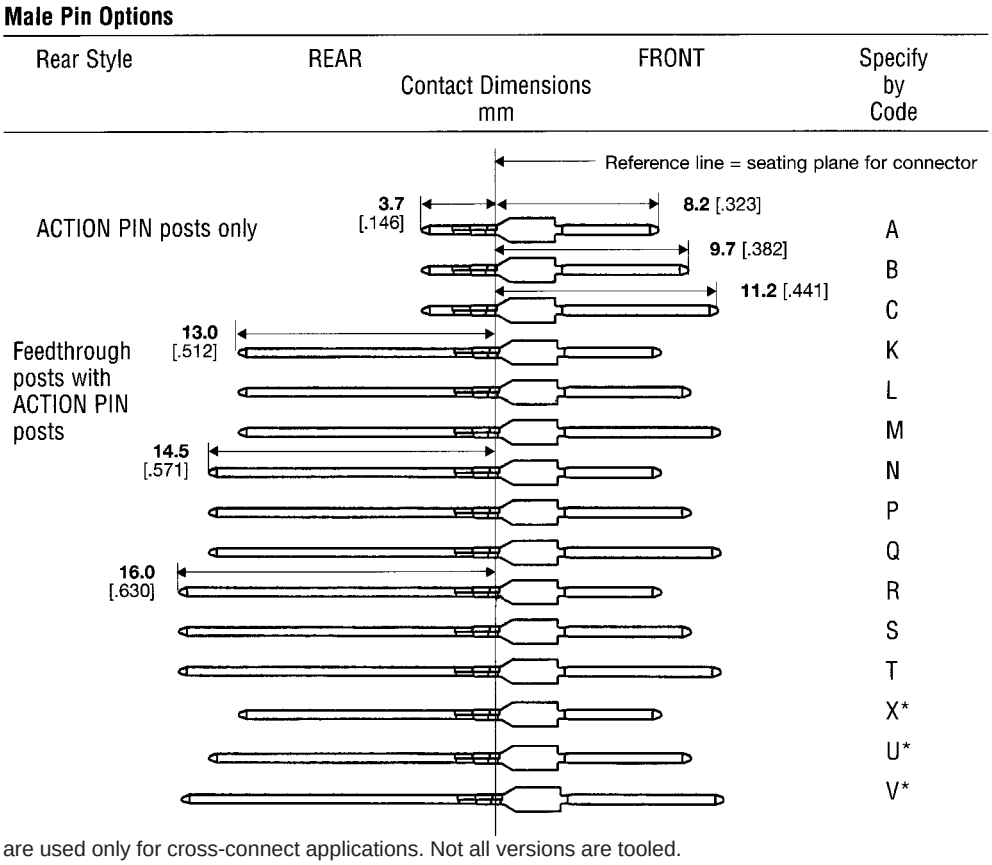


Five pins are used on the backplane, with three different lengths on the backplane daughter-card side. Pins A, B, and C are used for data/V_{CC}, BIAS V_{CC}, and GND, respectively. C-length pins are in the center, and A-length pins are in two rows on either side. The daughter-card connectors P1-1 through P1-20 use these three levels of pin height for power sequencing. The ground pins make contact first, followed by a pin for BIAS V_{CC}, then all other connections are made. There is only one B-length pin because BIAS V_{CC} can be distributed to all four GTLP devices on the board. The pin lengths of pins K and T are identical to those of pins A and C on the card side, but they protrude through the backplane board, providing connection to the termination cards that are on the reverse side.

Initial testing revealed that this pin configuration was unacceptable for actual operation because the BIAS V_{CC} circuitry was disabled before all I/O pins were connected. Any tilt on the card caused V_{CC} to be connected first. Some slots in selected EVMs have been modified, so that BIAS V_{CC} and GND are C length, data signal is B length, and V_{CC} is A length, to allow proper operation of the BIAS V_{CC} precharge circuitry.

Various AMP pin lengths, including pins A, B, C, K, and T, are shown in Figure 2–6, and the single-line-model data sheet is shown in Figure 2–7.

Figure 2–6. AMP Pin Lengths

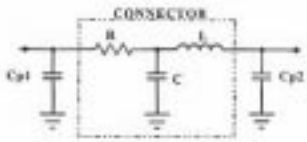


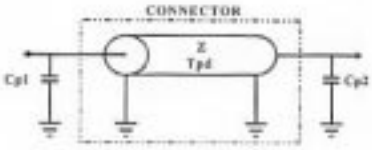
* X, U, V are used only for cross-connect applications. Not all versions are tooled.

Figure 2–7. AMP Single-Line-Model Data Sheet

AMP SINGLE LINE MODEL DATASHEET

Z-PACK, 2mm CL, HM, 5 Row With Long Shield (Compact PCI), Vertical Plug to Right Angle Receptacle
VALIDATED
1:1 S/G pattern





Connector Lumped Constant Model

Row	R (mΩ)	L (nH)	C (pF)
A	12	5.30	1.40
B	12	5.00	1.70
C	13	5.70	2.00
D	15	6.10	2.30
E	16	7.30	2.40
Mean	14	5.88	1.96

Connector Distributed Model

Z (Ω)	Tpd (ps)
62	86
54	92
53	107
51	118
55	132
55	107

Note: (1) The following RLC model is appropriate for edge speeds slower than ten times the highest propagation delay (Tr>=10 * Tpd(highest)). To accommodate faster edge speeds, the lumped model must be divided into two or more RLC sections. For best results, a section's propagation delay should be 1/10th of the edge speed.

(2) The single line inductance and capacitance values are extracted from a specified pattern. The placement and number of ground returns affect the inductance and capacitance of the single line model.

(3) The parameters for the Single Line Model are for the connector only without any mounting effects such as plated through holes or pads capacitance (Cp1 and Cp2). The impedance and propagation delay for the connector are calculated as follows:

$$Z_{Connector} = \sqrt{\frac{L}{C}}(\Omega) \text{ and } Tpd_{Connector} = \sqrt{L * C}(sec)$$

For an interconnection path model, the mounting effects must be added because the additional capacitance of the pad to ground or plated through hole (Cp1 and Cp2) decrease impedance and increase propagation delay of the interconnection path. The impedance and propagation delay for an interconnection path are calculated as follows:

$$Z_{Interconnect} = \sqrt{\frac{L}{C + (Cp1 + Cp2)}}(\Omega) \text{ and } Tpd_{Interconnect} = \sqrt{L * (C + Cp1 + Cp2)}(sec)$$

FOR ADDITIONAL ELECTRICAL MODELING/SIMULATION SUPPORT, CALL 717-986-7824 OR E-MAIL US AT modeling@amp.com

Datasheet Filename: ZPACK_2mmHM_5RowCPCI_V-P_RA-R_TH
Modeled by: [DWG]
Created on 03/05/98 10:41 AM

Reviewed By: [CTK]
SPICE File: [HM5CPCI]

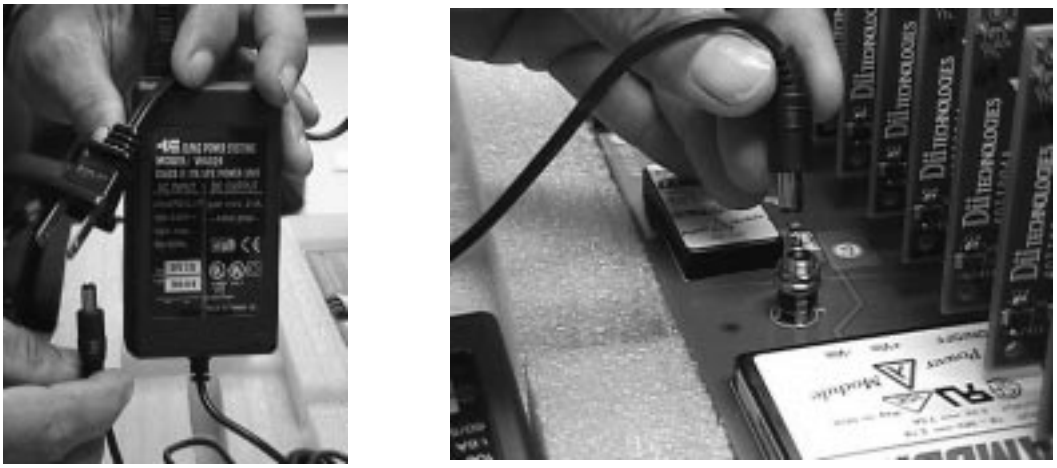
ACD Internal Form: Form_SLM-DS_1998_0504

2.5 Power Supply

The power supply (see Figure 2–8) is a universal power supply that accepts 100 V to 240 V, 50/60-Hz ac and uses any wall plug that connects to the IEC 320 two-connector universal socket with the US/Canada Edison plug. An alternate supply cord with a different wall plug must be procured locally, if required.

The power-supply output is 24-Vdc at 2.1 A, which is fed to the backplane board using the 5.5-mm plug to J5 (see Figure 2–8), and connects through a 2.5-A slow-blow fuse (F1). Power should not be applied to the backplane board until the cards have been inserted during the initial setup because the clock card is not hot insertable. The termination, daughter cards, and clock crystals are live insertable and can be inserted and removed to change position/values during testing without disconnecting the power supply.

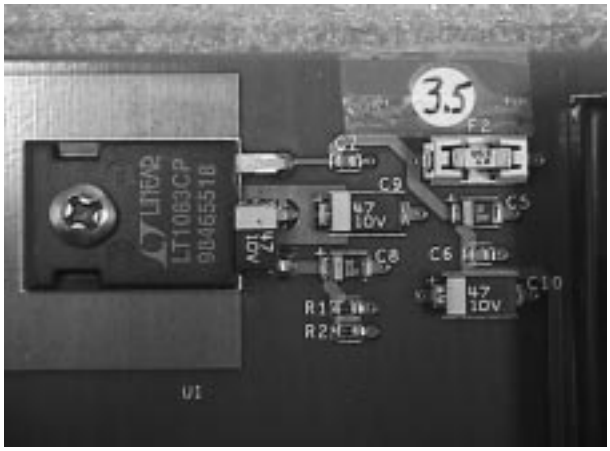
Figure 2–8. Power Supply (Left) and Backplane Connection (Right)



The 24-Vdc is reduced to 5 V, 1 A by the Lambda PM10-24S05 switching regulator (Figure 2–8 background) and to 3.3 V, 7.5 A by the Lambda PM30-24503 switching regulator (Figure 2–8 foreground) for V_{CC}, BIAS V_{CC}, and the linear regulator. The 3.3 V is supplied to all connectors through a 5-A fuse (F2). The 5 V also is applied to all connectors. Originally, F2 was specified as a 3.5-A fuse, but, at 100-MHz operation, current exceeds this value, so 5-A fuses are necessary.

The 3.3 V is further reduced to 1.5 V, 7.5 A by the LT1083CP linear regulator (see Figure 2–9) for the termination voltage (V_{TT}). V_{TT} is set by the combination of R1 and R2 and can be varied in the factory between 0.8 V to 1.8 V, but is set at 1.0 V for field use at GTLP levels. The 5-V power supply is required for driver cards that use both 5-V and 3.3-V V_{CC}, such as the SN74GTLPH16612. There is an option to change the 5-V power supply to 2.5 V for future devices at that voltage node. This is accomplished by removing JP1 (near the dc converter) and installing an LM317M regulator (U2), R5, and R6. The two resistors set the output voltage of the regulator.

Figure 2–9. 1.5-V V_{TT} Linear Regulator

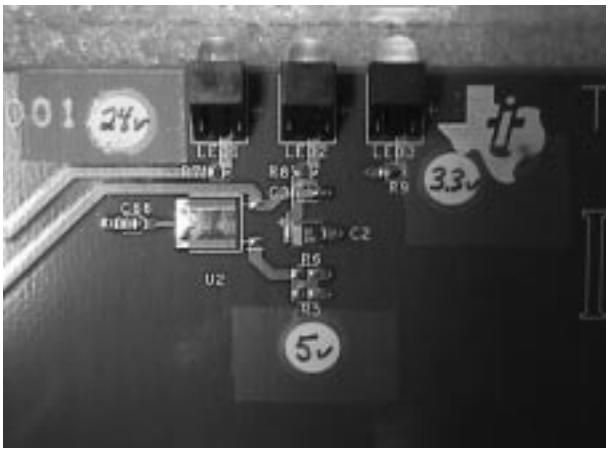


Unitrode offers two devices (UC382 and UC385) that can be used in place of the LT1083CP. They offer low dropout at a given current (500-mV dropout maximum at 5 A), the ability to handle transients with tight regulation, high-current capability, fast transient response, separate bias and V_{in} pins, and 5-pin TO220 and TO263 packages with Kelvin sensing. UC382 provides 3-A capacity and UC385 provides 5-A capacity with fixed (1.5 V, 2.1 V, or 2.5 V) or adjustable-output-voltage capability.

Power-supply operation indication is provided by three LEDs (see Figure 2–10) on the upper edge of the backplane opposite slot 16:

- LED 1 – 24-V green LED shows there is power coming to the board.
- LED 2 – 5-V green LED shows the 5-V power supply is operational.
- LED 3 – 3.3-V red LED shows the 3.3-V power supply is supplying power to the devices, BIAS V_{CC}, and linear regulator.

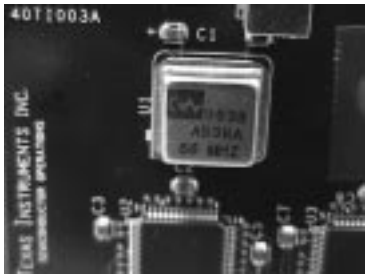
Figure 2–10. Power-Supply LED Indicators

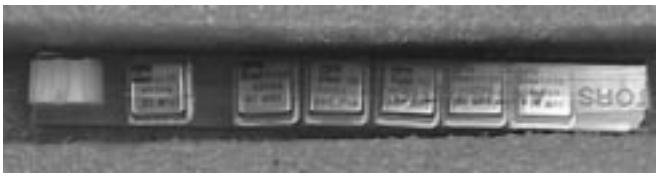


2.6 Clock Crystals

Clock frequency is controlled by the clock-driver card and is limited by clock-control components to 100 MHz. The GTLP receiver device is used in a latched mode of operation, so GTLP data frequency is equal to one-half the clock frequency. Clock crystals and spares, in frequencies of 66 MHz, 75 MHz, 87 MHz, and 100 MHz, are included with the kit. One crystal can be installed on each clock card, with the others stored in the clock-crystal tube (see Figure 2–11).

Figure 2–11. Clock Crystal on Card (Left) and Stored in Tube (Right)





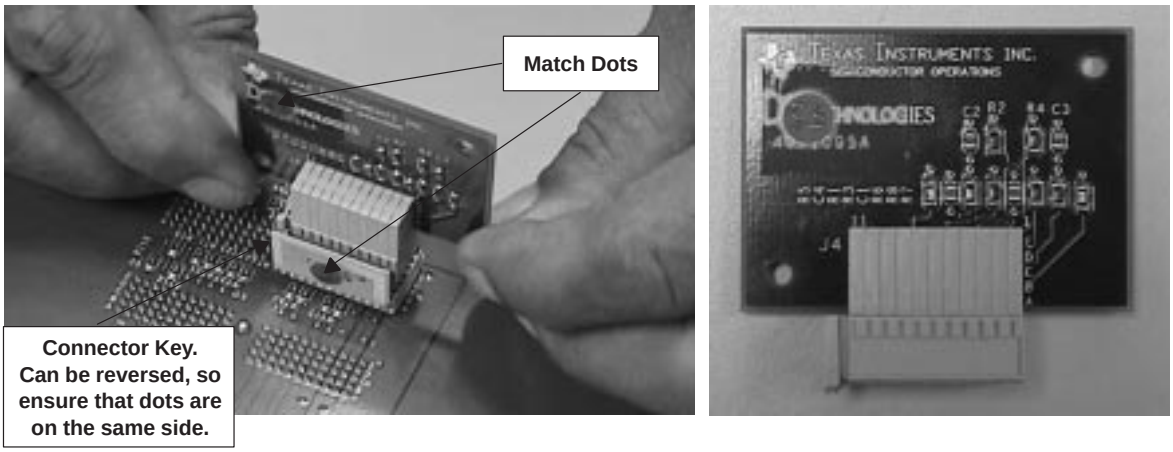
If you plan to store the clock-driver card with the crystal installed, insert the crystal far enough so that the leads barely protrude on the opposite side (see Figure 2–12). This prevents bending the leads if they catch on the foam when the card is placed in the case.

Figure 2–12. Clock Crystal With Leads in Position for Storage

2.7 Termination Cards

Because proper backplane termination has a large effect on signal integrity and is investigated easily, Group 1 has removable termination cards on the back of the backplane (see Figure 2–13). The termination cards are identical, except for the resistor values that are 25 Ω, 33 Ω, 38 Ω, or 50 Ω. One bypass capacitor is mounted with every other termination resistor to limit voltage fluctuations. The termination cards provide a method of varying the termination resistance to only Group 1 data lines. These termination resistors connect to the V_{TT} supply (1.5 V because GTLP levels are used).

Figure 2–13. Termination Card Location (Left) and Close-Up View (Right)



The termination cards have a four-layer stackup. The stackup is signal layer, V_{CC} plane, ground plane, and signal layer (see Table 2–4).

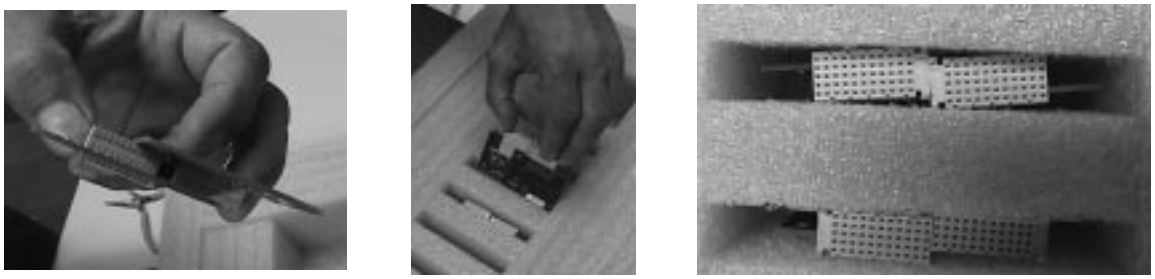
Table 2–4. Termination-Card Stackup

Trace Name	Use	Layer	Copper Weight (oz)	Physical Representation	Dielectric Height (in.)	Dielectric Name
Top	Data signal	1	0.5			
					0.004	B stage
V_{CC} plane	V_{CC} plane	2	1			
					0.004	Core
Ground plane	Ground plane	3	1			
					0.004	B stage
Bottom	Data signal	4	0.5			

Groups 2 through 6 have 25-Ω fixed termination resistors due to space limitations, and have one bypass capacitor for every four termination resistors. The 25-Ω termination is optimized for estimated 25-Ω loaded-line impedance.

The termination cards can remain installed on the backplane board or be removed during storage and transit. Both termination cards can be stored in the same slot in the tray (see Figure 2–14) or stored separately. If stored together, the resistor/capacitor sides must face each other.

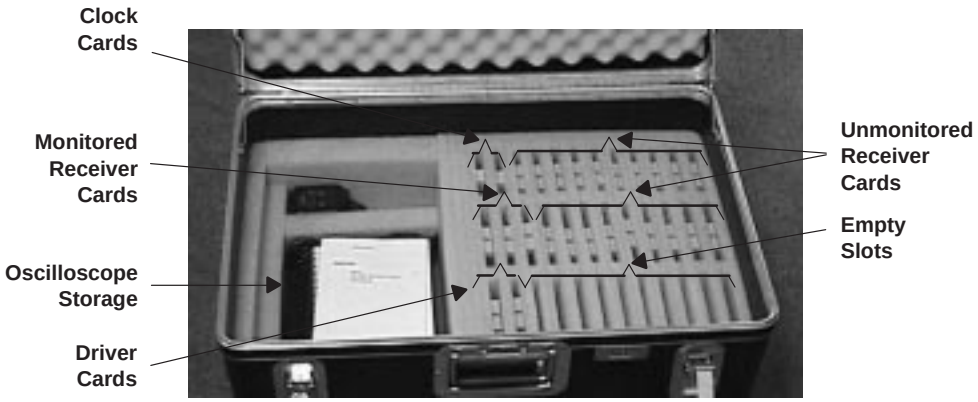
Figure 2–14. Termination-Card Storage



2.8 Bottom Compartment

The portable oscilloscope and backplane daughter cards are stored under the top tray of the GTLP EVM case (see Figure 2–15).

Figure 2–15. Oscilloscope and Backplane Daughter-Card Storage Area



There are 2 clock cards, 19 unmonitored receiver cards, 3 monitored receiver cards, and 2 driver cards in every GTLP EVM kit. Store the cards as shown in Figure 2–15, with the 2 clock cards (top left) followed by 10 unmonitored receiver cards, 3 monitored receiver cards (middle left) followed by 9 unmonitored receiver cards, 2 driver cards (bottom left) followed by 10 empty slots.

2.9 Measurement Equipment

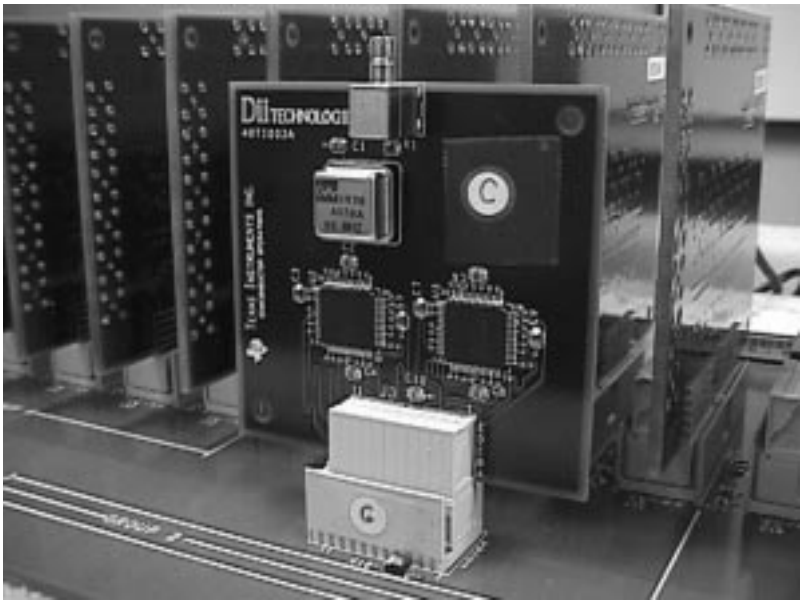
The Tektronix THS730A Oscilloscope/DMM (O-Scope) (see Figure 2–16) can be stored in the bottom of the case (see Figure 2–15). It is easy to operate and is portable. The O-Scope can monitor two channels simultaneously. Store the O-Scope face down to prevent damage to the buttons during transit. The probes can be stored on top of the O-Scope, as shown, or alongside, depending on the amount of space in either location. The O-Scope is not included with the loaned EVM kits. Chapter 3, *Oscilloscope Operation*, discusses O-Scope setup and operation and is included to provide assistance to TI product marketing engineers and technical sales representatives when demonstrating the GTLP EVM to customers in the field.

Figure 2–16. Tektronix THS730A O-Scope

2.10 Clock Cards

Two clock cards (see Figure 2–17) are included with the EVM, one primary and one spare. The clock cards generate the clock signal that is sent to every slot via mitered lines, so that the clock arrives at exactly the same time at each card. The clock card uses a plug-in half-can oscillator for a reference to two CDC2586 phase-locked-loop clock drivers. These two drivers provide the 20 system clocks used on the backplane. The CDC2586 supports a maximum frequency of 100 MHz. The clock card has one subminiature B connector (SMB) as specified by MIL-C-39012 coaxial connector specification test point to monitor the oscillator output.

Figure 2–17. GTLP EVM Clock Card



The clock-card board is a four-layer printed circuit board (PCB). The stackup is signal layer, V_{CC} plane, ground plane, and signal layer (see Table 2–5).

Table 2–5. Clock-Card Stackup

Trace Name	Use	Layer	Copper Weight (oz)	Physical Representation	Dielectric Height (in.)	Dielectric Name
Top	Data signal	1	0.5			
					0.004	B stage
V_{CC} plane	V_{CC} plane	2	1			
					0.004	Core
Ground plane	Ground plane	3	1			
					0.004	B stage
Bottom	Data signal	4	0.5			

2.11 Driver Cards

Separate driver and receiver daughter cards were manufactured for use on the backplane because, even though the bidirectional SN74GTLPH1655 device is used, each type of card is hardwired to operate in a certain direction. The driver card generates a data pattern from the system clock and drives the GTLP lines on the backplane. The GTLP devices are hardwired for clocked storage in the A-to-B direction. Data is transmitted on the rising edge of the system clock. The driver card is a six-layer PCB with two signal layers, a V_{CC} plane, a ground plane, then two signal layers. Stackup is shown in Table 2–6.

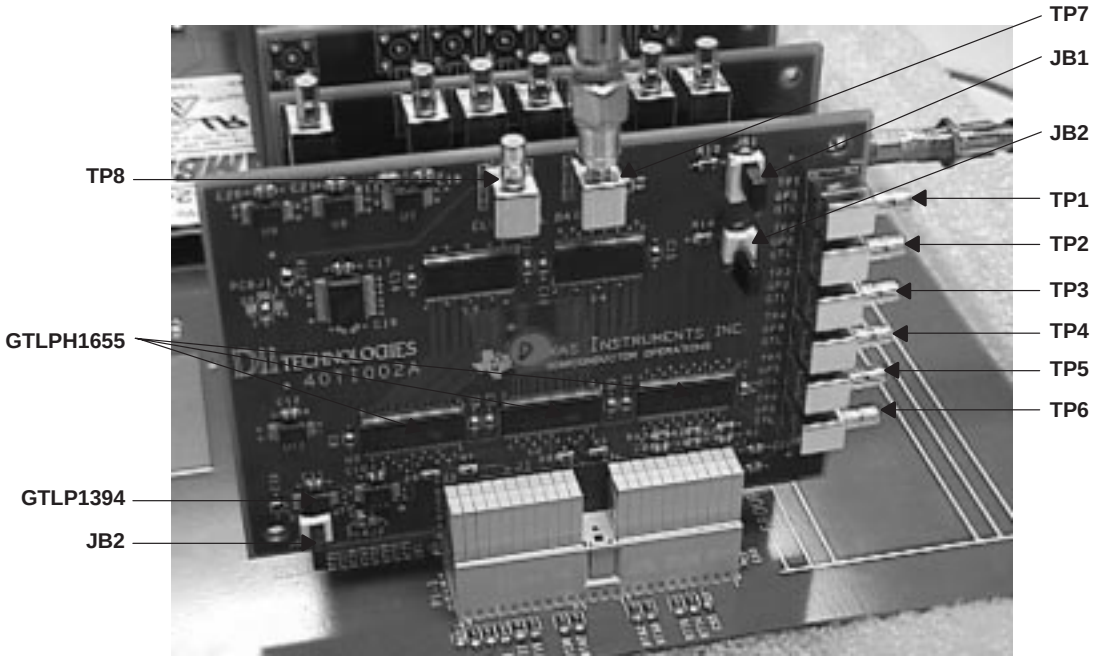
Table 2–6. Driver-Card Stackup

Trace Name	Use	Layer	Copper Weight (oz)	Physical Representation	Dielectric Height (in.)	Dielectric Name
Top	Data signal	1	0.5			
					0.004	B stage
Internal signal 2	Data signal	2	1			
					0.004	Core
V_{CC} plane	V_{CC} plane	3	1			
					0.004	B stage
Ground plane	Ground plane	4	1			
					0.004	Core
Internal signal 3	Data signal	5	1			
					0.004	B stage
Bottom	Data signal	6	1			

The driver daughter card (see Figure 2–18) has SMB monitor points for selected LVTTL and GTLP signals, in addition to jumpers for Group 1, bit 1 switching (JB1), system or SN74GTLP1394 source-synchronous clock selection (JB2), and selection of the SN74GTLPH1655 slow or fast edge rate (JB3). The monitor points along the top edge are the latch clock and the master data pattern sent to all SN74GTLPH1655 LVTTL A-port inputs. There are no LVTTL group-bit monitor points because the card always is driven. Monitor points along the right edge are GTLP Group 1, 2, 3, 4, 5, and 6. The following signals are monitored:

- ❑ TP1 GTLP level Group 1, bit 1
- ❑ TP2 GTLP level Group 2, bit 1
- ❑ TP3 GTLP level Group 3, bit 1
- ❑ TP4 GTLP level Group 4, bit 1
- ❑ TP5 GTLP level Group 5, bit 1
- ❑ TP6 GTLP level Group 6, bit 1
- ❑ TP7 LVTTL level Group 1, bit 1, and master data pattern
- ❑ TP8 LVTTL level GTLP latch clock

Figure 2–18. GTLP EVM Driver Daughter Card

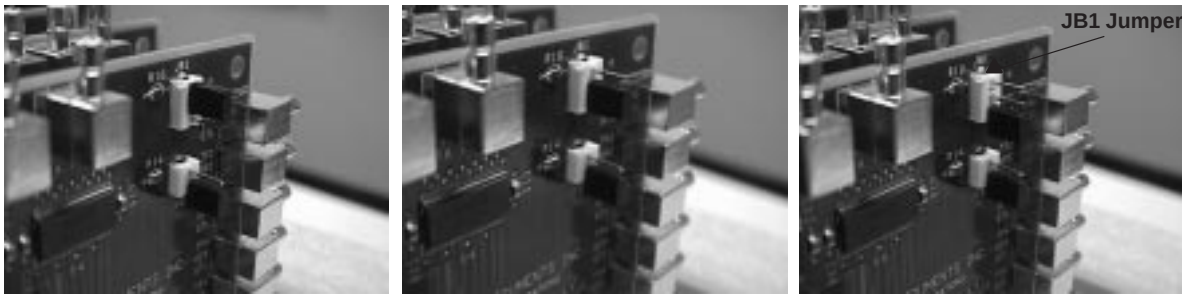


2.11.1 Single-Bit Selection

JB1 three-position jumper is used to set Group 1, bit 1 to pass the normal data pattern, set the signal low, or set the signal high (see Figure 2–19). The JB1 jumper is stored on the lowest pin (see Figure 2–19) when set high, to prevent losing it. The following options are available:

- ❑ JB1 1-2 shorted Group 1, bit 1 normal data pattern
- ❑ JB1 2-3 shorted Group 1, bit 1 held low
- ❑ JB1 open Group 1, bit 1 held high

Figure 2–19. Bit Selection for Normal Data Pattern (Left), Signal Held Low (Center), or Signal Held High (Right)

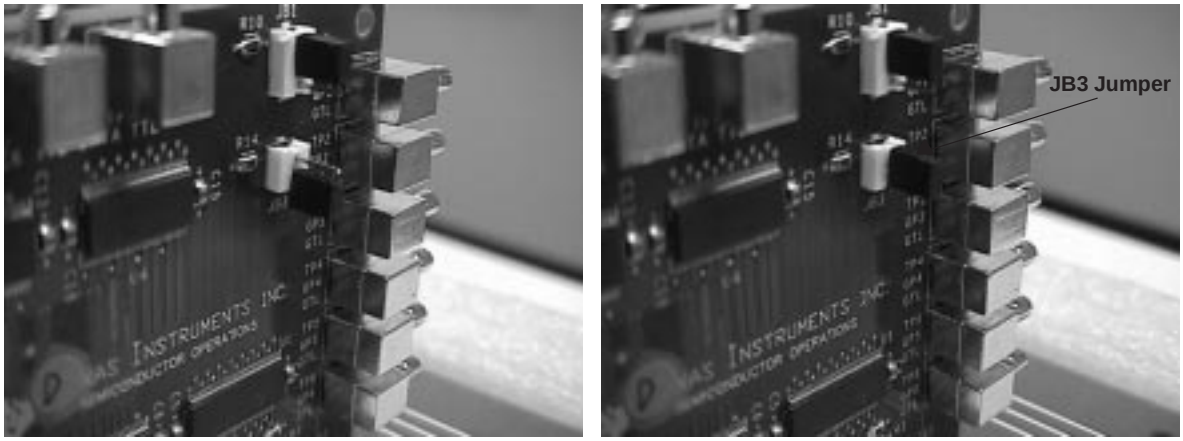


2.11.2 Edge-Rate Control

The device used as the backplane driver, SN74GTLPH1655, has a feature by which the backplane slew rate is adjustable via an external edge-rate-control (ERC) pin held at 3.3 V (slow) or GND (fast). The ERC is set by the JB3 jumper located below the bit-selection jumper and has two positions: not connected is slow, and shorted is fast (see Figure 2–20). The following ERC options are available:

- ❑ JB3 open — Slow edge rate
- ❑ JB3 shorted — Fast edge rate

Figure 2–20. ERC Bit-Selection Jumper Set for Slow (Left) or Fast (Right) Rate



2.11.3 Source-Synchronous Clock/System-Clock Selection

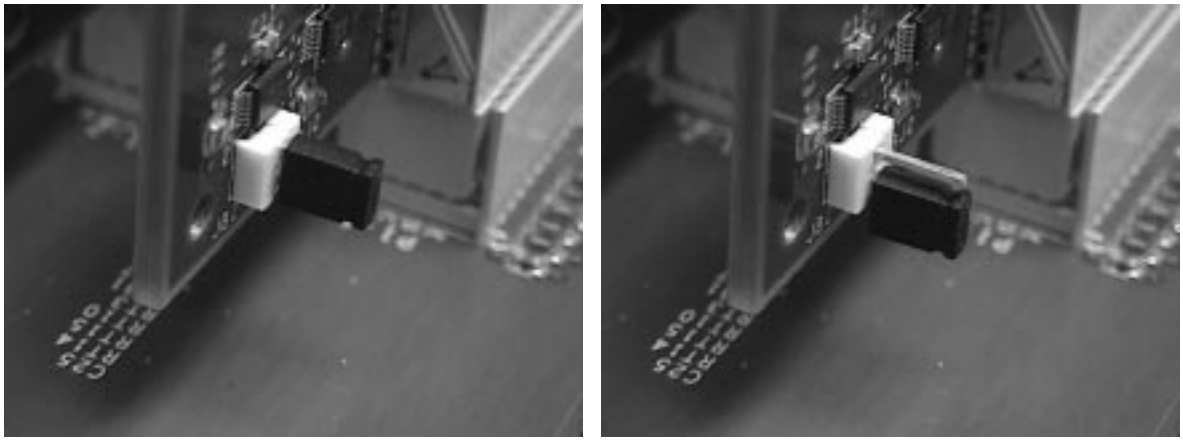
Backplanes usually have a system-wide synchronous clock. A system clock provides an absolute reference time signal from the clock card to every daughter card at exactly the same time. Source-synchronous clock operation is different because it allows the absolute system clock to be sent by the backplane driver along with the data. In the EVM, this is implemented with the SN74GTLP1394 transceiver on all daughter cards. This transceiver acts as the driver on the driver cards and as the receiver on the receiver cards. The SN74GTLP1394 has ERC that is set to the fast edge rate in conjunction with the JB3 selection.

Source-synchronous clock operation provides a relative clock to all receiver cards, which removes the flight-time delay restrictions required when an absolute system clock is used. The flight-time delay depends primarily on bus length and bus loading.

The driver card uses JB2 to select the transfer mode of operation and to drive the MODESEL line. Source-synchronous clock operation is selected when the JB2 jumper shorts the pins, and system-clock operation is selected when the pins are open (see Figure 2–21). When JB2 is shorted, the SN74GTLP1394 drives the GTLP clock line with a phased system clock. When JB2 is open, there is no activity on the GTLP clock line. The following options are available:

- ❑ JB2 shorted — Source-synchronous clock transfer
- ❑ JB2 open — System-clock transfer

Figure 2–21. JB2 Set to Source-Synchronous Clock (Left) or System-Clock (Right) Operation



2.12 Receiver Cards

Receiver cards place a load on the backplane and provide a point to monitor the signals. There are two types of receiver cards: one that has built-in monitor points, and one with no monitor points. Either type can be placed in any slot in the backplane, typically with the monitored receiver card placed in the slots under observation. There is a monitor point for only one bit per group. Only a few receiver cards have monitor points because the capacitance added by the monitor point affects backplane signal integrity. Minimal use of the monitored receiver card is encouraged because of the increased loading this card causes.

Receiver cards have GTLP devices hardwired for clocked storage in the B-to-A direction. Data is latched on the rising edge of the GTLP latch clock. The latch clock comes from the system clock when the MODESEL line is high, and from the GTLP clock when the MODESEL line is low. The receiver card is a six-layer PCB with two signal layers, a V_{CC} plane, a ground plane, then two signal layers. The GTLP data and clock stub lines are approximately 1 in. in length. Stackup is shown in Table 2–7.

Table 2–7. Receiver-Card Stackup

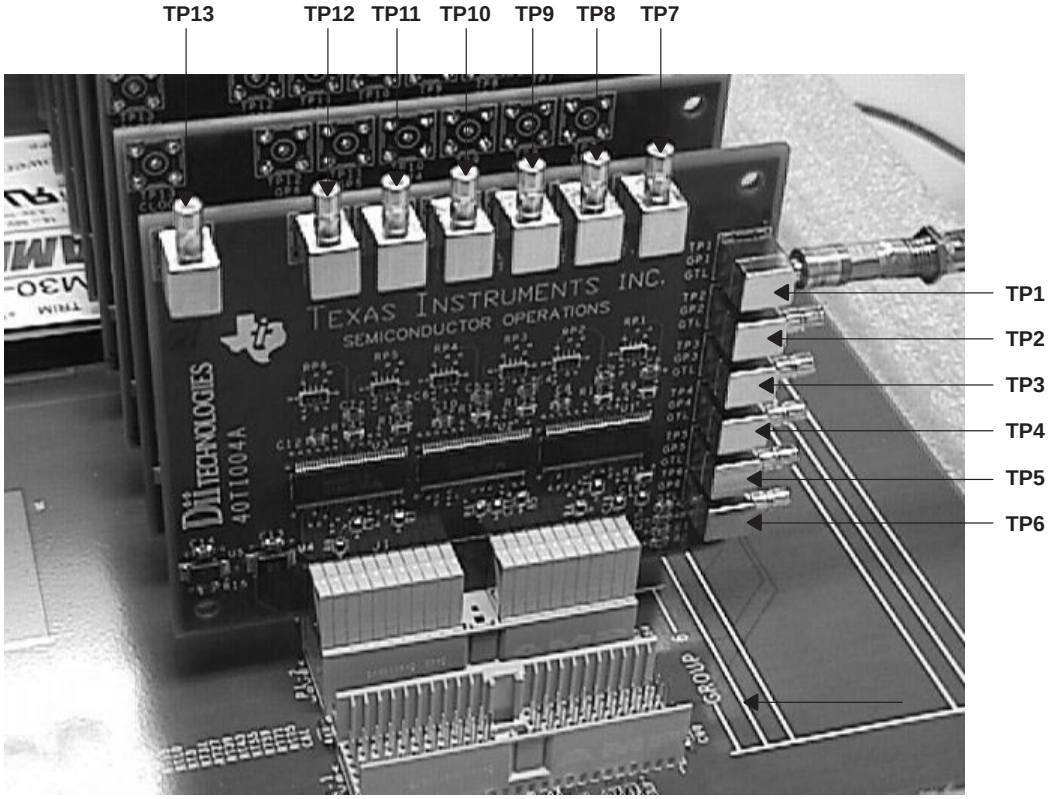
Trace Name	Use	Layer	Copper Weight (oz)	Physical Representation	Dielectric Height (in.)	Dielectric Name
Top	Data signal	1	0.5			
					0.004	B stage
Internal signal 2	Data signal	2	1			
					0.004	Core
V_{CC} plane	V_{CC} plane	3	1			
					0.004	B stage
Ground plane	Ground plane	4	1			
					0.004	Core
Internal signal 3	Data signal	5	1			
					0.004	B stage
Bottom	Data signal	6	1			

Figure 2–22 shows a monitored receiver card. Monitor points on the right side are for GTLP Groups 1, 2, 3, 4, 5, and 6. Monitor points on the top are for LVTTL latch clock, Groups 6, 5, 4, 3, 2, and 1. The LVTTL latch-clock source is either the system clock or source-synchronous clock. The source-synchronous clock is the system clock sent via the SN74GTLP1394 driver card along the 1-bit clock trace on the backplane to the SN74GTLP1394 receiver card that converts it back to LVTTL logic levels.

The monitored receiver card has SMB jacks to monitor selected signals:

- ❑ TP1 GTLP level Group 1, bit 1
- ❑ TP2 GTLP level Group 2, bit 1
- ❑ TP3 GTLP level Group 3, bit 1
- ❑ TP4 GTLP level Group 4, bit 1
- ❑ TP5 GTLP level Group 5, bit 1
- ❑ TP6 GTLP level Group 6, bit 1
- ❑ TP7 LVTTL level Group 1, bit 1
- ❑ TP8 LVTTL level Group 2, bit 1
- ❑ TP9 LVTTL level Group 3, bit 1
- ❑ TP10 LVTTL level Group 4, bit 1
- ❑ TP11 LVTTL level Group 5, bit 1
- ❑ TP12 LVTTL level Group 6, bit 1
- ❑ TP13 LVTTL level GTLP latch clock

Figure 2–22. GTLP EVM Monitored Receiver Card



Note:

SN74GTL1655 devices were used on the receiver cards. The SN74GTLPH1655 was in development and initial preproduction samples were used for the driver cards, but insufficient quantities were available for the receiver cards. The SN74GTL1655 and SN74GTLPH1655 are identical, except for the B-port output edge rate (slew) and B-port C_{io}. Because the GTLP signals only are received by the receiver cards, it is essentially immaterial which devices are used on the receiver cards, because both have the same differential input (except for the difference in B-port C_{io}, which is 6 pF typical and 8 pF maximum for the SN74GTL1655, and 8.5 pF typical and 10.5 pF maximum for the SN74GTLPH1655). GTLP devices have a larger B-port C_{io}, because a larger transistor and ESD cell is required by the newer CMOS process.

2.13 Backplane Setup

2.13.1 Insertion of Clock Cards

The clock-card connectors (see Figure 2–23) use AMP 55-pin, 2-mm, HM connectors and are identical to the backplane termination-card connectors. They can be mated improperly because they are keyed only on one side, whereas the backplane connectors are keyed in the center and do not allow improper insertion.

CAUTION

The clock card should be inserted or removed from the backplane only after power has been disconnected, to prevent damage to the CDC components.

Figure 2–23. AMP Z-PACK™, 2-mm, 55-Pin, HM Male (Left) and Female (Right) Clock-Card Connectors

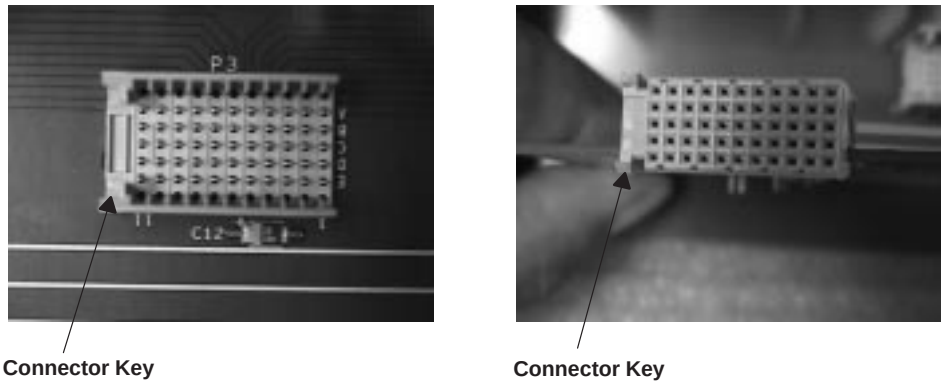


Figure 2–24 shows the mating sequence. When mated, the connectors should be firm with no lines showing. Some rocking action might be required to seat or remove the connectors, but should be minimal to prevent bending the pins.

Figure 2–24. Connector Premate (Left), Mating (Center), and Mated (Right)

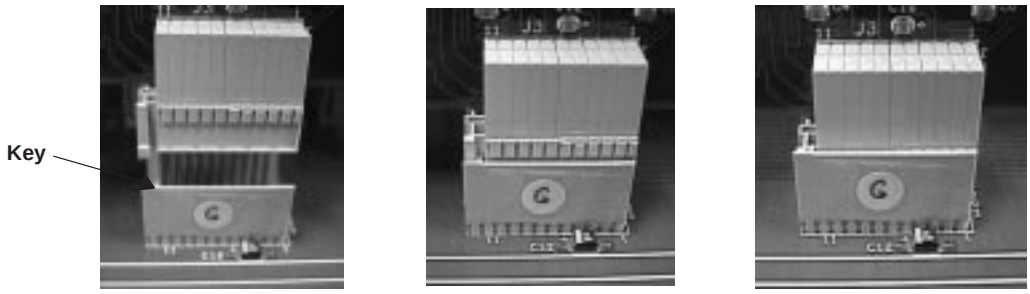
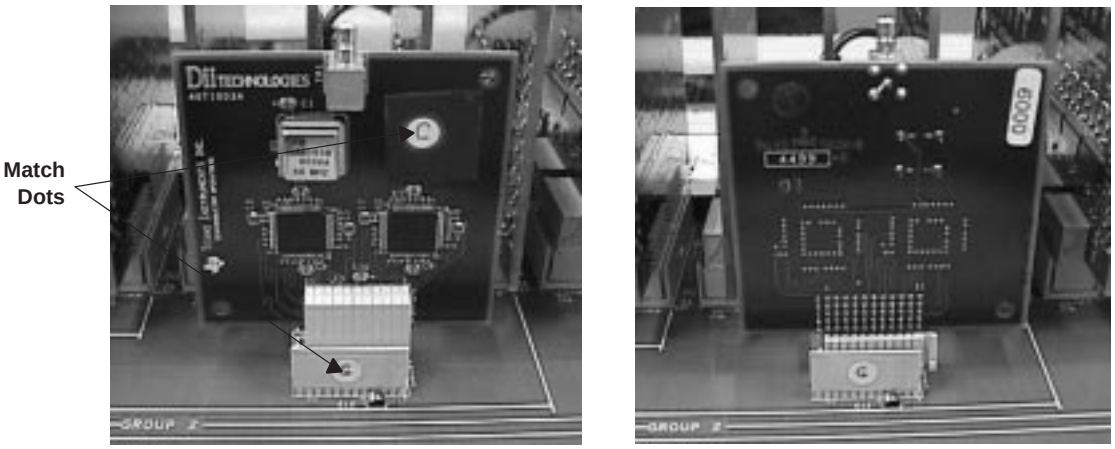


Figure 2–25 (left) shows the clock card properly inserted, with the CDC components and the clock crystal facing away from the backplane connectors and daughter cards. Yellow dots are located on the connector and the card to help ensure proper orientation. Figure 2–25 (right) shows the card improperly inserted.

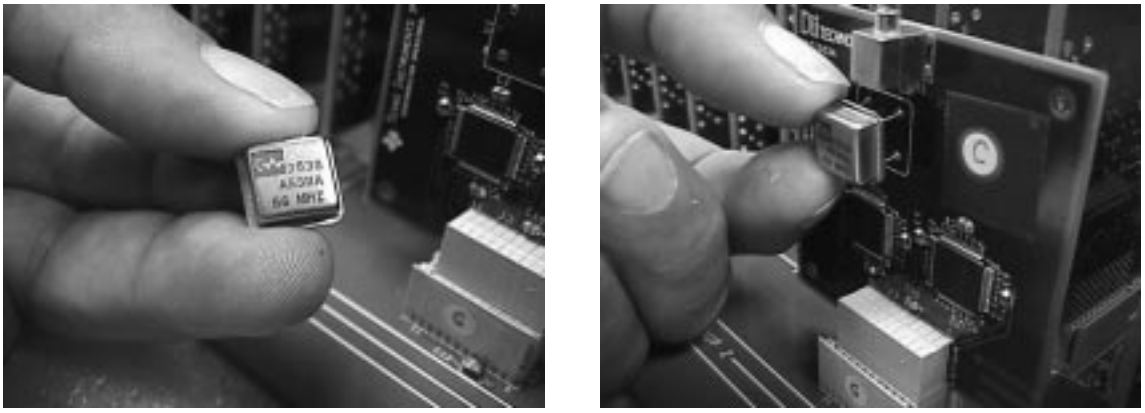
Figure 2–25. Clock Card Properly (Left) and Improperly (Right) Inserted



2.13.2 Insertion of Clock Crystals

Clock crystals are live insertable, unlike the clock card, which is not live insertable. Clock crystals are inserted easily on the clock card by pulling off one crystal and inserting the new crystal (see Figure 2–26). The leads can be bent gently to ease insertion. The clock crystal need not be inserted fully flush with the card for proper operation. In fact, this condition is preferred if the clock card is stored with the crystal inserted, otherwise, the foam liner can bend the exposed leads.

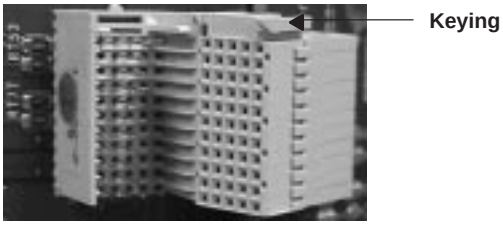
Figure 2–26. Clock Crystal Removal (Left) and Insertion (Right)



2.13.3 Insertion of Termination Cards

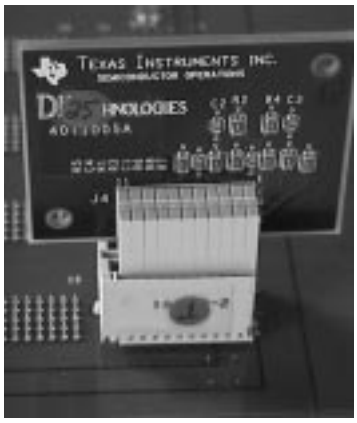
Termination-card, AMP Z-PACK, 2-mm, 55-pin, HM male and female connectors are identical to the clock-card connectors, and are inserted directly onto the K and T pins used for slots 1 and 20, V_{CC}, and data bits. Although the termination card connectors are keyed on the top (see Figure 2–27), they can be inserted backward because they are keyed on only one side.

Figure 2–27. Termination-Card Keying



Be sure that the red dot on the male connector and the card are facing each other, to prevent improper operation. Both termination-card components face the same direction, toward slot 20, so the key to proper operation is to inspect for the keying and line up the red dots (see Figure 2–28). If the backplane is not working, the proper orientation of the termination cards should be the first thing you check. The cards can be rocked slightly side to side to seat and remove them, but avoid bending the pins.

Figure 2–28. Slot 1 (Left) and Slot 20 (Right) Termination Cards on the Backplane



2.13.4 Insertion of Driver and Receiver Cards

The driver and receiver cards are live insertable and are easy to insert and remove, although some slight side-to-side rocking action might be required. The cards can be inserted into any slot in any order, but only one driver card should be used at any one time. There is no bus contention damage if multiple driver cards are in operation at the same time, this is one key benefit from using the GTLP open-drain technology. Figure 2–29 shows the connector keying that allows the cards to be placed on the connector in only one direction. When inserted properly, the component side of the card faces slot 1.

Figure 2–29. Driver and Receiver Connector Keying

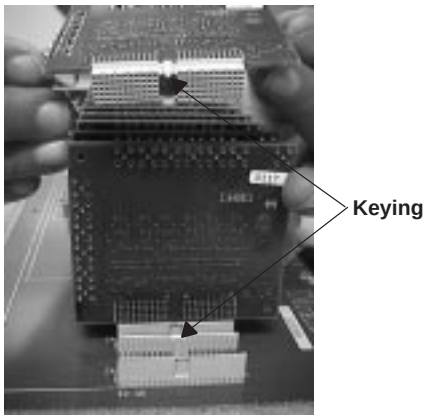
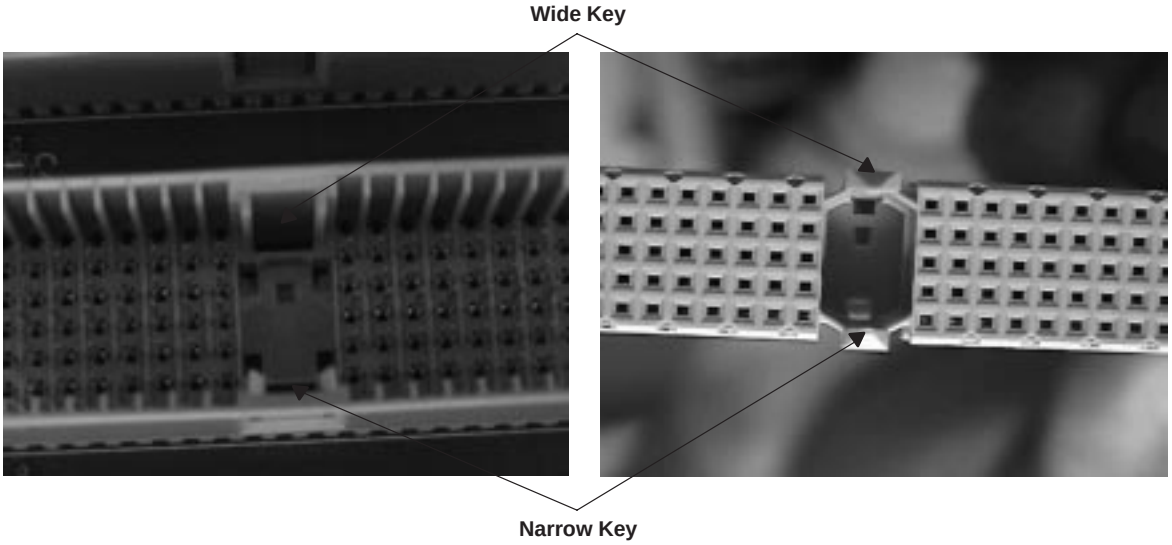


Figure 2–30 shows the keying in more detail. The upper key is wider than the lower key, preventing improper insertion.

Figure 2–30. Close-up View of Connector Keying



The card should be placed squarely on the connector and pressed down (see Figure 2–31), with very little side-to-side motion. The components are facing left towards slot 1, the power supplies are on the top/right, and the Group 1–6 markings are on the bottom/left. The card in Figure 2–31 is being inserted into slot 20.

Figure 2–31. Proper Connector Mating Sequence (Left to Right)

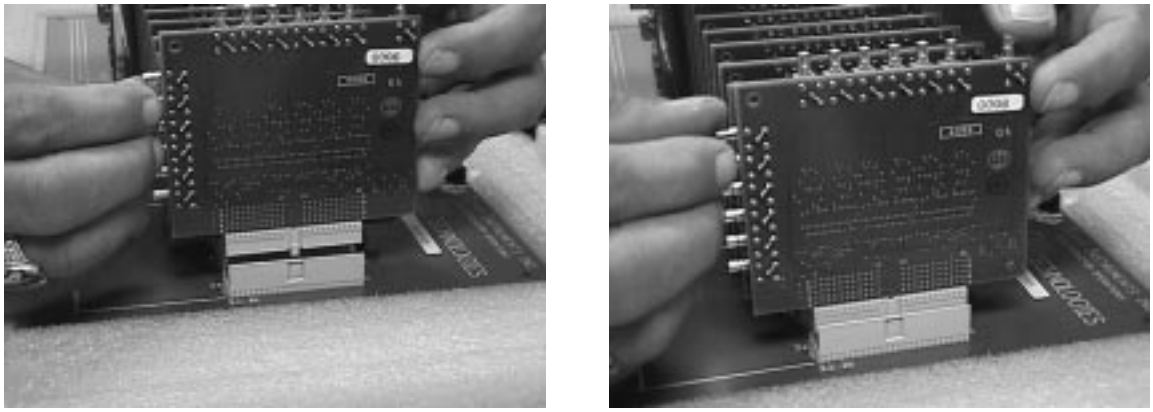
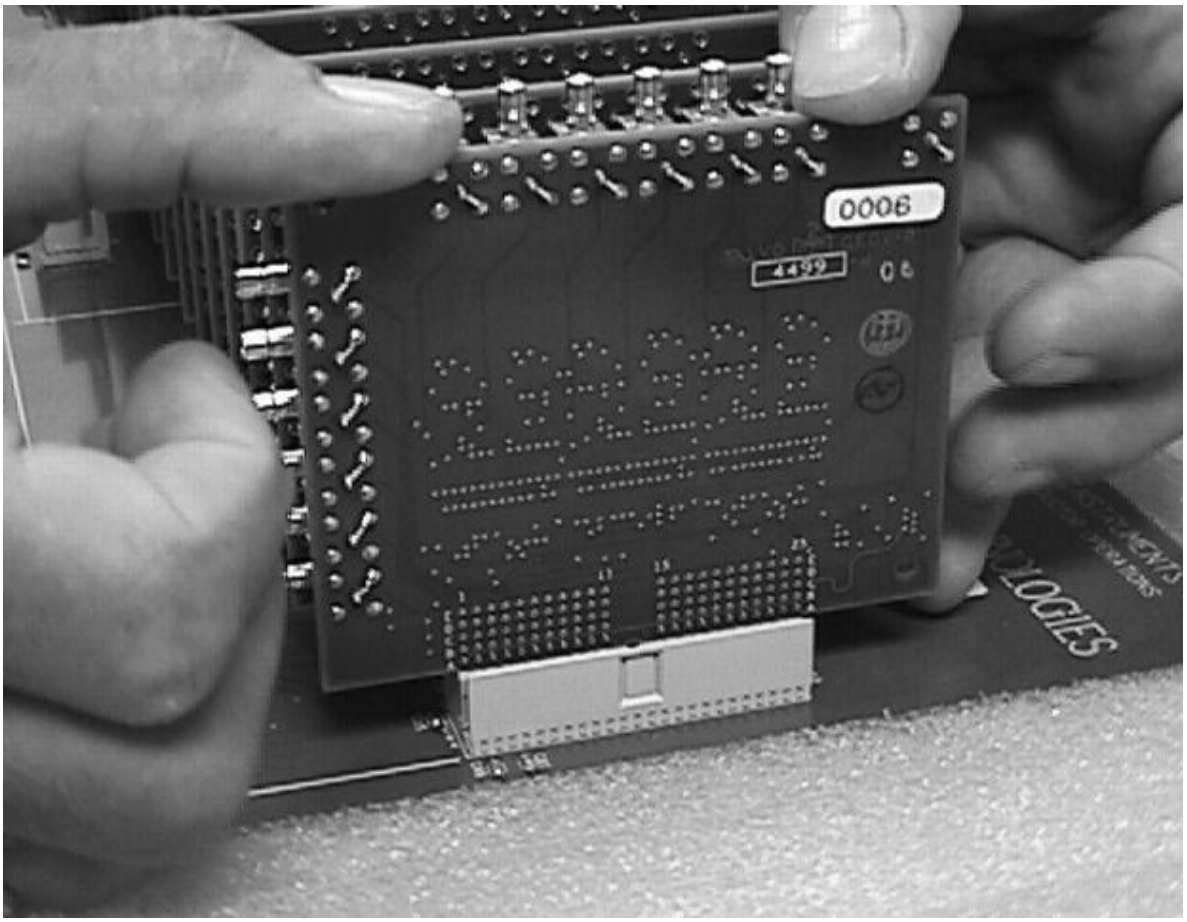


Figure 2–32 shows the connectors properly mated.

Figure 2–32. Connectors Properly Mated



Chapter 3

Oscilloscope Operation

Topic Page

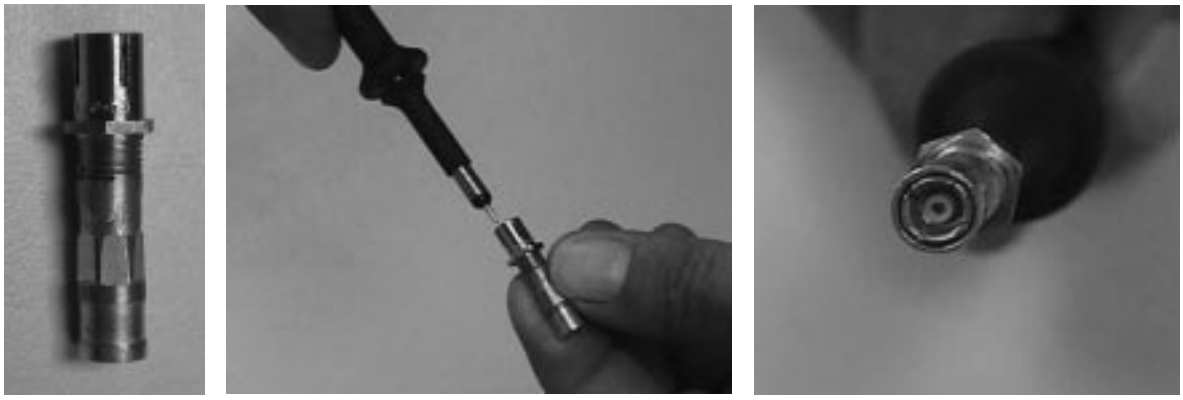
3.1 Oscilloscope Setup

The recommended oscilloscope (O-Scope) for the GTLP EVM is the Tektronix THS730A (see Figure 3–1). It allows only two-channel operation, which should be sufficient for most investigations done with the demonstration backplane.

Figure 3–1. Tektronix O-Scope Front (Left) and Top (Right)

SMB adapters (see Figure 3–2) are needed to properly mate Tektronix probes with the test points. These adapters are custom built for the Tektronix O-Scope probes and are not normally included in the GTLP EVM.

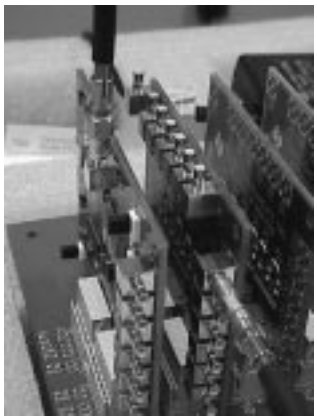
Figure 3–2. O-Scope Probe Monitor-Point Adapters



3.2 Measurements

The first step in taking measurements is to plug one probe into channel 1 (CH 1) of the O-Scope and connect the opposite end to the desired monitor point. Plug the other probe into channel 2 (CH 2) of the O-Scope and connect the opposite end to the desired monitor point (see Figures 3–1 and 3–3). Chapter 4, *Waveform Measurement and Interpretation*, discusses which monitor points should be used and why.

Figure 3–3. Simple Test-Measurement Connection

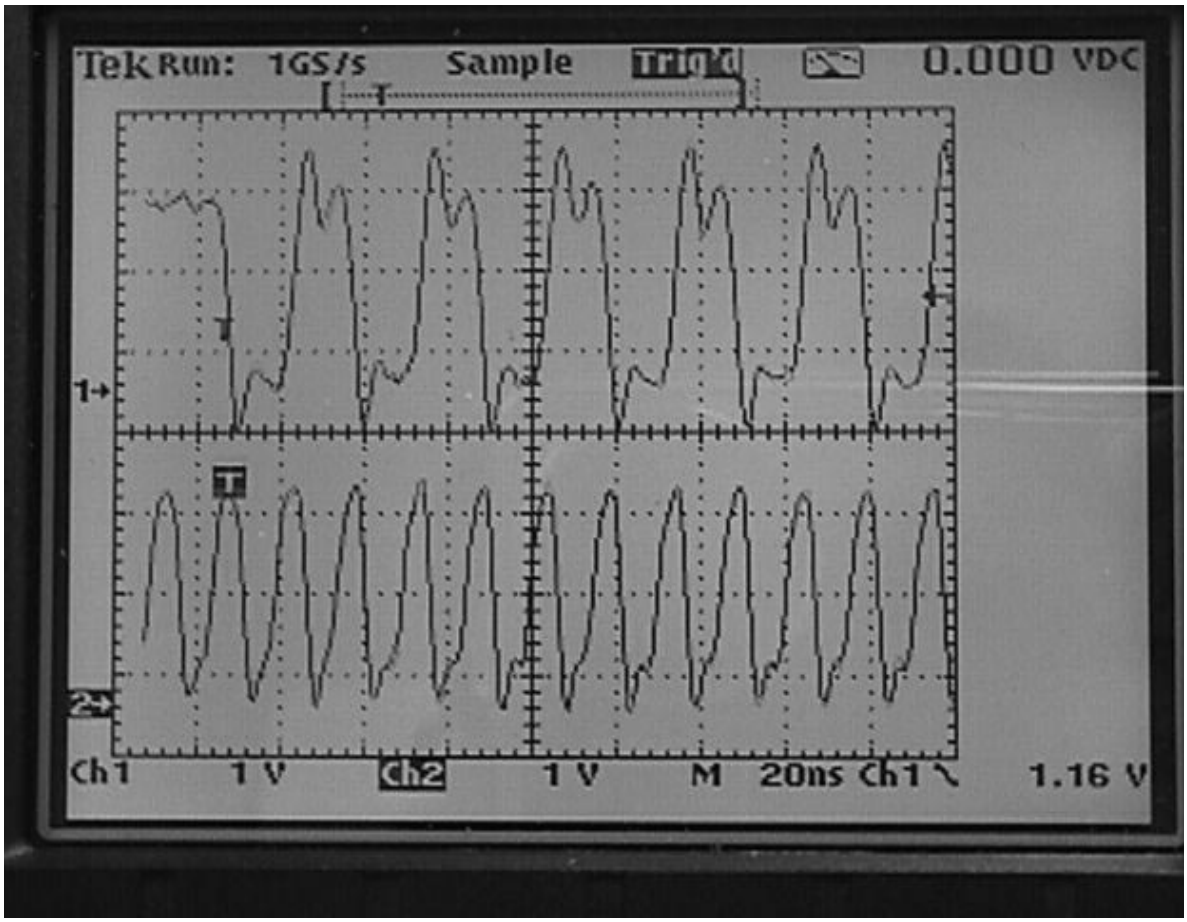


Press the ON/STBY button on the O-Scope (see Figure 3–4), and press the CH 1 or CH 2 button.

Figure 3–4. Turn On O-Scope (Left) and Select Channel (Right)

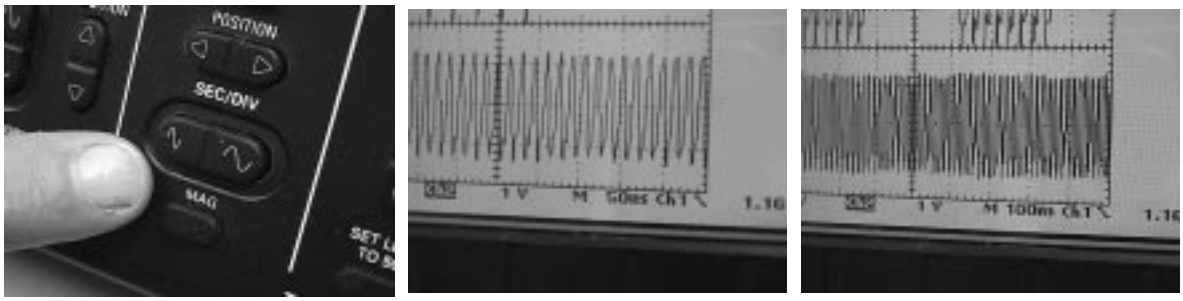
Waveforms similar to those in Figure 3–5, depending on how the O-Scope presets were set, are displayed. In Figure 3–5, CH 2 is selected.

Figure 3–5. O-Scope Display



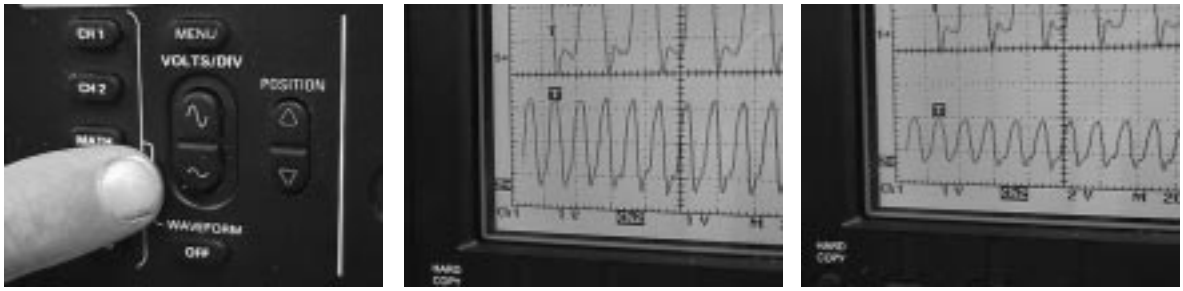
To adjust the timing (x or horizontal axis), press the appropriate side of the SEC/DIV button (see Figure 3–6). An example of the results is shown for 50 ns/division and 100 ns/division. Timing is the same for both channels and is independent of channel selection.

Figure 3–6. Timing Adjustment



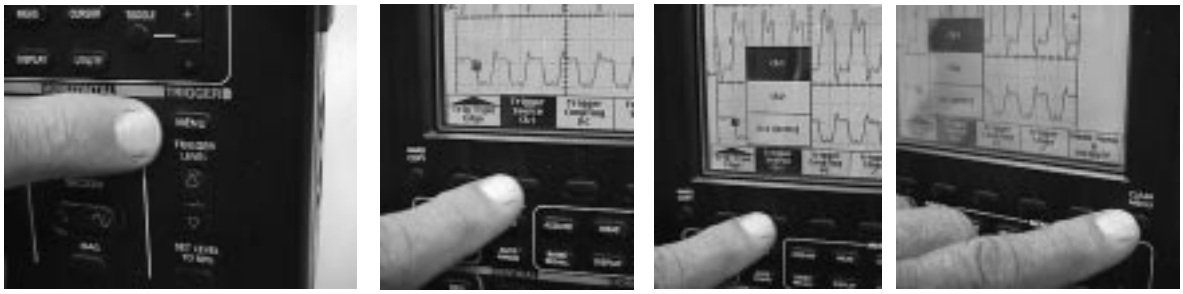
To adjust the voltage (y or vertical axis), press the top or bottom of the VOLTS/DIV button (see Figure 3–7). An example of the results is shown for Ch2 at 1 V (center) and Ch2 at 2 V (right). Voltage adjustment is independent of channels, which are selected by pressing either the CH 1 or the CH 2 button.

Figure 3–7. Voltage Adjustment



To adjust the trigger, press the MENU button (see Figure 3–8), then press Trigger Source to display a submenu. In the submenu, select Ch1, Ch2, or Ext [DMM] by repeatedly pressing the same Trigger Source button. After the appropriate trigger is selected, press the CLEAR MENU button to restore the O-Scope to operation.

Figure 3–8. Trigger Adjustment



Chapter 4

Waveform Measurement and Interpretation

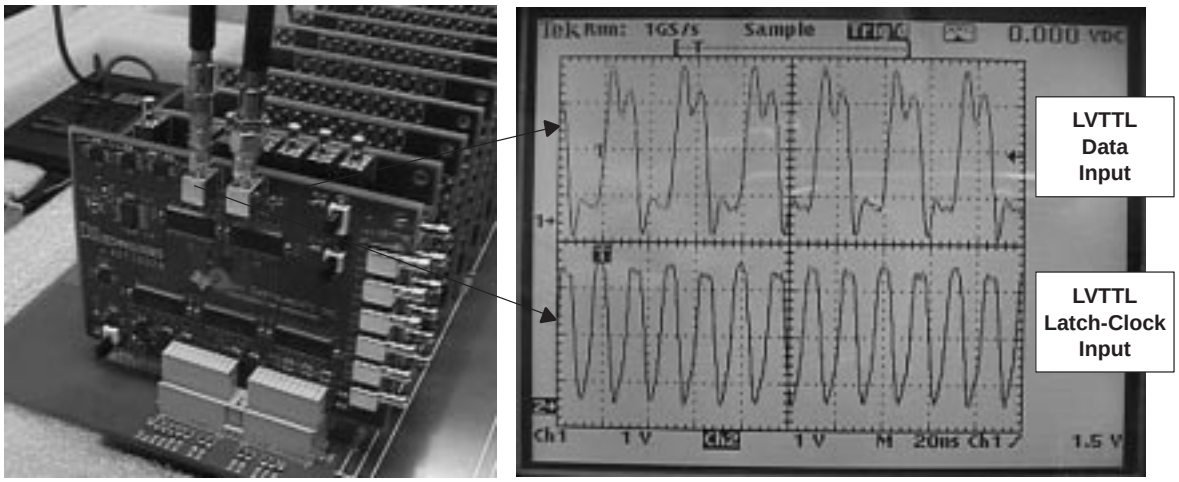
In this chapter, five different measurement cases are discussed in detail, and several more measurement combinations are outlined. Many other combinations are possible.

Topic **Page**

4.1 Timing Relationship of Driver Card (D1) Data Pattern (Ch1) and Driver Card (D1) Latch Clock (Ch2)

Figure 4–1 shows the probe hookup and related O-Scope output for Case 1. The LVTTL latch clock signal goes to the SN74GTLPH1655 driving device CLK pin, and the LVTTL data signal goes to the A-port input pin, specifically the Group 1, bit 1 data signal.

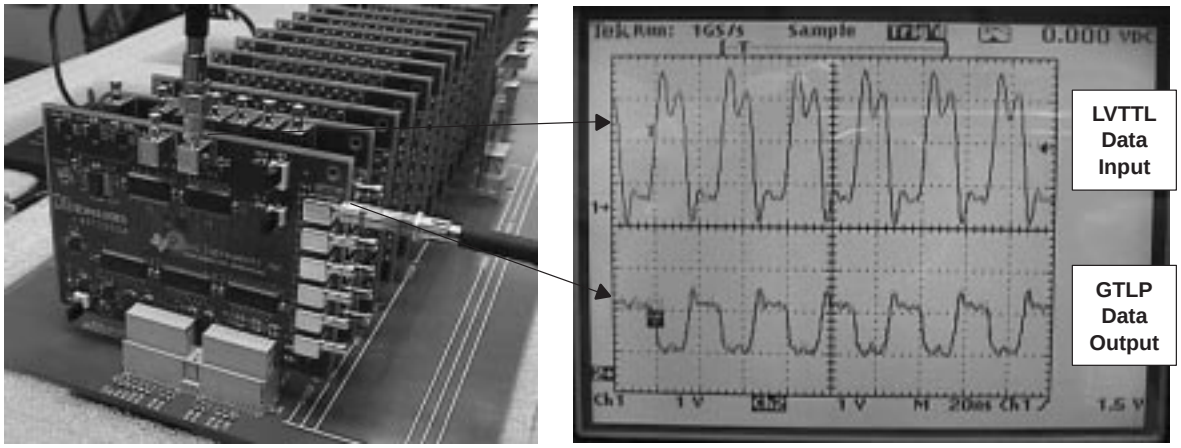
Figure 4–1. Case 1: D1 Data Pattern (Ch1) and D1 Latch Clock (Ch2)



4.2 Timing Relationship of Driver Card (D1) Data Pattern (Ch1) and Driver Card (D1) Group 1 GTLP Data Out (Ch2)

Figure 4–2 shows the probe hookup and O-Scope output for Case 2. The LVTTL data goes into the SN74GTLPH1655 driving device A-port input, and the GTLP data comes out of the B-port output. The driver-card GTLP data output comes out after the rising edge of the clock, in addition to the CLK-to-B propagation delay. This is why the signals look 180 degrees out of phase.

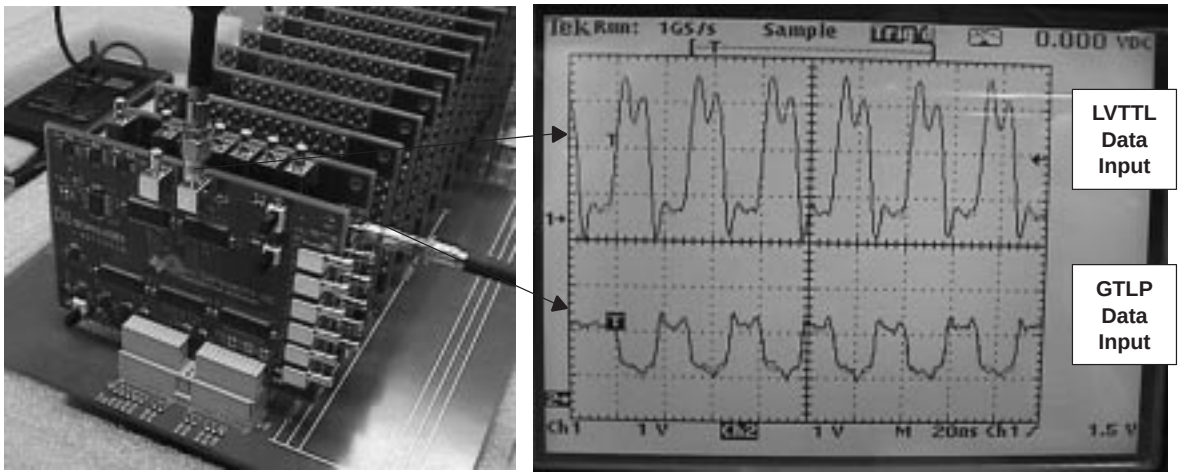
Figure 4–2. Case 2: D1 Data Pattern (Ch1) and D1 Group 1 GTLP Data Out (Ch2)



4.3 Timing Relationship of Driver Card (D1) Data Pattern (Ch1) and Receiver Card (R2) Group 1 GTLP Data In (Ch2)

Figure 4–3 shows the probe hookup and O-Scope output for Case 3. The LVTTL data input goes to the SN74GTLPH1655 driving device A-port input, and the GTLP data input goes to the SN74GTL1655 receiving device B-port in slot 2. These waveforms look similar to those in Figure 4–2, but with slightly more delay caused by the flight time between slots 1 and 2.

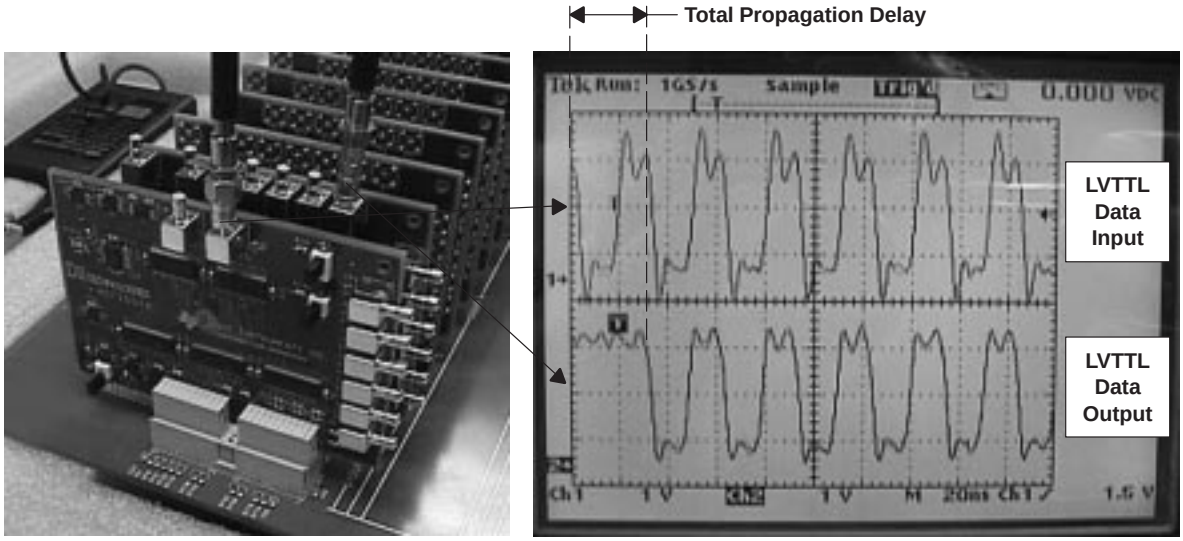
Figure 4–3. Case 3: D1 Data Pattern (Ch1) and R2 Group 1 GTLP Data In (Ch2)



4.4 Timing Relationship of Driver Card (D1) Data Pattern (Ch1) and Receiver Card (R2) Group 1 LVTTL Data Out (Ch2)

Figure 4–4 shows the probe hookup and O-Scope output for Case 4. The LVTTL data input goes to the SN74GTLPH1655 driving device A-port input, and the LVTTL data output of the SN74GTL1655 receiving device goes to A port in slot 2. Because the GTLP EVM is clocked using the central system clock (i.e., clock arrives at all daughter cards at the same time) the total delay from the LVTTL data input on slot 1 to the LVTTL data output on slot 2 is the sum of one clock cycle (20 ns), the setup time on the driver card (~9 ns), and the propagation delay of the GTLPH1655 CLK to A of about 3 ns. The GTLP EVM driver card is set up to transmit sixteen bits of data and then wait eight cycles before transmitting again. This allows the technician to determine the total delay. In this case, assuming the waveform in Ch1 had just started, the total delay is about 32 ns.

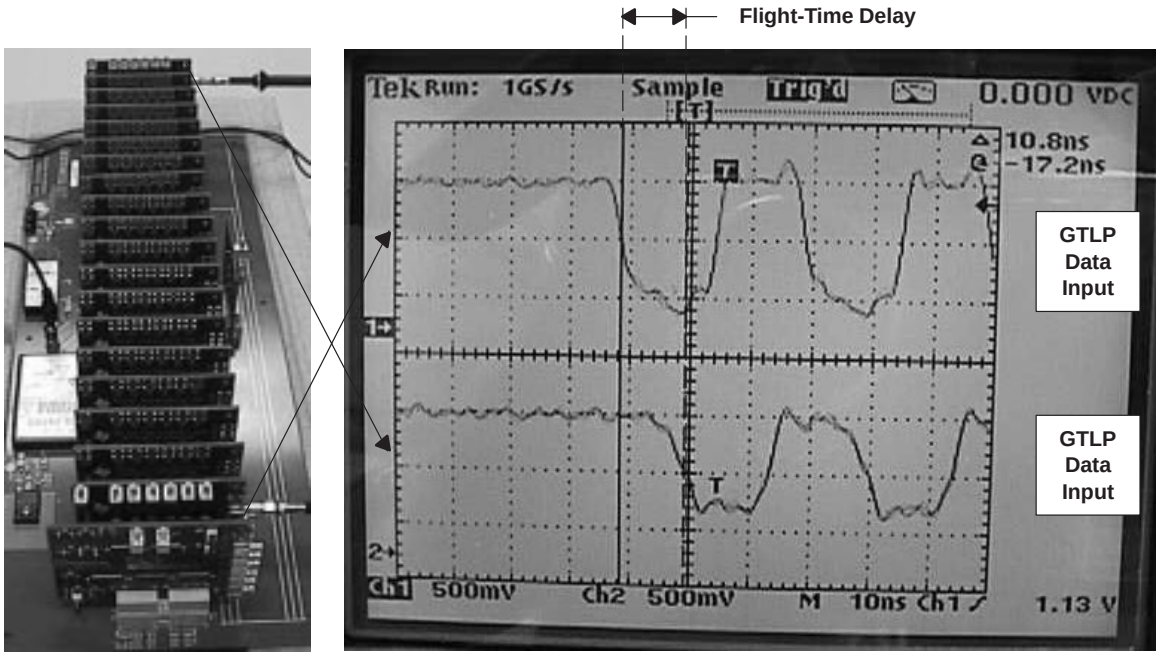
Figure 4–4. Case 4: D1 Data Pattern (Ch1) and R2 Group 1 LVTTL Data Out (Ch2)



4.5 Timing Relationship of Receiver Card (R2) Group 1 GTLP Data In (Ch1) and Receiver Card (R20) Group 1 GTLP Data In (Ch2)

Figure 4–5 shows the probe hookup and O-Scope output for Case 5. You can see the flight-time delay between the output of the SN74GTLPH1655 driving device B port in slot 1 and the SN74GTL1655 receiving device B port in slot 20. Total flight time is about 9 ns.

Figure 4–5. Case 5: R2 Group 1 GTLP Data In (Ch1) and R20 Group 1 GTLP Data In (Ch2)



4.6 Monitored Waveforms

There are differences in waveforms between GTLP monitor test points and measurements taken at the backplane connector pins, due to interference from LVTTL data and clock signals not shielded adequately on the daughter cards. This concern is only for this demonstration backplane because there is no reason to extend the GTLP signals past the GTLP device B-port output pins on operational daughter cards. Figures 4–6 and 4–7 show the difference between waveforms taken directly on the backplane and those taken from the monitor test points under fully loaded conditions at a clock frequency of 23 MHz. Waveforms shown in Figures 4–6 and 4–7 are at one-half clock frequency, or 11.5 MHz, and are taken with various termination cards.

Figure 4–6. GTLP Backplane Waveforms at 23-MHz Clock Frequency

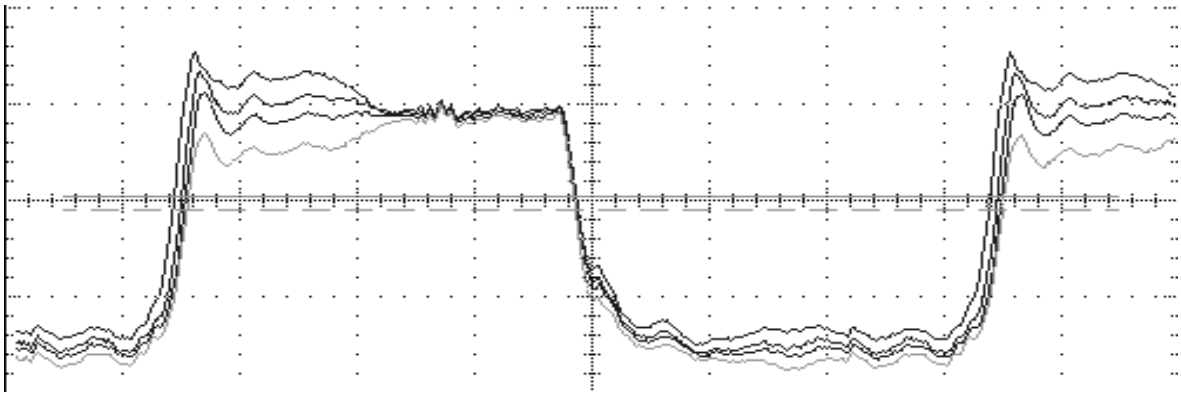
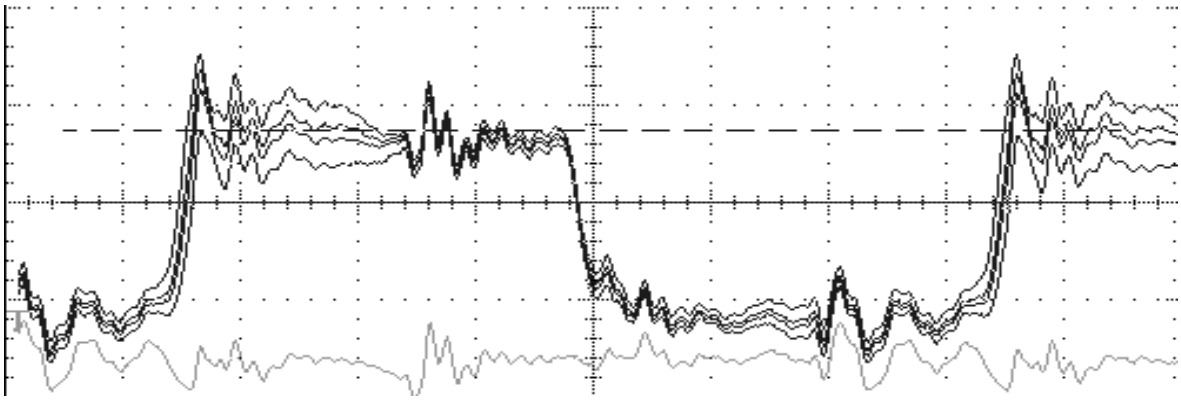


Figure 4–7. GTLP Monitor Test-Point Waveforms at 23-MHz Clock Frequency



Chapter 5

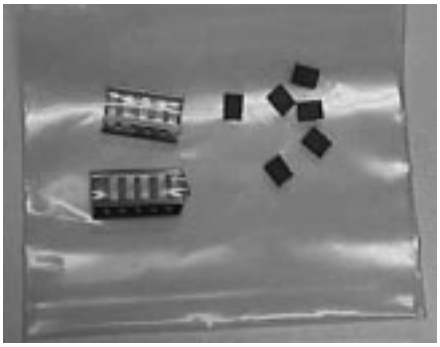
Troubleshooting

Topic | Page

5.1 Spare Parts

Each EVM is equipped with spare fuses and jumpers (see Figure 5–1).

Figure 5–1. Spare Fuses and Jumpers

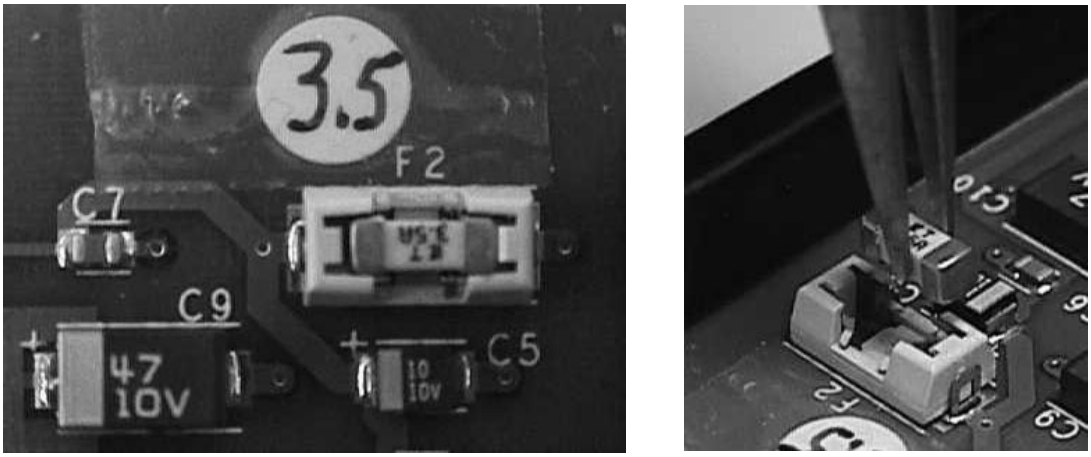


5.2 Replacing 5-A Fuse F2

Fuse F2 (see Figure 5–2) provides power from the 3.3-V switching regulator to the 3.3-V power plane and blows if V_{CC} is shorted to GND. Shorting can occur if a connector pin is bent during insertion or if measurements are taken directly from the backplane.

F2 can be replaced easily with one of the spare fuses. Simply disconnect power from the board, and pull out the fuse with pliers (see Figure 5–2). Push in the new fuse, and reconnect the power supply.

Figure 5–2. Fuse F2 (Left) and Removal Procedure (Right)



5.3 Replacing 2.5-A Fuse F1

Fuse F1 (see Figure 5–3) provides power from the power supply to the 3.3-V and 5-V switching regulators and blows if the switching regulators fail. It is replaced as easily as fuse F2. Disconnect the power from the board, pull out the fuse with pliers, push in the new fuse, then reconnect the power supply.

Figure 5–3. Fuse F1

5.4 Damage to the Daughter Cards

The daughter cards are not field repairable and must be returned to the factory for repair.

Appendix A

Bill of Materials, Schematics, Board Layouts, and Suggested Specifications

Topic Page

A.1 GTLP EVM Bill of Materials

❑ Backplane

Device Type	Quantity
Z-PAK 110-Pin Male Connector	20
Z-PAK 55-Pin Male Connector	1
2.5 AMP Fuseholder	1
5 AMP Fuseholder	1
Surface Mount 0.01uF Cap	3
Surface Mount 0.1uF Cap	75
Surface Mount Tantalum 10uF/10V Cap	4
Surface Mount Tantalum 1uF/35V Cap	2
Surface Mount Tantalum 47uF/10V Cap	2
Surface Mount 100 ohm Resistor	1
Surface Mount 120 ohm Resistor	1
Surface Mount 1.5K ohm Resistor	1
Surface Mount 20 ohm Resistor	1
Surface Mount 240 ohm Resistor	1
Surface Mount 25 ohm Resistor	1
Green LED	2
Red LED	1
LT1083CP Voltage Regulator	1
Powerjack	1
24V-to-5V DC-to-DC Converter	1
24V-to-3.3V DC-to-DC Converter	1

- Clock Driver Card

Device Type	Quantity
Z-PAK 55-Pin Female Connector	1
CDC2586 TQFP Clock Driver	2
Surface Mount 0.1uF Cap	10
Surface Mount 453 ohm Resistor	1
Oscillator Mount	1
SMB Coax Connector	1

- Termination Card

Device Type	Quantity
Z-PAK 55-Pin Female Connector	1
Surface Mount 0.1uF Cap	4
Surface Mount 25 ohm Resistor	8

- Monitored Receiver Card

Device Type	Quantity
Z-PAK 55-Pin Female Connector	1
10K ohm Resistor Network	6
SN74ALVC126 TVSOP Buffer	1
SN74GTLP1394 TVSOP Transceiver	1
SN74GTL1655 TSSOP UBT	3
Surface Mount 0.1uF Cap	12
Surface Mount 47pF Cap	6
Surface Mount 1K ohm Resistor	1
Surface Mount 2K ohm Resistor	1
Surface Mount 453 ohm Resistor	7
Surface Mount 51.1 ohm Resistor	13
SMB Coax Connector	13

- Monitored Driver Card

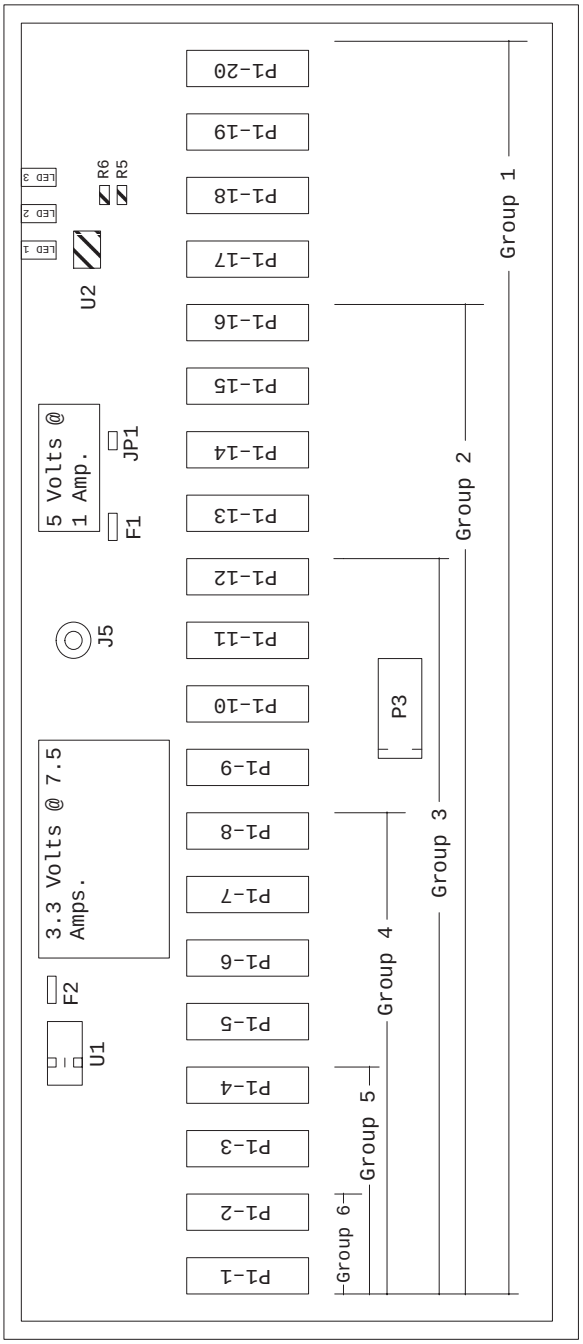
Device Type	Quantity
Z-PAK 55-Pin Female Connector	1
SN74ALVC126 TVSOP Buffer	1
SN74GTLP1394 TVSOP Transceiver	1
SN74GTLPH1655 TSSOP UBT	3
SN74ALVCH16344 TSSOP Buffer	2
CDC351 Clock Buffer	1
SN74LVC112A JK Flip-Flop	3
SN74LVC04 Inverter	1
Surface Mount 0.1uF Cap	23
Surface Mount 47pF Cap	1
Surface Mount 1K ohm Resistor	3
Surface Mount 2K ohm Resistor	1
Surface Mount 500 ohm Resistor	2
Surface Mount 243 ohm Resistor	1
Surface Mount 51.1 ohm Resistor	6
SMB Coax Connector	8

- Unmonitored Receiver Card

Device Type	Quantity
Z-PAK 55-Pin Female Connector	1
10K ohm Resistor Network	6
SN74ALVC126 TVSOP Buffer	1
SN74GTLP1394 TVSOP Transceiver	1
SN74GTL1655 TSSOP UBT	3
Surface Mount 0.1uF Cap	12
Surface Mount 47pF Cap	6
Surface Mount 1K ohm Resistor	1
Surface Mount 2K ohm Resistor	1

A.2 Board Layouts and Schematics

Figure A–1. Backplane Layout, Front Side



U2, R5, and R6 are not installed at this time.

Figure A–2. Backplane Layout, Back Side

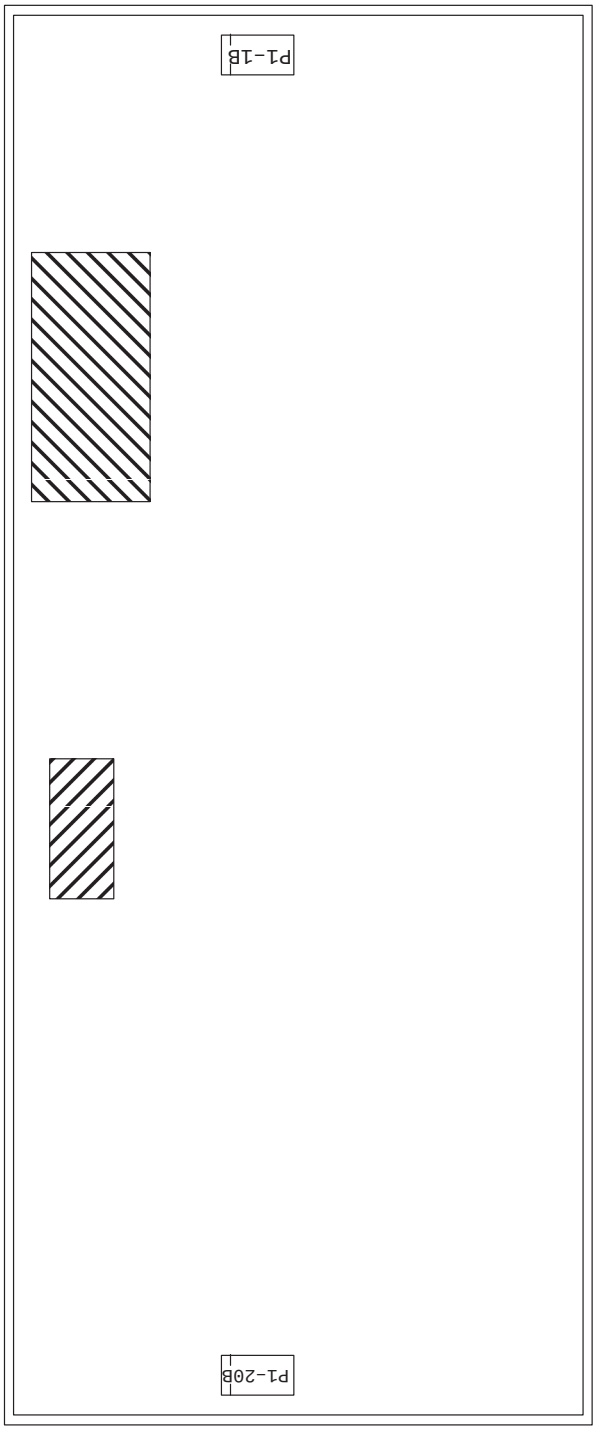


Figure A–3. Driver-Card and Receiver-Card Connector Pinout

P1-X

	A	B	C	D	E
1	Sys. Clk.	GND	GND	5V	5V
2	3.3V	3.3V	GND	3.3V	3.3V
3	G1D3	G1D1	GND	G1D4	G1D2
4	G1D7	G1D5	GND	G1D8	G1D6
5	1.5V	1.5V	GND	1.5V	1.5V
6	G2D3	G2D1	GND	G2D4	G2D2
7	G2D7	G2D5	GND	G2D8	G2D6
8	GND	GND	GND	GND	GND
9	G3D3	G3D1	GND	G3D4	G3D2
10	G3D7	G3D5	GND	G3D8	G3D6
11	GND	GND	GND	GND	GND
15	GND	GND	GND	GND	GND
16	G4D3	G4D1	GND	G4D4	G4D2
17	G4D7	G4D5	GND	G4D8	G4D6
18	GND	GND	GND	GND	GND
19	G5D3	G5D1	GND	G5D4	G5D2
20	G5D7	G5D5	GND	G5D8	G5D6
21	GND	GND	GND	GND	GND
22	G6D3	G6D1	GND	G6D4	G6D2
23	G6D7	G6D5	GND	G6D8	G6D6
24	GND	GND	GND	GND	GND
25	MODESEL	GND	GND	GND	GTL Clk.

P1-1B and P1-20B

	E	D	C	B	A
1		GND	GND		5V
2	3.3V		GND	3.3V	3.3V
3	G1D3	G1D1	GND	G1D4	G1D2
4	G1D7	G1D5	GND	G1D8	G1D6
5	1.5V	1.5V	GND	1.5V	1.5V
6			GND		
7			GND		
8	GND	GND	GND	GND	GND
9			GND		
10			GND		
11	GND	GND	GND	GND	GND

P3

	A	B	C	D	E
1	Clk.Out 20	GND	GND	GND	MODESEL
2	Clk.Out 18	Clk.Out 19	GND	GND	GND
3	Clk.Out 16	Clk.Out 17	GND	GND	GND
4	Clk.Out 14	Clk.Out 15	GND	GND	GND
5	Clk.Out 12	Clk.Out 13	GND	GND	GND
6	Clk.Out 10	Clk.Out 11	GND	GND	5V
7	Clk.Out 8	Clk.Out 9	GND	GND	GND
8	Clk.Out 6	Clk.Out 7	GND	GND	GND
9	Clk.Out 4	Clk.Out 5	GND	GND	GND
10	Clk.Out 2	Clk.Out 3	GND	GND	3.3V
11	Clk.Out 1	GND	GND	GND	3.3V

Figure A–4. Backplane Schematic

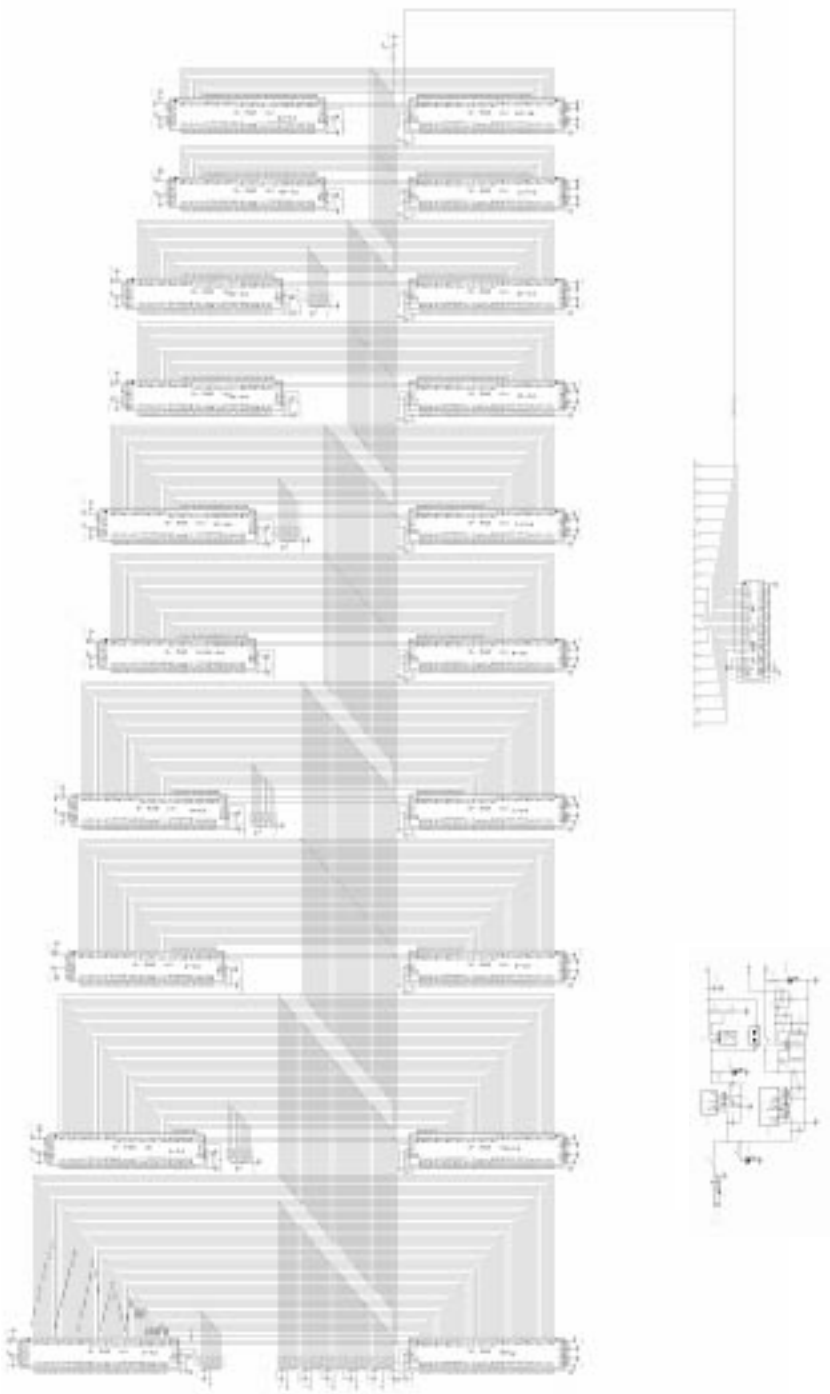


Figure A–5. Driver-Card Layout

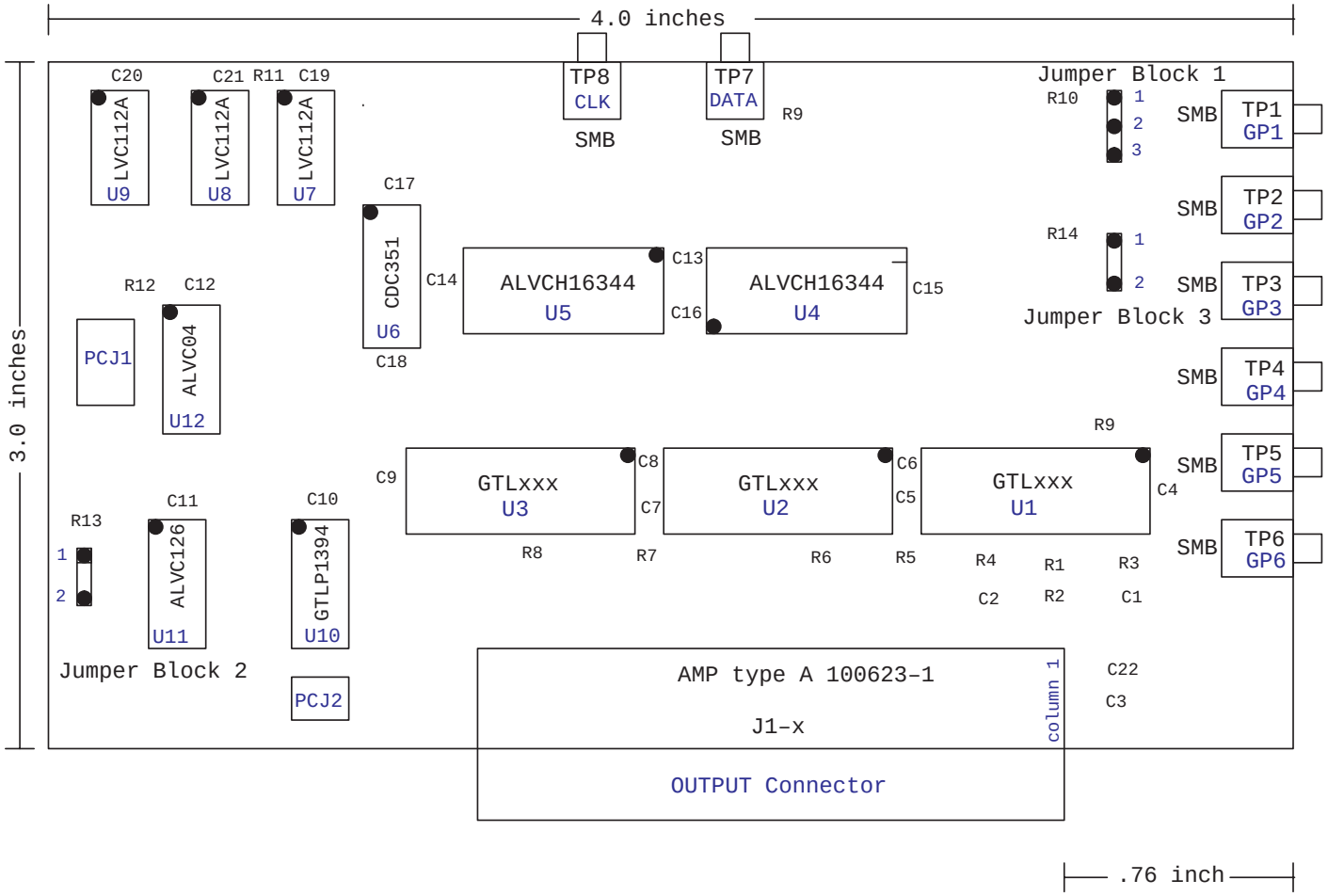


Figure A–6. Driver-Card Schematic

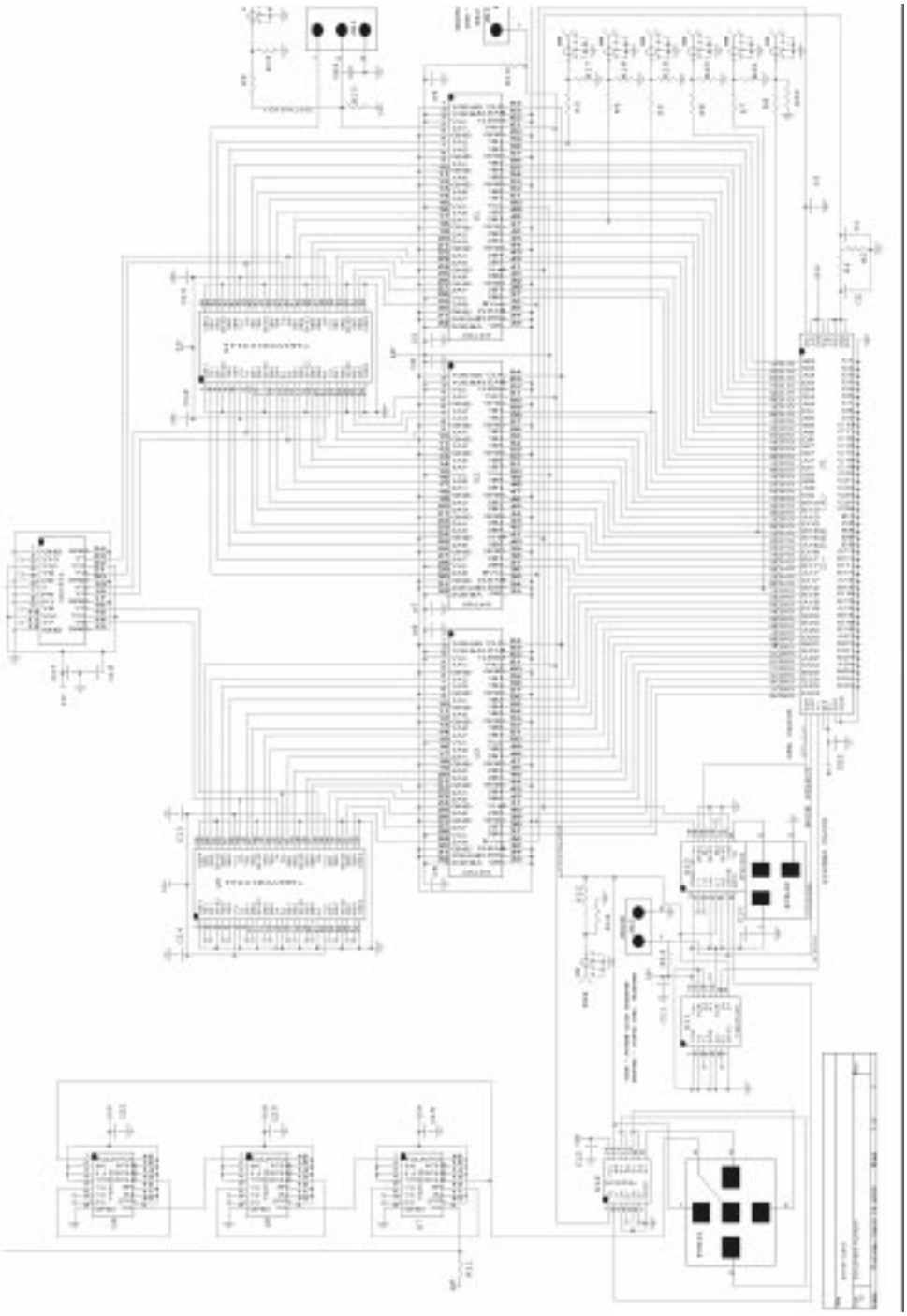


Figure A–7. Unmonitored-Receiver Card Layout

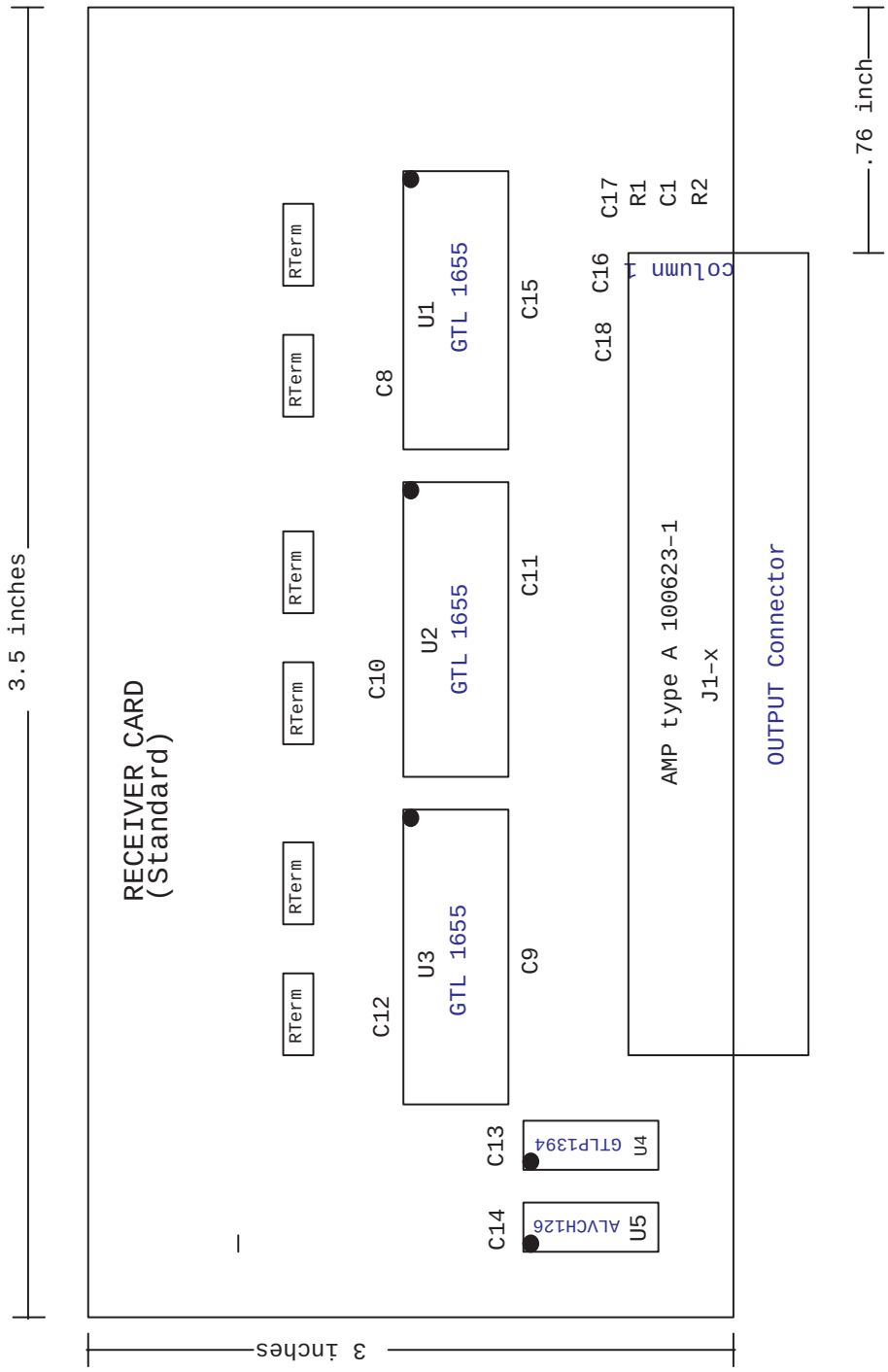


Figure A–8. Monitored-Receiver Card Layout

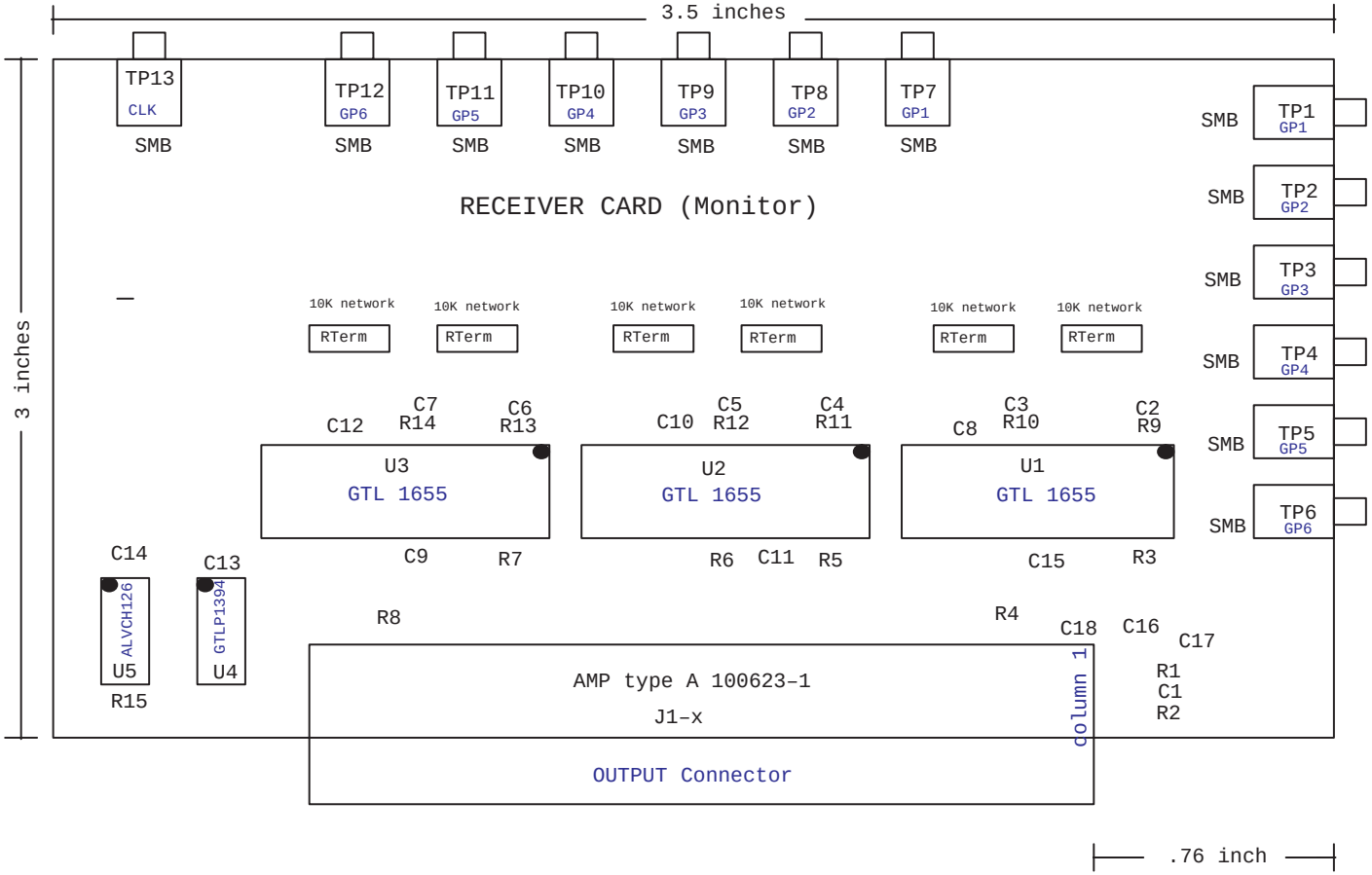


Figure A–9. Receiver-Card Schematic

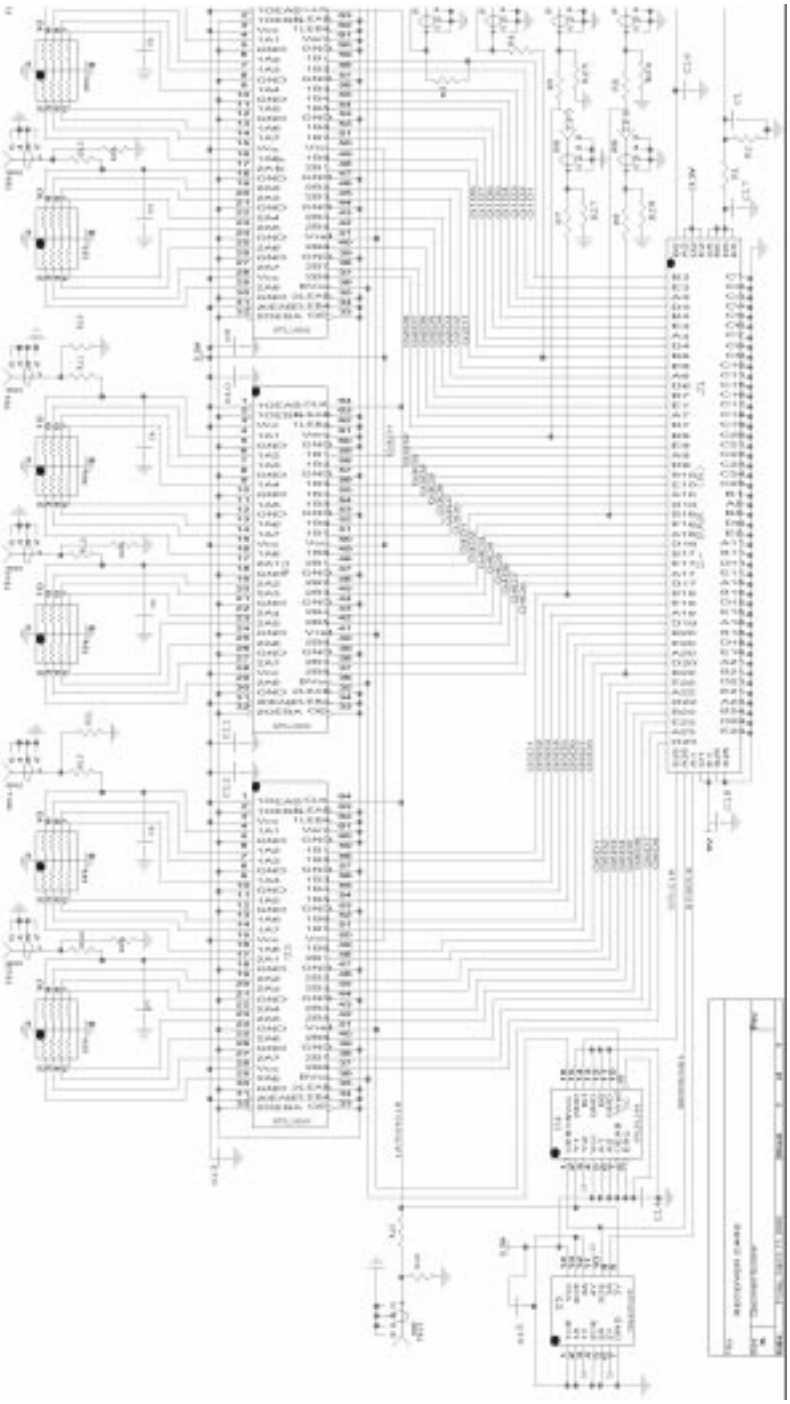


Figure A–10. Clock-Card Layout

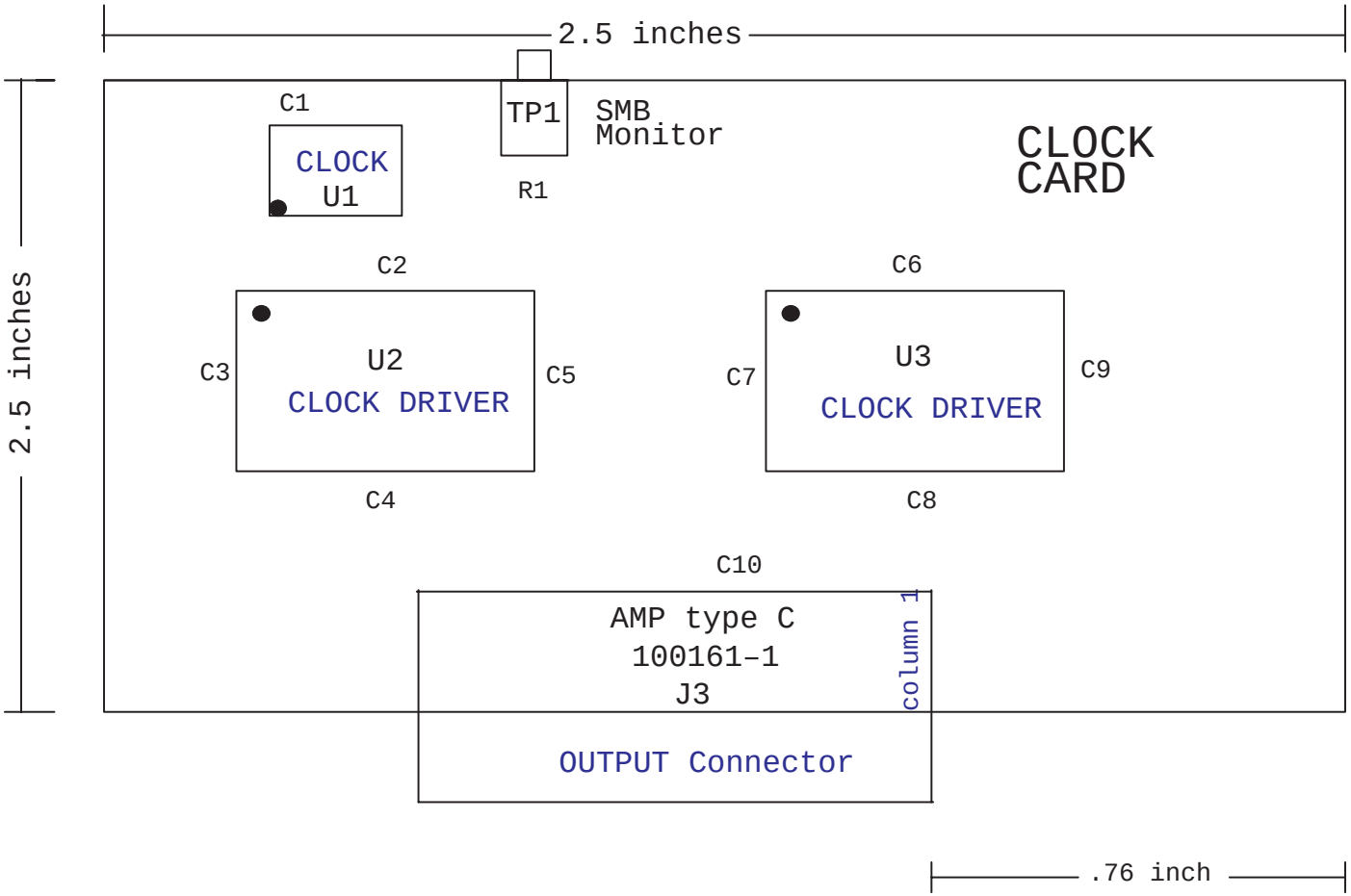


Figure A–11. Clock-Card Schematic

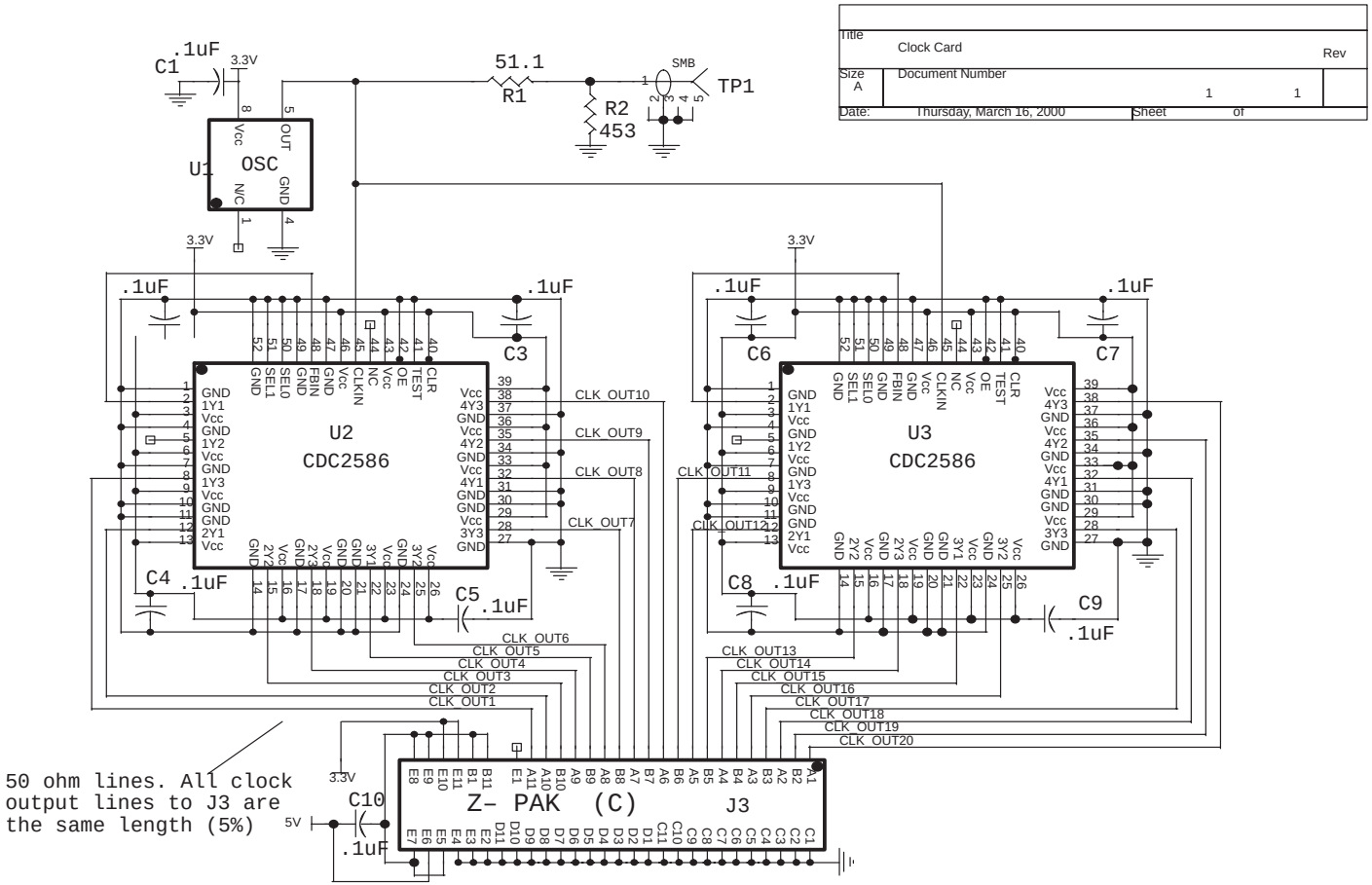


Figure A–12. Resistor-Termination-Card Layout

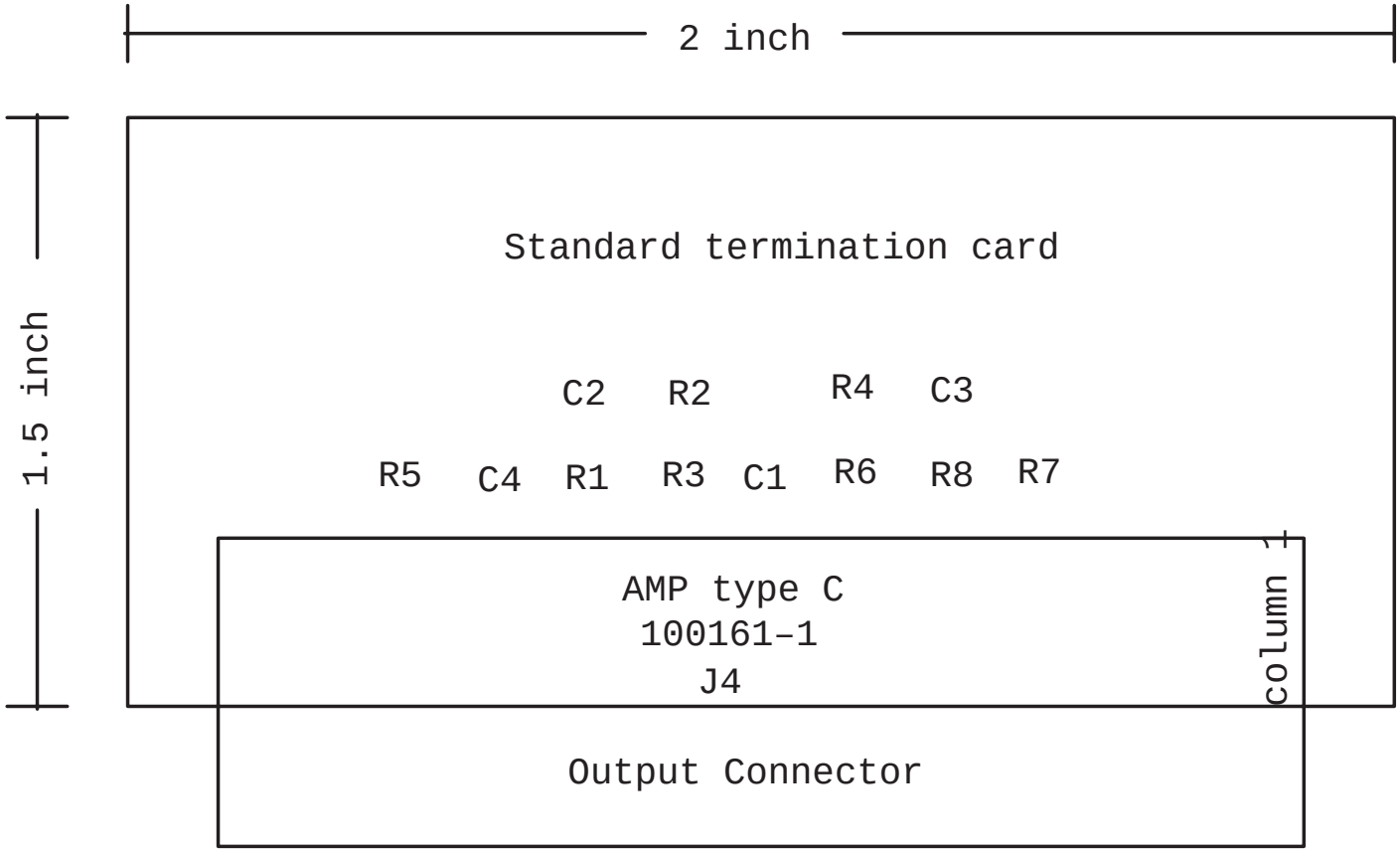
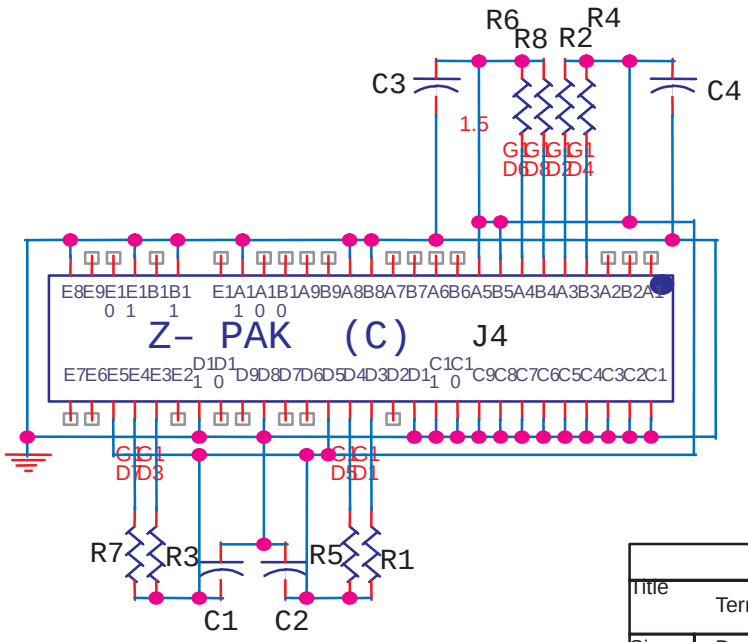


Figure A–13. Standard-Termination-Card Schematic



Title	Termination Card		
Size A	Document Number		Rev
Date: Wednesday, December 08, 1999	Sheet 1 of 1		

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: SN 74GTLPH32945 DGG R

Prefix

SN = Standard prefix
SNJ = Compliant to MIL-PRF-38535 (QML)

Unique Circuit Description

MUST CONTAIN EIGHT TO TWELVE CHARACTERS

Examples: 74FB1650
74GTLP2033
74GTLPH32945

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DGG, PW = plastic thin shrink small-outline package
DGV = plastic thin very small-outline package
DL = plastic shrink small-outline package
GKE, GKF = plastic ball-grid array
PCA = plastic thin quad flatpack
RC = plastic quad flatpack
WD = ceramic dual flatpack
(from pin-connection diagram on individual data sheet)

NOTE: For order entry for some devices, the package designation must be abbreviated as indicated on the data sheet.

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE LETTER

R = Standard tape and reel (required for DBB, DGG, and DGV; optional for D, DL, and DW packages)

Table 1. Normal Dimensions of Packing Materials

CARRIER-TAPE WIDTH (mm)	COVER-TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
8	5.4	9.0	178
12	9.2	12.4	330
16	13.3	16.4	330
24	21.0	24.4	330
32	25.5	32.4	330
44	37.5	44.4	330
56	49.5	56.4	330

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions of particular interest to the end user are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).

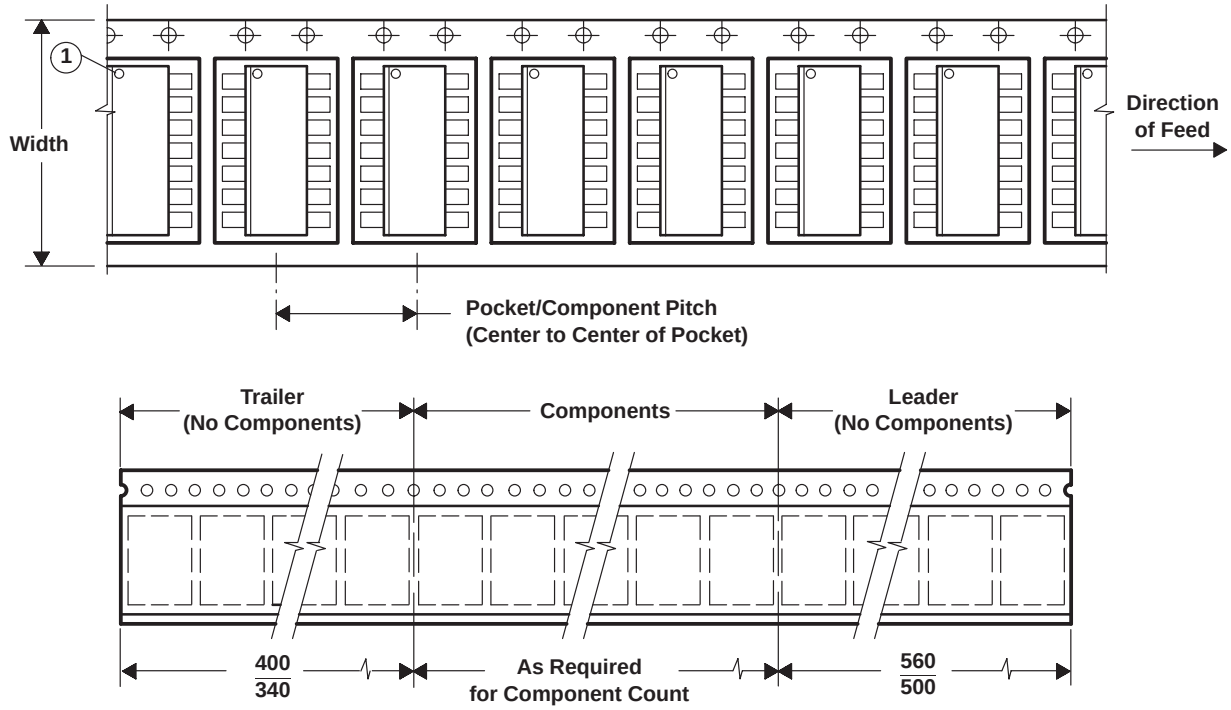


Figure 1. Typical Carrier-Tape Design

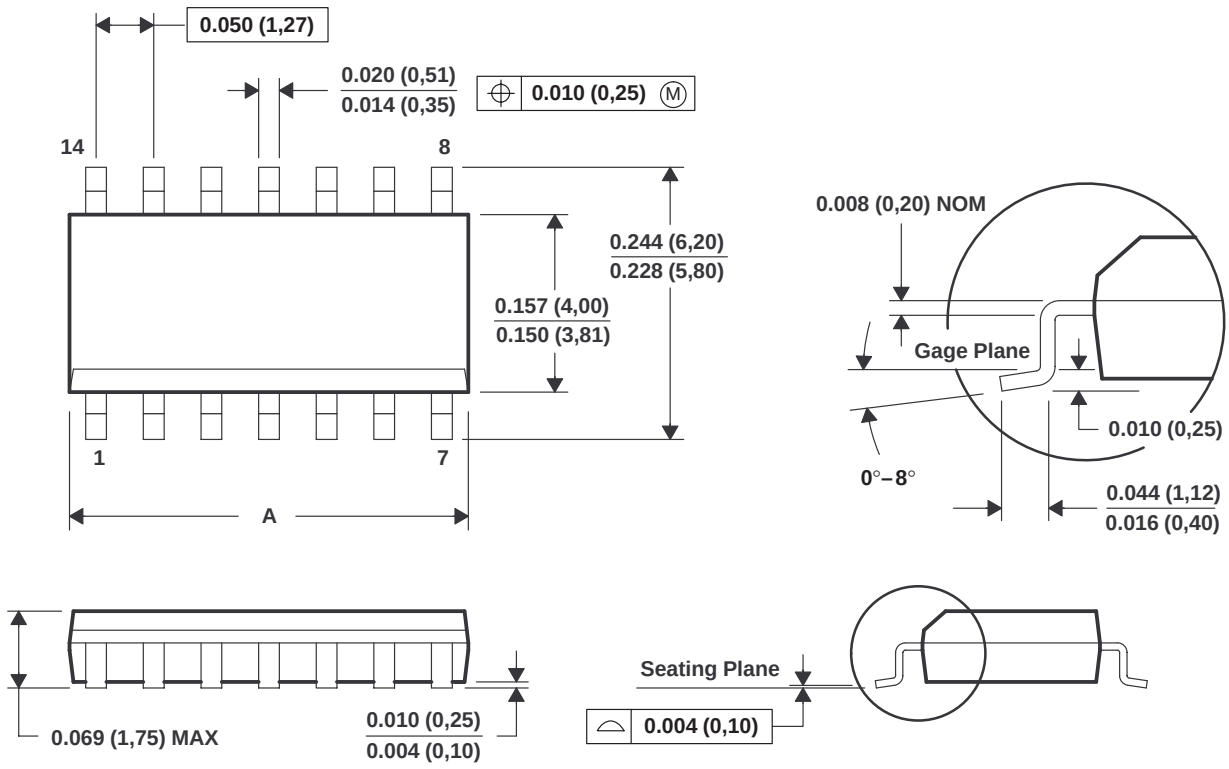
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Table 2. Selected Tape-and-Reel Specifications

PACKAGE		NO. OF PINS	CARRIER-TAPE WIDTH (mm)	POCKET PITCH (mm)	QTY/REEL
SOIC	D	14	16.00	8.00	2500
		16	16.00	8.00	2500
	DW	16	16.00	8.00/12.00	1000
		20	24.00	12.00	1000
SOT	DBV	5	8.00	4.00	3000
	DCK	5	8.00	4.00	3000
SSOP	DB	14	16.00	12.00	2000
		16	16.00	12.00	2000
		20	16.00	12.00	2000
		24	16.00	12.00	2000
	DL	48	32.00	16.00	1000
TSSOP	DGG	48	24.00	12.00	2000
		56	24.00	12.00	2000
		64	24.00	12.00	2000
	PW	8	12.00	8.00	2000
		14	12.00	8.00	2000
		16	12.00	8.00	2000
		20	16.00	8.00	2000
		24	16.00	8.00	2000
		28	16.00	8.00	2000
TVSOP	DBB	80	24.00	12.00	2000
	DGV	14	16.00	8.00	2000
		16	16.00	8.00	2000
		20	16.00	8.00	2000
		24	16.00	8.00	2000
		48	16.00	8.00	2000
		56	24.00	8.00	2000

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



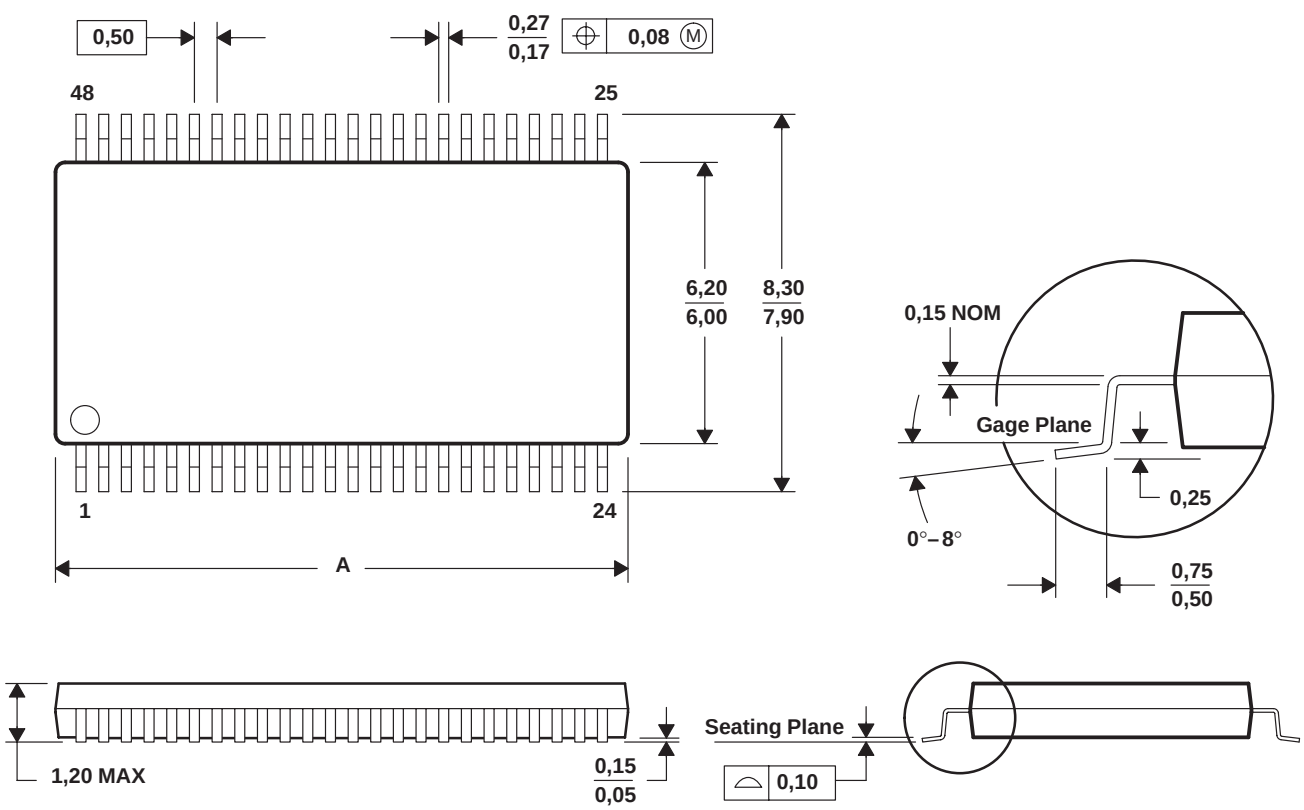
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



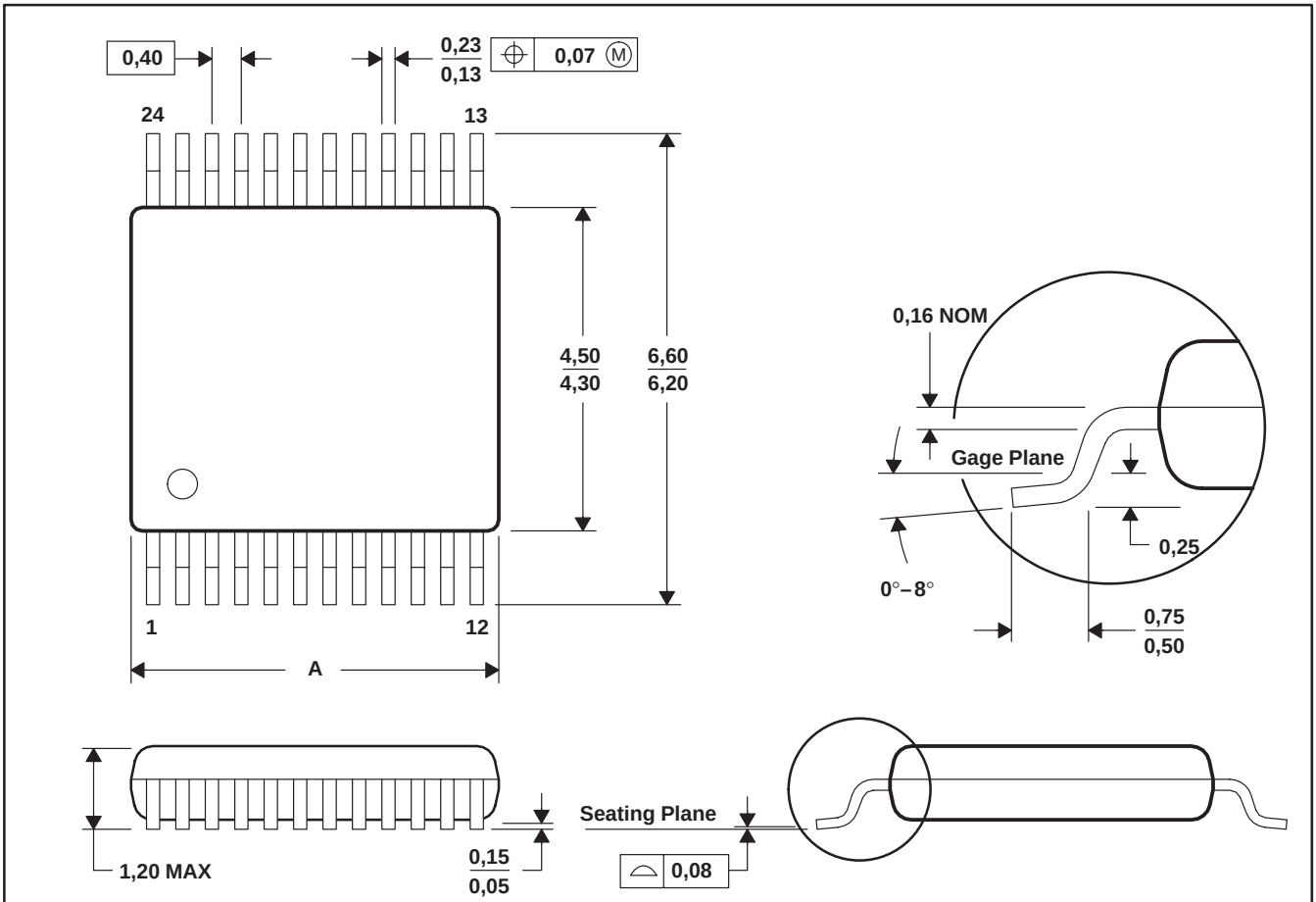
DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



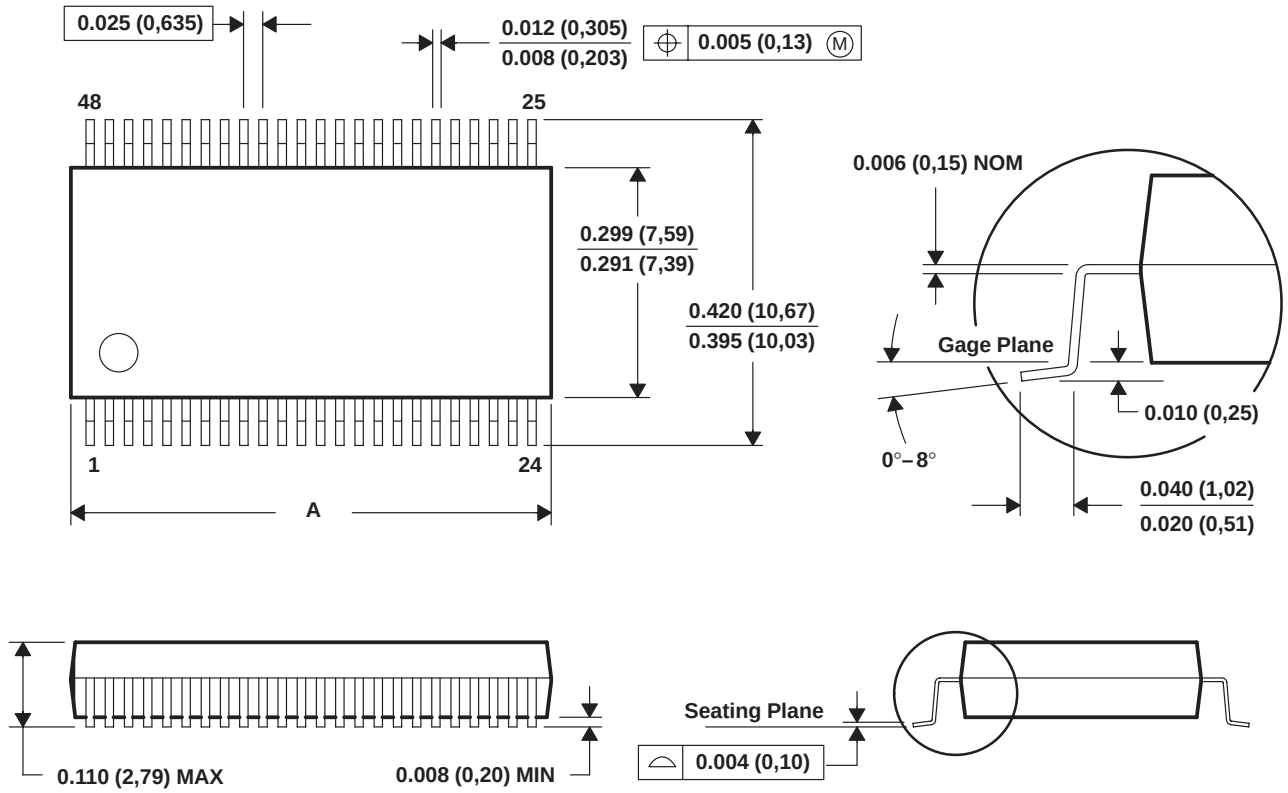
DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



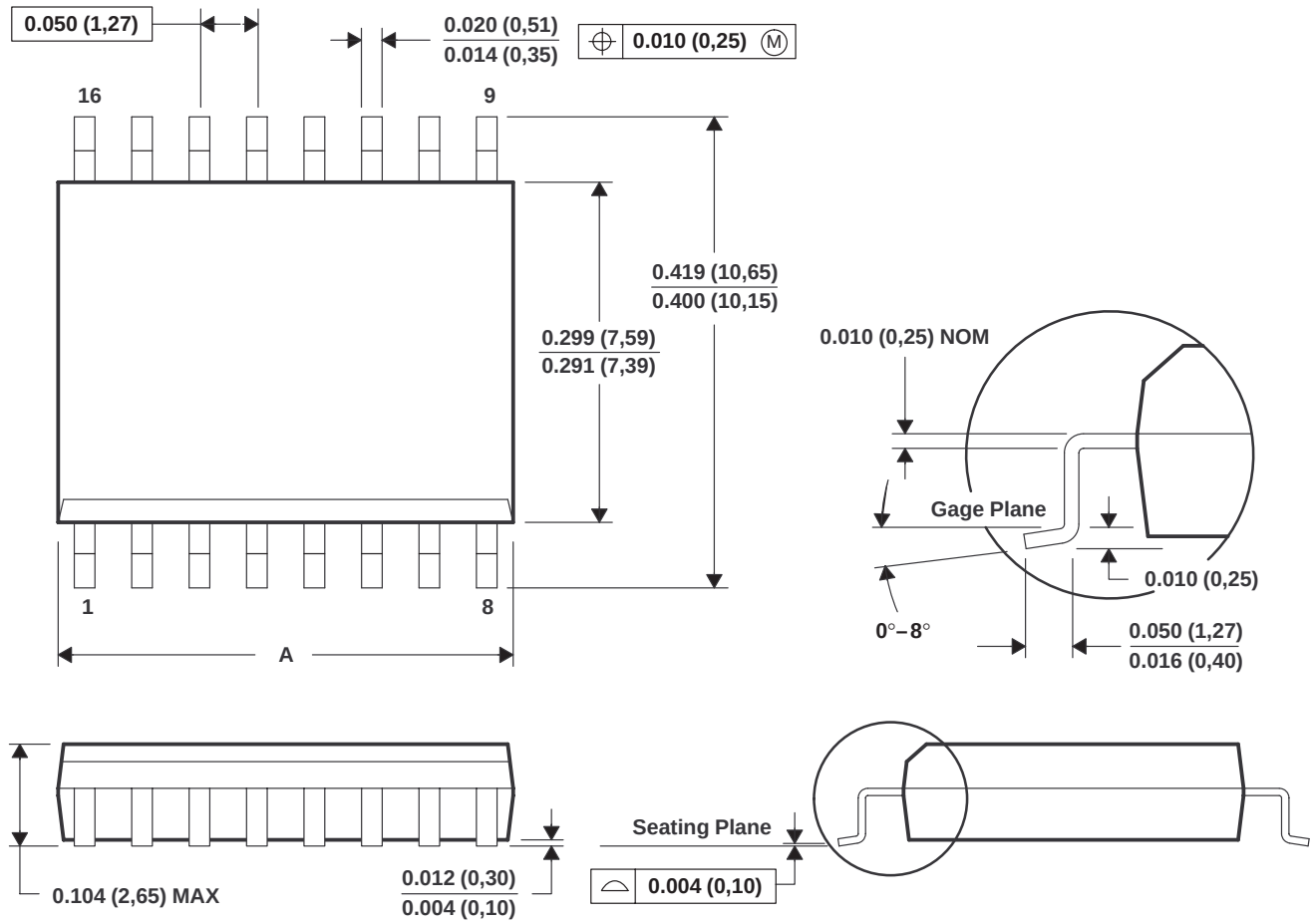
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/D 08/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN

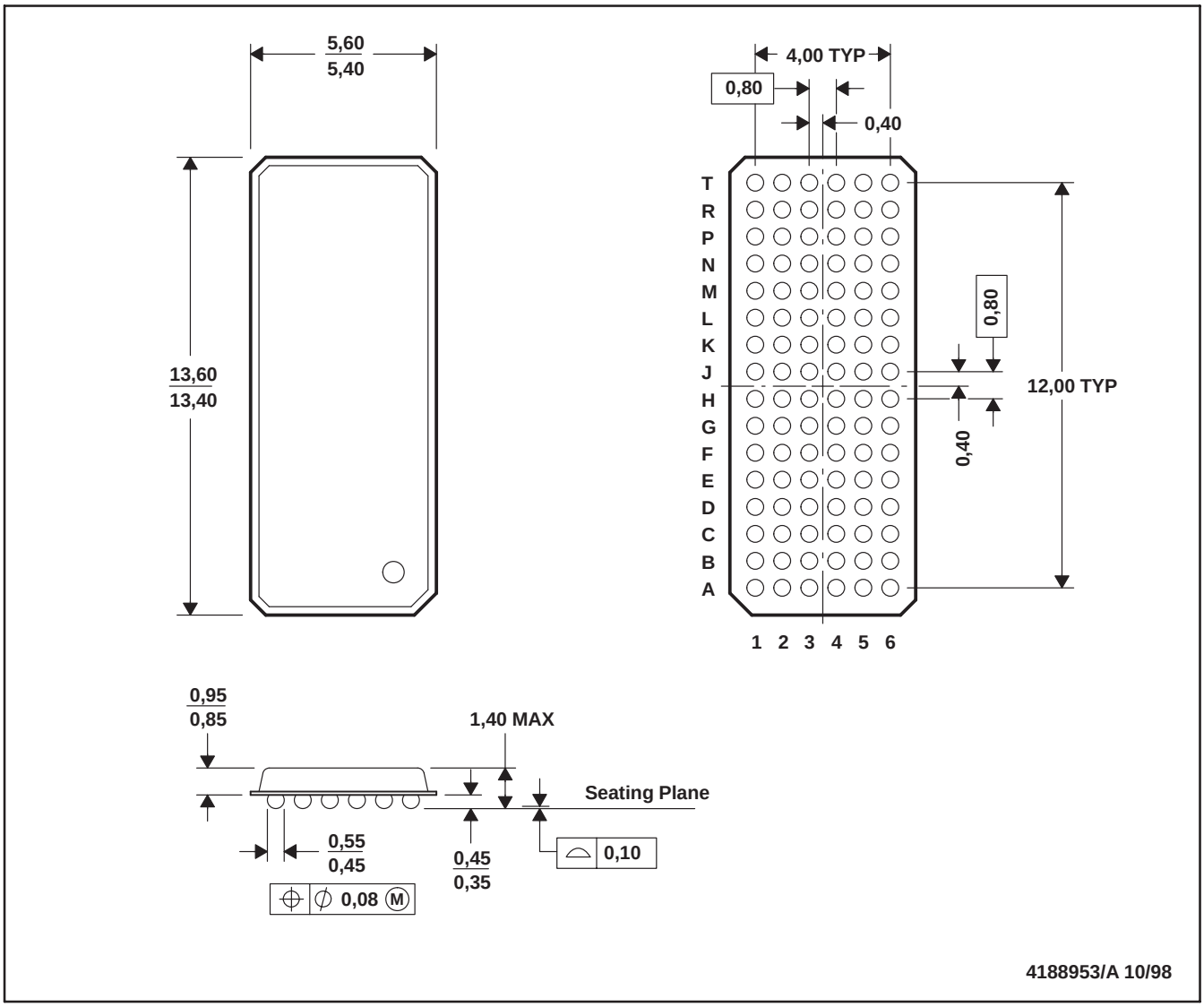


DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/D 01/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

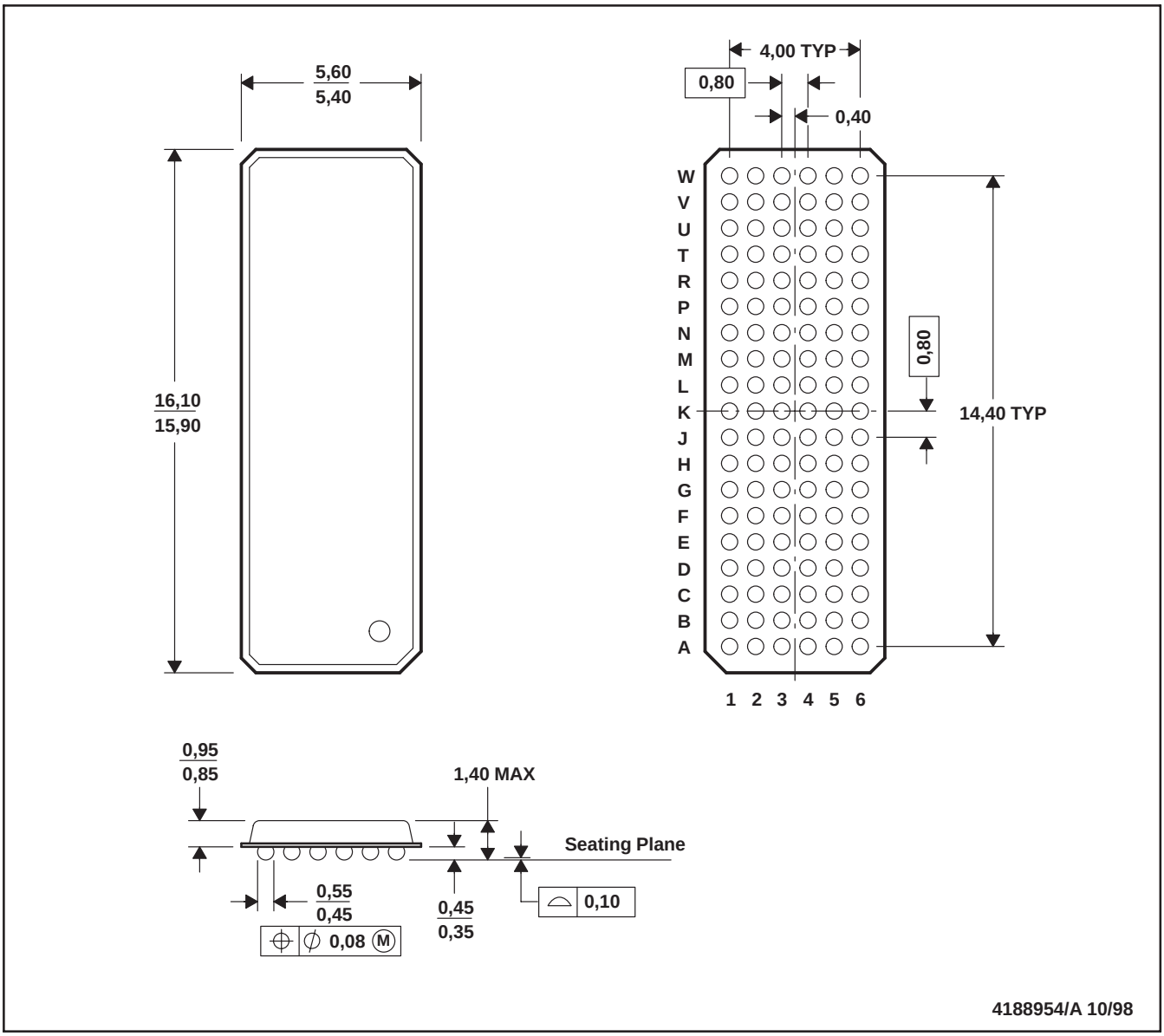
GKE (R-PBGA-N96) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments.

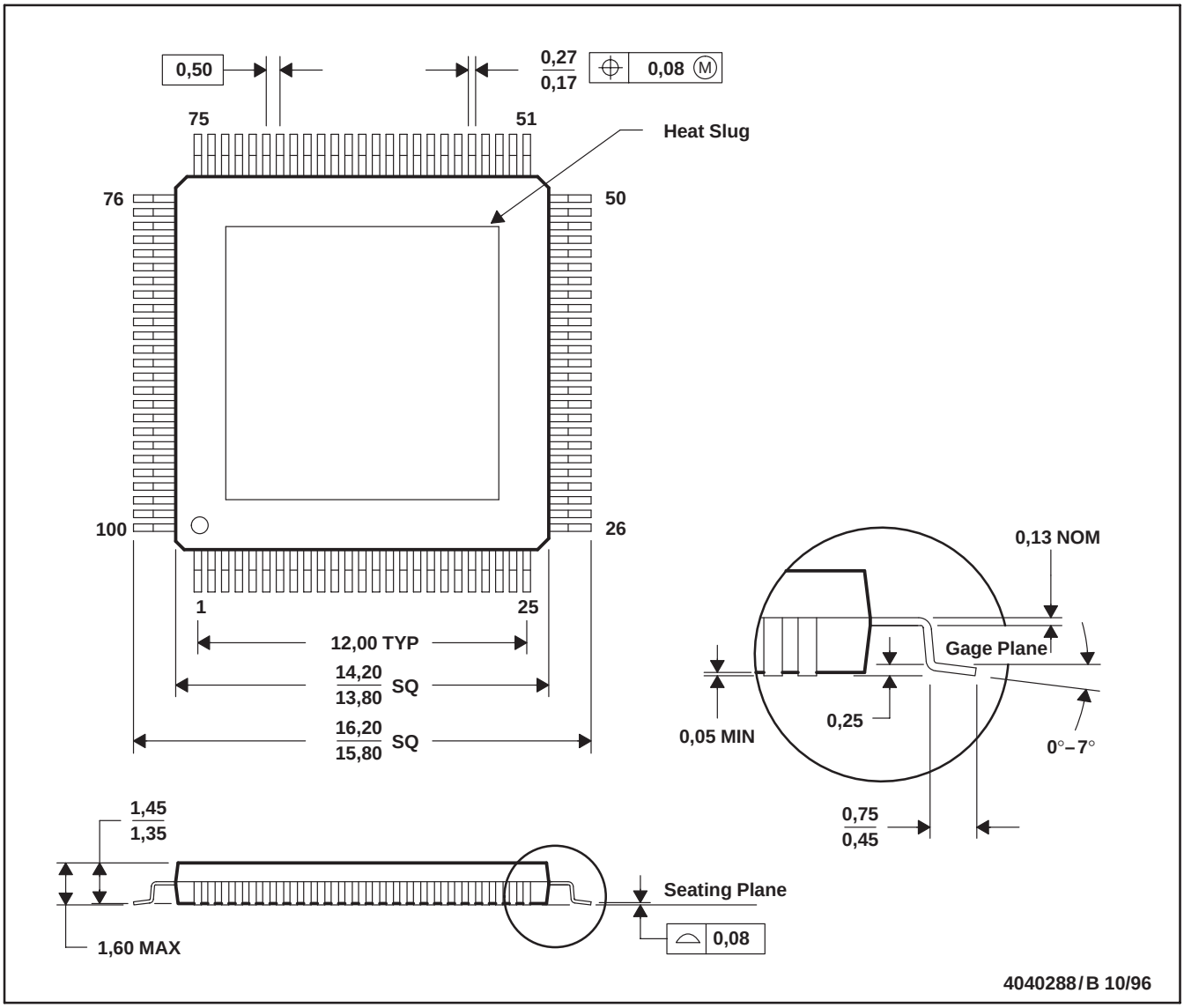
GKF (R-PBGA-N114) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments.

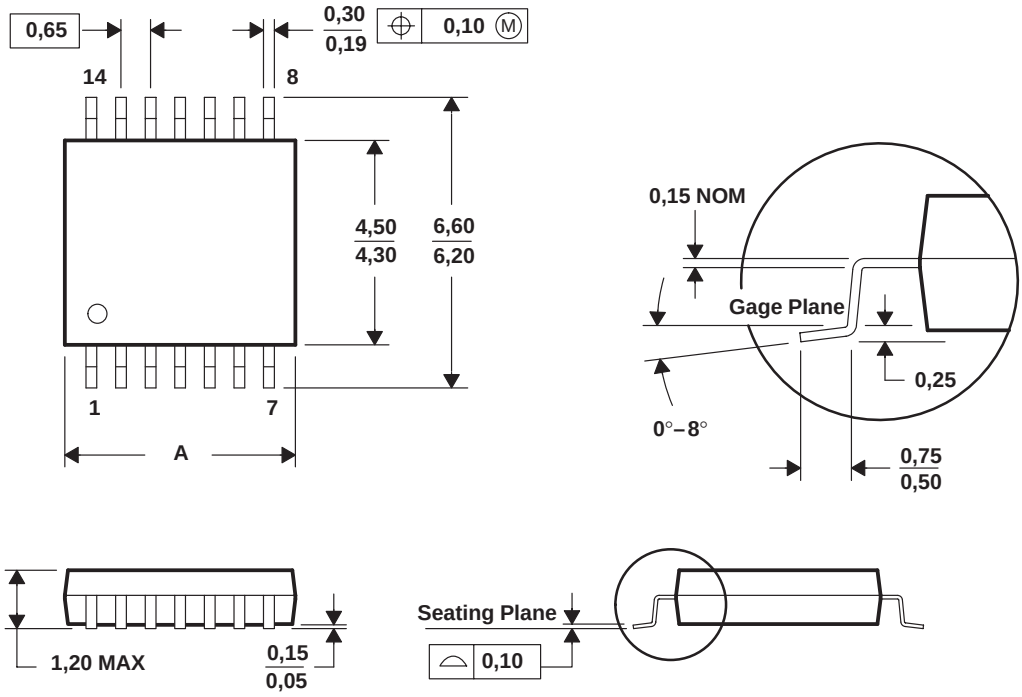
PCA (S-PQFP-G100) **PLASTIC QUAD FLATPACK (DIE DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat slug (HSL)
D. Falls within JEDEC MS-026

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

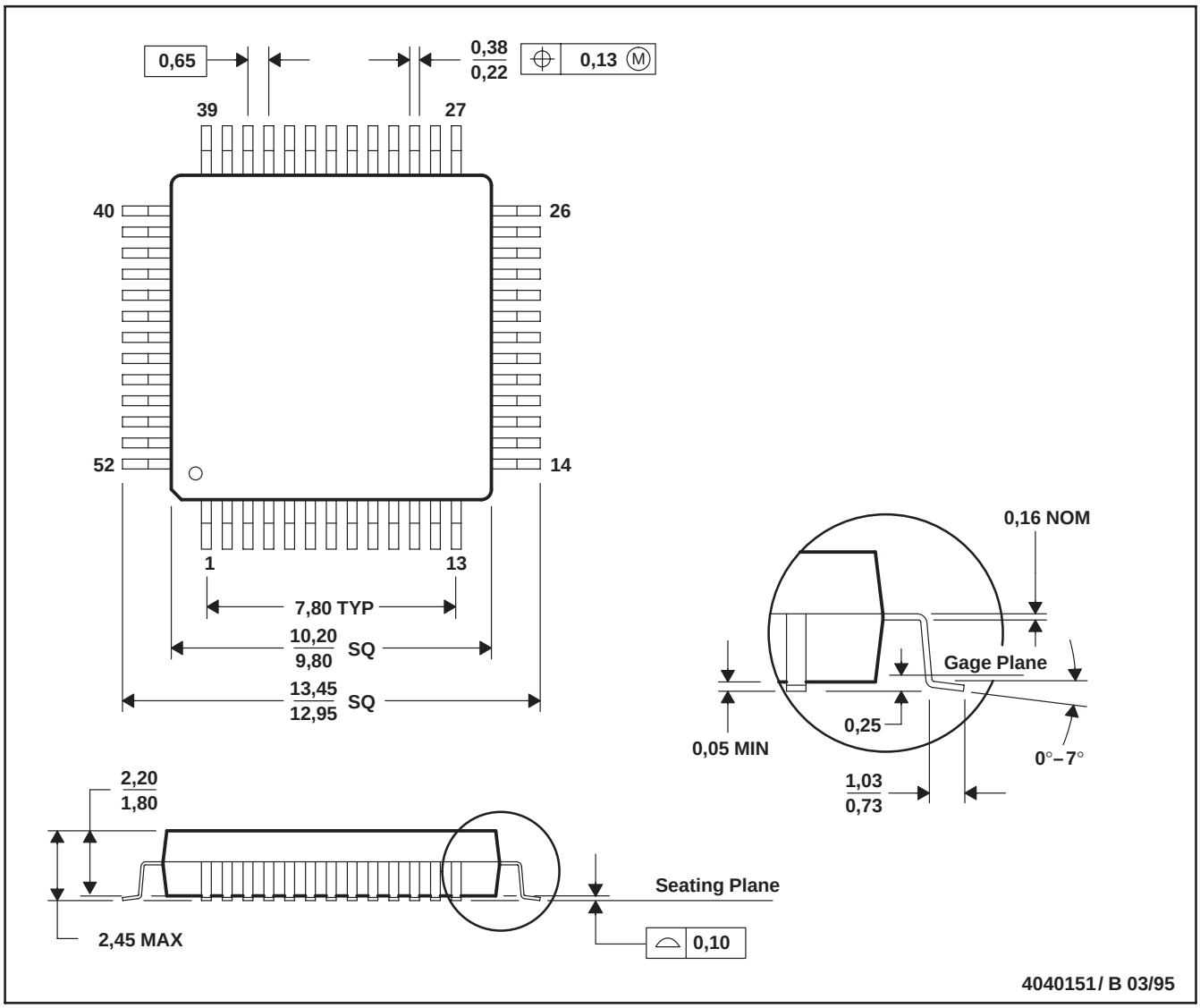


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

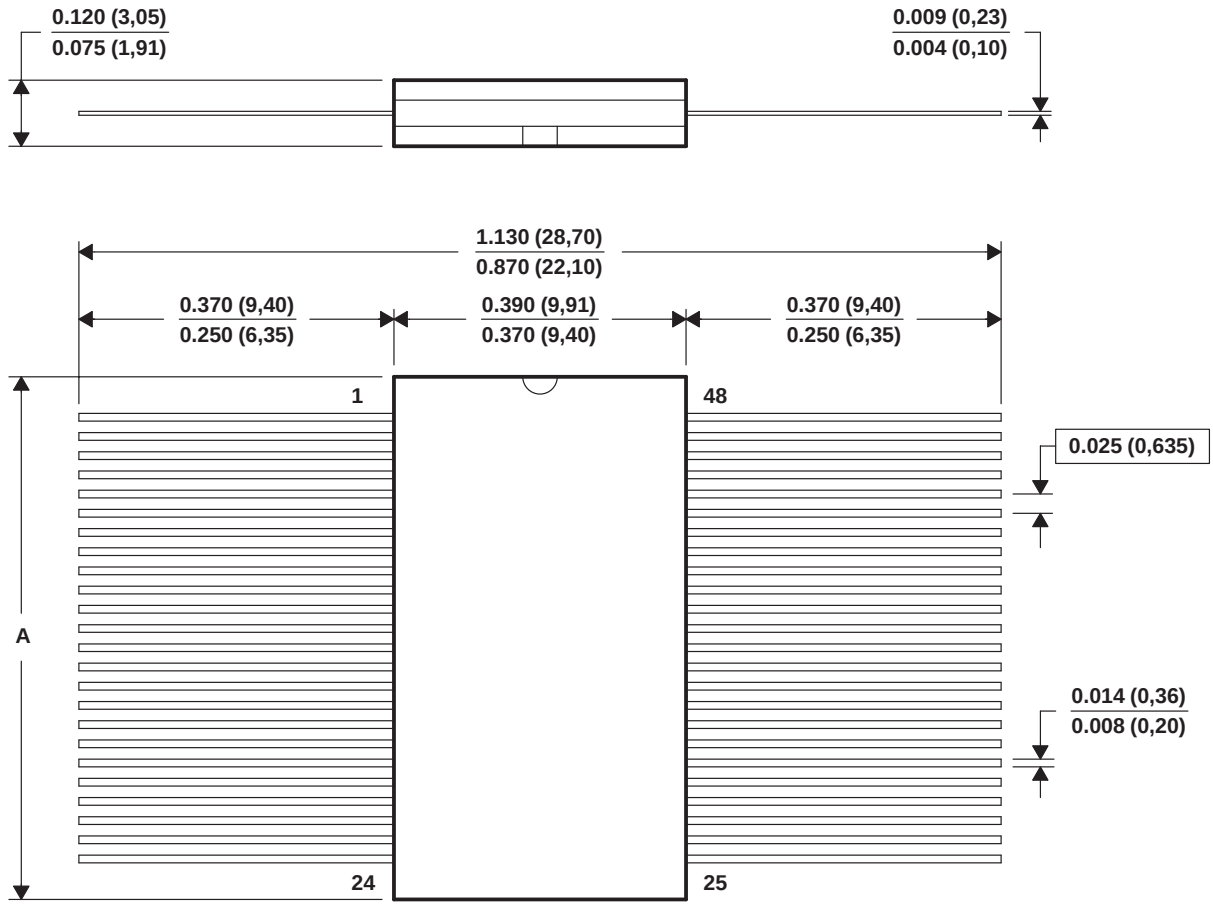
RC (S-PQFP-G52) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-022

WD (R-GDFP-F)** **CERAMIC DUAL FLATPACK**

48 LEADS SHOWN



NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB