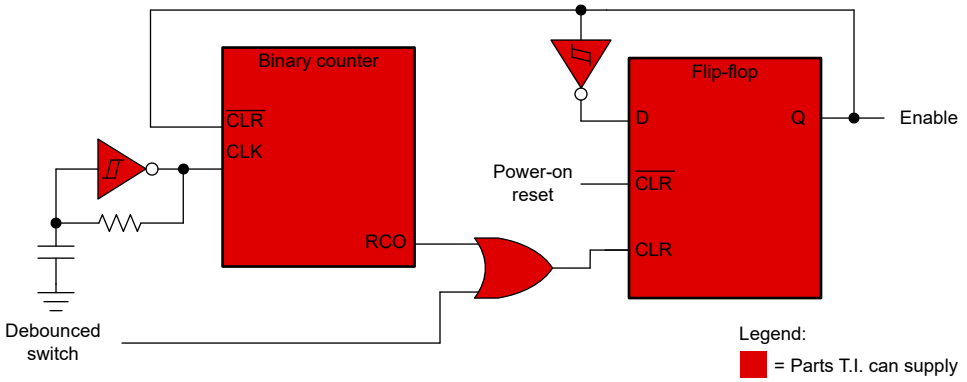
Product Overview

Generate a Timed Pulse Using a Binary Counter

A binary counter paired with a resistor-capacitor (RC) oscillator generates a timed enable pulse, when triggered. Triggering a system that is not enabled enables the system for an amount of time determined by the RC, after which the system disables. Triggering an already-enabled system disables the system prematurely.



Design Considerations

- A gate with Schmitt-trigger inputs connected to the debounced switch does not need a buffer to debounce the switch input
- The pulse width of the enable pulse when the switch is triggered is RC (number of bits)
  - Binary counters without an RCO output can use the highest bit output in the counter. Doing this reduces the effective number of bits of the counter by 1.
- When the device is first powered on, the flip-flop outputs an unknown state unless the device is reset with a power-on reset pulse
  - Systems which do not require starting in a specific state do not require asynchronous clear
- Ask a question on the TI E2E™ forum

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Function	Features
SN74LV163A		2 V – 5.5 V	Binary counter	4 bit, RCO output, load function
SN74HC4060		2 V – 6 V	Binary counter	14 bit, Integrated oscillator, Active high clear
SN74HC4060-Q1	✓			
SN74LVC1G08		1.65 V – 5.5 V	D-type flip-flop	1 channel
SN74LVC1G08-Q1	✓			
SN74LVC1G175		1.65 V – 5.5 V	D-type flip-flop	1 channel, Asynchronous clear
SN74LVC2G74		1.65 V – 5.5 V	D-type flip-flop	1 channel, Asynchronous clear, Inverted output, Preset
SN74LVC2G74-Q1	✓			
SN74LVC1G14		1.65 V – 5.5 V	Inverting buffer	1 channel, Schmitt-trigger inputs
SN74LVC1G14-Q1	✓			
SN74LVC1G32		1.65 – 5.5 V	OR gate	1 channel
SN74LVC1G32-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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