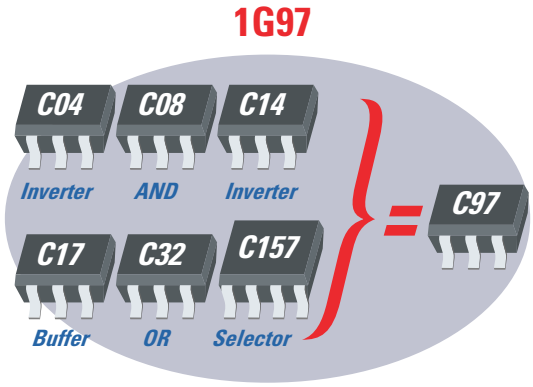
Product Clip

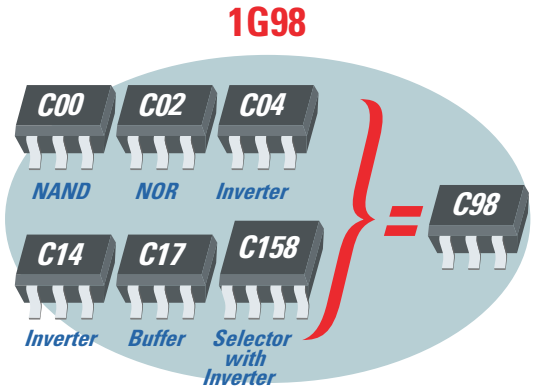
Standard Linear and Logic

Configurable multi-function Little Logic devices

www.ti.com/nanostar

Texas Instruments (TI) adds the next-generation configurable devices to its Little Logic portfolio with the 1G97/98 functions in both LVC and the new AUP technologies. By providing nine single-gate logic solutions in one device, the 1G97/98 allow reductions in device inventory and simplify part management. 1G97/98 devices are available in SOT-23 (DBV), SC-70 (DCK) as well as NanoStar™ (YEP) and NanoFree™ (YZP) WCSP.





The LVC family offers higher drive and quicker propagation-delay times which is ideal for ASIC bug fixes as well as space-constrained PCBs. TI's new AUP family is designed for use in portable applications such as cell phones and PDAs. The new family consumes 90% less static power than other industry standard 3.3-V logic families which aides in extending the battery life of portable applications. AUP can also be used in fixed applications such as servers, where low power dissipation is required.

Benefits

- Most configurable functions (9) in one device
- Industry's smallest configurable logic device (SN74LVC/AUP1G97/98YEP/YZP)
- 1G97/98 offer one-input inversion options to eliminate two-stage designs
- All inputs are Schmitt-trigger circuit which allows for slow input transition
- Overvoltage-tolerant inputs of LVC facilitate 5- to 3-V translation
- AUP is 3.6-V I/O tolerant to support mixed-mode signal operation

Selection Guide

The table below breaks down the differences between the 1G57/58 and 1G97/98 functions.

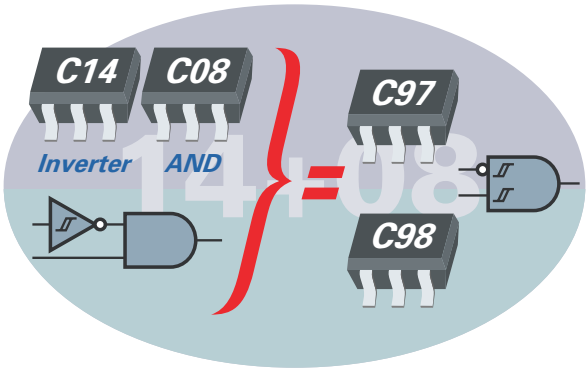
Family	Operating Voltage Range (V)	Optimized Volltage (V)	Propagation Delay t_{pd} (typ) (ns)	Output Drive (mA)	Input Tolerance (V)	I_{OFF} Protection
AUP	0.8 to 3.6	3.3	4	4	3.6	Yes
LVC	1.65 to 5.5	3.3	3.5	24	5.5	Yes

Function	LVC1G57	LVC1G58	AUP1G57	AUP1G58	LVC1G97	LVC1G98	AUP1G97	AUP1G98
2-to-1 data selector/MUX					✔	✔	✔	✔
2-input AND	✔		✔		✔		✔	
2-input NAND		✔		✔		✔		✔
2-input OR (w/1 input inverted)	✔		✔		✔	✔	✔	✔
2-input NAND (w/1 input inverted)	✔		✔		✔	✔	✔	✔
2-input AND (w/1 input inverted)		✔		✔	✔	✔	✔	✔
2-input NOR (w/1 input inverted)		✔		✔	✔	✔	✔	✔
2-input OR		✔		✔	✔		✔	
2-input NOR	✔		✔			✔		✔
2-input XOR		✔		✔				
2-input XNOR	✔		✔					
Inverter	✔	✔	✔	✔	✔	✔	✔	✔
Buffer	✔	✔	✔	✔	✔	✔	✔	✔
Total functions in one package	**7**	**7**	**7**	**7**	**9**	**9**	**9**	**9**

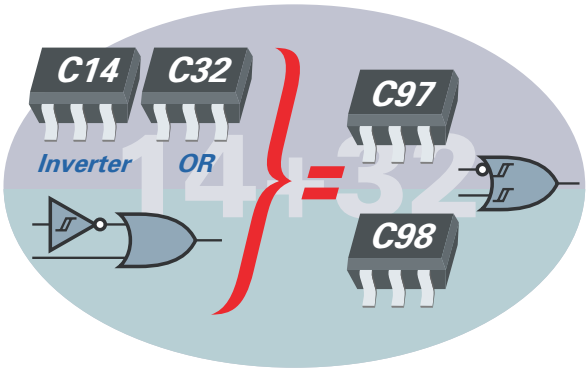
Space-Saving Comparisons

Besides the standard 2-input logic gate functions, the 1G97/98 both offer four additional functions. This allows functions that were once only achievable with two ICs to be embedded in one small chip. In turn, crucial board space is saved for more critical functions or miniaturization.

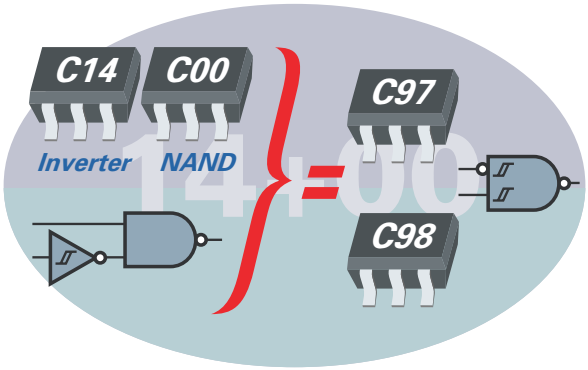
Inverter (04/14) + AND (08)



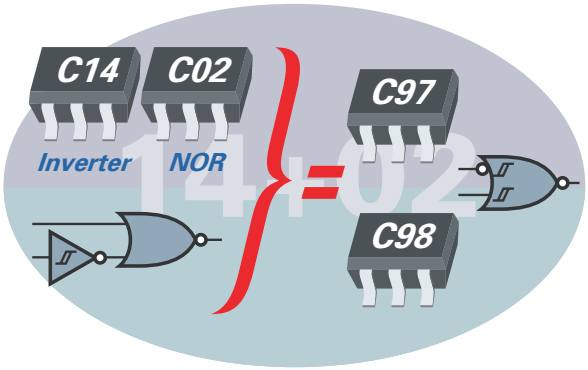
Inverter (04/14) + OR (32)



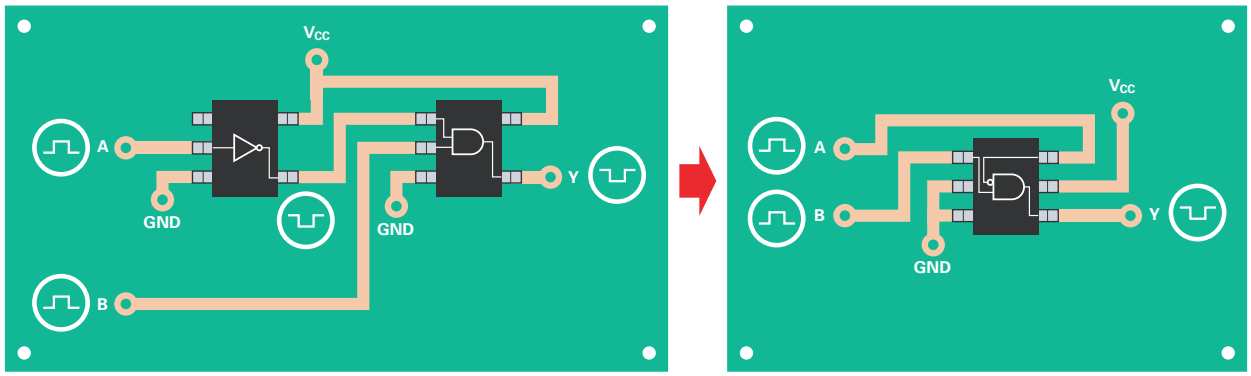
Inverter (04/14) + NAND (00)



Inverter (04/14) + NOR (02)



Board-Space Reduction



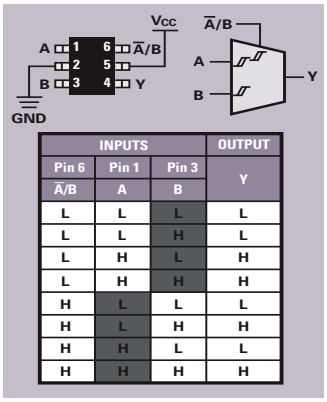
Inverter (04/14) + AND (08) | 1G97/98

Wiring Method and Truth Table for 1G97/98

1G97 Configurations

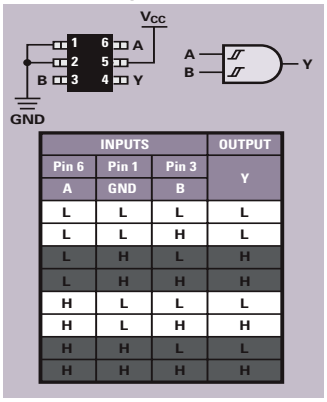
Input pins 1, 3 and 6 are for wiring, V_{CC} = pin 5, GND = pin 2 and Y Output = pin 4. Any unwired pin should be connected to GND or V_{CC}.

157: 2-to-1 Data Selector/MUX



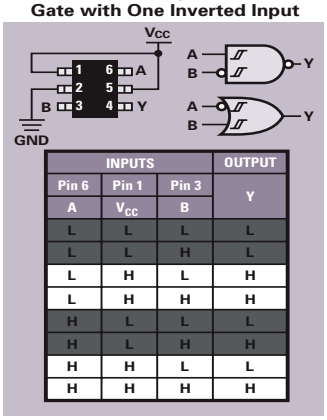
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
$\overline{A}/B$	A	B	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

08: 2-Input AND Gate



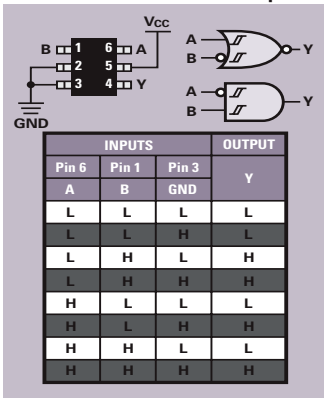
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	GND	B	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

14+00/14+32: 2-Input OR/NAND Gate with One Inverted Input



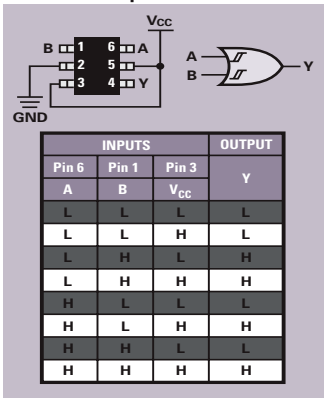
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	V_{CC}	B	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

14+02/14+08: 2-Input AND/NOR Gate with One Inverted Input



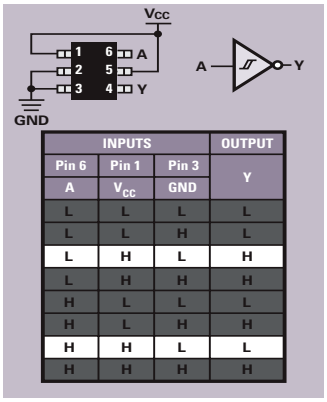
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	B	GND	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

32: 2-Input OR Gate



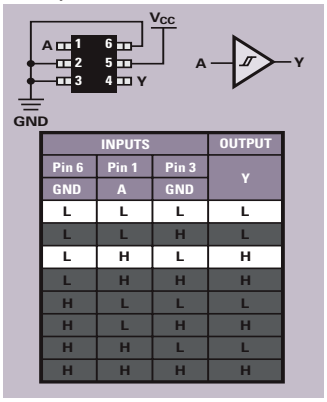
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	B	V_{CC}	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

04/14: Inverter



INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	V_{CC}	GND	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

17/34: Noninverted Buffer

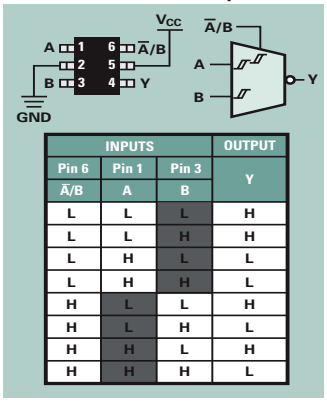


INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
GND	A	GND	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

1G98 Configurations

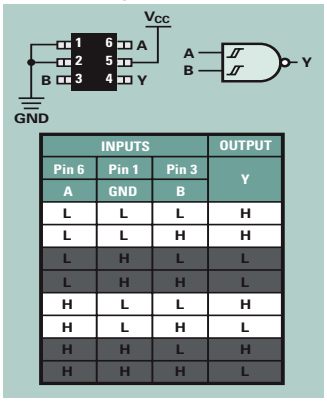
Input pins 1, 3 and 6 are for wiring, V_{CC} = pin 5, GND = pin 2 and Y Output = pin 4. Any unwired pin should be connected to GND or V_{CC}.

158: 2-to-1 Data Selector/MUX with Inverted Output



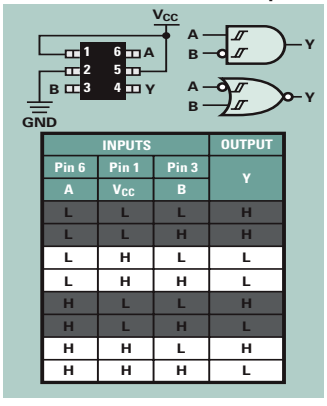
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
$\overline{A}/B$	A	B	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

00: 2-Input NAND Gate



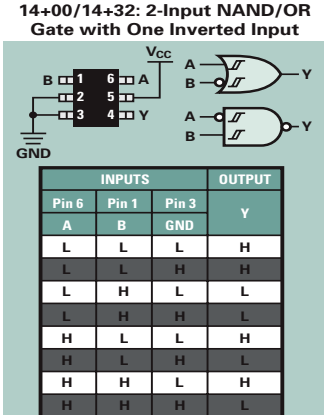
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	GND	B	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

14+02/14+08: 2-Input NOR/AND Gate with One Inverted Input



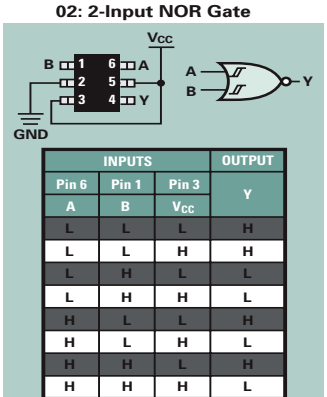
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	V_{CC}	B	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

14+00/14+32: 2-Input NAND/OR Gate with One Inverted Input



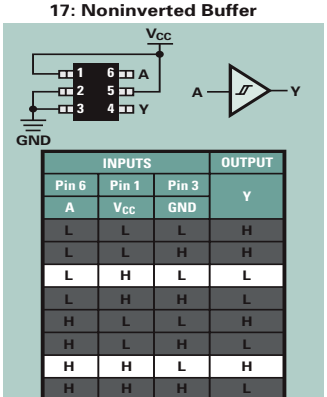
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	B	GND	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

02: 2-Input NOR Gate



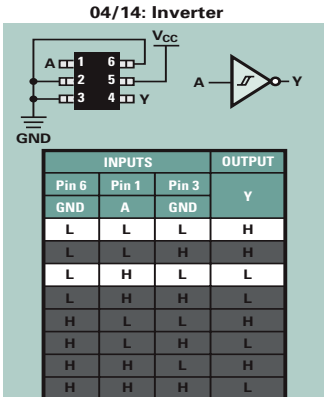
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	B	V_{CC}	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

17: Noninverted Buffer



INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
A	V_{CC}	GND	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

04/14: Inverter



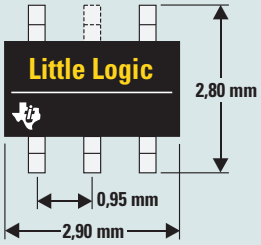
INPUTS			OUTPUT
Pin 6	Pin 1	Pin 3	Y
GND	A	GND	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

Packaging Options

Lead Frame

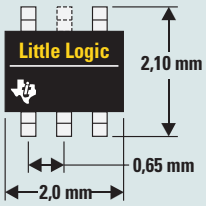
DBV (SOT-23)
5-pin or 6-pin

(Actual Size)



DCK (SC-70)
5-pin or 6-pin

(Actual Size)

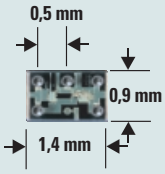


Wafer Chip-Scale

NanoStar™ (YEP)
5-pin or 6-pin

(Actual Size)

NanoFree™ (YZP)



Industry's Smallest Configurable Logic Device

Pb-FREE

For more information on samples, datasheets, application reports and design summaries, visit:

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