Functional Safety Information

SN65HVD1781A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for SN65HVD1781A-Q1 (SOIC) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

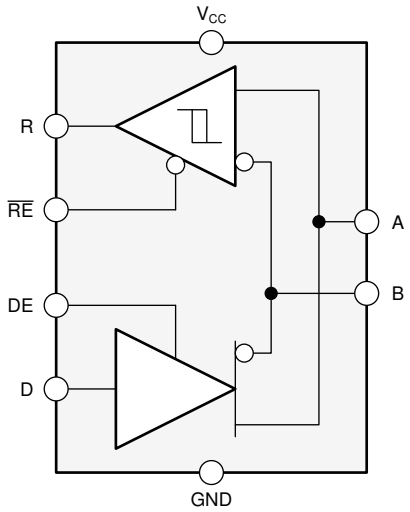

Figure 1-1. Functional Block Diagram

SN65HVD1781A-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for SN65HVD1781A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 Part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 for SN65HVD1781A

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D) JEDEC high-K model	FIT (Failures Per 10^9 Hours) 8-pin SOIC (D) JEDEC low-K model
Total Component FIT Rate	19	12
Die FIT Rate	10	4
Package FIT Rate	9	8

- Mission Profile: Motor Control from Table 11
- Power dissipation: 290 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN65HVD1781A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Receiver fail	15%
Transmitter fail	63%
I/O	12%
PCU	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN65HVD1781A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the SN65HVD1781A-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the SN65HVD1781A-Q1 datasheet.

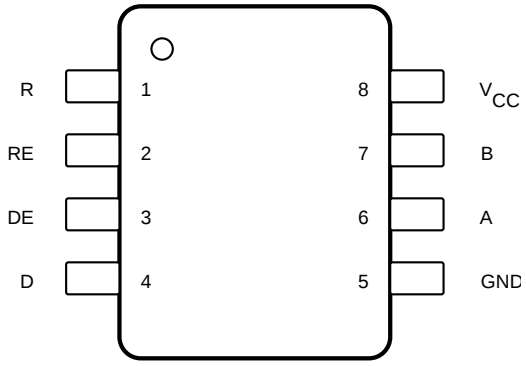

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
R	1	Host unable to receive data from bus via transceiver. Increased output current and ICC when the output state is high.	B
$\overline{RE}$	2	Receiver output always enabled.	D
DE	3	Driver output always disabled.	B
D	4	Host unable to transmit data to bus via transceiver. Output state is low when the driver is enabled.	B
GND	5	Intended operation.	D
A	6	Non-inverting signal stuck low; bus unable to reach differential high level. Communication errors likely.	B
B	7	Inverting signal stuck low; bus unable to reach differential high level. Communication errors likely.	B
VCC	8	Device unpowered; neither transmit nor receive functionality available. Large current load on the external VCC regulator.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
R	1	Host unable to receive data from the bus via transceiver	B
$\overline{RE}$	2	Receiver output always disabled.	B
DE	3	Driver output always disabled.	B
D	4	Host unable to transmit data to the bus via transceiver. Output state is indeterminate when the driver is enabled.	B
GND	5	Device unpowered; neither transmit nor receive functionality available.	B
A	6	Communication errors likely; may work with degraded margin if the bus termination is not implemented.	B
B	7	Communication errors likely; may work with degraded margin if the bus termination is not implemented.	B
VCC	8	Device unpowered; neither transmit nor receive functionality available.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
R	1	$\overline{RE}$	Undetermined state of shared net; receive functionality unlikely to work.	B
$\overline{RE}$	2	DE	Receiver is enabled when driver is disabled, and the driver is enabled when the receiver is disabled. Transceiver state may not be well-defined when this short results in contention between two active control lines from the host.	B
DE	3	D	Driver output can only be output-high or disabled (high-Z). State may not be well-defined due to contention between host control lines.	B
GND	5	A	Non-inverting signal stuck low; bus unable to reach differential high level. Communication errors likely.	B
A	6	B	Bus unable to reach differential-high or differential-low states; communication cannot occur on bus.	B
B	7	VCC	Inverting signal stuck high; bus unable to reach differential high level. Communication errors likely.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
R	1	Host unable to receive data from bus via transceiver. Increased input current when the output state is low.	B
$\overline{RE}$	2	Receiver output always disabled.	B
DE	3	Driver output always enabled.	D
D	4	Host unable to transmit data to bus via transceiver. Output state is high when driver is enabled.	B
GND	5	Device unpowered; neither transmit nor receive functionality available. Large current load on the external VCC regulator.	B
A	6	Non-inverting signal stuck high; bus unable to reach differential high level. Communication errors likely.	B
B	7	Inverting signal stuck high; bus unable to reach differential high level. Communication errors likely.	B
VCC	8	Intended operation	D

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