Functional Safety Information

LMR33630AP-Q1 and LMR33620AP-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for LMR33630AP-Q1 and LMR33620AP-Q1 in the VQFN-12 package (RNX designator) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

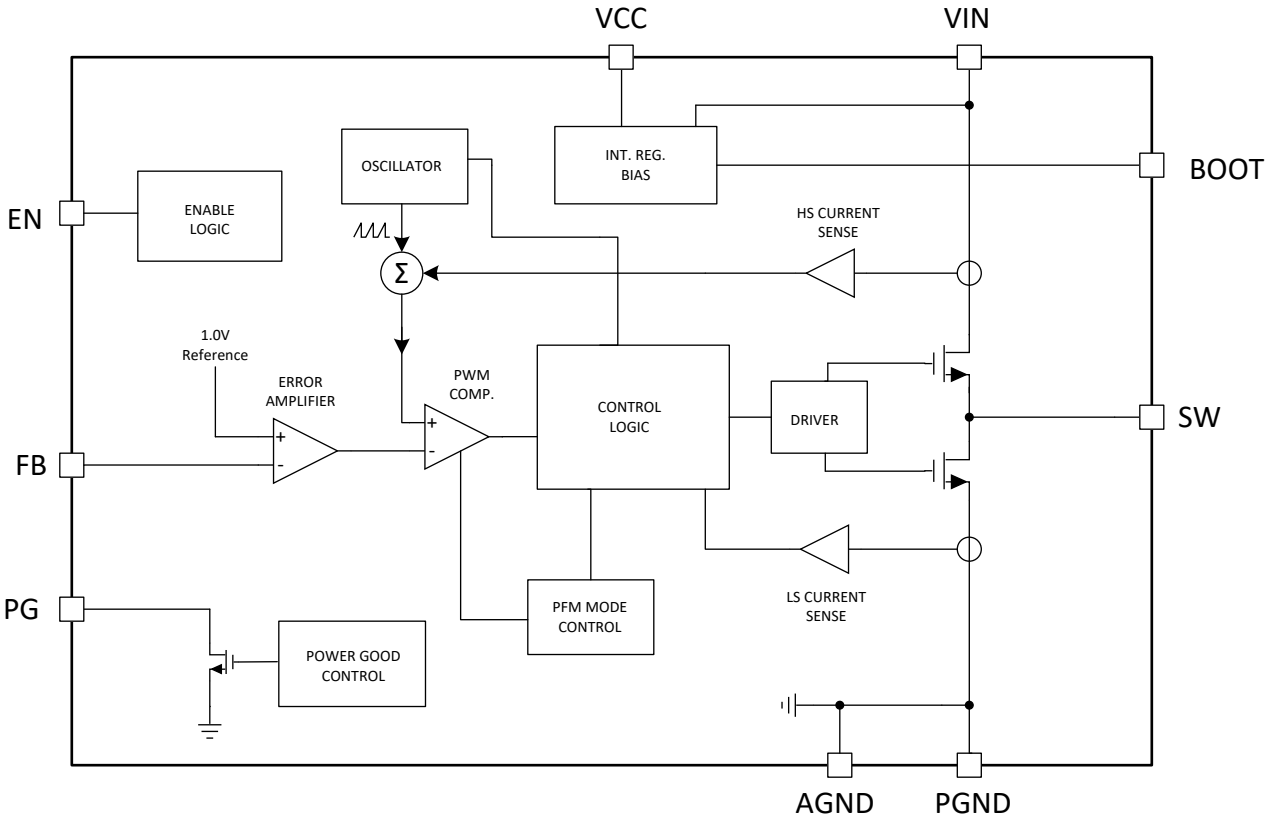

Figure 1-1. Functional Block Diagram

LMR33630AP-Q1 and LMR33620AP-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LMR33630AP-Q1 and LMR33620AP-Q1 in Table 2-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 2-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW Output	60%
SW output not in specification -- voltage or timing	25%
SW driver FET suck on	5%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 2-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

3 Functional Safety Failure In Time (FIT) Rates

3.1 LMR33630AP-Q1

This section provides Functional Safety Failure In Time (FIT) rates for the LMR33630AP-Q1 based on the following two different industry-wide used reliability standards:

- Table 3-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 3-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 3-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	21
Die FIT Rate	9
Package FIT Rate	12

The failure rate and mission profile information in Table 3-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 555 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 3-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICS Analog and Mixed ≤ 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 3-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3.2 LMR33620AP-Q1

This section provides Functional Safety Failure In Time (FIT) rates for the LMR33620AP-Q1 based on the followingtwo different industry-wide used reliability standards:

- Table 3-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 3-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 3-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	6
Package FIT Rate	12

The failure rate and mission profile information in Table 3-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 370 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 3-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICS Analog and Mixed ≤ 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 3-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LMR33630AP-Q1 and LMR33620AP-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device used within the '*Recommended Operating Conditions*' and the '*Absolute Maximum Ratings*' found in the appropriate device data sheet.
- Configuration as shown in the '*Example Application Circuit*' found in the appropriate device data sheet.

4.1 LMR33630AP-Q1 and LMR33620AP-Q1

Figure 4-1 shows the LMR33630AP-Q1 and LMR33620AP-Q1 pin diagram for the VQFN-12 package (RNX designator). For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the appropriate device datasheet.

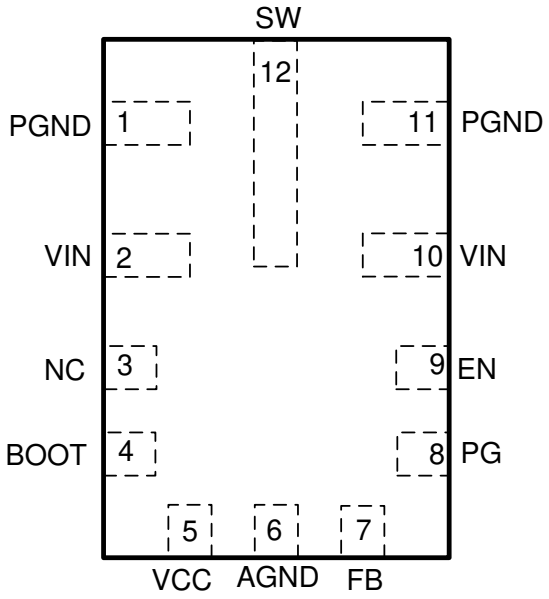

Figure 4-1. Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	No effect	D
VIN	2,10	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), damage to internal power FET(s) and/or other internal circuits.	A
BOOT	4	Damage to internal circuits	A
VCC	5	Fault mode will shut device off	B
AGND	6	No effect	D
FB	7	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
PG	8	Power good functionality will be lost.	B
EN	9	Loss of ENABLE functionality Device will remain in shut-down mode.	B
SW	12	Damage to internal power FET(s) and/or other internal circuits	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	With either one or both pins open, possible device damage.	A
VIN	2,10	With both pins open: loss of output voltage. With one pin open: possible device damage.	A
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), the effect is the same as "open on pin 4"	B
BOOT	4	Loss of output voltage regulation; low or no output voltage.	B
VCC	5	VCC LDO will be unstable. Loss of output voltage regulation and possible damage to internal circuits.	A
AGND	6	Loss of output voltage regulation. Possible damage to internal circuits.	A
FB	7	Loss of output voltage regulation. Output voltage may rise or fall outside of intended regulation window.	B
PG	8	PG functionality will be lost.	B
EN	9	Loss of ENABLE functionality. Erratic operation; probable loss of regulation.	B
SW	12	Loss of output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1	VIN	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2	N/C	No effect if this pin is not used by customer.	D
			When used to route the SW node to connect CBOOT (as recommended), the output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
N/C	3	BOOT	No effect if this pin is not used by customer.	D
			When used to route the SW node to connect CBOOT (as recommended), damage to internal circuits. No output voltage will be produced.	A
BOOT	4	VCC	Loss of output regulation, possible damage to internal circuits	A
VCC	5	AGND	Fault mode will shut device off	B
AGND	6	FB	The regulator will operate at maximum duty cycle. Output voltage will rise to nearly the input voltage (VIN) level. Possible damage to customer load and/or output stage components may occur. No effect on device.	B
FB	7	PG	Erratic operation; probable loss of regulation. Possible output voltage increase and damage to customer load.	B
PG	8	EN	Erratic operation; probable loss of regulation.	B
EN	9	VIN	This is a valid connection for the EN input. Enable functionality will be lost; the device will remain on.	B
VIN	10	PGND	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
PGND	11	SW	Damage to internal power FET(s) and/or other internal circuits	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGND	1,11	Device will not operate. No output voltage will be generated. Output capacitors will discharge through input short. Large reverse current may damage device.	A
VIN	2,10	No effect.	D
N/C	3	No effect if this pin is not used by customer.	D
		When used to route the SW node to connect CBOOT (as recommended), the output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A
BOOT	4	Damage to internal circuits	A
VCC	5	Damage to internal circuits for VIN>5.5 V	A
AGND	6	Possible damage to internal circuits or package	A
FB	7	Damage to internal circuits will occur for VIN>5.5 V.	A
PG	8	Damage to internal circuits.	A
EN	9	No damage to device. Loss of ENABLE functionality.	B
SW	12	The output voltage will rise to nearly the level of VIN. Customer load will be damaged. Possible damage to device	A

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