Functional Safety Information

TPS62A01-Q1 and TPS62A01A-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS62A01-Q1 and TPS62A01A-Q1 (SOT-563 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

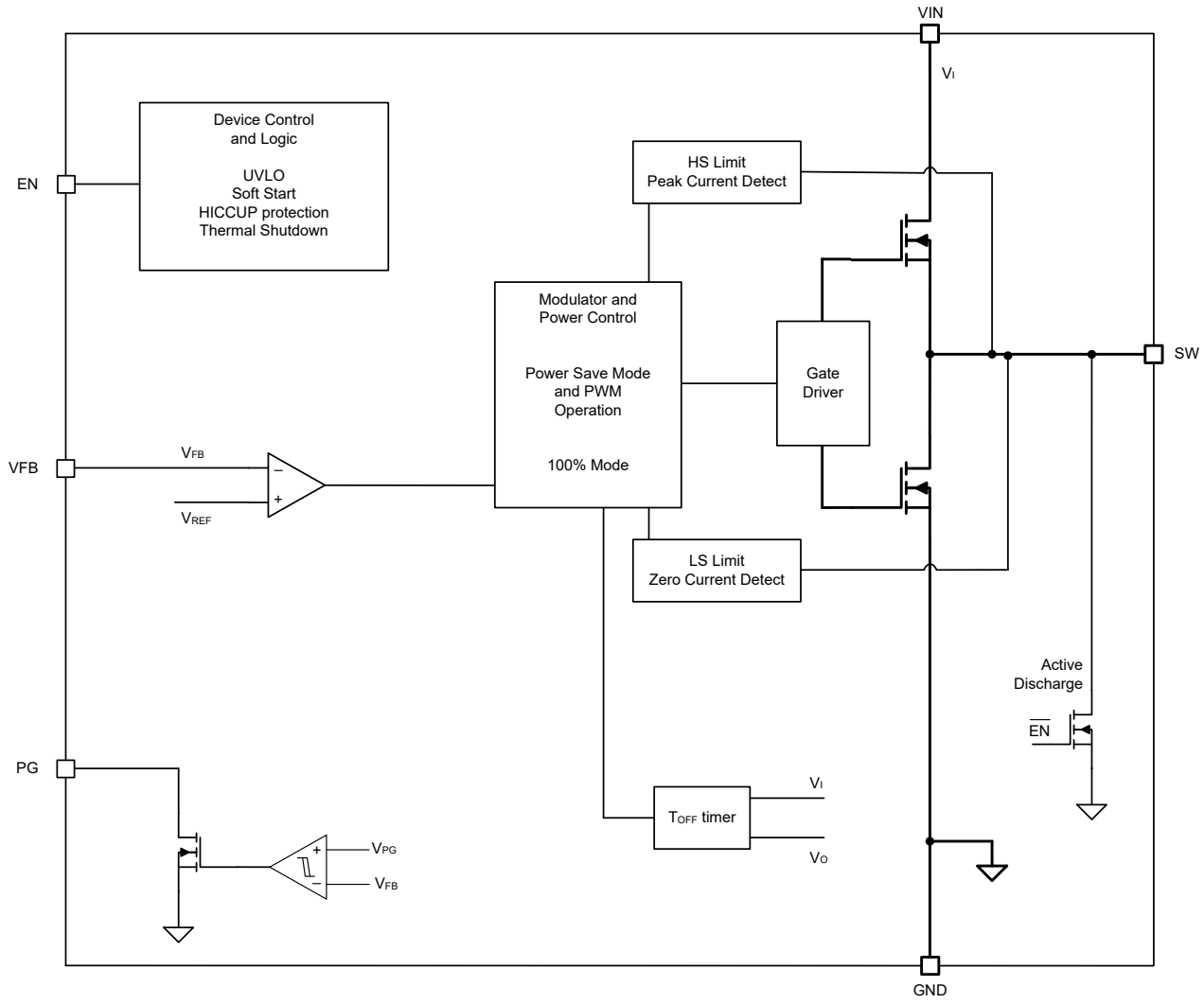

Figure 1-1. Functional Block Diagram

TPS62A01-Q1 and TPS62A01A-Q1 were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS62A01-Q1 and TPS62A01A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	3
Package FIT Rate	1

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 85 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2T

Table	Category	Reference FIT Rate	Reference Virtual T_j
5	CMOS, BICMOS Digital, analog/ mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_j (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS62A01-Q1 and TPS62A01A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35%
SW output not in specification - voltage or timing	45%
SW power HS or LS FET stuck on	10%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS62A01-Q1 and TPS62A01A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS62A01-Q1 and TPS62A01A-Q1 pin diagram. For a detailed description of the device pins, please refer to the '*Pin Configuration and Functions*' section in the TPS62A01-Q1 and TPS62A01A-Q1 data sheet.

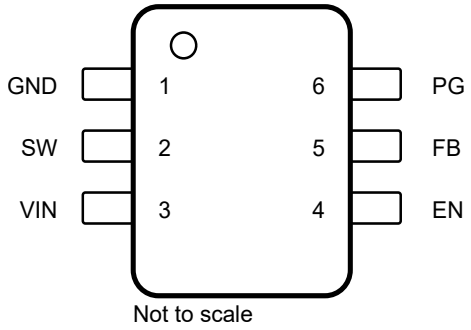

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating in the typical application. Please refer to the 'Simplified Schematics' on the first page in the TPS62A01-Q1 and TPS62A01A-Q1 data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Intended functionality	D
SW	2	Potential device damage; incorrect output voltage	A
VIN	3	Device not functional; no power supply.	B
EN	4	Device not functional; device cannot be enabled.	B
FB	5	Incorrect output voltage; device performance degradation	C
PG	6	Lost the pin functionality; device keeps functioning	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Missing ground reference; device not functional.	B
SW	2	Open loop operation; device not functional.	B
VIN	3	Device not functional; No power supply.	B
EN	4	Unintended device functionality; undefined state of pin EN.	B
FB	5	Undetermined output voltage behavior, open loop operation.	B
PG	6	Lost the pin functionality; device keeps functioning.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	SW	Potential device damage ; Incorrect output voltage	A
SW	2	VIN	Potential device damage ; Incorrect output voltage	A
VIN	3	EN	Intended Functionality	D
EN	5	FB	Potential device damage	A
FB	6	PG	Potential device damage	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device not functional; Open loop operation	B
SW	2	Potential device damage; Incorrect output voltage	A
VIN	3	Intended functionality	D
EN	4	Intended functionality; Device permanently enabled	D
FB	5	Potential device damage	A
PG	6	Lost the pin functionality; VIN shorted to GND with a low resistance path during start-up; potential device damage	A

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