*Functional Safety Information*

# *MC33063A-Q1*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for the MC33063A-Q1 (SOIC D package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

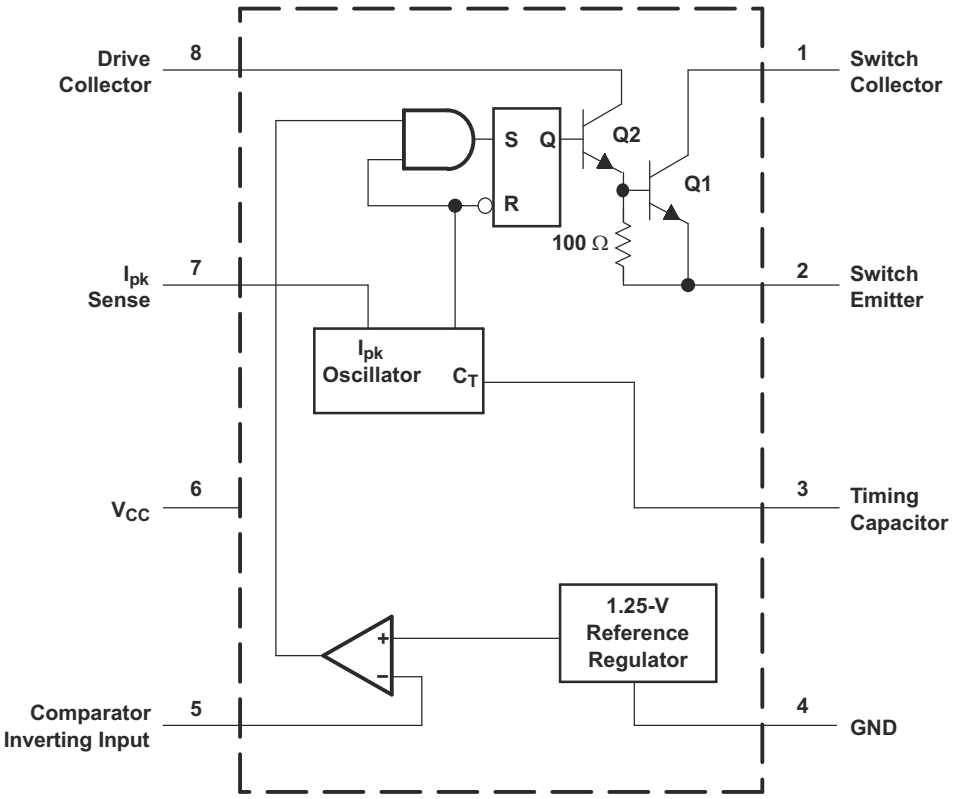


**Figure 1-1. Functional Block Diagram**

The MC33063A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the MC33063A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 24 |
| Die FIT rate | 15 |
| Package FIT rate | 9 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Switched Regulators - (DC-DC, BUCK, BOOST) | 10 FIT | 55°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the MC33063A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| Output voltage is not in specification (transistor, comparator or logic issue) | 80 |
| Frequency shift | 5 |
| Output voltage shift due to reference deviate from the designed value | 15 |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the MC33063A-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality. |
| B | No device damage, but loss of functionality. |
| C | No device damage, but performance degradation. |
| D | No device damage, no impact to functionality or performance. |

Figure 4-1 shows the MC33063A-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the MC33063A-Q1 data sheet.

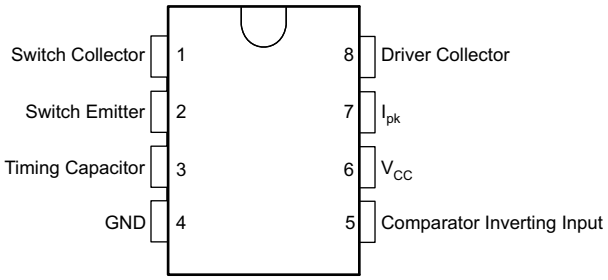


**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is used within the Recommended Operating Conditions and the Absolute Maximum Ratings found in the MC33063A-Q1 data sheet.
- For the analysis, the step-up converter with $V_{IN}$ = 12 V and $V_{OUT}$ = 28V and the step-down converter with $V_{IN}$ = 25 V and $V_{OUT}$ = 5 V shown in the Typical Application section of the MC33063A-Q1 data sheet are considered.

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| Switch Collector | 1 | Step-up converter: Short circuits $V_{IN}$ through sense resistor and inductor. Converter does not operate. | B |
| | | Step-down converter: Short circuits $V_{IN}$ through the sense resistor. Converter does not operate. | B |
| Switch Emitter | 2 | Step-up converter: No effect. | D |
| | | Step-down converter: Short circuits synchronous rectifier. Power transistor might get damaged. | A |
| Timing Capacitor | 3 | Device is disabled. | B |
| GND | 4 | No effect. | D |
| Comparator Inverting Input | 5 | Step-up converter: Feedback loop open. Output may rail high and cause damage. | A |
| | | Step-down converter: Feedback loop open. Converter output close to $V_{IN}$. | B |

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| $V_{CC}$ | 6 | Short circuits $V_{IN}$. Converter will not power up. | B |
| $I_{PK}$ | 7 | Possible device damage. | A |
| Driver Collector | 8 | No effect on IC, but converter does not operate. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| Switch Collector | 1 | No effect on IC, but converter does not operate. | B |
| Switch Emitter | 2 | No effect on IC, but converter does not operate. | B |
| Timing Capacitor | 3 | Clock frequency will be much higher than intended. | C |
| GND | 4 | Possible device damage. | A |
| Comparator Inverting Input | 5 | Step-up converter: Feedback loop open. Output may rail high and cause damage. | A |
| | | Step-down converter: Feedback loop open. Converter output close to $V_{IN}$. | B |
| $V_{CC}$ | 6 | The device is not powered, so converter does not operate. | B |
| $I_{PK}$ | 7 | No current limit function. | C |
| Driver Collector | 8 | No effect on IC, but converter does not operate. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| Switch Collector | 1 | Switch Emitter | Step-up converter: Short circuits $V_{IN}$ through sense resistor and inductor. Converter does not operate. | B |
| | | | Step-down converter: Short circuits $V_{IN}$ through the sense resistor. Converter does not operate. | B |
| Switch Emitter | 2 | Timing Capacitor | Step-up converter: converter does not operate. | B |
| | | | Step-down converter: clock frequency unpredictable. | B |
| Timing Capacitor | 3 | GND | No effect on IC, but converter does not operate. | B |
| GND | 4 | Comparator Inverting Input | Step-up converter: Feedback loop open. Output may rail high and cause damage. | A |
| | | | Step-down converter: Feedback loop open. Converter output close to $V_{IN}$. | B |
| Comparator Inverting Input | 5 | $V_{CC}$ | No effect on IC, but converter not switching as too high output voltage is detected. | B |
| $V_{CC}$ | 6 | $I_{PK}$ | No current limit function. | C |
| $I_{PK}$ | 7 | Driver Collector | Step-up converter: Possible drive transistor damage due to overcurrent. | A |
| | | | Step-down converter: No effect. | D |
| Driver Collector | 8 | Switch Collector | Step-up converter: Possible power transistor damage due to overcurrent. | A |
| | | | Step-down converter: No effect. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| Switch Collector | 1 | Step-up converter: Possible power transistor damage due to overcurrent. | A |
| | | Step-down converter: No current limit function. | C |
| Switch Emitter | 2 | Step-up converter: Short circuits $V_{IN}$. Converter will not power up. | B |
| | | Step-down converter: No effect on IC, but short circuits $V_{IN}$ to $V_{OUT}$ through the sense resistor. | B |
| Timing Capacitor | 3 | Possible power transistor damage due to overcurrent. | A |
| GND | 4 | Short circuits $V_{IN}$. Converter will not power up. | B |
| Comparator Inverting Input | 5 | No effect on IC, but converter not switching as too high output voltage is detected. | B |
| $V_{CC}$ | 6 | No effect. | D |
| $I_{PK}$ | 7 | No current limit function. | C |
| Driver Collector | 8 | Step-up converter: Possible drive transistor damage due to overcurrent. | A |
| | | Step-down converter: No current limit function. | C |

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