Functional Safety Information

TPSI310x-Q1, TPSI310x Functional Safety FIT Rate, FMD, and Pin FMA

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1 Overview

This document contains information for the TPSI310x-Q1 and TPSI310x family (SSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Failure Mode Distribution (FMD)
- Pin failure mode analysis (Pin FMA)

Functional Block Diagram shows the device functional block diagram for reference.

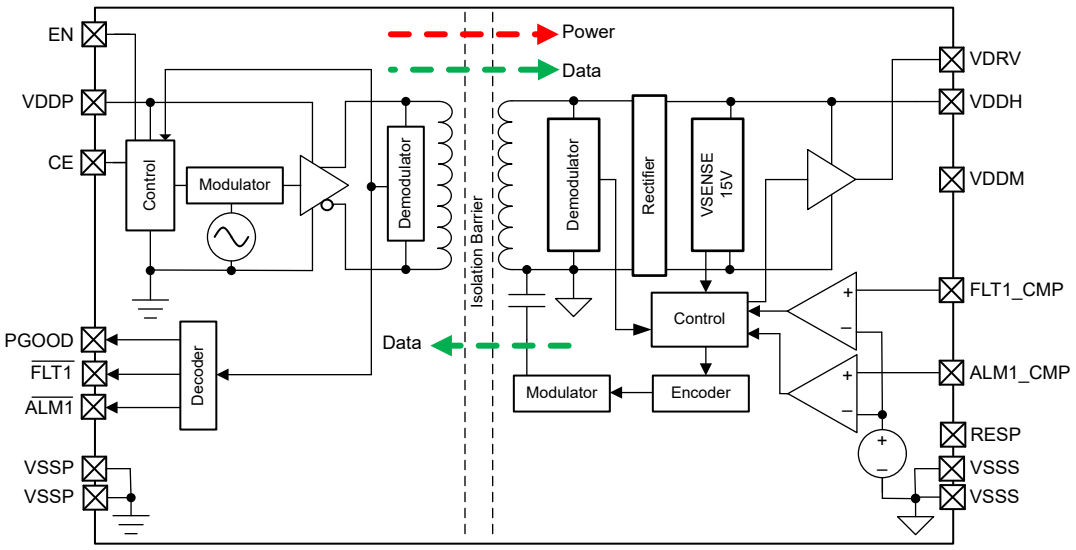

Figure 1-1. Functional Block Diagram

The TPSI310x-Q1 and TPSI310x family was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

ADVANCE INFORMATION for preproduction products; subject to change without notice.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPSI310x-Q1 and TPSI310x family based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	19
Die FIT Rate	3
Package FIT Rate	16

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed = < 50-V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution for the TPSI310x-Q1 and TPSI310x families in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VDDH/VDDM rails fail to power up. VDRV remains low.	25%
VDRV does not respond to EN signaling.	15%
Output power not meeting specification. Longer VDDH/VDDM start-up and recovery times.	25%
VDDH not regulated, potential device damage	15%
VDRV propagation times longer than specified	5%
Higher EMI	5%
Unpredictable power down sequence	5%
VDRV output held high	5%

The FMD in Die Failure Modes and Distribution excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSI310x-Q1 and TPSI310x family. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPSI310x-Q1 and TPSI310x pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the data sheets.

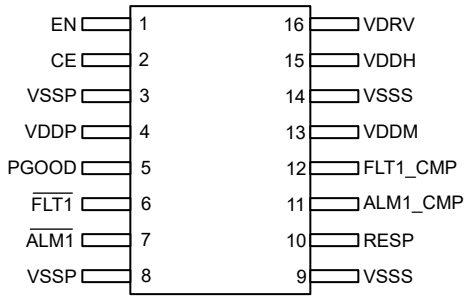

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device in normal operation prior to any open or short condition being applied to the respective pin
- EN set to a static logic low or high (VDRV asserted low or high respectively)
- CE set to a static logic low or high.
- Opens or shorts occur relative to primary and secondary sides of the device and is a static event

Table 4-2. Pin FMA for Device Pins Short-Circuited to VSSP or VSSS

Pin Name	Pin No.	Ground	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	VSSP	VDRV asserted low.	B
CE	2	VSSP	Device in standby. No power transfer. VDDH and VDDM rail discharge. VDRV asserted low with active clamp enabled.	B
VDDP	4	VSSP	No power transfer. VDDH and VDDM rail collapse. VDRV asserted low with active clamp enabled.	B
PGOOD	5	VSSP	PGOOD asserted low. If PGOOD not used, tie to VSSP.	B
$\overline{\text{FLT1}}$	6	VSSP	$\overline{\text{FLT1}}$ asserted low. If $\overline{\text{FLT1}}$ not used, tie to VSSP.	B
$\overline{\text{ALM1}}$	7	VSSP	$\overline{\text{ALM1}}$ asserted low. If $\overline{\text{ALM1}}$ not used, tie to VSSP.	B
RESP	10	VSSS	Comparator de-glitch is set to minimum value which may be less than the application requirements.	C
ALM1_CMP	11	VSSS	$\overline{\text{ALM1}}$ open-drain output is high-impedance. If ALM1_CMP not used, tie to VSSS.	B
FLT1_CMP	12	VSSS	$\overline{\text{FLT1}}$ open-drain output is high-impedance. If FLT1_CMP not used, tie to VSSS.	B
VDDM	13	VSSS	VDDH and VDDM rail collapse. VDRV asserted low with active clamp enabled.	B
VDDH	15	VSSS	VDDH and VDDM rail collapse. VDRV asserted low with active clamp enabled.	B
VDRV	16	VSSS	If VDRV was high, VDDH and VDDM rail collapse. VDRV asserts low with active clamp enabled. If VDRV was low, no effect.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	VDRV asserted low. EN pin has an internal resistive pull-down to VSSP.	B
CE	2	Device powers off. VDDH and VDDM rails discharge. VDRV asserted low. CE pin has an internal resistive pull-down to VSSP.	B
VSSP	3	Device has additional ground path through pin 8 (VSSP).	C
VDDP	4	No power transfer. VDDH and VDDM rail collapse. VDRV asserted low with active clamp enabled.	B
PGOOD	5	If PGOOD unused, no effect. If PGOOD used, PGOOD asserted high is indicated to the system regardless of actual status.	B
$\overline{\text{FLT1}}$	6	If $\overline{\text{FLT1}}$ unused, no effect. If $\overline{\text{FLT1}}$ used, $\overline{\text{FLT1}}$ asserted high is indicated to the system regardless of actual status of FLT1_CMP comparator output.	B
$\overline{\text{ALM1}}$	7	If $\overline{\text{ALM1}}$ unused, no effect. If $\overline{\text{ALM1}}$ used, $\overline{\text{ALM1}}$ asserted high is indicated to the system regardless of actual status of ALM1_CMP comparator output.	B
VSSP	8	Device has additional ground path through pin 3 (VSSP).	C
VSSS	9	Device has ground path through pin 14 (VSSS). Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows state of EN logic level.	C
RESP	10	Comparator de-glitch is set to maximum value which may be more than the application requirements.	B
ALM1_CMP	11	ALM1_CMP pin has a weak internal resistive pull-down to VSSS and can be susceptible to switching noise causing false alarm indications. If ALM1_CMP not used, tie to VSSS	B
FLT1_CMP	12	FLT1_CMP pin has a weak internal resistive pull-down to VSSS and can be susceptible to switching noise causing false alarm indications. If FLT1_CMP not used, tie to VSSS	B
VDDM	13	VDDH and VDDM can collapse under loading or switching events.	B
VSSS	14	Device has ground path through pin 9 (VSSS). Normal power transfer. VDDH and VDDM rails remain charged. VDRV follows state of EN logic level.	C
VDDH	15	VDDH can collapse under loading or switching events.	B
VDRV	16	No drive to external switch. External switch gate control can float dependent upon application circuitry.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDRV	16	VDDH	If VDRV was low, VDDH and VDDM rail collapse. VDRV remains low with active clamp enabled. If VDRV was high, no effect.	B
FLT1_CMP	12	VDDM	If strength of signal driving FLT1_CMP is high, VDDM and VDDH rails may collapse, and VDRV will be asserted low. Power transfer continues, although at a much lower amount. If strength of signal driving FLT1_CMP is weak, FLT1_CMP comparator threshold may be reached causing VDRV to be asserted low.	B
FLT1_CMP	12	ALM1_CMP	FLT1_CMP comparator threshold may be reached causing VDRV to be asserted low, along with $\overline{\text{FLT1}}$ asserting low. Similarly, if ALM1_CMP threshold reached, $\overline{\text{ALM1}}$ asserts low.	B
ALM1_CMP	11	RESP	Depending on strength of signal driving ALM1_CMP, ALM1_CMP threshold may not be reached, and no $\overline{\text{ALM1}}$ events will occur. De-glitch of comparators may increase or decrease depending on strength of signal driving ALM1_CMP.	B
EN	1	CE	EN can be tied to CE in the application if desired.	D
PGOOD	5	$\overline{\text{FLT1}}$	Electrical ORing of PGOOD and $\overline{\text{FLT1}}$open-drain outputs. All status indicators can be tied in the application if desired.	D
$\overline{\text{FLT1}}$	6	$\overline{\text{ALM1}}$	Electrical ORing of $\overline{\text{FLT1}}$ and $\overline{\text{ALM1}}$open-drain outputs. All status indicators can be tied in the application if desired.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDDP

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN	1	EN can be tied to VDDP in the application if desired.	D
CE	2	CE can be tied to VDDP in the application if desired. Device powers up depending on voltage level of VDDP.	D
PGOOD	5	Potential high current from VDDP while PGOOD asserted low. Device may thermal cycle or may get damaged.	A
$\overline{\text{FLT1}}$	6	Potential high current from VDDP while $\overline{\text{FLT1}}$ asserted low. Device may thermal cycle or may get damaged.	A
$\overline{\text{ALM1}}$	7	Potential high current from VDDP while $\overline{\text{ALM1}}$ asserted low. Device may thermal cycle or may get damaged.	A

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