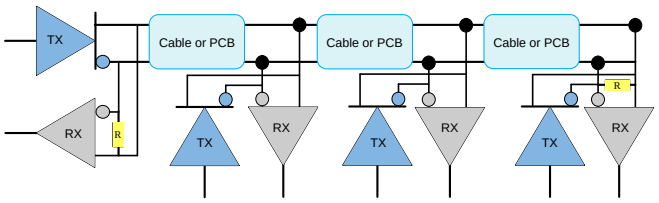
How Far, How Fast Can You Operate M-LVDS Transceivers?

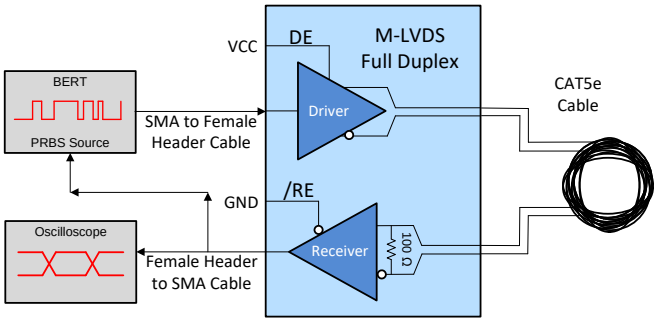
Multipoint Low Voltage Differential Signaling (M-LVDS) devices give LVDS benefits to the multipoint data transmission world. In a multipoint configuration, transmitters/drivers and receivers are interconnected on a single transmission line. The line is doubly terminated on both ends with matching impedance (usually 100Ω), see Figure 1. This technical note shows the performance in maximum data rates and distances connecting M-LVDS transceivers.

Figure 1. Multipoint Typical Application



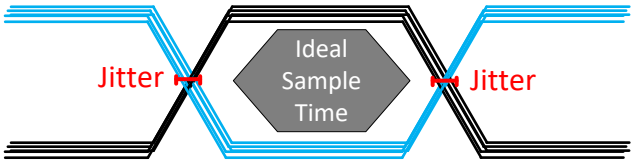
The test setup shown in Figure 2 connects a pseudo-random binary sequence (PRBS) source with two M-LVDS Evaluation Module (EVM) Boards to an oscilloscope. The three parts that use the half duplex configuration in Figure 4 are: SN65MLVD201, SN65MLVD206, and the SN65MLVD206B. The test set up for the full duplex configuration of the SN65MLVD207 is shown in Figure 2. The tests were conducted at the following cable lengths: 1m, 5m, 10m, 50m, and 100m; and each Cat-5e cable was modified with female headers to connect to the male headers on the EVM boards. A Bit Error Rate Tester (BERT) generates a 2^{31}-1 PRBS pattern, it is sent to the system and loops back to the analyzer, which compares to the generated signal. If the pattern matches, the system is said to have no errors. The error margin to not be surpassed in this lab experiment was 1 x 10^{-12} for the bit error rate.

Figure 2. Full Duplex M-LVDS Test Setup



The signal passing through the driver and receiver is connected to an oscilloscope to be observed as an eye diagram. Eye diagrams are made when a signal is repeatedly sampled over itself and is used to measure jitter. Jitter is the measured "error" in time difference of when a system cannot tell the difference between a high or a low bit. It is measured at the crossing point of the bits in an eye diagram as shown in Figure 3.

Figure 3. Eye Diagram



Jitter percentage is valuable when seeing what percentage of the eye will be open, providing a window of bit time to correctly sample the signal. To better understand jitter, Figure 5 shows examples of what 5%, 10%, 20% jitter. Up to 20% jitter, the signal should be clean enough to get readings with no errors. Above 20% it is not ensured that the signal is error free; however, higher jitter percentages were shown to be below the error margin of 1 x 10^{-12} bit error rate using the BERT.

Figure 4. Half Duplex M-LVDS Test Setup

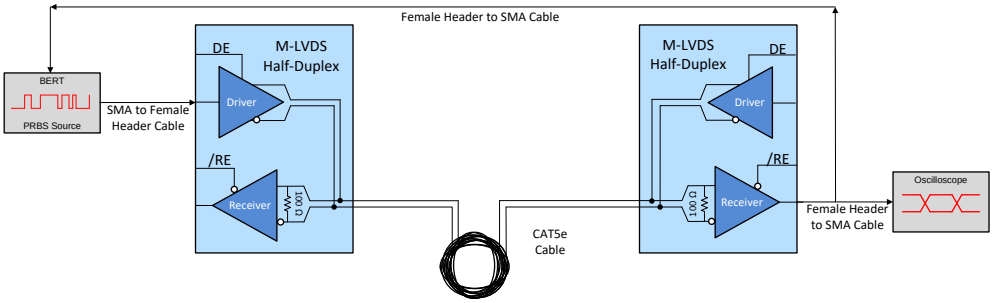
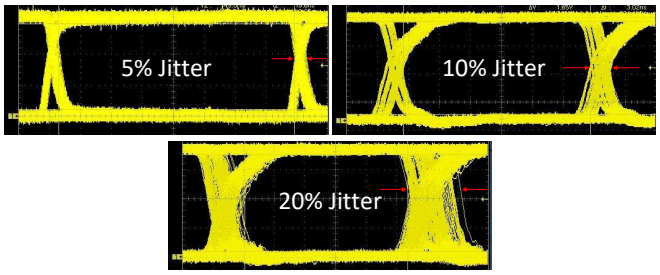
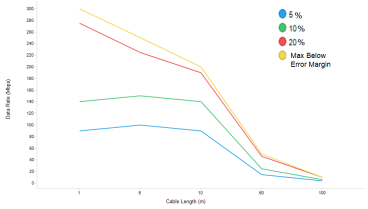


Figure 5. Example of 5%, 10%, and 20% Jitter



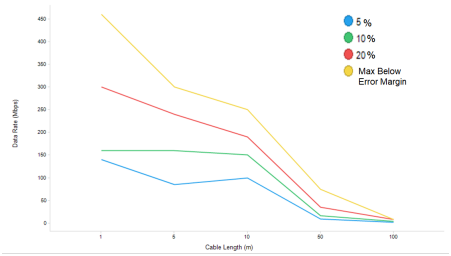
All of the parts chosen for this experiment (SN65MLVD201, SN65MLVD206, SN65MLVD206B, SN65MLVD207) have data sheet specifications of being able to achieve signaling rates up to 200 Mbps. As you can see, in Figure 6, Figure 7, and Figure 8, all devices meet and exceed the specified up to 200 Mbps signaling rates from the data sheets.

Figure 6. SN65MLVD201 Results



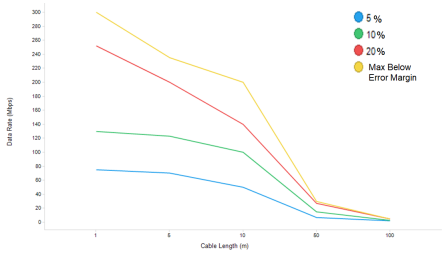
SN65MLVD201 operates up to 300 Mbps at short distances, 100 Mbps above what is specified on the data sheet. At a longer distance of 50m, the SN65MLVD201 is able to function up to 50 Mbps.

Figure 7. SN65MLVD206



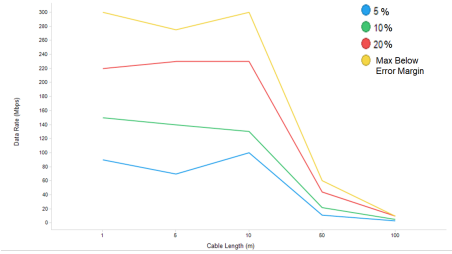
SN65MLVD206 operates up to 450 Mbps at short distances, 250 Mbps above what is specified on the data sheet. The limitation of M-LVDS standard is 500 Mbps. At a longer distance of 50m, the SN65MLVD206 is able to function up to 50 Mbps.

Figure 8. SN65MLVD206B



SN65MLVD206B operates up to 300 Mbps at short distances, 100 Mbps above what is specified on the data sheet up to 10m.

Figure 9. SN65MLVD207



SN65MLVD207 performed above the 200 Mbps at short distances, and in longer distances like 5m it could handle a data rate of 60 Mbps.

Table 1. Final Results[1][2]

Jitter	5%				10%				20%				Max Below Error Margin			
EVM	201	206	206B	207	201	206	206B	207	201	206	206B	207	201	206	206B	207
1m	90	140	75	90	140	160	160	150	275	300	252	220	300	460	300	300
5m	100	85	70	70	150	160	160	140	225	240	200	230	250	300	235	275
10m	90	100	50	100	140	150	150	135	190	190	140	230	200	250	200	250
50m	15	9	7	11	25	17	17	22	46	35	27	44	50	50	27	60
100m	4	3	2	3	6	4	4	5	10	8	5	10	10	8	5	10

(1) All data values are in Mbps.

(2) '201' is representative of the SN65MLVD201; '206' is representative of the SN65MLVD206; '206B' is representative of the SN65MLVD206B; '207' is representative of the SN65MLVD207

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265