Application Report
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AFE768x Power Dissipation Comparison Across Modes

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ABSTRACT

The AFE768x is a family of 4T4R RF sampling transceivers. There are a variety of ways to configure the device related to sampling frequency, data rate, number of SerDes lanes, number of channels, and FDD/TDD duplex options. Each option impacts the power consumption of the device. This document illustrates the power consumption trade-offs between modes so that the designer can implement the best options for the system at the optimum power dissipation.

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Trademarks

1 Introduction

The AFE768x is a family of RF sampling transceivers. There are a variety of ways to configure the device to achieve required system performance and allocation and to minimize power consumption. The parameters varied were:

- Clock frequency
  - Int: 5898.24 MHz or 8847.36 MHz
  - Ext: 5898.24 – 3500 MHz
- Interpolation Rate / Decimation Rate
- Number of Lanes
- Channel count: 2 or 4
- Duplex Options: FDD or TDD

The above parameters are not all independent. Interpolation/Decimation rate, sample frequency, number of lanes and channel count determine appropriate LMFS JESD204B parameters and Serdes speed. For this analysis the SerDes speed was limited to 10-Gbps or less and the TX/RX serdes speeds were kept the same.

The relationship to the above parameters is shown below.

- Fdata = Fs (Sampling Frequency) / INT
- Total Bit Rate = Fdata * 16-bits * 10/8 (encoding) * I/Q Channels * # of Channels

- Bit Rate per Lane = Total Bit Rate / Number of Lanes.

Let's look at an example calculation with the following parameters:

- Fs = 8847.36 MSPS
- INT = 18x
- 4 I/Q Channels
- 8 Lanes

The calculations yield:

- Fdata = 8847.36 MSPS / 18 = 491.52 MSPS
- Total Bit Rate = 491.52 MSPS * 16 * 10/8 * 2 (I/Q) * 4 (Channels) = 78.6432 Gbps
- Bit Rate per lane = 78.6432 / 8 = 9.8304 Gbps per lane

In this example, the SerDes speed is just at the (artificial) limit. Reducing the speed would require increasing the number of lanes (except it is already at the limit) or reducing the sampling clock and/or increasing the interpolation/decimation (i.e. reducing data rate) or decreasing the channel count. Reducing the data rate will decrease bandwidth capability. Reducing sampling clock generally reduces higher frequency operation. Though these modifications limit the performance capability of the device, it will reduce power consumption. The designer has the flexibility to weigh the trade-offs to meet system requirements. This document provides insights into the power consumption relative to device parameters with the intent to showcase which parameters have the most significant impact on current consumption.

Note, official power consumption specifications are outlined in the datasheet. The power consumption parameters used in this analysis were taken on a single device on the AFE7686 evaluation module (EVM) and may have slight differences due to power management configurations. The primary intent is to provide relative consumption performance across different parameters.

2 Power Analysis

2.1 4-Channel FDD Power Dissipation

Figure 1 shows the power dissipation for 4-channels operating in FDD for a variety of data rates over two sample clock frequencies and across either 4- or 8-lanes.

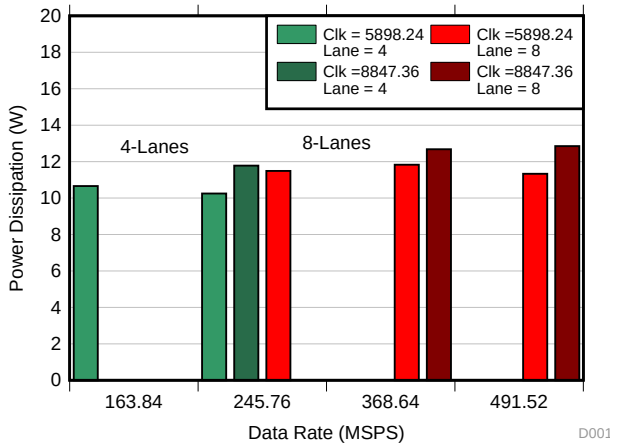

Figure 1. 4-Channel Power Dissipation across Data Rate, Sample clock, and SerDes Lanes

The far-right power dissipation is at the highest sample clock and highest number of lanes operating at the highest (within this analysis) data rate. This mode corresponds to the E1 mode within the datasheet and represents the highest power consumption reference point. The key observations from the data show:

- Reducing clock from ~9-GSPS to ~6-GSPS will save 1-1.5 W of dissipation
- Reducing data rate in itself has minimal impact on power dissipation; may see some increase due to different digital decimation/interpolation configuration.

- Reducing lane count in half provides about 1-1.25 W power saving.

2.2 2-Channel FDD Power Dissipation

Figure 2 shows the power dissipation for 2 channels operating in FDD for a variety of data rates over two sample clock frequencies and across either 2- or 4- or 8-lanes.

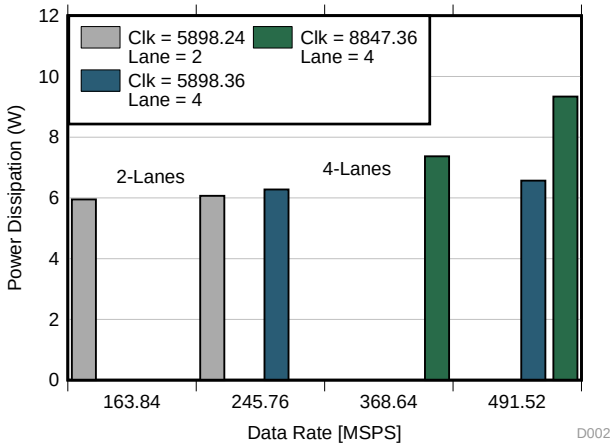

Figure 2. 2-Channel Power Dissipation across Data Rate, Sample clock, and SerDes Lanes

The following key observations for this data are below:

- Reducing from 4 channels to 2 channels saves around 3.5 – 5 W
- Reducing from ~9 GSPS clock to ~6-GHz clock yield savings of: ~2-W
- Reducing data rate in itself has minimal impact on power dissipation
- Reducing lane count in half provides about 200 mW power saving.

Operating with ~6-GHz clock in 2-lanes at the lower data rate results in total power consumption just under 6-W which is a good threshold for narrow-band systems.

2.3 Power Dissipation over Sampling Frequency

Reducing the sample clock rate further reduces the power consumption. The internal PLL/VCO minimum limit is around 6-GHz, but an external clock can provide any arbitrary value. The power consumption as a function of clock frequency is shown in Figure 3.

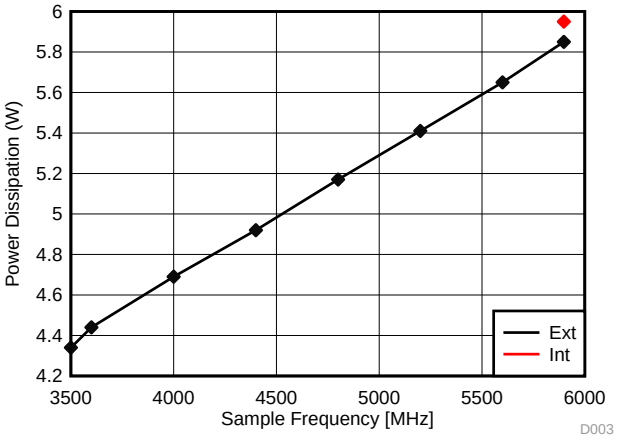

Figure 3. Power Dissipation vs. External Sample Clock

2.4 TDD Power Dissipation

The previous analysis assumed FDD operation implying the transmitter and receiver operated simultaneously. In TDD applications the transmitter and receiver alternate. As expected, the average current is drastically reduced when only one side is on at a time. Figure 4 shows the power dissipation with ~6-GHz clock in TDD mode across 4- and 2-channels. For reference, the ~9-GHz TX only 4-channel data point is shown which corresponds to mode E2 in the datasheet.

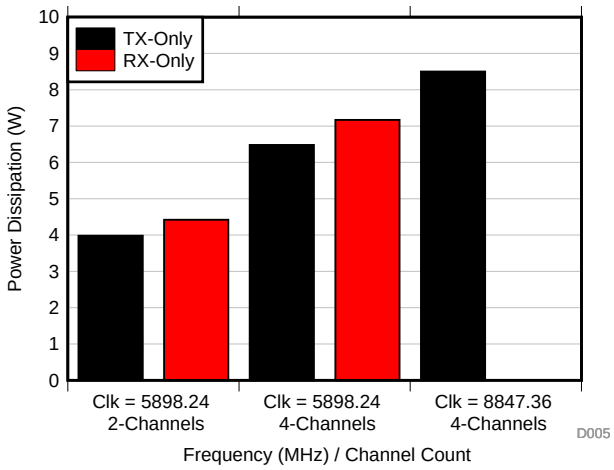

Figure 4. Power Dissipation in TDD Mode

The power dissipation in TDD mode in 2-channel configuration operating with a ~6-GHz clock is less than 4.5-W.

3 Conclusion

The configuration of the AFE768x device directly impacts power dissipation. In critical power consumption systems or thermally constrained mechanics the variables outlined within the report provide a means to adjust the parameters to estimate power consumption for a given system constraint like bandwidth requirements or SerDes speed limitation. Table 1 shows the details of the configurations used in the graphs and analysis.

Table 1. Power Dissipation Analysis Parameters

Clk Input	Clk	Int	Dec	DataRate	Channels	Lanes	Serdes/Lane	Duplex	Pdiss
Int	8847.36	18	6	491.52	4	8	9830.4	FDD	12.85
Int	8847.36	24	8	368.64	4	8	7372.8	FDD	12.68
Int	5898.24	12	6	491.52	4	8	9830.4	FDD	11.33
Int	5898.24	16	8	368.64	4	8	7372.8	FDD	11.83
Int	5898.24	24	12	245.76	4	8	4915.2	FDD	11.49
Int	8847.36	36	12	245.76	4	4	9830.4	FDD	11.78
Int	5898.24	24	12	245.76	4	4	9830.4	FDD	10.25
Int	5898.24	36	18	163.84	4	4	6553.6	FDD	10.66
Int	8847.36	18	6	491.52	2	4	9830.4	FDD	9.34
Int	8847.36	24	8	368.64	2	4	7372.8	FDD	7.37
Int	5898.24	12	6	491.52	2	4	9830.4	FDD	6.57
Int	5898.24	24	12	245.76	2	4	4915.2	FDD	6.28
Int	5898.24	24	12	245.76	2	2	9830.4	FDD	6.07
Int	5898.24	36	18	163.84	2	2	6553.6	FDD	5.95
Ext	5898.24	36	18	163.84	2	2	6553.6	FDD	5.85
Ext	5600	36	18	155.56	2	2	6222.2	FDD	5.65
Ext	5200	36	18	144.44	2	2	5777.8	FDD	5.41

Table 1. Power Dissipation Analysis Parameters (continued)

Clk Input	Clk	Int	Dec	DataRate	Channels	Lanes	Serdes/Lane	Duplex	Pdiss
Ext	4800	36	18	133.33	2	2	5333.3	FDD	5.17
Ext	4400	36	18	122.22	2	2	4888.9	FDD	4.92
Ext	4000	36	18	111.11	2	2	4444.4	FDD	4.69
Ext	3600	36	18	100.00	2	2	4000.0	FDD	4.44
Ext	3500	36	18	97.22	2	2	3888.9	FDD	4.34
Int	5898.24	24	12	245.76	2	4	4915.2	TDD-TX	3.98
Int	5898.24	24	12	245.76	2	4	4915.2	TDD-RX	4.42
Int	5898.24	24	12	245.76	4	8	4915.2	TDD-TX	6.48
Int	5898.24	24	12	245.76	4	8	4915.2	TDD-RX	7.17
Int	8847.36	18	6	491.52	4	8	9830.4	TDD-TX	8.5

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