Application Report
SLAA892–March 2019

# PLL and Clocking Configuration for Audio Devices

**ABSTRACT**

In audio applications, the clocking scheme, routing, and synchronization are strongly related to the quality of treated audio signal. Although Texas Instruments (TI) audio devices are complex and offer some flexibility on their configuration, the clocking scheme is always sensitive and crucial to get the best results. Correct clocking configuration avoids issues that can affect the audio experience. In addition, most part of audio converters and audio amplifiers require at least one system clock or master clock for full operation. Hence, clocking generation from internal Phase-Locked Loop (PLL) and clock dividers is important.

This application report is intended to be a complement of TI audio devices documentation and can be used as a guide to understand and configure the PLL and clock dividers blocks of TI audio devices. It also provides some suggestions for designing configuration stages and takes some of the TI audio amplifiers and converters that are used in common applications as examples.

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## Trademarks

# 1 Introduction

Audio devices represent an important role in electronics applications nowadays. From a single beep in an alarm clock to a sophisticated audio system in a vehicle, audio components have become necessary in every electronic solution of global market.

However, from this need of an audible event in the daily life, one of the main challenges is audio experience improvement. This challenge normally means the elimination or reduction of common issues such noise, pops, echo, clipping, or artifacts. All these issues depend on the design or configuration of filters and in some cases, an audio conversion. Whatever the required solution is, it is necessary to include a robust clocking scheme to satisfy all the requirements to have a correct audio treatment.

TI offers audio devices with an advanced clocking scheme, giving a high priority to its flexibility and configuration. You have to understand the clocking scheme behavior and some rules for its correct usage.

# 2 Clocking Scheme Concepts

In order to understand how the TI audio devices clocking scheme works, it is necessary to talk a about the basis of the blocks that compose the devices clock generation trees. These concepts are used in this entire document since they are essential parts of the audio devices.

## *2.1 Frequency Divider*

A frequency divider is a circuit that takes an input signal with a defined '$f_{in}$' frequency and generates an output signal with a '$f_{out}$' frequency. This $f_{out}$ frequency is 'n' times lower than $f_{in}$, where 'n' is an integer.

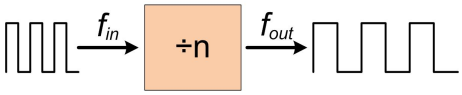



**Figure 1. Frequency Divider**

Communication and information technology are examples of final areas where the frequency dividers are used. These areas often require of data conversion and technology to convert or interpret protocols. In audio devices, the frequency dividers allow to reduce the frequency from a master or a system clock and generate one or more clocks that can be used for different purposes.

For example, assume that you send two data channels of 32 bits each. You need a sampling rate (fs) or a Word Clock (WCLK) of 48 KHz, but you also need a clock for a bit transmission (BCLK) of 3.072 MHz (48 KHz × 32 bits/channel × 2 channels). As a solution, you can route two clocks (WCLK and BCLK) with these frequencies to the audio device. However, for cases where the circuit design or the resources are limited, a master clock can be adapted for the audio device and the rest of electronic components in the circuit. Some devices feature frequency dividers that can reduce the input clock frequency down to 256 times. Then, you can connect a 12.288 MHz oscillator to the entire circuit and the WCLK and BCLK can be generated by the supported frequency dividers.

In some TI audio devices, there are up to six frequency dividers that can be combined to generate many clocks for internal operation or even for external components. The audio devices have also the capability to work in master or slave mode, making the clocking scheme flexible for many applications.

## *2.2 Phase-Locked Loop (PLL)*

The PLL is a feedback control system composed of at least three blocks: Phase Comparator, Loop Filter, and Voltage Controlled Oscillator (VCO). The Phase Comparator is the first part of the PLL system. In this stage, it is necessary to consider that the entire system is looped. Figure 2 shows the output signal is taken for the system input operation.. The Phase Comparator, as is it is named, compares the phases of the input and output signals. Then, it generates a voltage signal that depends of the phase error.

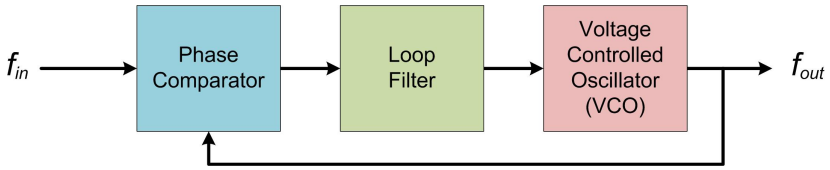


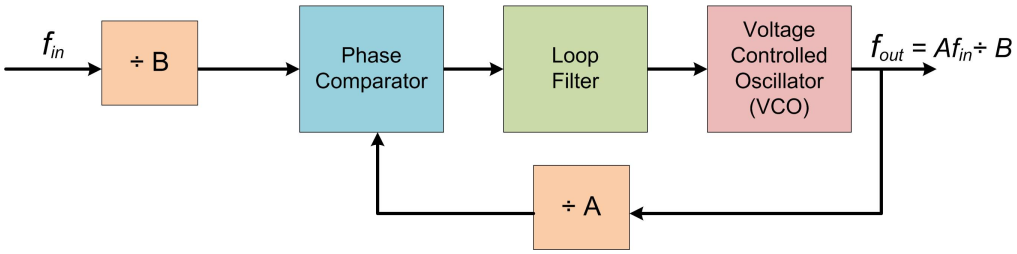

**Figure 2. Phase-Locked Loop**

The Phase Comparator can be also understood as a multiplier block whose output results in two components $2\pi f_{in} \pm 2\pi f_{out}$ (or $w_{in} \pm w_{out}$). The Loop Filter is placed as a low-pass filter that eliminates the high frequency components. When $f_{out} = f_{in}$, the Loop Filter rejects the $2\pi f_{in} + 2\pi f_{out}$ part, and the remaining signal results in a DC component.

The VCO generates a frequency that is linearly proportional to $f_{in}$. The VCO output or fout is balanced until $f_{out} = f_{in}$ since this relation produces a constant oscillation at the output. The simplest phase-locked loop produces an output signal with the same phase than the input signal. This is a control used in applications involved with signal demodulation or clock synchronization.

In some applications, the PLL can be also complemented with frequency dividers, phase shift blocks, or edge detectors. When frequency dividers are included in the feedback path and in the initial phase, the PLL is configured as a Frequency Synthesizer.

**Figure 3. PLL in Frequency Synthesizer Configuration**




A Frequency Synthesizer generates a frequencies range from a single input frequency. The output frequency ($f_{out}$) can be calculated once the input frequency ($f_{in}$) and the dividers are fixed. The frequency dividers in this system can also increase the input frequency as high as the system capacity allows. This is the principle used in the TI Audio Devices Clocking Scheme.

## 3 PLL and Clocks Distribution Tree in Audio Devices

In general terms, an audio device requires of a clock scheme when a serial data interface is supported. This means that the device contains at least one section dedicated to data conversion. It implies that you have a sampling clock that is used to convert analog waveforms into digital signals or vice versa.

Normally, it is suggested to use external clock values with frequencies 256 times the desired sampling rate. This help to reduce additional operations and, consequently, current consumption. The devices feature frequency dividers that generate the sampling clocks from an external oscillator. However, when it is not possible to use a clock with these conditions (due to some design limitations or the external components that need nonstandard clock frequencies), an internal PLL is required.

The on-chip PLL generates the clocks for the audio DAC, digital processing, serial interface, digital microphone, or other features depending on the audio device. Evidently, the clock distribution scheme can vary depending of the features that the device supports. TAS2562, TAS2552, and TLV320DAC3203 are examples from different families. They support a different clock distribution since their features need multiple frequencies to work.

### 3.1 TAS2562

Instead of configuring the PLL parameters and dividers like in the TAS2552 and TLV320DAC3203 families (as explained in further sections), TAS2562 clocking scheme only requires of few bits to select between the manual or auto detection modes. Once the mode is selected and the SBCLK to FSYNC ratio is determined, the clock engine generates the sampling rate by itself.

**Table 1. TAS2562 Supported SBCLK Frequencies (44.1 KHz Based Sample Rates)**

| SAMPLE RATE | SBCLK to FSYNC RATIO | | | | | | |
|---|---|---|---|---|---|---|---|
| | 64 | 96 | 128 | 192 | 256 | 384 | 512 |
| 7.35 KHz | 470.4 KHz | 705.6 KHz | 940.8 MHz | 1.4112 MHz | 1.8816 MHz | 2.8224 MHz | 3.7632 MHz |
| 14.7 KHz | 940.8 MHz | 1.4112 MHz | 1.8816 MHz | 2.8224 MHz | 3.7632 MHz | 5.6448 MHz | 7.5264 MHz |
| 22.05 KHz | 1.411 MHz | 2.116 MHz | 2.8224 MHz | 4.2336 MHz | 5.6448 MHz | 8.4672 MHz | 11.2896 MHz |
| 29.4 KHz | 1.8816 MHz | 2.8224 MHz | 3.7632 MHz | 5.6448 MHz | 7.5264 MHz | 11.2896 MHz | 15.0528 MHz |
| 44.1 KHz | 2.8224 MHz | 4.2336 MHz | 5.6448 MHz | 8.4672 MHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz |
| 88.2 KHz | 5.6448 MHz | 8.4672 MHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz | - | - |
| 176.4 KHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz | - | - | - | - |

Page 0 / Register 0x06 contains the entire configuration to set the sample rate and its clock polarity. When the clock frequencies are stable and respect the selected ratio, the output signal can reach the expected electrical characteristics according to the datasheet. Figure 4 shows an example of how a filtered Class-D output signal must look when the ratios are respected. In this example, the Class-D output is connected to a 8 Ω load. The measured THD+N was 0.018% at 1 W.

(Yellow signal: Class-D Positive terminal waveform; red signal: Class-D differential waveform; green signal: Class-D negative terminal waveform).

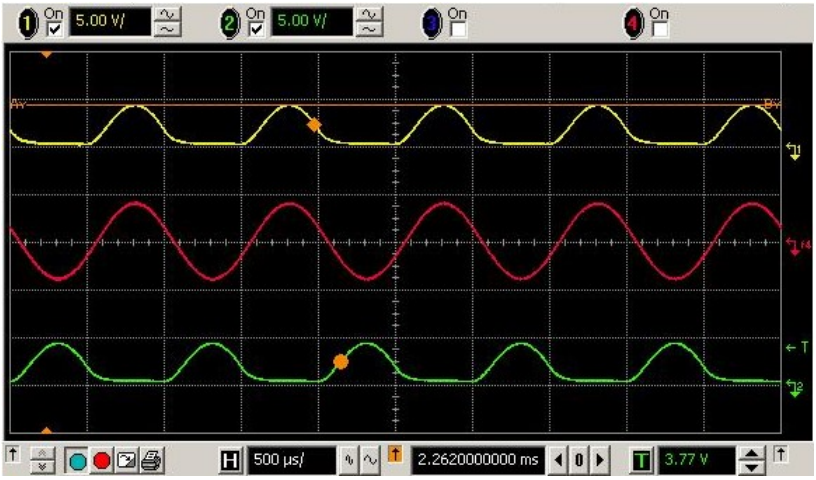



**Figure 4. TAS2562 Class-D Output With Correct Clocking Scheme (THD+N = 0.018%, 8 Ω, 1 W)**

The sample rate auto detection is enabled in this example and its sample rate is fixed to 44.1 KHz or 48 KHz. In addition, the selected clocks for this case are FSYNC = 44.1KHz and SBCLK = 2.2884 MHz, having a ratio of 64. This configuration allows to reach THD + N = 0.018% with a 8 Ω load at 1 W.

When the clocking configuration is correct, the page 0 / register 0x11 shows the detected SBCLK to FSYNC ratio (04h = 64 in this case) and the sample rate (100b = 44.1/48 KHz for this example).

However, if the ratio is not respected, the signal performance may change significantly, affecting the audio experience. Even if the auto detection mode is enabled and the registers configuration is correct, the output may be directly affected if the ratio is not supported. Using a SBCLK = 2.5 MHz and FSYNC = 44.1 KHz, it results in a ratio of ~56.68. This ratio is not detected correctly by the device and the page 0 / register 0x11 shows it as invalid ratio (0F).

Although the output signal seems to be correct and the sampling rate is correctly detected, the THD+N noticeably changes. The same configuration with a wrong clock ratio results in THD+N = 0.084%.

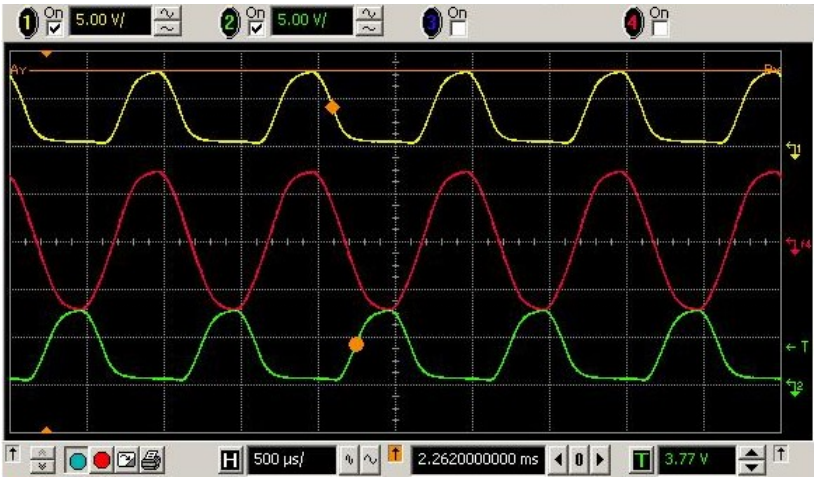



**Figure 5. TAS2562 Class-D Output With Wrong Clocking Scheme (THD+N = 0.084%, 8 Ω, 1 W)**

In case of the manual clocking configuration, it is important to select the correct settings according to the provided clocks. The manual configuration requires of a sampling rate selection through the register 0x06, bits 3-1. It is necessary to configure the device with the same sample rate to be used. Using a different value may result in a THD+N increment.

Figure 6 shows an example of a correct sample rate selection. The TAS2562 is configured to use 44.1 KHz. THD+N resulted in 0.022%.

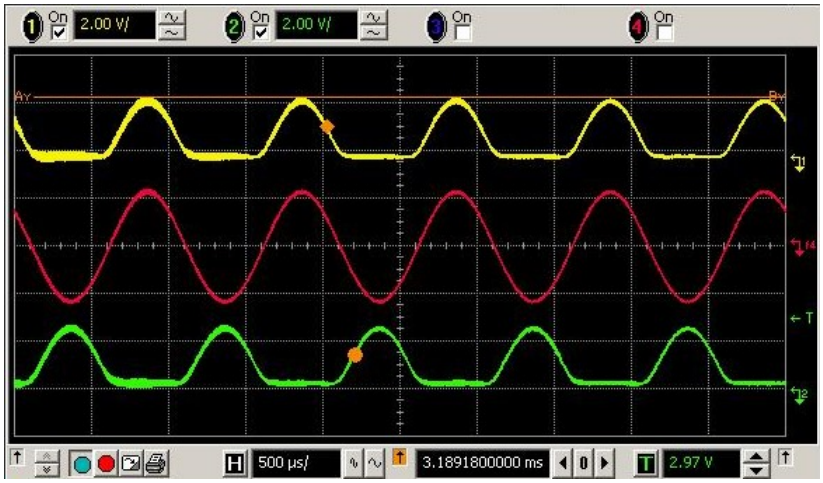



**Figure 6. TAS2562 Class-D Output With Correct Manual Clocking Configuration (THD+N = 0.022%, 8 Ω, 0.5 W)**

However, if the same sampling clock is used (FSYNC = 44.1 KHz) but the register 0x06 is configured to select a higher frequency value (88.2 Khz or 176.4 KHz), the THD+N is affected even if the waveform is similar to the correct configuration. In the example below, the sampling rate is selected as 176.4 KHz, but the THD+N value changed from 0.022% to 0.098%

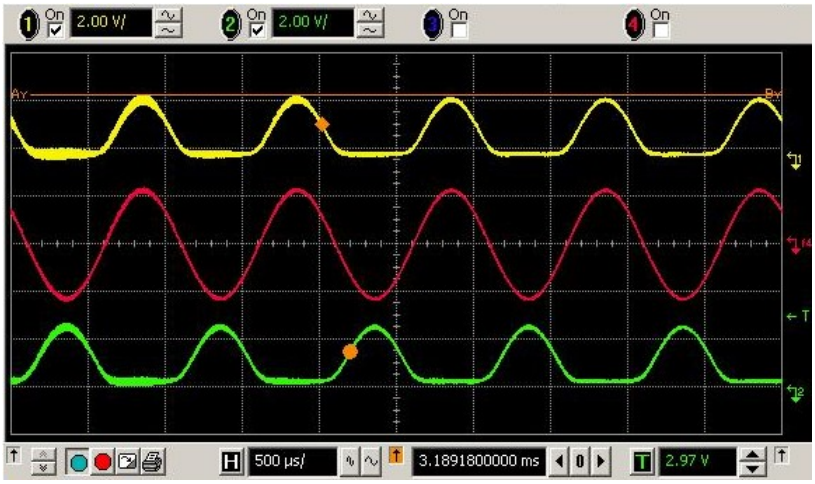



**Figure 7. TAS2562 Class-D Output With Incorrect Manual Clocking Configuration (THD+N = 0.098%, 8 Ω, 0.5 W)**

### 3.2 TAS2552

TAS2552 is an audio amplifier which features a different clocking scheme. It allows more flexibility for the clock inputs due to its internal and programmable PLL.

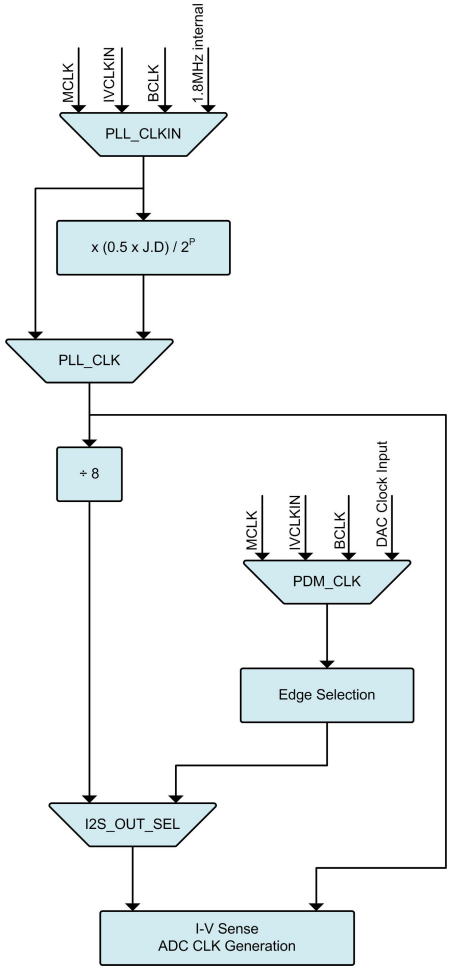



**Figure 8. TAS2552 Clock Distribution Tree**

You can take advantage of many possibilities that the clock distribution trees offer: Multiple clock inputs, frequency dividers, clocks generation, frequency ranges, and so forth. Due to this flexibility that TI audio devices offer, you can easily design the clock lines in the PCB. In addition, these devices can be configured as master devices and generate the clock signals for I2S or PDM protocols.

However, there are many limitations that you must respect when the PLL and clock distribution trees are configured. Figure 8 shows the TAS2552 tree contains a PLL section. This section acts as frequency divider or multiplier that depends of up to four parameters. They can be easily configured by the registers settings. The parameters J, D, and P support many values and, consequently, there are hundreds of possible PLL output frequencies. Although the audio devices offer a good flexibility in the clock lines, it is important to consider that the audio devices have defined clock ranges. Hence, having a clock rate configured out of the ranges may result in a device malfunction.

**Table 2. PLL_CLKIN Rule Comparison**

| TAS2552 |
|---|
| 512 KHz ≤ (PLL_CLKIN / $2^P$) ≤ 12.288 MHz; when D = 0 |
| 1.1 MHz ≤ (PLL_CLKIN / $2^P$) ≤ 9.2 MHz; when D ≠ 0 |

Table 2 contains some conditions that you must consider when the external clock is selected. In these cases, only the parameter P and the PLL input clock can cause a misconfiguration in the device. Consequently, the device can be affected and you can risk having low performance on the treated audio signal.

In addition to the Table 2 conditions, this device has more rules that must be satisfied to get a correct PLL configuration. The PLL section of the *TAS2552 4.0-W Class-D Mono Audio Amplifier with Class-G Boost and Speaker Sense Data Sheet* includes all the necessary information that must be followed before selecting the PLL input clock and the rest of parameters.

Equation 1 shows a correct configuration of the clocking scheme through the registers settings. The selected clocks for this case are MCLK = 11.2896 MHz; LRCLK = 44.1 KHz; BCLK = 2.8224 MHz. Notice that this configuration only contains the clocking settings. You must configure the rest of register. Registers command is in the following format:

w 80 xx yy

where

- 'w' is the write command
- 80 is the I2C address
- xx is the register number in hex format
- yy is the register data in hex format (1)

| REGISTER CONFIGURATION | REGISTERS DESCRIPTIONS AND RULES |
|---|---|
| w 80 01 02 | Register 0x01 is used to select the PLL input, mute the Class-D channel and also enable the software shutdown. This command shuts down all blocks (B7 = 1), unmutes the Class-D channel (B2) and selects MCLK as PLL input (B5-B4). Bit 1 must be placed as '1' until the entire device configuration is complete. |
| w 80 00 20 | This I2C command unlocks the PLL block. Bit 5 is used to lock (0) or unlock (1) the PLL. |
| w 80 03 5d | Register 0x03 controls the kind of data to be read (digital / analog input). If digital input is selected, it also determines the input source (left / right channel or a mix of both). It selects the desired WCLK frequency to use (from 8 KHz to 192 KHz). This configuration selects the digital input, mixes both channels data and selects 44.1 KHz as WCLK frequency. |
| w 80 08 40 | PLL Control 1 is located in register 0x08. It determines the "P" Parameter Pre-Scaler value (0 or 1) and configures the "J" Parameter as well (from J = 4 to J = 96). In this case, P = 0 and J = 64. Notice that this configuration respects the rule mentioned in Table 2 (11.2896 MHz / 20 = 11.2896 MHz ≤ 12.288 MHz). |
| w 80 09 00 | PLL Control 2 (Register 0x09) determines if the PLL block is bypassed or not. Additionally, it determines the "D" parameter value (from 0 to 9999) of the PLL equation. This command does not bypass the PLL and configures D = 0. |
| w 08 01 00 | Register 0x08 is programmed again to change Bit 1 value, enabling all the device blocks. |

This is a correct way to configure the PLL and clocking registers. It is important to place special attention to the PLL rules in this kind of devices. As mentioned in the past section, some devices only require of a ratio between the serial data interface clocks. For those cases, it is not required to modify the PLL parameters and the device generates the sampling frequency based on the frequency values of the external clocks.

For this particular case, the Class-D outputs performance strongly depends of the clocking scheme. This configuration allows getting a good performance at the outputs. Using a 8 Ω load at 0.5 W, the measured THD+N is 0.098%.

(Yellow signal: Class-D Positive terminal waveform; red signal: Class-D differential waveform; green signal: Class-D negative terminal waveform)

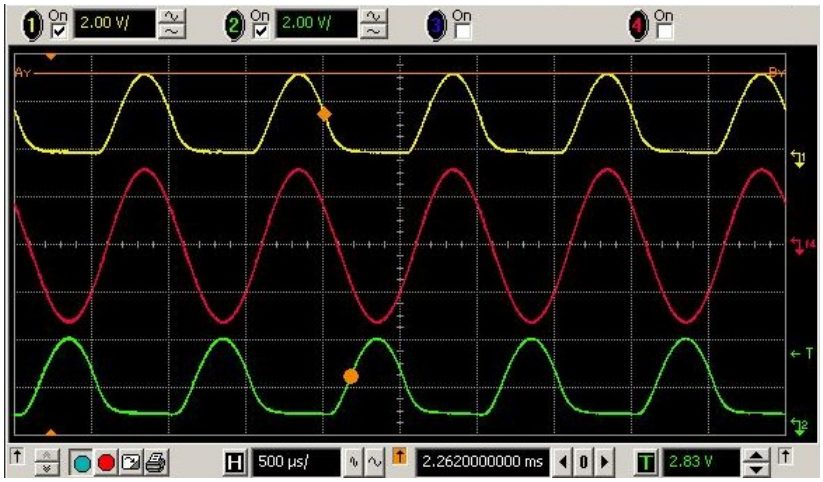



**Figure 9. TAS2552 Class-D Output With Correct Clocking Scheme (THD+N = 0.098%, 8 Ω, 0.5 W)**

By other hand, if a PLL rule is not respected or if a wrong clock frequency is selected in the clocking scheme, the Class-D output can be directly affected. The example below is configured for a MCLK = 16.9344 MHz and a WCLK = 44.1 KHz. Notice that only one register is modified and this configuration generates the 44.1 KHz sampling rate. However, the PLL_CLKIN rule is not respected.

| REGISTERS CONFIGURATION | REGISTERS DESCRIPTION AND RULES |
|---|---|
| w 80 08 60 | Only register 0x08 is modified from 0x40 to 0x60. This command configures J = 96 (J = 64 in past example). In this case, P is also '0'. Since the MCLK frequency was modified from 11.2896 MHz to 16.9344 MHz, the PLL_CLKIN limits are exceeded (16.9344 MHz / 20 = 16.9344 MHz > 12.288 MHz).<br>The rest of registers remain similar than the past example. |

Even if the sampling rate is calculated correctly, the PLL rule was omitted. This can decrease the Class-D output signal performance and affect the audio experience.

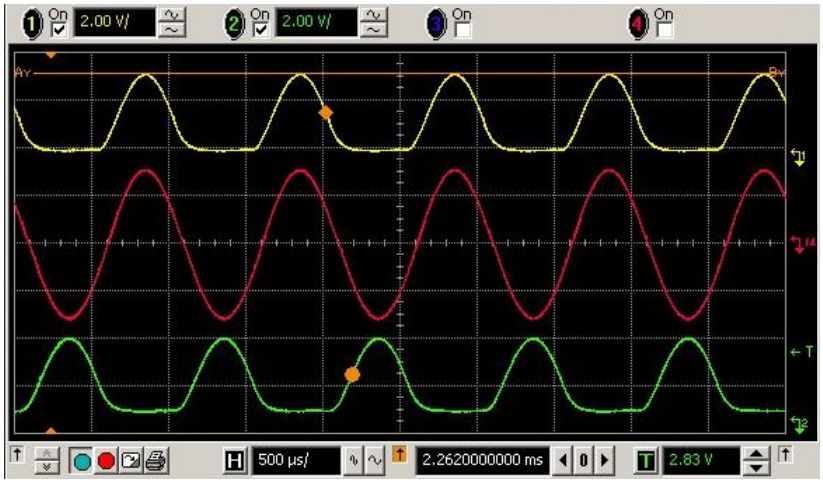



**Figure 10. TAS2552 Class-D Output With Wrong Clocking Scheme (THD+N = 0.801%, 8 Ω, 0.5 W)**

### 3.3 TLV320DAC3203

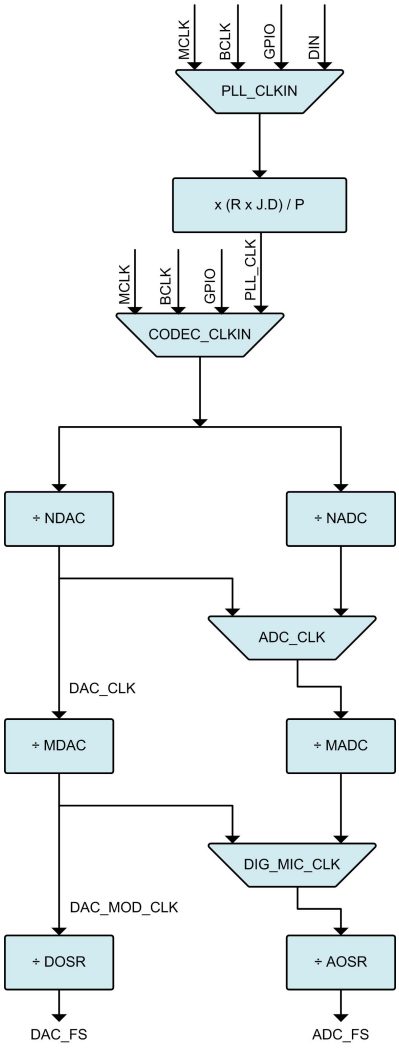



**Figure 11. TLV320DAC3203 Clock Distribution Tree**

As mentioned in the previous section, some of the TI audio devices require a registers configuration in order to configure the PLL parameters, frequency dividers, and additional features related to the clocking scheme. However, you must take care about the rules and sequences that can affect the device performance. In some cases, even the power supply voltage can be involved with the PLL behavior. Additionally, a register value can result in a device misconfiguration and the audio experience can be affected. TLV320DAC3203 has flexible clocking schemes, but it is also sensitive to wrong registers values. The PLL and the frequency dividers are the bases of all their behavior since the serial interface is the data input and output.

The TLV320DAC3203 is composed of around 20 registers that directly affect the PLL and clocking scheme, but at least four of them are required for a minimum configuration. The example below shows the correct way to configure the PLL registers map from a fixed master clock frequency. The registers configuration is in the format:

w 30 xx yy

where

- 'w' is the write command
- 30 is the I2C address
- xx is the register number in hex format
- yy is the register data in hex format
- **PLL CLKIN = MCLK = 11.2896** (2)

| REGISTERS CONFIGURATION | REGISTERS DESCRIPTION AND RULES |
|---|---|
| w 30 00 00 | In all the Registers Pages, Register 0 is used to select the Page to write. |
| w 30 01 01 | When Page 0 / Register 1 / Bit D0 is placed in high state, the entire device is reset. It sets all the registers in their default state. This is a good practice when the device is powered up. |
| w 30 04 03 | Page 0 / Register 4 selects the CODEC Clock Input. MCLK, BCLK, GPIO and PLL can be selected by Bits D1-D0. When PLL is required and chosen, Bits D3-D2 determine the PLL input. In addition, the PLL Clock Range is selected by bit D6. This bit modifies the low and high ranges of PLL. This can be used to allow generating frequencies as low as 80 MHz or frequencies as high as 137 MHz. In this example, the PLL is configured in low mode and it is selected as CODEC CLK input. |
| w 30 05 91 | This register sets the first PLL parameters: P and R. Additionally, it enables or disables the PLL block. The value 0x91 enables the PLL and configures P = 1 and R = 1. It is important to modify the PLL values only when the DAC block is disabled. Otherwise, the DAC output performance can be affected or it may generate issues such pops. |
| w 30 06 08 | This register sets the first PLL parameters: P and R. Additionally, it enables or disables the PLL block. The value 0x91 enables the PLL and configures P = 1 and R = 1. It is important to modify the PLL values only when the DAC block is disabled. Otherwise, the DAC output performance can be affected or it may generate issues such pops. |
| w 30 07 00<br>w 30 08 00 | The registers 7 and 8 of page 0 must be always written sequentially. These registers represent the D parameter MSB and LSB respectively. This parameter supports values from 0 (00 0000 0000 0000) to 9999 (10 0111 0000 1111). At this point, the generated PLL CLK is 90.3168 MHz. |
| w 30 0b 82<br>w 30 0c 90 | These registers configure the first frequency dividers blocks. They do not require to be configured sequentially, but it is good practice to do. In this case, N divider is NDAC = 2 and M divider is NDAC = 16. Notice that if NDAC = 2, DAC_CLK = 45.1584 MHz. This value is only allowed if DVDD ≥ 1.65 V (see Maximum TLV320DAC3203 Clock Frequencies Table of Reference Guide for details). Then, NDAC = 16 generates a DAC_MOD_CLK frequency of 2.8224 MHz. |
| w 30 0d 00<br>w 30 0e 40 | Register 14 is used to set the DOSR value. In this case, it is configured at DOSR = 64, resulting a DAC sampling rate of DAC_Fs = 44.1 KHz. |

This is an example of a correct PLL and frequency dividers registers configuration. When the rest of settings are also correctly configured, the TLV320DAC3203 can reach its best performance and the expected electrical characteristics of datasheet.

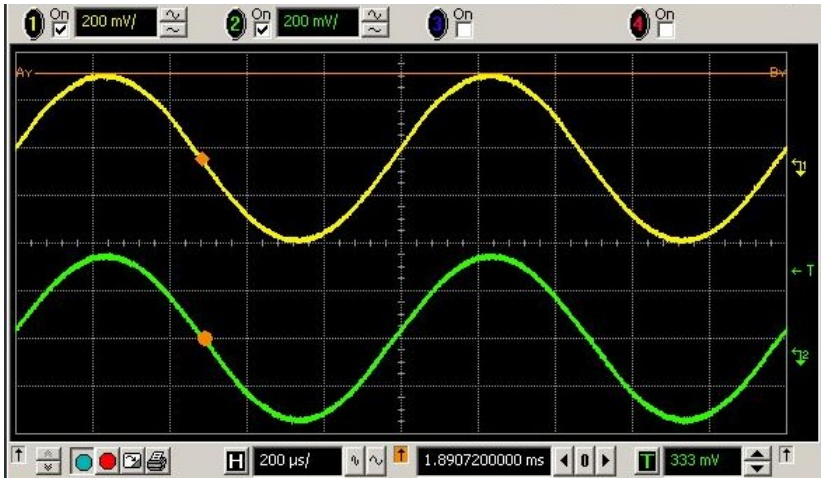



**Figure 12. TLV320DAC3203 Headphone Output With Correct Clocking Scheme (THD+N = 0.0058%, Full-Scale Signal, No Load)**

However, if any PLL rule or clock range is not respected, you can experience unexpected results even if the rest of registers and hardware design are correct. The registers configuration below is an example of a 12 misconfiguration of the PLL registers. Notice that this configuration respects almost all rules and it results in a correct sampling rate (44.1 KHz).

| REGISTERS CONFIGURATION | REGISTERS DESCRIPTION AND RULES |
|---|---|
| w 30 00 00 | Register 14 is used to set the DOSR value. In this case, it is configured at DOSR = 64, resulting a DAC sampling rate of DAC_Fs = 44.1 KHz. |
| w 30 04 03 | PLL is configured in low mode and it is selected as CODEC CLK input |
| w 30 05 84 | The value 0x94 enables the PLL and configures P = 8 and R = 4 |
| w 30 06 10 | Page 0 / Register 6 is used to configure the J = 10 |
| w 30 07 00<br>w 30 08 00 | D is configured as 0. At this point the generated PLL CLK is 90.3168 MHz. Same PLL CLK value than the correct configuration. All PLL rules are correct. |
| w 30 0b a0<br>w 30 0c 82 | In this case, N divider is NDAC = 32 and M divider is NDAC = 2. This results in a DAC_MOD_CLK = 1.4112 MHz and DAC_CLK = 2.8114 MHz. Both values respect the clocking limits. |
| w 30 0d 00<br>w 30 0e 40 | In this case, it is configured at DOSR = 32, giving a DAC sampling rate of DAC_Fs = 44.1 KHz. |

However, this value omits the rule 2.8 MHz < DOSR × DAC_Fs < 6.2 MHz. The result of the DOSR_F2 results in 1.4112 MHz. This can generate distortion or low performance in output signal as shown in the following picture.

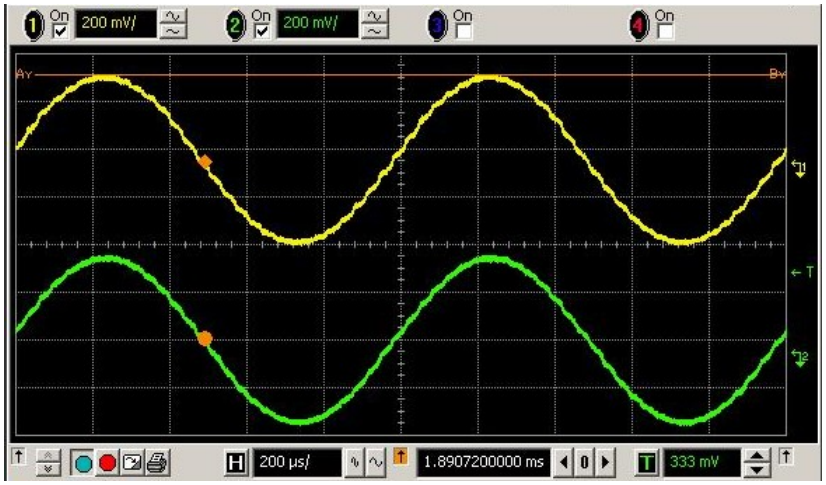



**Figure 13. TLV320DAC3203 Headphone Output With Wrong Clocking Scheme (THD+N = 0.092%, Full-Scale Signal, No Load)**

## 4 Conclusion

Each device family is composed by a different PLL and clocking schemes that you must consider when selecting an audio device. Even if the devices offer a good flexibility on their clocks distribution trees, it is crucial to know all the limitations and rules during the master or system clock selection. Omitting the details of PLL acceptable ranges can result in a misconfiguration that can affect the signal behavior and its performance.

A high percentage of issues that other users have with audio devices are related to the clocking scheme. Hence, it is important to verify multiple times the clock dividers and PLL (if used). TI audio devices offer many features that the user may take advantage of during the designing or prototyping phase. You can even configure general purposes inputs and outputs (GPIOx) or multifunction pins (MFPx) in order to generate clocks for testing purposes. This is a good practice that can save a lot of time during the first stages of a project.

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