

# ***ADS8364EVM***

## *User's Guide*

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Read This First

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### ***About This Manual***

This users guide describes the characteristics, operation, and use of the ADS8364EVM 16-bit parallel analog-to-digital converter evaluation board. A complete circuit description as well as schematic diagram is included.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1—EVM Overview
- Chapter 2—Analog Interface
- Chapter 3—Digital Interface
- Chapter 4—Power Supply
- Chapter 5—Initial Setup of the Board
- Chapter 6—EVM Schematic

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This book may contain cautions and warnings.

**This is an example of a caution statement.**

**A caution statement describes a situation that could potentially damage your software or equipment.**

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<b>Data Sheets</b>	<b>Literature Number</b>
ADS8364	SBAS219
OPA2132	SBOS054
OPA2350	SBOS099
TPS2104	SLVS235
SN74CBT3257	SCDS017

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# EVM Overview

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The ADS8364 is a high-speed, low power, dual 16-bit A/D converter that operates from independent 5-V  $AV_{DD}$  and  $DV_{DD}$  supplies. The digital output is delivered through a built-in buffer circuit that can be powered from  $DV_{DD}$  or separate 2.7-V to 5.25-V ( $BV_{DD}$ ) sources. This allows for flexibility when designing within mixed voltage environments.

The six fully differential sample and hold circuits are divided into three pairs (A, B, and C). Each pair of channels has a hold signal (HOLDA, HOLDB, and HOLDC) which, when strobed together, allows simultaneous sampling on all six analog inputs. The part accepts an analog input voltage in the range of  $-V_{REF}$  to  $+V_{REF}$  centered on the internal 2.5-V reference. The part also accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry (see Figure 2-1).

Conversion time for the ADS8364 is 3.2  $\mu$ s when a 5-MHz external clock is used. The corresponding acquisition time is 0.8  $\mu$ s. To achieve the maximum output rate (250 KSPS), the read function can be performed during the start of the next conversion.

The ADS8364 EVM includes the following features:

- Full-featured evaluation board for the ADS8364 250-kHz, 16-bit, 6-channel simultaneous sampling analog-to-digital converter

- Analog inputs can be configured as single-ended or differential

- Direct connection to C5000 and C6000 DSK platforms through the 80-pin interface connectors

- Built-in reference

- High-speed parallel interface



# Analog Interface

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The analog portion of the board is divided in two parts. The input buffer represents the front-end circuit of the A/D converter. Its function is to provide level and impedance changes to the input signal. The second part is the voltage reference circuit. In addition to being the conversion reference, the ADS8364's reference output is used for level shifting the analog input.

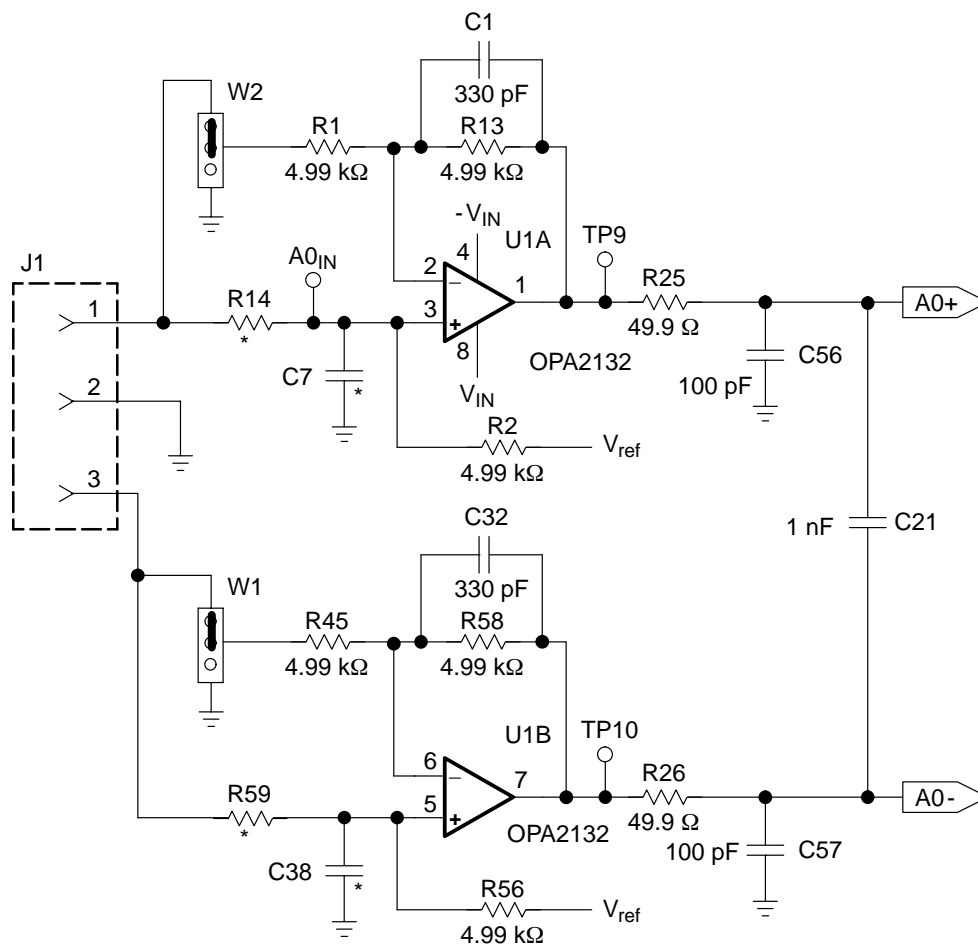
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## 2.1 Dual Supply—Input Buffer

The analog input to the ADS8364EVM board is comprised of six independent OPA2132 operational amplifiers. The OPA2132s are powered from the  $\pm 12\text{-V}$  analog supply and connected as inverting amplifiers with a gain of 1. The internal  $2.5\text{-V}$  reference voltage is applied to the noninverting input of the OPA2132s for level shifting.

Even though the ADS8364EVM board is configured at the factory for  $\pm 12\text{-V}$  analog operation, the EVM can tolerate maximum power supplies of  $\pm 15\text{ VDC}$ . However, care must be taken to ensure the  $\pm 15\text{ VDC}$  limit is not exceeded or potential damage to the op-amp circuits can occur.

Figure 2 - 1. ADS8364EVM Schematic—Analog Input Section



**Note:** Components marked with an asterisk (\*) are NOT INSTALLED.

This configuration allows single-ended signals of  $\pm 2.5\text{ V}$  ( $5\text{ V}_{pp}$ ) to be applied to either input of channels A, B, or C (JX pin 1 or 3 referenced to pin 2). Differential signal inputs of  $\pm 1.25\text{ V}$  ( $2.5\text{ V}_{pp}$ ) can be applied to the channel input pairs (JX pin 1 and 3).

## 2.2 Bipolar Inputs

Table 2-1 lists various combinations of resistors, capacitors and jumpers. By changing components and setting the appropriate jumper, it is possible to adapt the input buffer to accept bipolar input voltages. Table 2-1 is related to the schematic presented in Table 2-1 and represents channel A0 of the ADC. Channels B0, C0, A1, B1, and C1 follow a similar placement pattern. Refer to the schematic at the end of this document for reference description details.

The capacitors C7, C38 and C1, C32 are used only in differential signal configurations. For single-ended signals, the second operational amplifier can be used to buffer the reference voltage to the input of A/D converter.

Table 2-1. Typical Analog Input Buffer Circuit Values (A0 Shown)

Refer to Figure 2-1	Input Voltage	R14 R59	R1 R45	R2 R56	R13 R58	C7 C38	C1 C32	W2 W1
	0-5	5 k $\Omega$	open	open	short	330 pF	open	open
	0-2.5	5 k $\Omega$	5 k $\Omega$	open	5 k $\Omega$	open	330 pF	1-2
	-2.5 -2.5	20 k $\Omega$	4 k $\Omega$	20 k $\Omega$	4 k $\Omega$	open	330 pF	1-2
	-5-5	20 k $\Omega$	4 k $\Omega$	10 k $\Omega$	2 k $\Omega$	open	330 pF	1-2
	-10-10	20 k $\Omega$	4 k $\Omega$	5 k $\Omega$	1 k $\Omega$	open	330 pF	1-2
	-5-0	open	5 k $\Omega$	open	5 k $\Omega$	short	330 pF	2-3
	0-5	open	5 k $\Omega$	open	5 k $\Omega$	short	330 pF	2-3

## 2.3 Analog and Digital 5-V Supplies

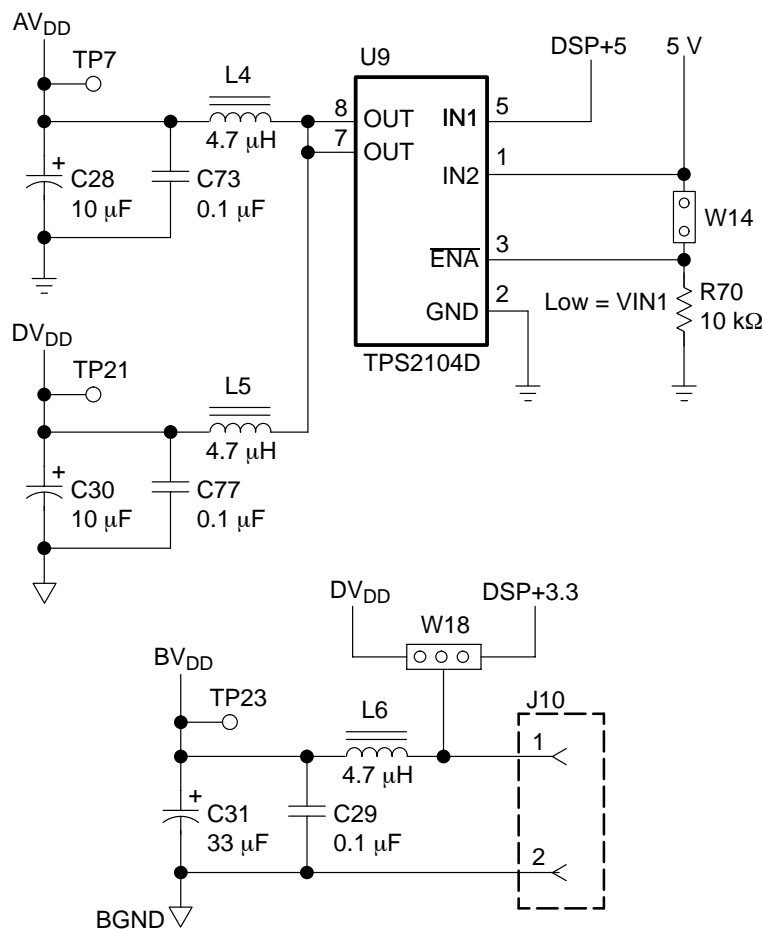
The ADS8364EVM board is configured at the factory for operation on the TMS320C6711 DSK platform. By default, W14 is open, which allows the DSP 5-V supply to be routed through U9 to the filter inductors L4 and L5. By closing W14, an external voltage source of 4.75 VDC to 5.25 VDC can be applied via J8.

## 2.4 Output Buffer 3.3-V Supply

As mentioned above, the ADS8364EVM board is configured at the factory for operation on the TMS320C6711 DSK platform. Since the interface to this DSP is 3.3 V, the buffer supply voltage is taken from the DSP 3.3-V source found on the interface connector at J11 (pins 41 and 42). The 3.3-V DSP supply is routed through the shunt jumper on W18 (pins 2-3). Placing the shunt on pins 1 and 2 supplies the 5-V digital source (via V9) to the buffer circuit.

The digital buffer circuit of the ADS8364 can also be powered from an external source via J10. When operated in this fashion, the shunt jumper at W18 should be completely removed in order to prevent possible damage to the EVM or DSK circuitry. The buffer voltage has a range of 2.7 VDC to 5.5 VDC maximum.

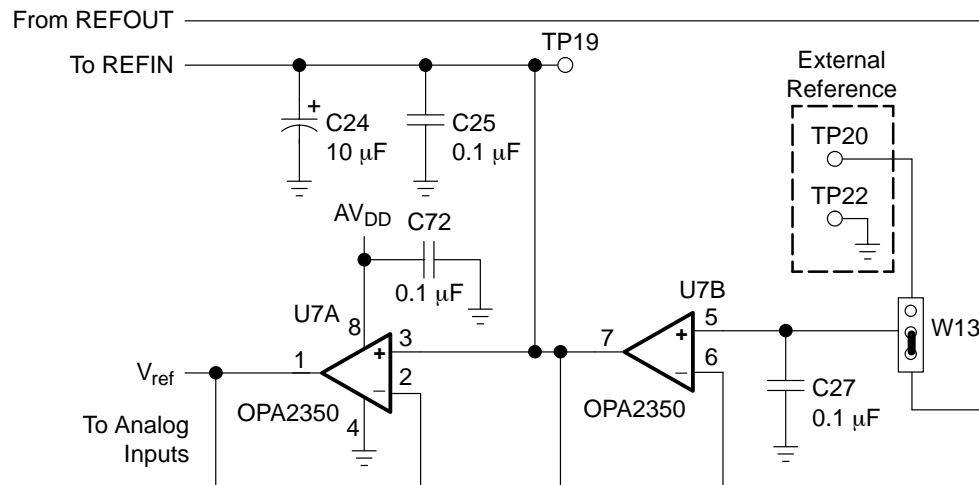
Figure 2-2. Digital Buffer Voltage Selection



## 2.5 Reference Voltage

The ADS8364 has an internal 2.5-V reference source, which is accessed by placing a shunt jumper on W13 pins 2 and 3 (factory default). If an external reference is desired, the shunt jumper on W13 must be moved to cover pins 1 and 2. The ADS8364EVM provides two test-points, TP20 and TP22, as a means to connect an external source. An external source should be applied to TP20, referenced to TP22. The voltage input range on this node is 1.5 VDC to 2.6 VDC. This voltage is buffered through the unity-gain noninverting buffer and fed to the REFIN pin as well as the analog input circuitry.

Figure 2-3. ADS8364EVM Reference Circuit







# Digital Interface

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The ADS8364 EVM is designed for easy interfacing with the C5000 and C6000 series DSK platforms from Texas Instruments. Two 80-pin interface connectors located on the bottom side of the EVM allow direct plug-in to the DSK platforms.

If an alternate control system is desired, mating connector part numbers SFM-140-01-S-D or SFM-140-02-S-D can be used to wire the control and data signals. Please consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for price and availability of these connectors.

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### 3.1 Control Signals

The ADS8364EVM was developed on the TMS320C6711 DSK platform. The HOLDx signals, ADD pin control, and reset are all derived from the GPIO function of McBSP port 1. These signals are located on J12. The address and data lines are available on J11. The EVM is factory configured to use address 0xA000 0020 as its base. Channel A0 can be accessed from this location, with channels A1 through C1 located at the base address + 0x04, as listed in Table 3-1.

An alternate address base can be selected by removing the shunt jumper on W17. This assigns A17 or 0xA002 0000 as the base address of the EVM. In this configuration, channels A1 through C1 are located at the base address + 0x4000.

Table 3-1. Address Map

	W17 CLOSED	W17 OPEN
A0	0xA000 0020	0xA002 0000
A1	0xA000 0024	0xA002 4000
B0	0xA000 0028	0xA002 8000
B1	0xA000 002C	0xA002 C000
C0	0xA000 0030	0xA003 0000
C1	0xA000 0034	0xA003 4000
Cycle	0xA000 0038	0xA003 8000
FIFO	0xA000 003C	0xA003 C000

### 3.2 Bus Width

The ADS8364 features a byte mode in which data can be read from the ADC in two consecutive 8-bit reads. W16 controls the byte feature, which is disabled by default. To enable byte mode, remove the jumper from W16. Please consult the data sheet for a complete description of byte mode operation.

### 3.3 External Clock

The BNC connector (J9) and W15 allow for the selection of an external conversion clock source. Factory default settings provide the clock source via the TOUT1 signal of the DSP by placing a shunt jumper on pins 1 and 2 of W15. By moving the shunt to pins 2 and 3, the EVM user can apply an external clock source of not more than 5 MHz to J9.

# Power Supply

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The power supply requirements for the ADS8364EVM board can be split into three categories— analog front end, ADC power, and digital interface. While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

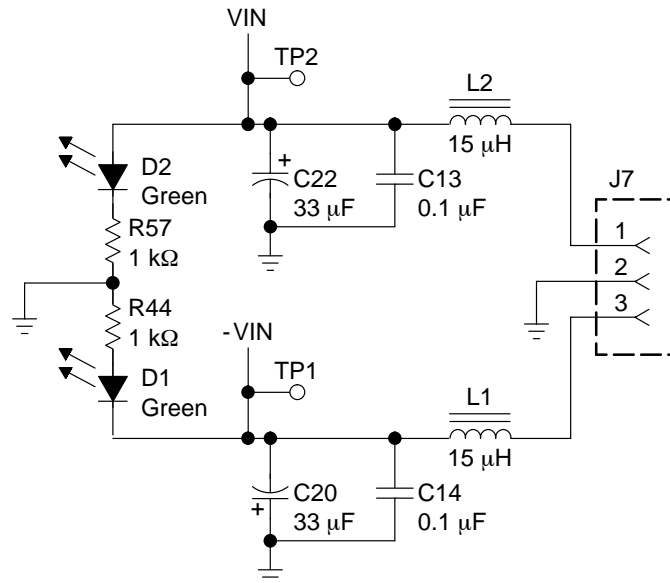
The power and ground planes on the inner layers of the EVM are split into digital and analog sections, with the ground planes tied together at a single point near the filter circuits.

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## 4.1 Analog Front-End Supply

The analog front end of the EVM includes six OPA2132 operational amplifiers. These amplifiers are powered through J7 and are configured for bipolar operation. The circuits are designed to operate from a maximum supply voltage of  $\pm 12$  VDC. Single supply operation can be achieved by applying a positive dc voltage to pin 1 of J7 (marked as +12 V on EVM) while applying a ground reference to both pins 2 and 3.

Figure 4-1. Analog Front-End Supply

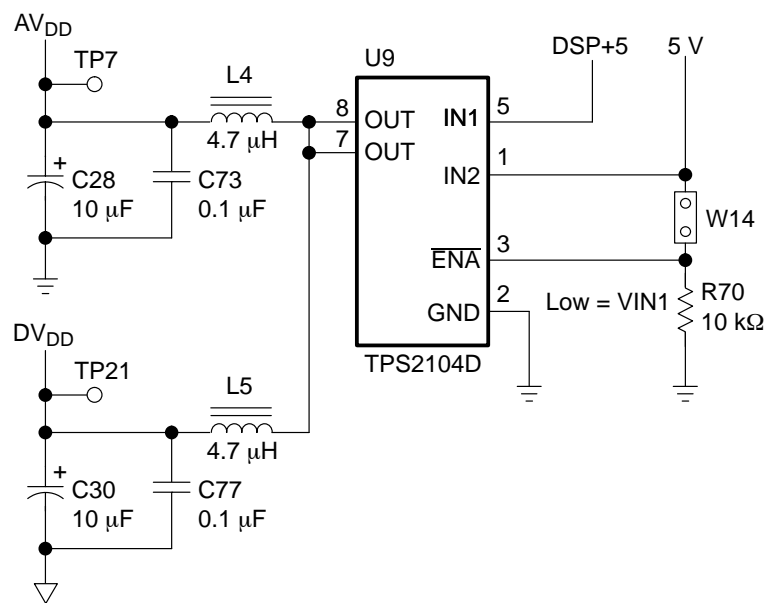


## 4.2 ADC Power Supply

The ADS8364 requires analog and digital supplies in the range of 4.75 VDC to 5.25 VDC. The EVM provides both analog and digital supply voltages through a single input supply source. The 5-V input supply is filtered and split into the digital and analog power planes located on the inner layer of the PCB.

W14 can be used to determine the source of the input supply. With W14 closed, the 5-V ADC power supply source is located at J8. The TPS2104 power switch at U9 directs the voltage from J8 to the analog/digital filters. With W14 open, the TPS2104 power switch directs 5-V power from the C5000/C6000 DSK board via J12, which is the factory default setting.

Figure 4-2. ADC Power-Supply Input



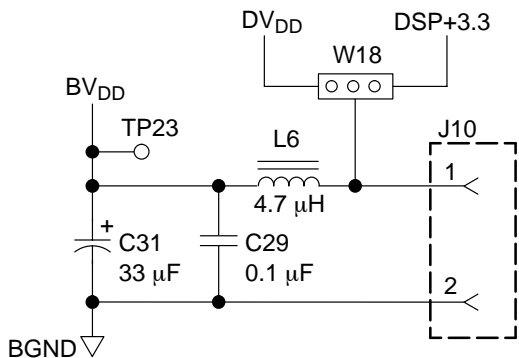
### 4.3 Digital Interface Supply

A unique feature of the ADS8364 is the built-in data buffer circuit with an independent power source. The EVM provides a jumper—W18, which allows for flexible voltage selection. When the shunt at W18 is in the factory default position (W18 pins 2 and 3 shorted), the 3.3-V DSP supply taken from J11 is applied to the  $BV_{DD}$  pins of the ADS8364. By moving the shunt jumper on W18 to pins 1 and 2, the user chooses the 5-V ADC supply as the source of the  $BV_{DD}$  voltage.

J10 provides a means of supplying an alternative independent buffer voltage. If desired, the shunt jumper at W18 can be totally removed, and a dc source of 2.7 V to 5.25 V can be applied to J10 as a means to provide  $BV_{DD}$  power.

**Caution**  
**While J10 is used, ensure that W18 remains completely open.**

Figure 4-3. Digital Buffer Alternate Supply Input



## Initial Setup of the Board

Factory set up of the board is for a  $\pm 5\text{-V}$  to  $\pm 12\text{-V}$  analog front-end supply at J7, and 5-V ADC power provided through J8. The  $BV_{DD}$  supply is provided from the DSK platform via J11 and W18 (pins 2 and 3 shorted). The maximum analog inputs are 0-V/5-V for a differential signal. The reference circuit is connected to the internal reference of the ADC (W13 pins 2 and 3 shorted).

*Table 5-1. Factory Defaults—Analog Input Buffers (A0 Shown)*

Refer to Figure 2-1 and Schematic	Input	R14	R1	R2	R13	C7	C1	W2
	Voltage	R59	R45	R56	R58	C38	C32	W1
	0-5	open	4.99 k $\Omega$	4.99 k $\Omega$	4.99 k $\Omega$	N/I	330 pF	1-2

The analog inputs to the ADS8364EVM board can be applied to any one or all of the input channels. Single-ended inputs are to be applied between analog ground (center terminal of J1–J6) and either the positive or negative terminals. Differential signals are to be applied between the positive and negative terminals.





## **EVM Schematic**

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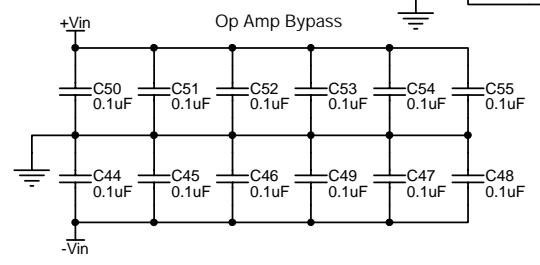
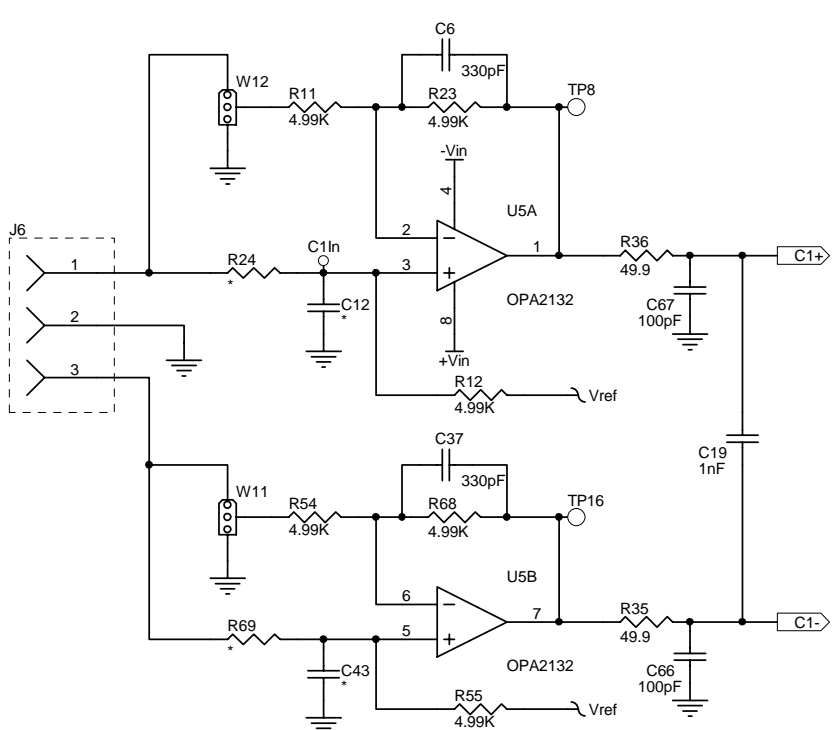
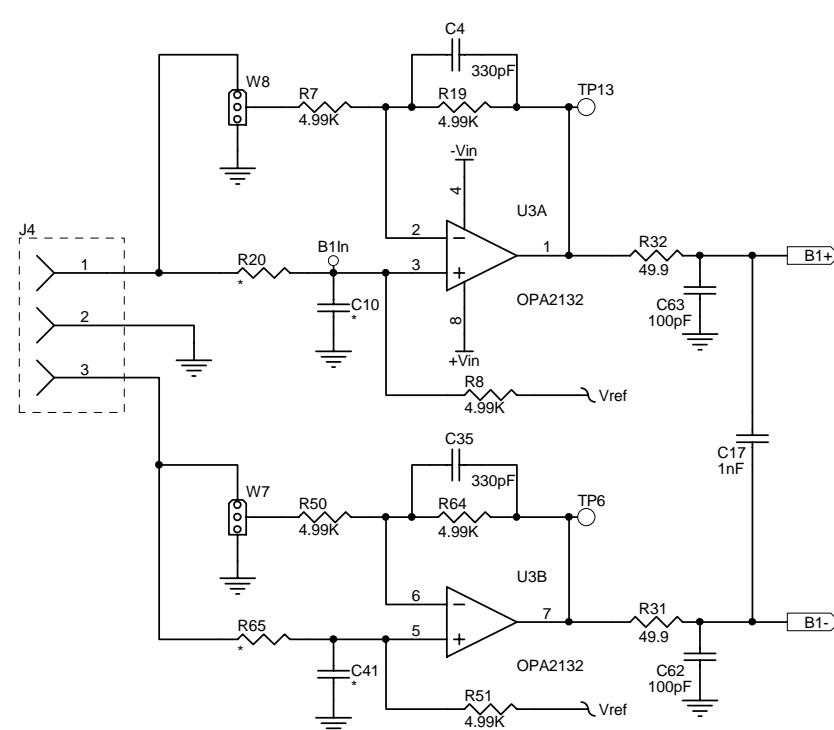
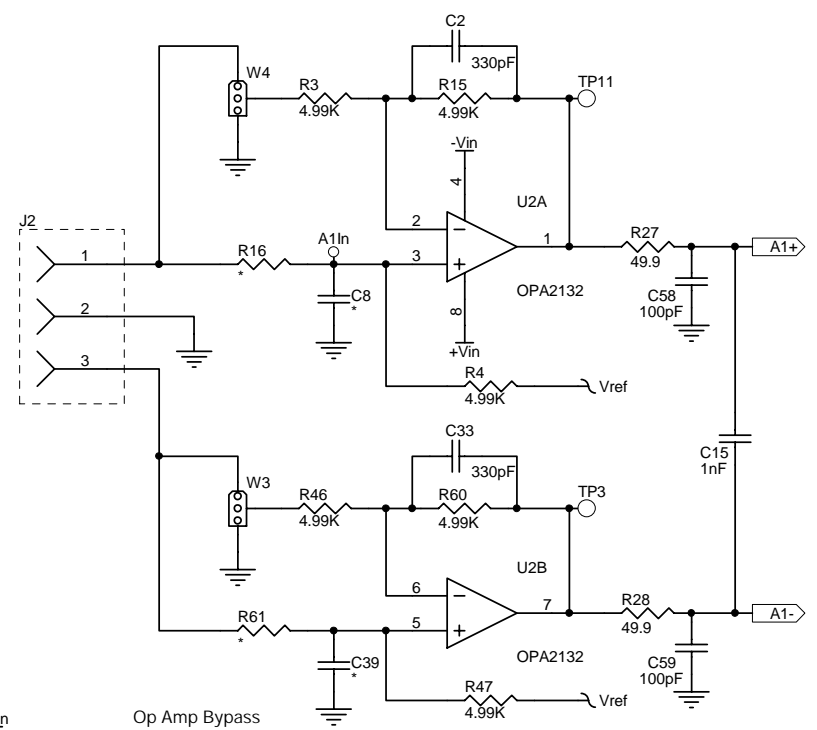
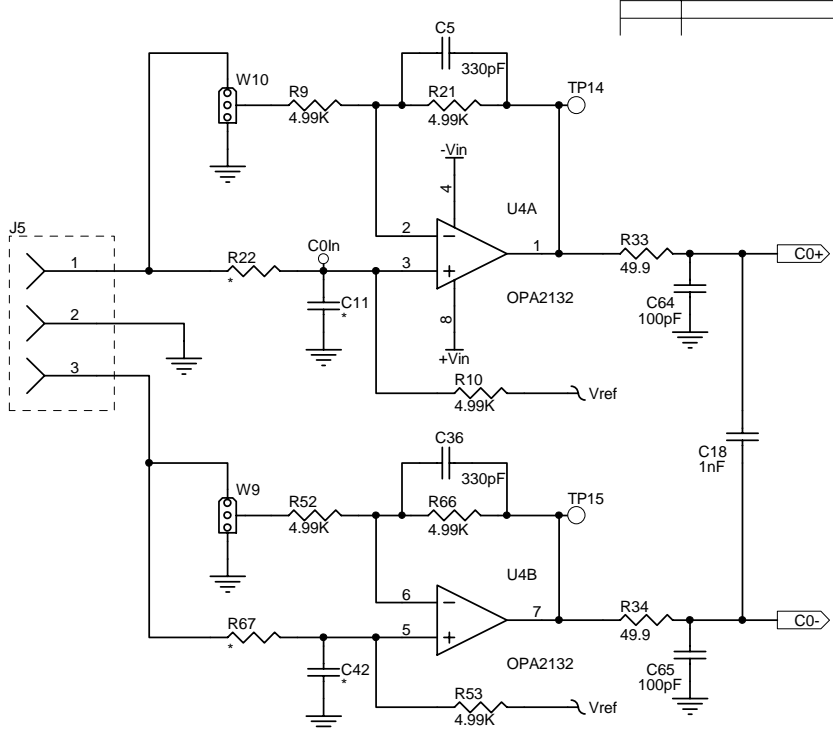
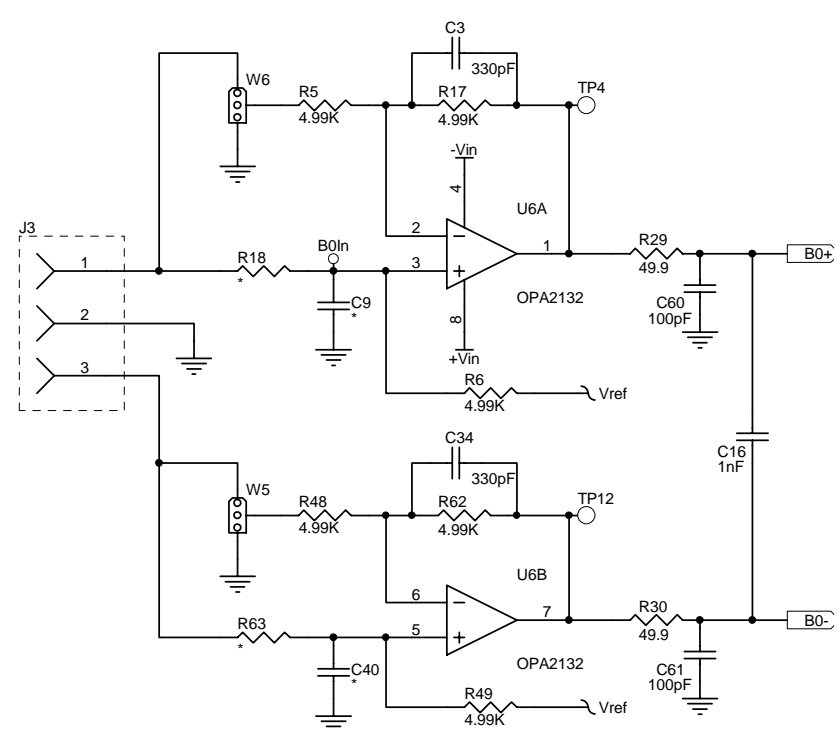
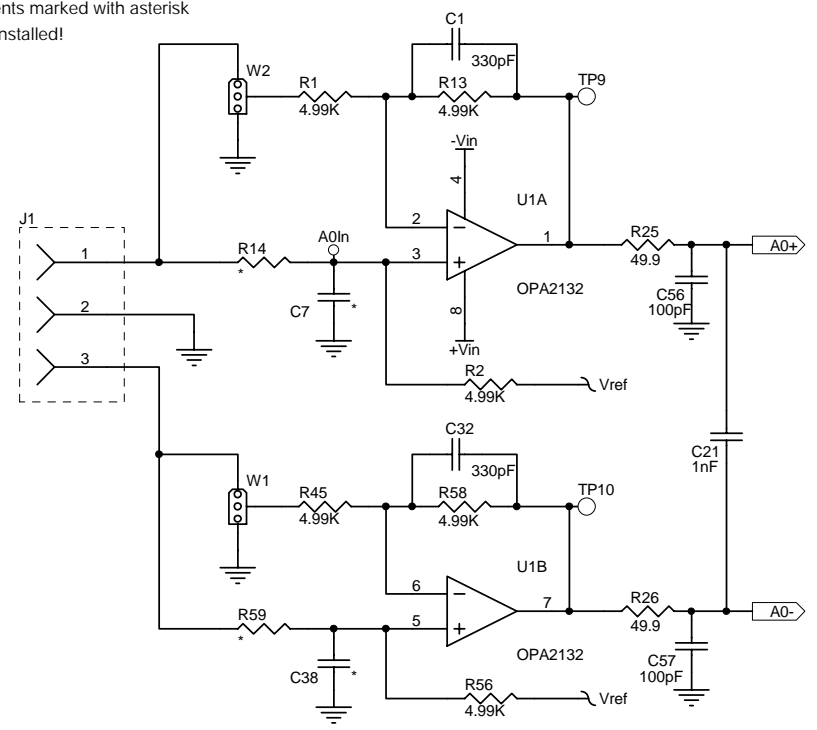
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The following pages contain the ADS8364EVM circuit diagram.

Revision History		
REV	ECN Number	Approved

Note:  
Components marked with asterisk are NOT installed!

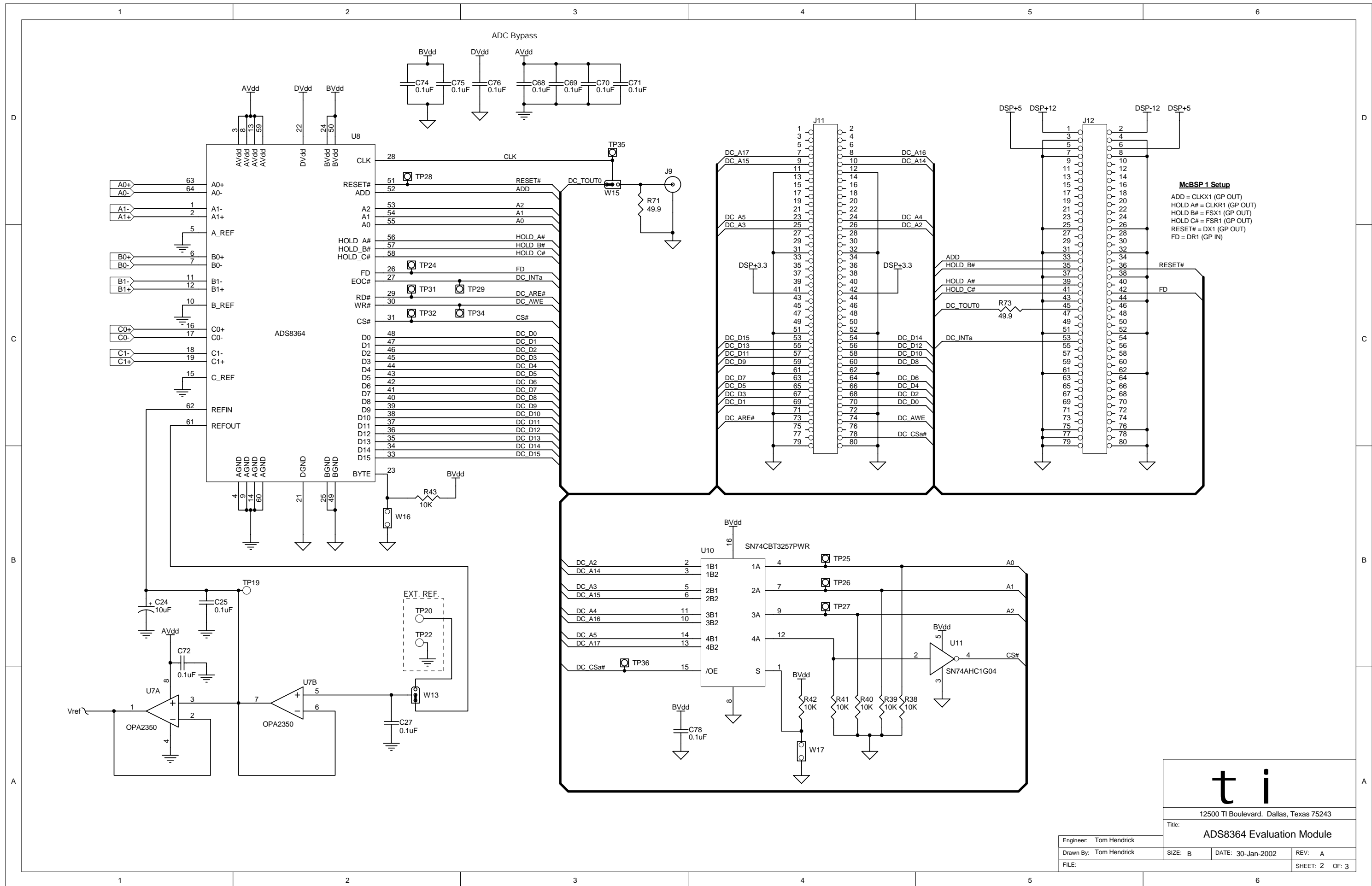


**ti**

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Title: **ADS8364 Evaluation Module**

Engineer: Tom Hendrick	SIZE: B	DATE: 30-Jan-2002	REV: A
Drawn By: Tom Hendrick	FILE: ADS8364_A_SH1.Sch		SHEET: 1 OF 3

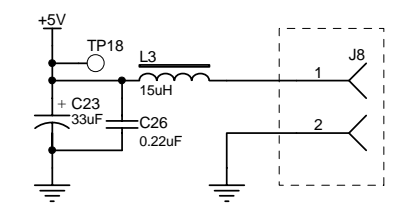
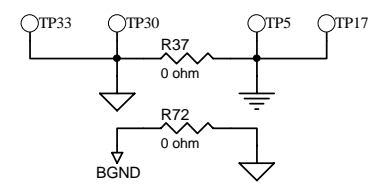
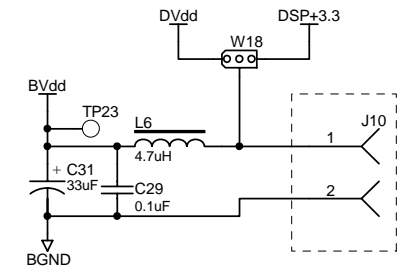
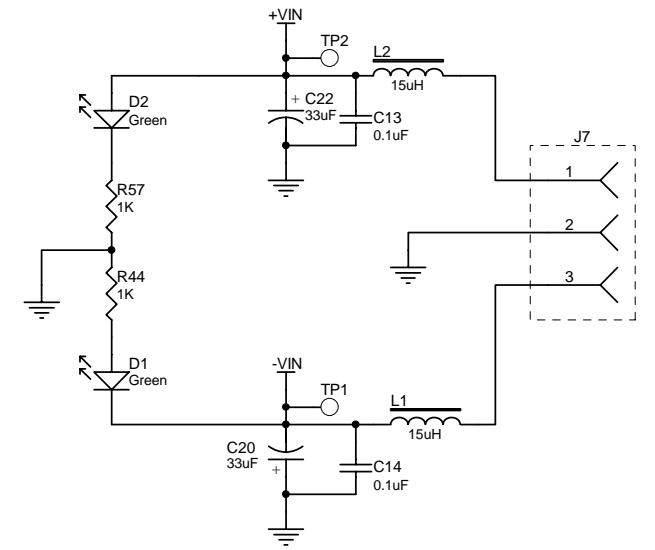
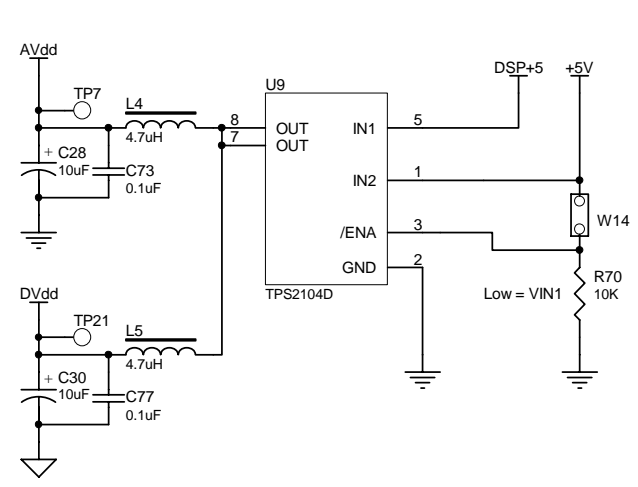


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Title: ADS8364 Evaluation Module

Engineer: Tom Hendrick	SIZE: B	DATE: 30-Jan-2002	REV: A
Drawn By: Tom Hendrick	FILE:		SHEET: 2 OF 3



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