PCM3060EVM

This user's guide contains a description of the PCM3060EVM evaluation module. Included are the schematic, the bill of materials, and the printed-circuit board layout.

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1 Description

The DEM-DAI3060 is an evaluation board for the PCM3060, a 96-kHz/192-kHz, 24-bits PCM audio CODEC, with digital audio interface receiver and transmitter, optical and coaxial interface, onboard multiple clock generator, –3-dB differential or +3-dB single-ended input amplifier with LPF for DAC and –6-dB single-ended input amplifier with LPF for ADC, I^2C or SPI mode controller which can be controlled by PC via USB, and switches or jumpers for various mode or clock configuration.

The DEM-DAI3060 operates under +5-V and ±15-V analog power supplies with 2-Vrms unbalanced analog signal output and 1-Vrms or 2-Vrms unbalanced analog signal input.

PCM3060 control application software, attached to DEM-DAI3060, is used for controlling PCM3060 through serial control port.

1.1 Block Diagram

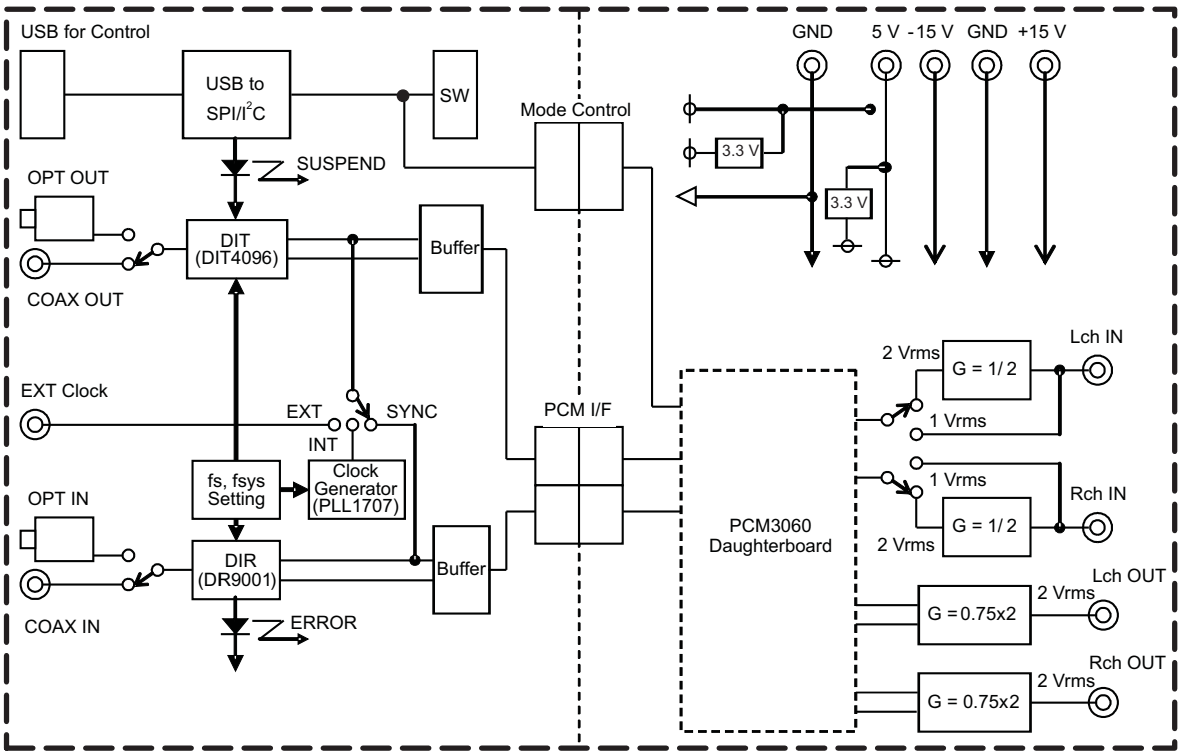


Figure 1. DEM-DAI3060 Block Diagram

1.2 Connection, Configuration, and Operation

1.2.1 Basic Connections and Configurations

- Save application software and document files (PCM3060 data sheet, DEM-DAI3060 user's guide, PCM3060 control application software, and TUSB3410 driver), which are attached to the EVM in the CD-ROM, into the appropriate folder of the PC which is used to control this EVM, and install the TUSB3410 driver according to the installation instructions.
- Connect the +5-V and ±15-V power supplies to +Vcc, ±AVcc, and GND on CN001-CN005 (007). The ±15-V power supplies are required for 2-Vrms input and output.
- Connect the S/PDIF input to CN102 (coaxial) or U102 (optical) and output to CN101 (coaxial) or U101 (optical), and analog input/output to appropriate equipment.

- Connect the USB cable to the USB connecter of the EVM for mode control.
- Select the system clock 1 configuration, synchronous with system clock 2 generated by DIR9001, asynchronous clock source from 256/512 fs or 384 fs generated by the onboard clock generator (PLL1707), or external clock input connector (CN103) using JP101, and verify the presence of system clock 1 on TP101.
- Set the system clock rate (256, 384, 512 fs), interface mode (master or slave) and format (LJ-24 or I^2S-24) for ADC interface using SW105 CLK1/0, M/S, FMT for board and PCM3060 control application software for PCM3060.
- Set the system clock rate (128, 256, 384, 512 fs) and the interface format (LJ-24, I^2S-24, etc.) for DAC interface using SW106 PSCK1/0 and FMT1/0 for board and PCM3060 control application software for PCM3060. The DAC interface is always EVM: master and PCM3060: slave for S/PDIF input signal.
- Set the sampling frequency (16 to 96 kHz) and system clock frequency using SW107, SR, FS2/1 for asynchronous mode internal clock 1 source.
- Set the channel status for DIT4096, if required. (It is not required for PCM3060 evaluation.)

1.2.2 Configuration Controls

1.2.2.1 S/PDIF Output Connector Selection

The S/PDIF output from the transmitter is selectable as Table 1 shows.

Table 1. S/PDIF Output From Transmitter

SW101	Description
OPT	Transmit S/PDIF output via optical connector
COAX	Transmit S/PDIF output via coaxial connector

1.2.2.2 S/PDIF Input Connector Selection

The S/PDIF input to receiver is selectable as Table 2 shows.

Table 2. S/PDIF Input to Receiver

SW102	Description
OPT	Receive S/PDIF input via optical connector
COAX	Receive S/PDIF input via coaxial connector

1.2.2.3 System Clock 1 Source Selection

The system clock 1 (master clock 1) source for the EVM including PCM3060, which is associated with sampling frequency 1, is selectable by the JP101 setting as Table 3 shows.

The system clock 2 source is always the recovered system clock from S/PDIF input signal by DIR, DIR9001.

Table 3. JP101 Settings

JP101	Description
DIR	Internal, synchronous with system clock 2, DIR9001 generated (Default)
256	Internal, asynchronous, 256/512 times of sampling frequency
384	Internal, asynchronous, 384 times of sampling frequency
EXT	External, asynchronous, TTL interface level, 75-Ω terminated, up to 50 MHz

1.2.2.4 Master/Slave Interface Mode and System Clock Rate Selection for ADC Interface

The audio interface mode and system clock rate of the PCM3060 and the EVM for ADC interface is selectable as Table 4 shows.

In slave mode, the audio interface clock, BCK1, and LRCK1 are generated in DIT4096 and supplied to PCM3060 through the buffer. In master mode, they are generated in PCM3060 and supplied to DIT4096.

Mode control to PCM3060 can be performed by PCM3060 control application software through serial control port.

Table 4. Master/Slave Interface Mode and System Clock Rate Selection for ADC Interface

SW105(1)			PCM3060 Reg 72 (&h48) Bit6-4(1)			Description
M/S	CLK1	CLK0	MS12	MS11	MS10	
OFF	OFF	OFF	0	0	0	Slave, 512 fs (Default)
OFF	OFF	ON				Slave, 384 fs
OFF	ON	OFF				Slave, 256 fs
ON	OFF	OFF	0	1	0	Master, 512 fs
ON	OFF	ON	0	1	1	Master, 384 fs
ON	ON	OFF	1	0	0	Master, 256 fs

(1) Other inconsistent combinations between SW105 M/S, CLK1/0, and PCM3060 Reg 72 MS12/11/10 selections are unavailable.

1.2.2.5 Master/Slave Interface Mode and System Clock Rate Selection for DAC Interface

The audio interface mode for the DAC interface is always DIR9001: master, PCM3060: slave for S/PDIF input signal.

The system clock rate is selectable as Table 5 shows, using SW106, PSCK1/0.

Table 5. System Clock Rate Selection for DAC Interface

SW106(1)		PCM3060 Reg 67 (&h43) Bit6-4(1)			Description
PSCK1	PSCK0	MS22	MS21	MS20	
OFF	OFF	0	0	0	Slave, 128 fs
OFF	ON				Slave, 256 fs
ON	OFF				Slave, 384 fs
ON	ON				Slave, 512 fs (Default)

(1) Other inconsistent combinations between SW106 PSCK1/0 and PCM3060 Reg 67 MS22/21/20 selections are unavailable.

1.2.2.6 Interface Format Selection for ADC Interface

The audio interface format of the PCM3060 and the EVM for the ADC interface is selectable as Table 6 shows.

Table 6. Interface Format Selection for ADC Interface

SW104(1)	SW105(1)	PCM3060 Reg 72 (&h48) Bit1-0(1)		Description
FMT1	FMT0	FMT11	FMT10	
OFF	OFF	1	1	Right-justified 16 bits
OFF	ON	1	0	Right-justified 24 bits
ON	OFF	0	0	I^2S 24 bits (Default)
ON	ON	0	1	Left-justified 24 bits

(1) Other inconsistent combinations between SW104 FMT1, SW105 FMT0 and PCM3060 Reg 72 FMT11/10 selections are unavailable.

1.2.2.7 Interface Format Selection for DAC Interface

The audio interface format of the PCM3060 and the EVM for the DAC interface is selectable as Table 7 shows.

Table 7. Interface Format Selection for DAC Interface

SW106[1]		PCM3060 Reg 67 (&h43) Bit1-0[1]		Description
FMT1	FMT0	FMT21	FMT20	
OFF	OFF	1	1	Right-justified 16 bits
OFF	ON	1	0	Right-justified 24 bits
ON	OFF	0	1	Left-justified 24 bits
ON	ON	0	0	I^2S 24 bits (Default)

(1) Other inconsistent combinations between SW106 FMT1/0 and PCM3060 Reg 67 FMT21/20 selections are unavailable.

1.2.2.8 Sampling Frequency 1 and System Clock Frequency 1 Selection

For asynchronous mode, the sampling frequency 1 and the system clock frequency 1 for the ADC interface of PCM3060 and EVM is selectable by the SW107 setting, as Table 8 shows.

A 16- to 96-kHz sampling frequency and an 8.192- to 36.864-MHz system clock frequency are available on the EVM, and the possible combinations of them are shown in Table 8. The system clock rate, 256 fs, 384 fs, or 512 fs setting must be made between the EVM setting and the PCM3060 setting.

Table 8. Sampling Frequency 1 and System Clock Frequency 1 Selection

SW107[1]			Frequencies
SR	FS2	FS1	Sampling Clock (kHz)/System Clock (MHz)
256fs Operation			
OFF/Low	ON/High	OFF/Low	32/8.192
OFF/Low	OFF/Low	ON/High	44.1/11.2896
OFF/Low	OFF/Low	OFF/Low	48/12.288
ON/High	ON/High	OFF/Low	64/16.384
ON/High	OFF/Low	ON/High	88.2/22.5792
ON/High	OFF/Low	OFF/Low	96/24.576
384fs Operation			
OFF/Low	ON/High	OFF/Low	32/12.288
OFF/Low	OFF/Low	ON/High	44.1/16.9344
OFF/Low	OFF/Low	OFF/Low	48/18.432
ON/High	ON/High	OFF/Low	64/24.576
ON/High	OFF/Low	ON/High	88.2/33.8688[2]
ON/High	OFF/Low	OFF/Low	96/36.864[2]
512fs Operation			
OFF/Low	ON/High	OFF/Low	16/8.192[3]
OFF/Low	OFF/Low	ON/High	22.05/11.2896
OFF/Low	OFF/Low	OFF/Low	24/12.288
ON/High	ON/High	OFF/Low	32/16.384
ON/High	OFF/Low	ON/High	44.1/22.5792
ON/High	OFF/Low	OFF/Low	48/24.576 (Default)

(1) Select the clock output frequency of PLL1707 SCKOx; the combination of FS2 = ON/High and FS1 = ON/High is reserved.
(2) Not applicable through the S/PDIF interface due to limitation of the DIT4096. They are applicable for PCM direct interface between PCM3060 and externals.
(3) Might not be applicable through the S/PDIF interface due to a limitation of interface receiver of audio equipments. It is applicable for PCM direct interface between PCM3060 and externals.

1.2.2.9 Reset Control and EVM Power, DIR Clock Source Setting

The DEM-DAI3060 supports a Reset Control for the EVM by SW103 and for the PCM3060 by SW108. Also, the following settings are used for the present EVM firmware and application software.

JP001 : Must be fixed as always ON for power supply to EVM circuit
JP102 : Must be fixed on AUTO position for clock source selection of DIR9001

1.2.2.10 S/PDIF Transmitter Format (Channel Status) Setting for DIT4096

The extended configurations of the digital audio interface transmitter, DIT4096, and the channel status of S/PDIF can be set using the DIP switch, SW104. The individual switch settings and their functions are described in Table 9. For general evaluation or test of function and performance of the PCM3060, a change from the default setting of this SW104 is unnecessary. This is provided for evaluation of the DIT4096 function, mainly related to channel status information.

Table 9. S/PDIF Transmitter Format (Channel Status) Setting for DIT4096

SW104	On/Off	Description
CSS	Off (High)	Channel status data bits are set in serial fashion at the COPY/C input with clock input at the SYNC input.
	On (Low)	COPY/C, L, $\overline{\text{AUDIO}}$, and $\overline{\text{EMPH}}$ inputs are used to set associated channel status data bits. (default)
COPY/C (1)	Off (High)	Copy and Generation Status information with L input for CSS = Low, Channel Status Data Bit = 1 for CSS = High
	On (Low)	Copy and Generation Status information with L input for CSS = Low, Channel Status Data Bit = 0 for CSS = High (default)
U	Off (High)	User data input = 1
	On (Low)	User data input = 0 (default)
V	Off (High)	Validity data input = 1
	On (Low)	Validity data input = 0 (default)
L (1)	Off (High)	Copy and Generation status with COPY/C for CSS = Low
	On (Low)	Copy and Generation status with COPY/C for CSS = Low (default)
$\overline{\text{AUDIO}}$	Off (High)	Audio data valid control input, Not linear PCM
	On (Low)	Audio data valid control input, Linear PCM (default)
$\overline{\text{EMPH}}$	Off (High)	Pre-emphasis status input. Not applied pre-emphasis (default)
	On (Low)	Pre-emphasis status input. Applied pre-emphasis
BLSM	Off (High)	BLS mode control input, BLS is an output (default)
	On (Low)	BLS mode control input, BLS is an input
BLS	Off (High)	Block start input for BLSM = Low, output for BLSM = High (default)
	On (Low)	Not block start

(1) Copy and Generation Status information for CSS = Low, definition is shown in following table.

COPY/C	L	Copy and Generation Status
On (Low)	On (Low)	Consumer mode, PRO = 0, COPY = 0, L = 0 (default)
On (Low)	Off (High)	Consumer mode, PRO = 0, COPY = 0, L = 1
Off (High)	On (Low)	Consumer mode, PRO = 0, COPY = 1, L = 0
Off (High)	Off (High)	Professional mode, PRO = 1, no copy protection

1.2.2.11 Serial/Parallel Mode Control Configuration Selection

The serial/parallel mode control configuration of the EVM is selectable as Table 10 shows, according to the SW301 setting for the PCM3060. SW001 must be always open for serial mode control, and JP002 and JP003 must be always open for parallel mode control.

Table 10. Serial/Parallel Mode Control Configuration

JP002			JP003			SW001				Description
MC	**MDO**	**MDI**	**MS**	**SCL**	**SDA**	**F4**	**F3**	**F2**	**F1**	
ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	I^2C (default)
ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	SPI
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON /OFF	H/W (ADC I/F mode selection)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON /OFF	OFF	H/W (I/F format selection)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON /OFF	OFF	OFF	H/W (de-emphasis control)

1.2.2.12 DAI Bridge and Control Bridge Selection

The DEM-DAI3060 supports flexible PCM audio interface through the DAI bridge, so that the PCM3060 can interface with external devices or equipment in place of DIR9001 and DIT4096 through an internal buffer. Interfacing with externals can be done by changing JP202 and JP203 connections for SCK1, BCK1, LRCK1, DOUT, SCK2, BCK2, LRCK2, DIN, and GND as shown in the following illustration. The DEM-DAI3060 also supports flexible mode and format control to PCM3060 by re-direction of the control port through header setting of control bridge, JP201. The default setting is the interface with the internal I^2C/SPI controller, which can be controlled by the PC through USB.

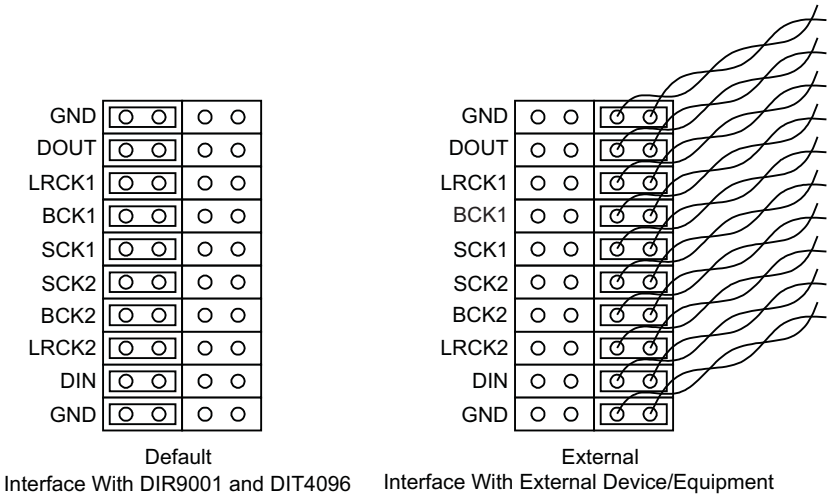


Figure 2. Flexible PCM Audio Interface

1.2.2.13 Analog Input Level/Path Selection

The DEM-DAI3060 supports a 1-Vrms input and a 2-Vrms input for full scale of the analog input signal by JP204, JP205 setting. For the 2-Vrms input selection, the onboard 100-kHz LPF and –6-dB attenuator are applied on the input signal. The default setting is 2-Vrms input.

DC position of JP204, 205 is applicable only for 2-Vrms input under the condition of Vcom position for JP206 setting, which controls the center level of the input buffer amplifier. The default setting of JP206 is GND position.

Table 11. Analog Input Level/Path Selection for ADC

JP204/205	Description
1 Vrms	1.06 Vrms full scale, analog input is fed to ADC directly
2 Vrms	2.08 Vrms full scale, analog input is fed to ADC through 100-kHz LPF and -6-dB attenuator (default).

1.2.2.14 Analog Output Single-Ended/Differential Selection

The DEM-DAI3060 supports 100-kHz LPF and buffer amplifier with single-ended and differential input configurations for DAC output. The output voltage of buffer amplifier is single-ended 2-Vrms for both input configurations.

Table 12. Analog Output Input Configuration (Single-Ended/Differential) Selection for DAC

JP207/210	JP208/211	JP209/212[(1)]	Description
DIFF	ON	OFF	Differential mode, 2.12 Vrms out (default)
S/E	OFF	ON	Single-ended mode, 2.08 Vrms out

(1) Other inconsistent combinations among JP207/210, JP208/211, JP209/212 settings are unavailable.

1.2.2.15 Control Port Mode Selection

The control port of the PCM3060 is selectable by SW301 on the daughterboard as Table 13 shows.

Table 13. PCM3060 Control Port Selection via SW301

SW301				
SPI	S/E	DIFF	I^2C	Description
OFF	OFF	OFF	ON	I^2C
OFF	OFF	ON	OFF	H/W (Differential DAC output)
OFF	ON	OFF	OFF	H/W (Single-ended DAC output)
ON	OFF	OFF	OFF	SPI

1.2.2.16 EVM Status Indicators

The SUSPEND LED indicates that the USB interface device, TUSB3410VF, is in suspend mode, which means that the host PC has entered into standby mode or is not powered on.

The ERROR LED indicates that the S/PDIF input data received by DIR9001 has one or some of the following errors, bi-phase, frame-length, preamble, or parity error.

1.2.3 Operation Guide for PCM3060 Control Application Software

The mode control, including the audio interface mode and format control for PCM3060, can be set through the serial control port by the PCM3060 control application software in I^{2}C or SPI control mode, or SW001 on the EVM in H/W control mode. This section describes the PCM3060 control application software for DEM-DAI3060. The details about each function in mode control registers and register definitions are described in the PCM3060 data sheet.

Figure 3. PCM3060 Control Panel Screen

The PCM3060 control application software supports serial mode control with I^{2}C or SPI protocol. This application software is not used for H/W control mode of the PCM3060. Run the application software after powering on the EVM. Otherwise, press the Reset button if the EVM is powered on after the application software is started. A blue indication on *Communication* at right-most bottom of window indicates that the serial mode control is available for a given environment. If a red indication does not change to blue, the EVM setting and PC environment must be checked.

1.2.3.1 Mode and Configuration Control

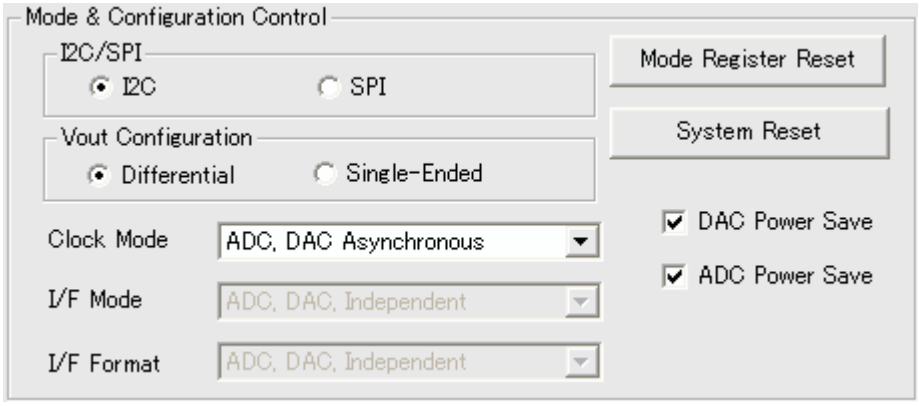


Figure 4. Mode and Configuration Control Panel

- I^2C/SPI selects the interface protocol for serial control according to the EVM and SW301 settings.
- Vout Configuration selects the input type of post DAC LPF and buffer amplifier according to the EVM setting. Inconsistent selection between EVM and PCM3060 setting causes performance degradation.
- Mode Register Reset initializes all registers of PCM3060 to default value.
- System Reset initializes the data path and starts clock re-synchronization of PCM3060; the content of the mode registers are kept.
- DAC Power Save enables/disables DAC operation; need to disable power save for normal operation
- ADC Power Save enables/disables ADC operation; need to disable power save for normal operation.
- Clock Mode selects the system clock and audio interface configuration according to the EVM setting. *Synchronous with clock 1* is not available for S/PDIF input application.
- I/F Mode selects the interface mode for common system clock and audio interface, if synchronous mode is selected for clock mode.
- I/F Format selects the interface format for common system clock and audio interface, if synchronous mode is selected for clock mode.

1.2.3.2 ADC Control Panel

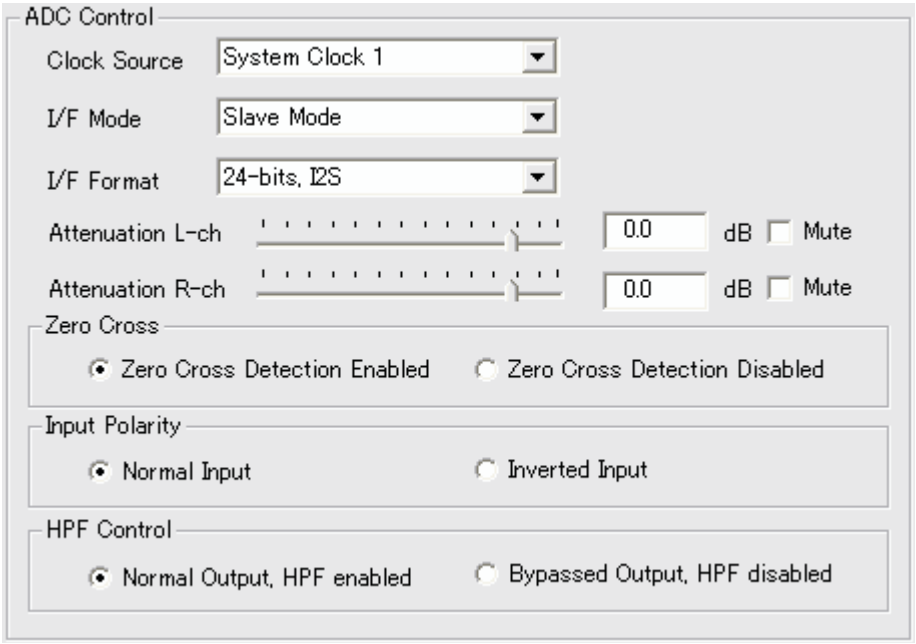


Figure 5. ADC Control Panel

- Clock Source selects the system clock source for ADC operation, system clock 1 or system clock 2.
- I/F Mode selects the interface mode for ADC operation from five possible modes.
- I/F Format selects the interface format for ADC operation from four possible formats. Right-justified formats are not available due to EVM limitation.
- Attenuation Lch/Rch controls the gain/attenuation level of the ADC digital attenuator from +20 to –107.5 dB.
- Mute Lch/Rch controls the software mute function enable/disable using digital attenuator.
- Zero Cross selects enabling/disabling of zero cross detection for the input signal for the digital attenuator control.
- Input Polarity controls the polarity of the analog input to digital output.
- HPF Control controls the HPF enable/disable for digital output

1.2.3.3 DAC Control Panel

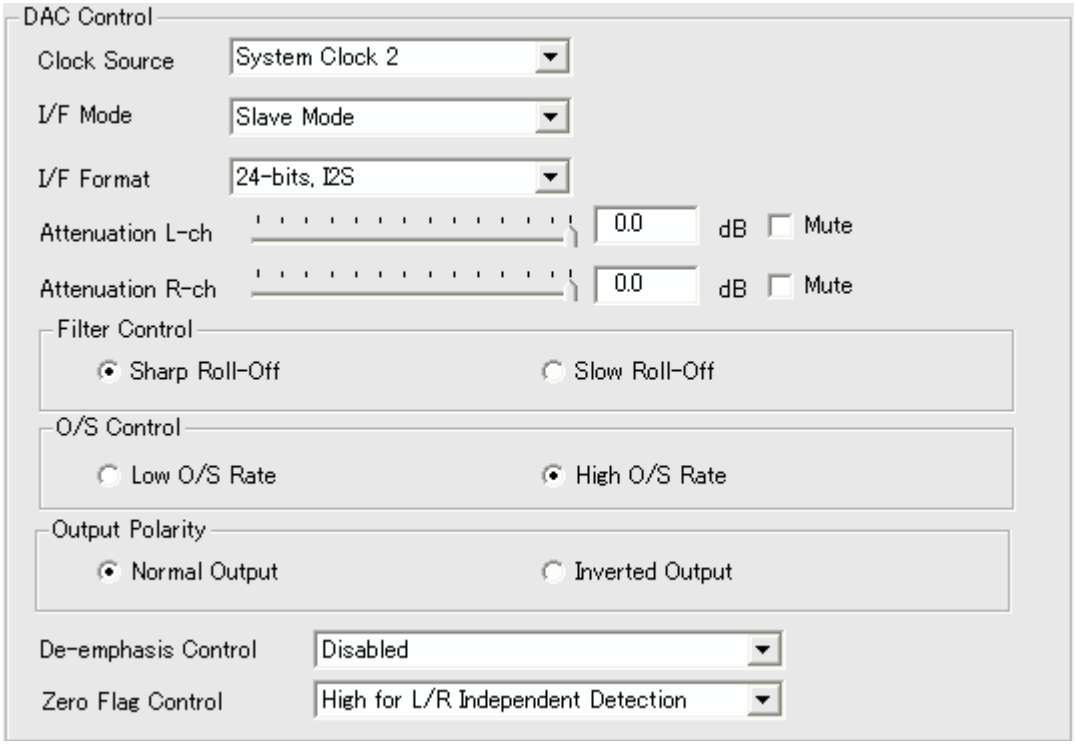
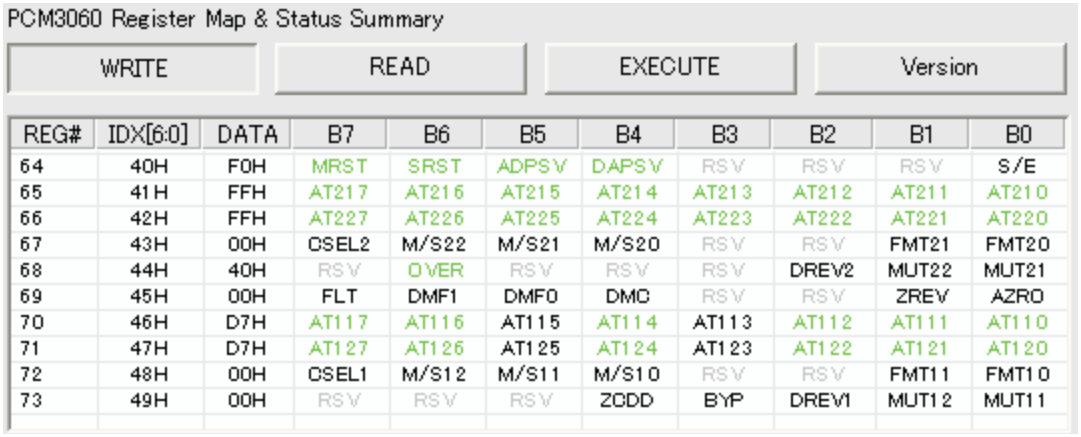


Figure 6. DAC Control Panel

- Clock Source selects the system clock source for DAC operation, system clock 2, or system clock 1. System clock 1 cannot be selected for S/PDIF input configuration.
- I/F Mode selects the interface mode for DAC operation from seven possible modes.
- I/F Format selects the interface format for DAC operation from four possible formats.
- Attenuation Lch/Rch controls attenuation level of DAC digital attenuator from 0 to -127.5 dB.
- Mute Lch/Rch controls the software mute function enable/disable using digital attenuator.
- Filter Control selects the characteristic of digital filter, sharp roll-off or slow roll-off.
- O/S Control selects the oversampling rate of DAC sigma-delta modulator.
- Output Polarity controls the polarity of analog output to digital input.
- De-emphasis Control selects filter characteristic and controls de-emphasis digital filter operation.
- Zero Flag Control selects zero detection mode and zero flag output logic.

1.2.3.4 Register Map and Status Summary



REG#	IDX[6:0]	DATA	B7	B6	B5	B4	B3	B2	B1	B0
64	40H	F0H	MRST	SRST	ADPSV	DAPSV	RSV	RSV	RSV	S/E
65	41H	FFH	AT217	AT216	AT215	AT214	AT213	AT212	AT211	AT210
66	42H	FFH	AT227	AT226	AT225	AT224	AT223	AT222	AT221	AT220
67	43H	00H	CSEL2	M/S22	M/S21	M/S20	RSV	RSV	FMT21	FMT20
68	44H	40H	RSV	OVER	RSV	RSV	RSV	DREV2	MUT22	MUT21
69	45H	00H	FLT	DMF1	DMF0	DMC	RSV	RSV	ZREV	AZRO
70	46H	D7H	AT117	AT116	AT115	AT114	AT113	AT112	AT111	AT110
71	47H	D7H	AT127	AT126	AT125	AT124	AT123	AT122	AT121	AT120
72	48H	00H	CSEL1	M/S12	M/S11	M/S10	RSV	RSV	FMT11	FMT10
73	49H	00H	RSV	RSV	RSV	ZCDD	BYP	DREV1	MUT12	MUT11

Figure 7. Register Map and Status Summary

A green display indicates logic 1. A black display indicates logic 0, and a gray, *RSV* display indicates no definition or is reserved for a non-application purpose.

WRITE indicates that all register data that is displayed on the Register Map is sent to the PCM3060 by pressing the EXECUTE button.

READ indicates that all register data is read from the PCM3060 by pressing the EXECUTE button, and it is reflected on the Register Map and each control panel.

EXECUTE starts write or read operation according to WRITE or READ status.

Version indicates the version information of this application software.

1.2.3.5 Register Direct Access

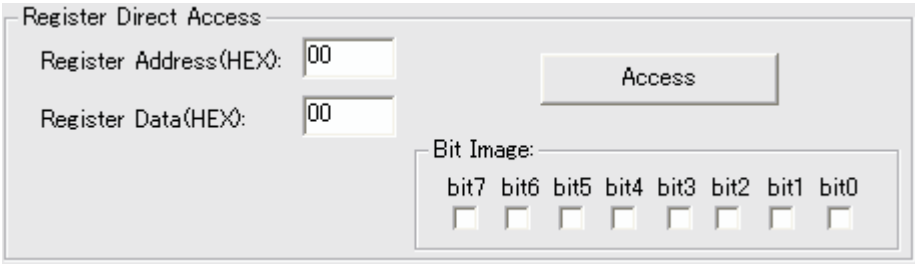


Figure 8. Register Direct Access

Register Address is the data window with a hexadecimal expression for the register address.

Register Data is the data window with hexadecimal expression for the register data. Bit image is the register data expressed in binary.

Access sends the register address and data which are displayed.

1.2.3.6 Load and Save for Register Control

Figure 9. Load and Save for Direct Access

SAVE stores the present register data displayed on the Register Map into the file, *register*.

LOAD reads the last register data from file, *register*, and reflects it on the Register Map and each panel.

1.2.3.7 COM Port Search and Interface Reset

Figure 10. COM Port Search and Interface Reset

This application software automatically searches for an available COM port for connecting application software with a USB port. When application software is opened, a blue color indicates that the COM port is available, and a red color indicates that the COM port is unavailable for a given environment.

Reset performs another available COM port search and initialization of application software, EVM hardware, and PCM3060.

1.2.4 Example of System Clock and Audio Interface Control

The PCM3060 can run in the following three system clock and audio interface configurations.

1.2.4.1 Synchronous With Clock 1 or Clock 2

In this mode, ADC and DAC run with a common system clock and a common audio interface, which is either clock 1 and clock 2. PCM3060 control application software supports both synchronous with clock 1 and synchronous with clock 2, but it is restricted only in synchronous with clock 2 for ADC on S/PDIF input and output configuration of EVM.

- EVM Board Setting
  - JP101 : select DIR
  - SW105 : M/S; ON
  - SW104–SW106 : SW104 FMT1, SW105 CLK1/0, FMT0 setting must be met with SW106 PSCK1/0, FMT1/0 setting
  - SW107 : CIF; ON
- PCM3060 control application software
  - Select synchronous with clock 2 in configuration panel, and select common I/F mode (slave) and common format in configuration panel, which must be met with EVM setting.

1.2.4.2 Synchronous With Different Audio Interface (Default)

In this mode, ADC and DAC can run with a common system clock, which is supplied on both system clock pins, and different interface mode and format. For example, system clock is S/PDIF recovered clock for both clock 1 and clock 2, slave and 256 fs for clock 2, and master and 256 fs for clock 1.

- EVM Board Setting
  - JP101 : select DIR
  - SW105 : M/S; ON
  - SW105–SW106 : SW105 CLK1/0 setting must be met with SW106 PSCK1/0 setting
  - SW107 : CIF; OFF
- PCM3060 control application software
  - Select ADC, DAC independent in configuration panel and select appropriate I/F mode and format in each ADC and DAC panel, which must be met with EVM setting.

1.2.4.3 Asynchronous With Different Audio Interface

In this mode, ADC and DAC can run with different system clock and different audio interface mode and format. Asynchronous clock source can be selectable from internal 256/512 fs or 384 fs clocks or external clock, and audio interface mode and format can be different between ADC and DAC. For example, a combination of 384 fs, slave, RJ-24, fs = 44.1 kHz for DAC and 256 fs, master, LJ-24, fs = 48 kHz for ADC is supported.

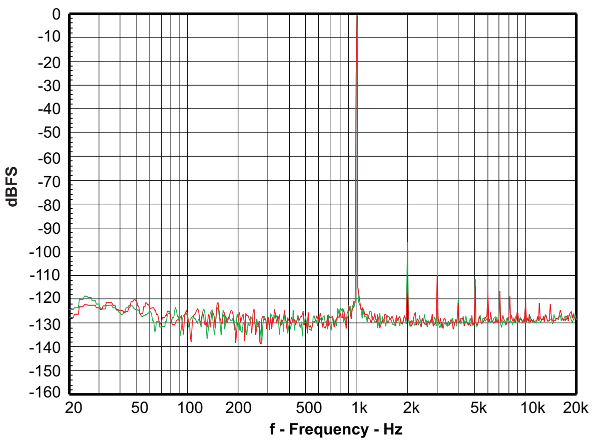
- EVM Board Setting
  - JP101 : select 256 fs
  - SW104 : FMT1; ON
  - SW105 : M/S; ON, CLK1/0; ON/OFF, FMT0; ON
  - SW106 : PSCK1/0; ON/OFF, FMT1/0; OFF/ON
  - SW107 : CIF; OFF, FS2/1; OFF/OFF, SR; OFF
- PCM3060 control application software
  - Select ADC, DAC independent in configuration panel and select appropriate I/F mode and format in each ADC and DAC panel, which must be met with EVM setting.

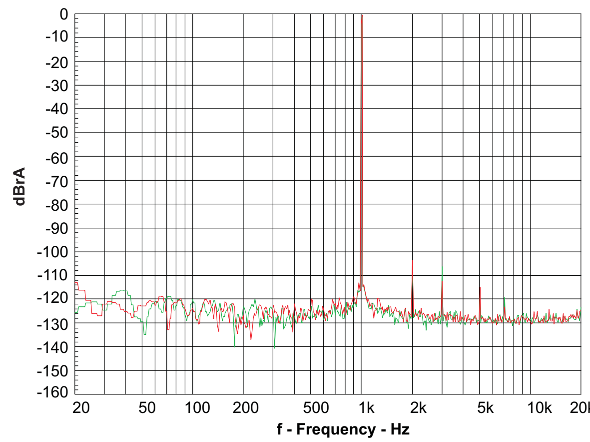
1.3 Typical Performance and Measurement Example

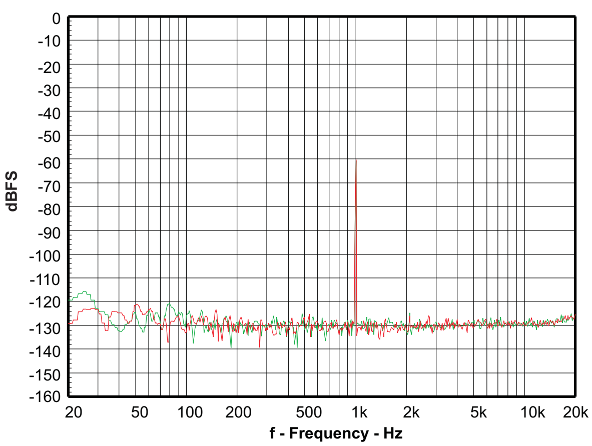
Measurement example of PCM3060 on DEM-DAI3060 at default condition is as follows, and FFT results for full scale, –60 dB and zero input are shown in the following graphs.

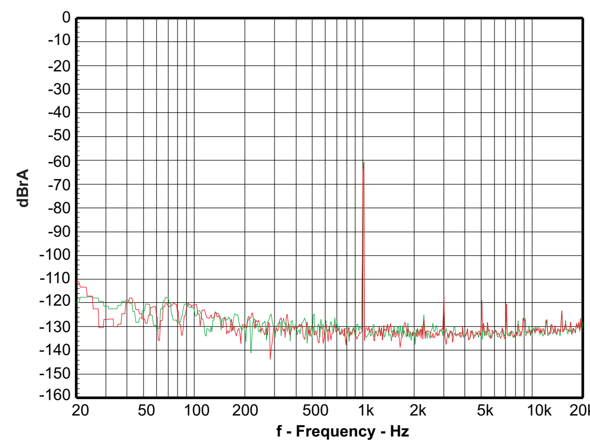
ADC performance in synchronous mode
THD+N at 48 kHz/512 fs: –92.3 dB
D. Range at 48 kHz/512 fs: 99 dB
SNR at 48 kHz/512 fs: 98.8 dB

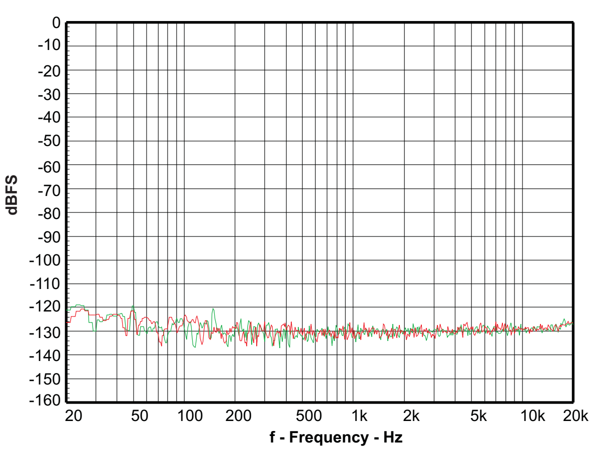
DAC performance in synchronous mode
THD+N at 48 kHz/512 fs: –94.8 dB
D. Range at 48 kHz/512 fs: 103.6 dB
SNR at 48 kHz/512 fs: 104.2 dB

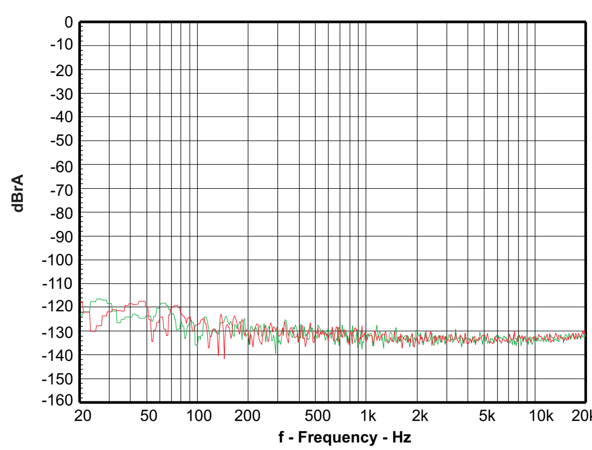




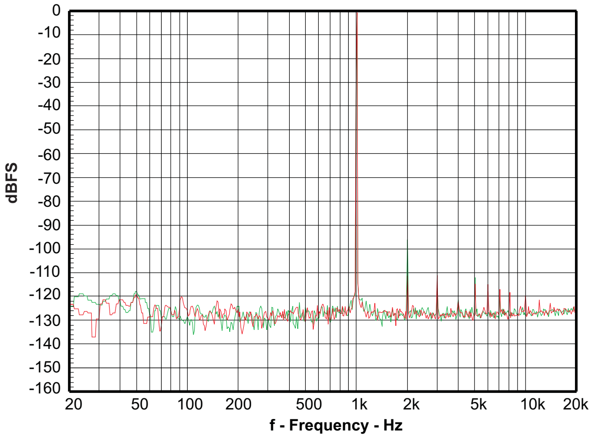


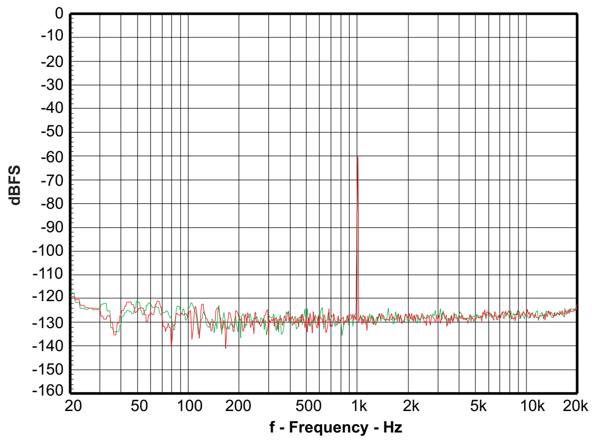


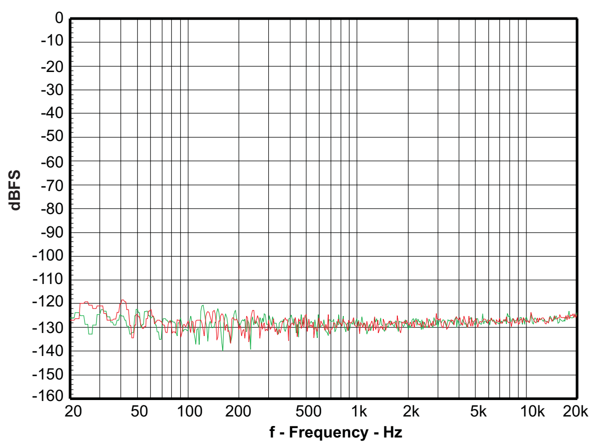




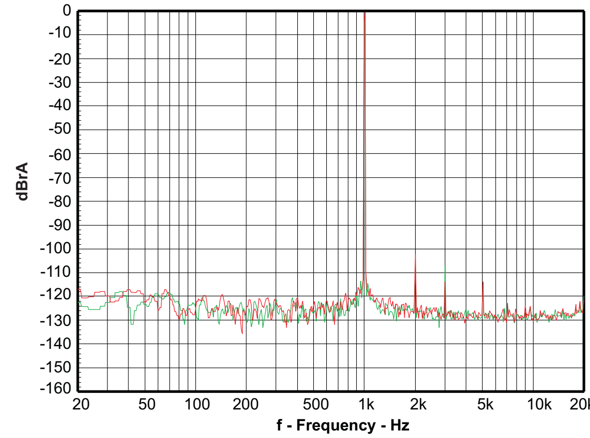
ADC performance in asynchronous mode
THD+N at 48 kHz/512 fs: –90.7 dB
D. Range at 48 kHz/512 fs: 96.3 dB
SNR at 48 kHz/512 fs: 96.3 dB

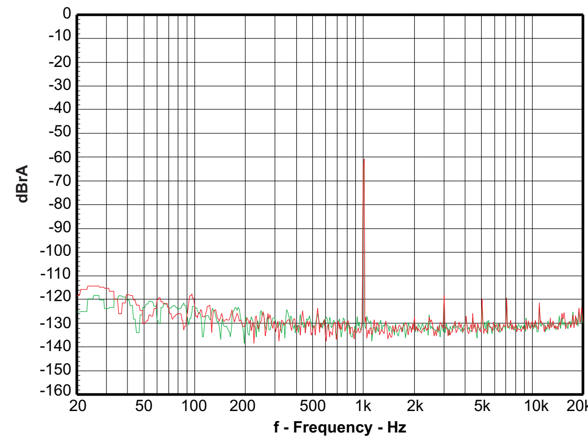


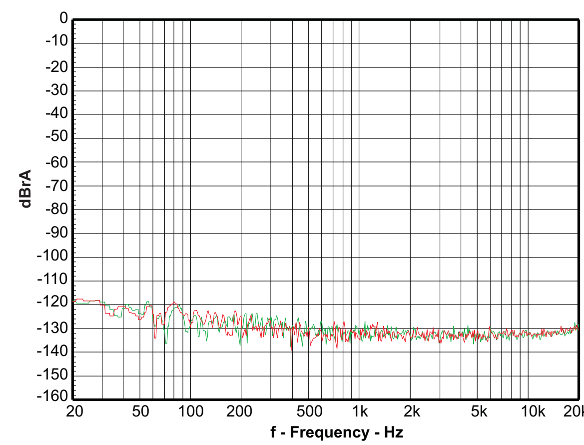




DAC performance in asynchronous mode
THD+N at 44.1 kHz/512 fs: –94.9 dB
D. Range at 44.1 kHz/512 fs: 102.7 dB
SNR at 44.1 kHz/512 fs: 103.5 dB

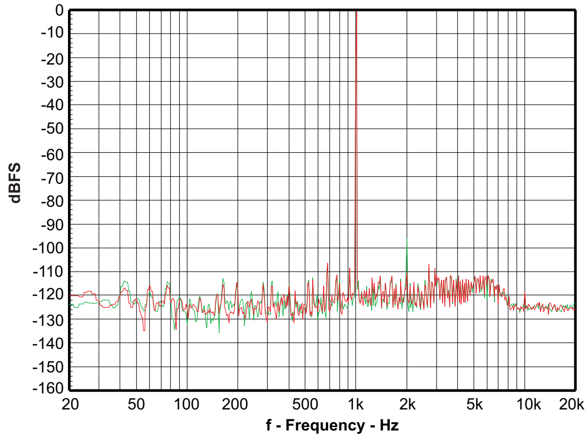


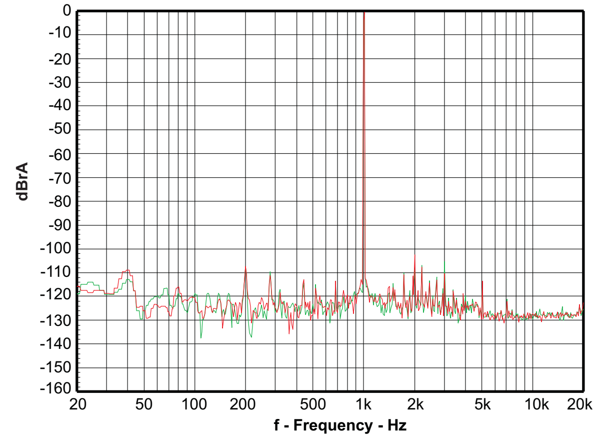


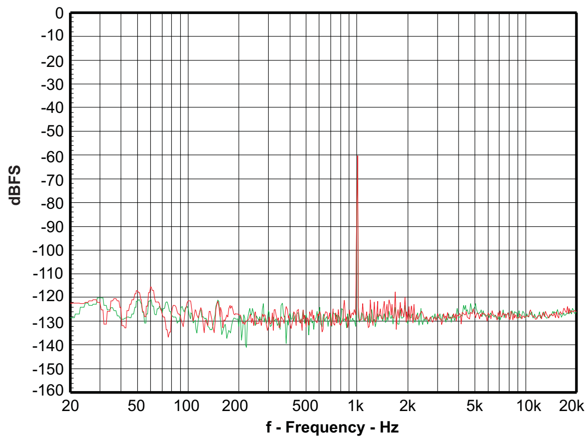


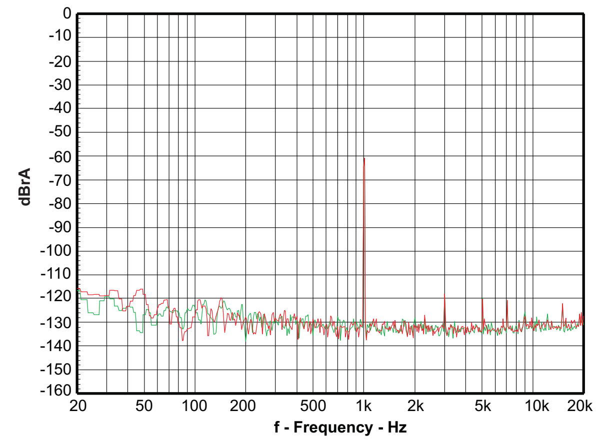
ADC performance in asynchronous mode
THD+N at 48 kHz/512 fs: –86.2 dB
D. Range at 48 kHz/512 fs: 97.3 dB
SNR at 48 kHz/512 fs: 97.2 dB

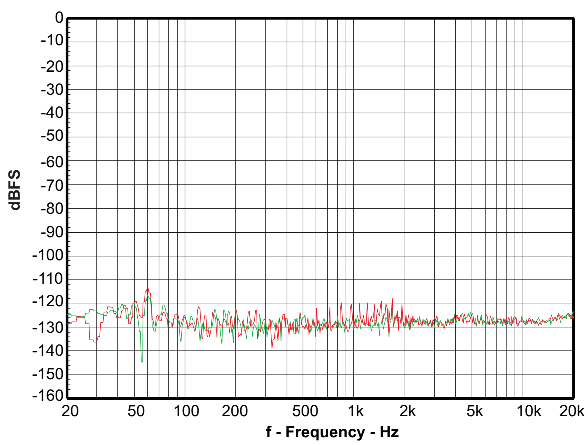
DAC performance in asynchronous mode
THD+N at 48 kHz/512 fs: –94.8 dB
D. Range at 48 kHz/512 fs: 103.7 dB
SNR at 48 kHz/512 fs: 104.3 dB

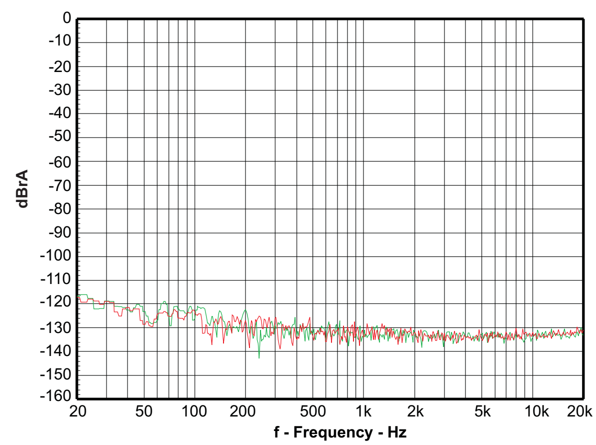








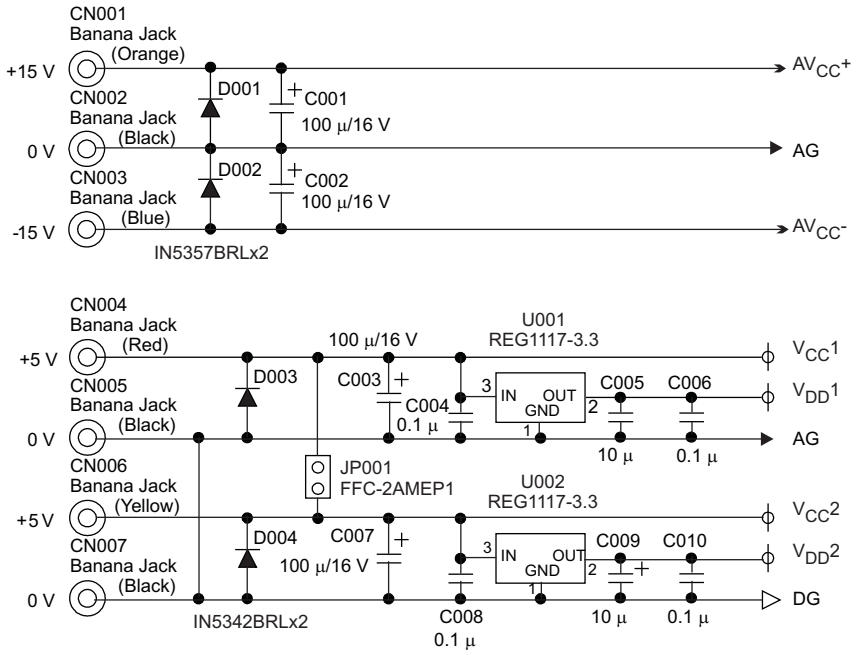




2 Schematic, Bill of Materials (BOM) and Printed-Circuit Board

This section presents the DEM-DAI3060 schematics, BOM, and printed-circuit board.

2.1 DEM-DAI3060 Schematic



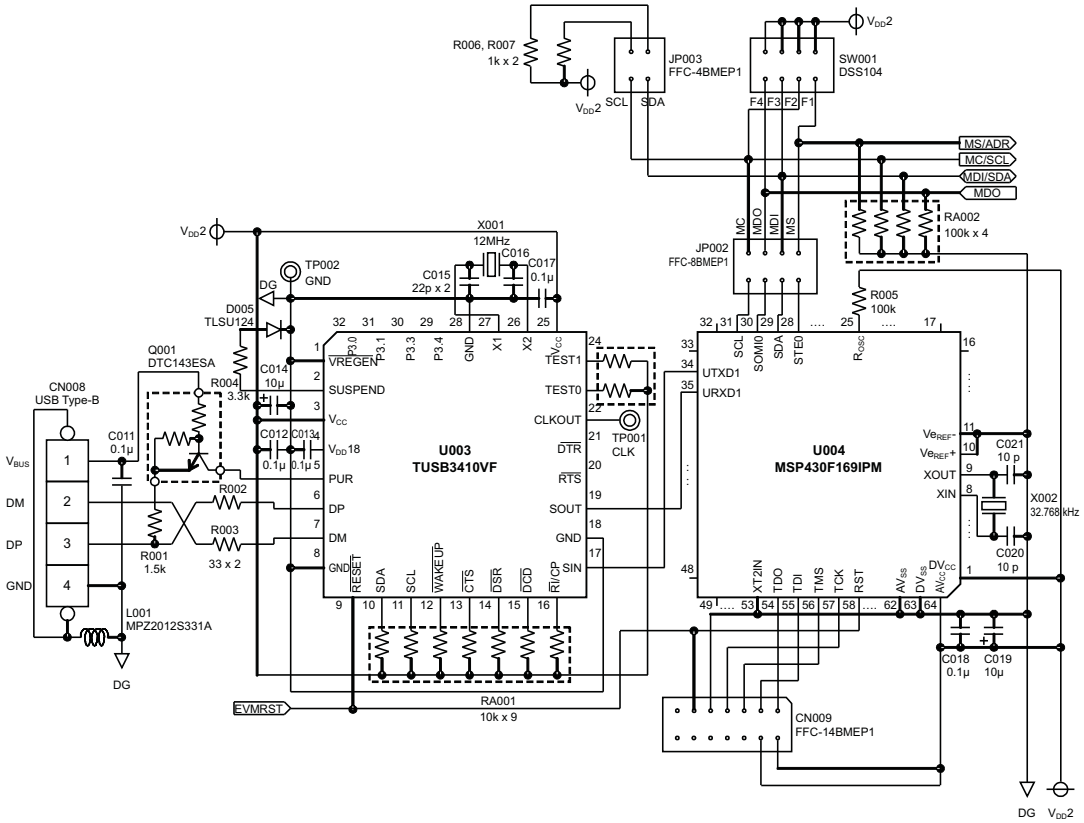


Figure 11. Regulator and Mode Control

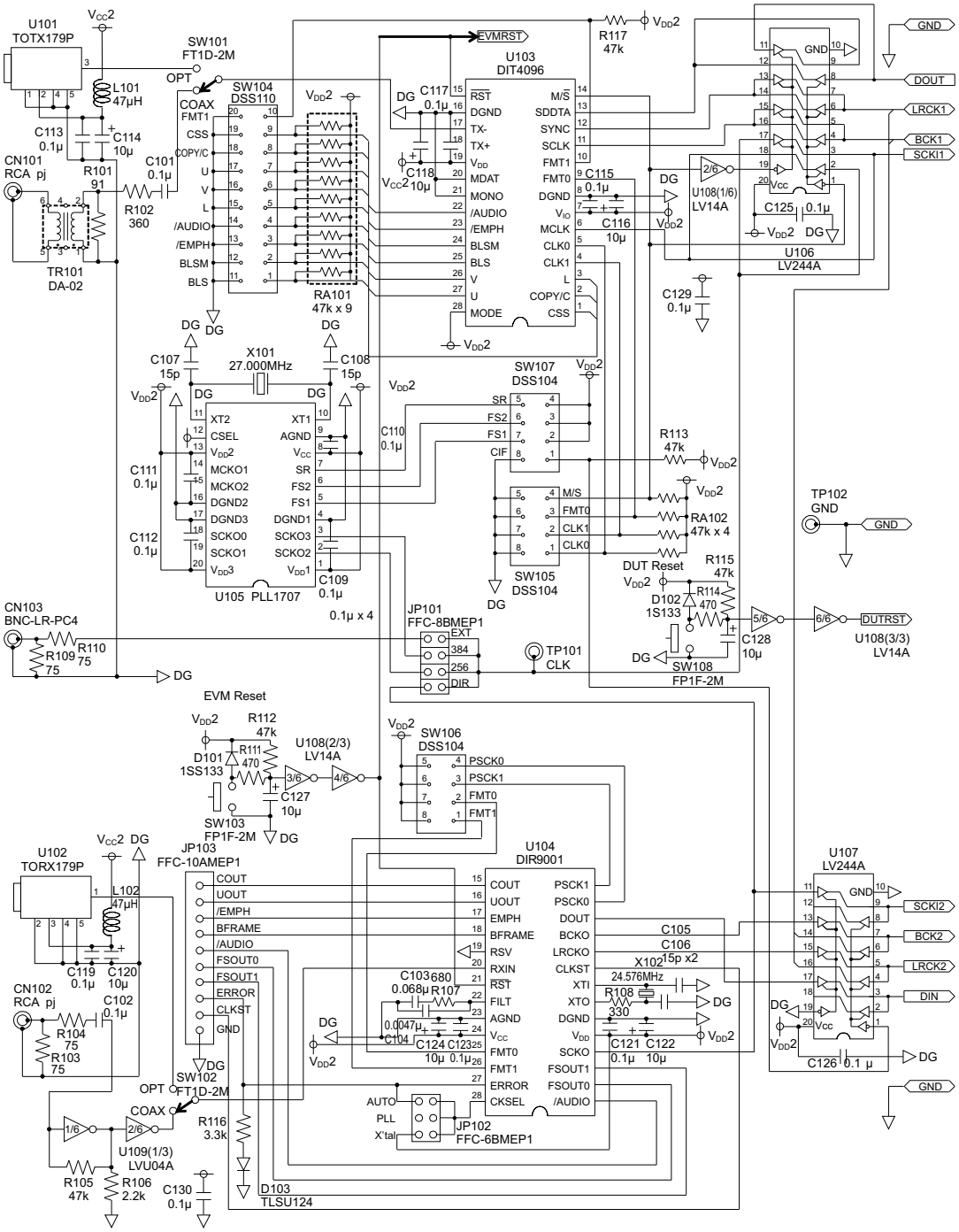


Figure 12. DIR, DIT, and Clock Generator

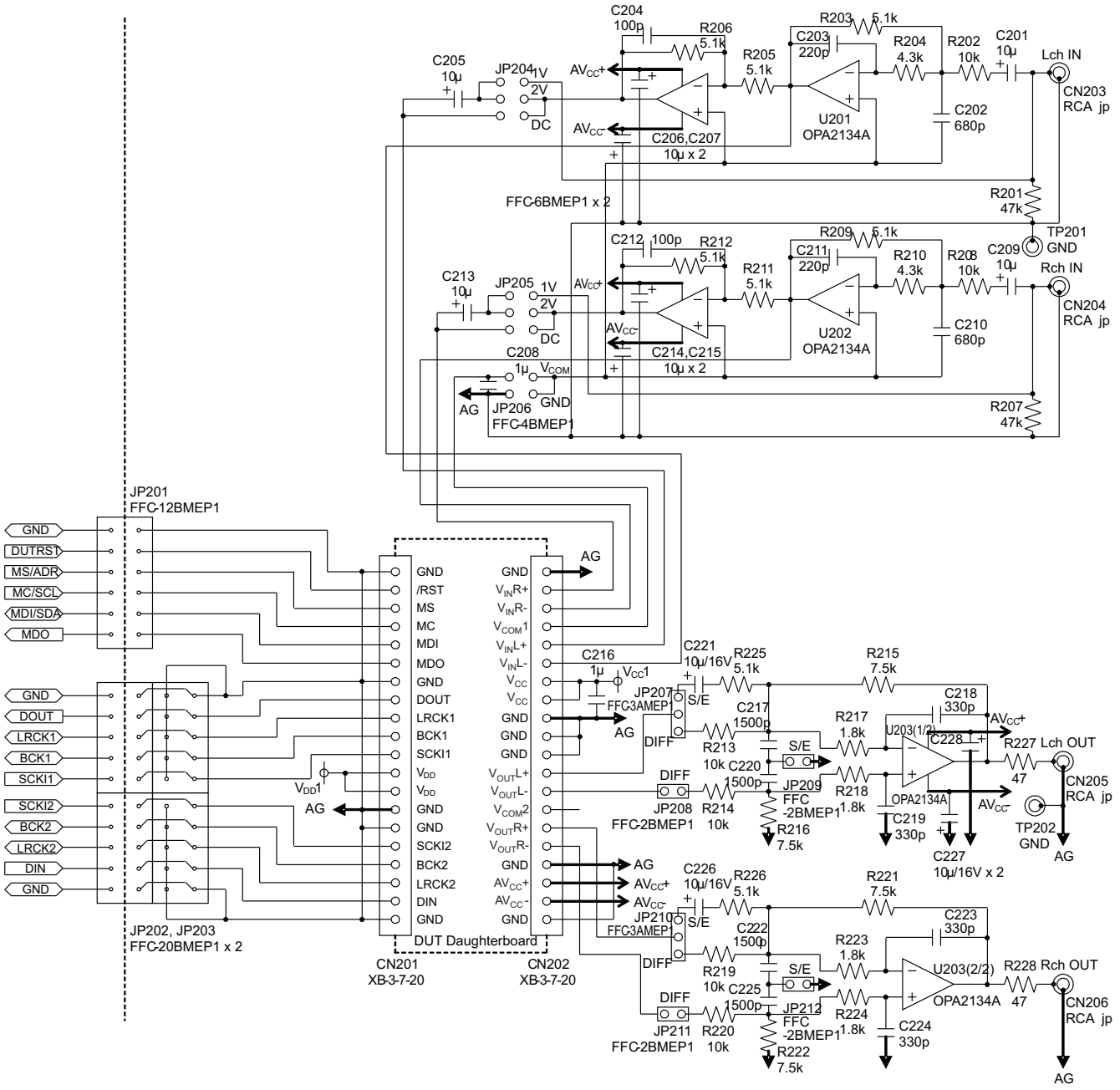


Figure 13. LPF and Buffer for Analog Input/Output

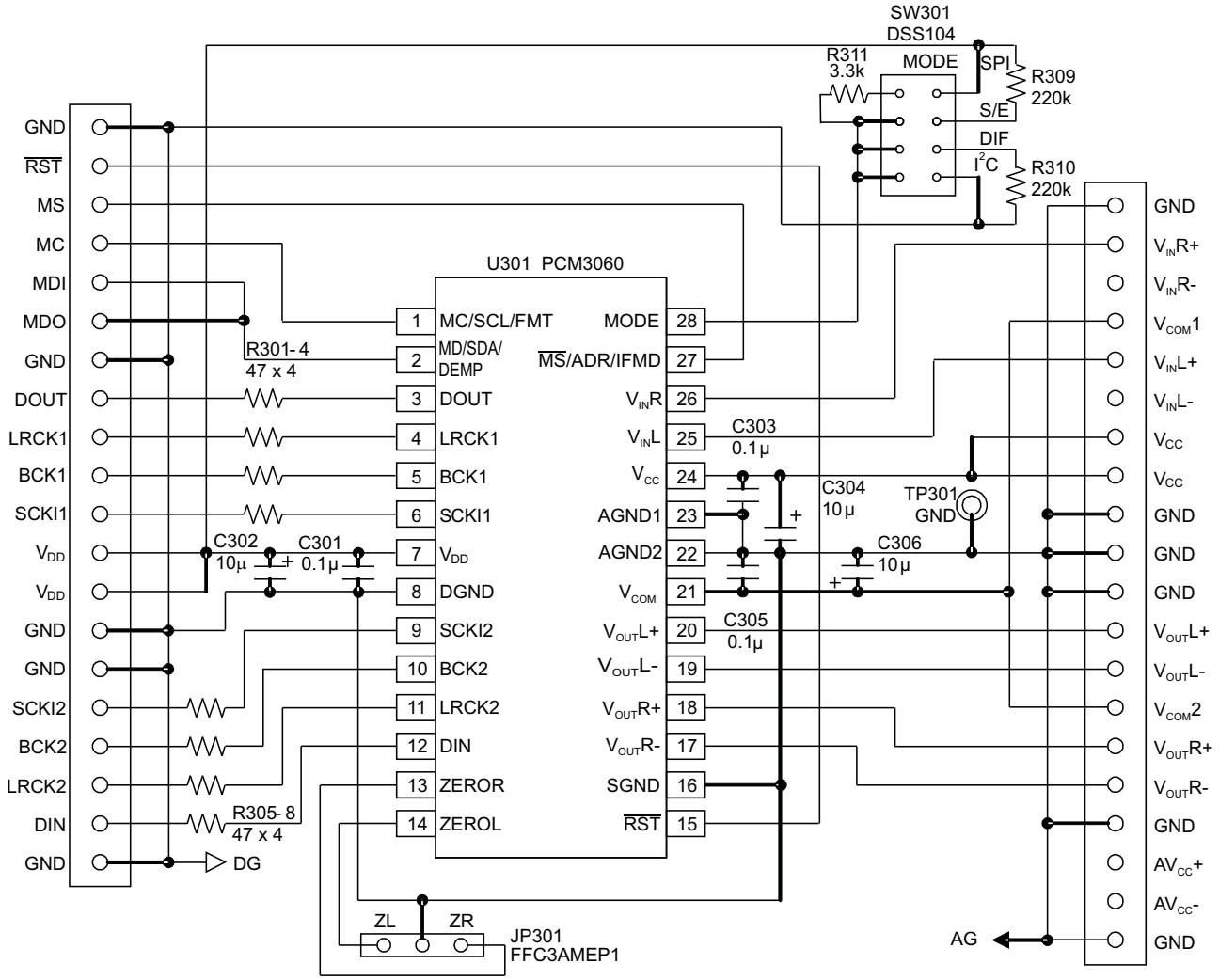


Figure 14. DUT PCM3060 Daughterboard

2.2 DEM-DAI3060 Bill of Materials (BOM)

Table 14. Bill of Materials

Reference Designators	Qty	Part Description	Specification	Mfg Part No.	Mfg
C020, C021	2	Ceramic Capacitor, Chip 1608	10 pF, 50V, J, CH		
C105–C108	4	Ceramic Capacitor, Chip 1608	15 pF, 50V, J, CH		
C015, C016	2	Ceramic Capacitor, Chip 1608	22 pF, 50V, J, CH		
C204, C212	2	Film Capacitor	100 pF, J		
C203, C211	2	Film Capacitor	220 pF, J		
C218, C219, C223, C224	4	Film Capacitor	330 pF, J		
C202, C210	2	Film Capacitor	680 pF, J		
C217, C220, C222, C225	4	Film Capacitor	1500 pF, J		
C104	1	Film Capacitor	0.0047 µF, 50V, J		
C103	1	Film Capacitor	0.068 µF, 50V, J		
C004, C006, C008, C010 – C013, C017, C018, C109–C113, C115, C117, C119, C121, C123, C125, C126, C129, C130, C301, C303, C305	26	Ceramic Capacitor, Chip 1608	0.1 µF, 25V, Z, F		
C101, C102	2	Ceramic Capacitor	0.1 µF, 50V, J		
C208, C216	2	Ceramic Capacitor, Chip 1608	1 µF, 10V, Z, F		
C005, C009, C014, C019, C114, C116, C118, C120, C122, C124, C127, C128, C206, C207, C214, C215, C227, C228, C302, C304, C306	21	Electrolytic Capacitor	10 µF, 16V	R3A-16V100M	ELNA
C201, C205, C209, C213, C221, C226	6	Electrolytic Capacitor	10 µF, 16V	ROA-16V100M	ELNA
C001–C003, C007	4	Electrolytic Capacitor	100µF, 16V	ROA-16V101M	ELNA
L001	1	EMC Filter, Chip 2012	0.47 µH, 0.05Ω	MPZ2012S331A	TDK
L101, L102	2	Micro Inductor	47 µH, J	EL0606SKI-470J	TDK
TR101	1	Pulse Transformer	75 Ω	DA-02	JPC
R002, R003	2	Metal Film Resistor, Chip 1608	33, 1/16W, J		
R227, R228	2	Metal Film Resistor, Chip 1608	47, 1/16W, F		
R301–R308	8	Metal Film Resistor, Chip 1608	47, 1/16W, J		
R103, R104, R109, R110	4	Metal Film Resistor, Chip 1608	75, 1/16W, J		
R101	1	Metal Film Resistor, Chip 1608	91, 1/16W, J		
R108	1	Metal Film Resistor, Chip 1608	330, 1/16W, J		
R102	1	Metal Film Resistor, Chip 1608	360, 1/16W, J		
R111, R114	2	Metal Film Resistor, Chip 1608	470, 1/16W, J		
R107	1	Metal Film Resistor, Chip 1608	680, 1/16W, J		
R006, R007	2	Metal Film Resistor, Chip 1608	1k, 1/16W, J		
R001	1	Metal Film Resistor, Chip 1608	1.5k, 1/16W, J		
R217, R218, R223, R224	4	Metal Film Resistor, Chip 1608	1.8k, 1/16W, F		
R106	1	Metal Film Resistor, Chip 1608	2.2k, 1/16W, J		
R004, R116, R311	3	Metal Film Resistor, Chip 1608	3.3k, 1/16W, J		
R204, R210	2	Metal Film Resistor, Chip 1608	4.3k, 1/16W, F		
R203, R205, R206, R209, R211, R212, R225, R226	8	Metal Film Resistor, Chip 1608	5.1k, 1/16W, F		
R215, R216, R221, R222	4	Metal Film Resistor, Chip 1608	7.5k, 1/16W, F		
R202, R208, R213, R214, R219, R220	6	Metal Film Resistor, Chip 1608	10k, 1/16W, F		
R201, R207	2	Metal Film Resistor, Chip 1608	47k, 1/16W, F		
R105, R112, R113, R115, R117	5	Metal Film Resistor, Chip 1608	47k, 1/16W, J		
R005	1	Metal Film Resistor, Chip 1608	100k, 1/16W, J		
R309, R310	2	Metal Film Resistor, Chip 1608	220k, 1/16W, F		
RA001	1	Resistor Array	10k × 9, J		
RA102	1	Resistor Array	47k x 4, J		
RA101	1	Resistor Array	47k × 9, J		
RA002	1	Resistor Array	100k × 4, J		

Table 14. Bill of Materials (continued)

Reference Designators	Qty	Part Description	Specification	Mfg Part No.	Mfg
D101, D102	2	Diode		1SS133	ROHM
D003, D004	2	Zener Diode	6.8V, 5W	1N5342BRL	On Semi
D001, D002	2	Zener Diode	20V, 5W	1N5357BRL	On Semi
D005, D103	2	LED		TLSU124	Toshiba
Q001	1	Digital Transistor	4.7k/4.7k	DTC143ESA	ROHM
U001, U002	2	3.3V Regulator	SOT-223	REG1117-3.3DCY	TI
U003	1	USB-to-Serial Port Converter	LQFP	TUSB3410VF	TI
U004	1	Mixed Signal Microcontroller	LQFP	MSP430F169IPM	TI
U103	1	Digital I/F Transmitter	TSSOP	DIT4096IPW	TI
U104	1	Digital I/F Receiver	TSSOP	DIR9001PW	TI
U105	1	PLL Clock Generator	QSOP	PLL1707DBQ	TI
U106, U107	2	Bus Buffer	TSSOP	SN74LV244A	TI
U108	1	Schmitt Trigger Inv.	TSSOP	SN74LV14A	TI
U109	1	Unbuffered Inv.	TSSOP	SN74LVU04A	TI
U201, U202, U203	3	Dual Op Amp	DIP	OPA2134PA	TI
U301	1	Async. Codec (DUT)	TSSOP	PCM3060PW	TI
U101	1	Optical Transmitter		TOTX-179P	Toshiba
U102	1	Optical Receiver		TORX-179P	Toshiba
X001	1	Crystal Resonator, HC-49/U-S	12MHz		Epson
X002	1	Crystal Resonator, SMT type	32.768 kHz	FC-135, 12.5pF	Epson
X101	1	Crystal Resonator, HC-49/U-S	27 MHz, 50ppm		Kinseki
X102	1	Crystal Resonator, HC-49/U-S	24.576 MHz, 50ppm		Kinseki
SW001, SW105– SW107, SW301	5	DIP Switch, 4 Poles		DSS104	Fujisoku
SW104	1	DIP Switch, 10 Poles		DSS110	Fujisoku
SW101, SW102	2	Toggle Switch		FT1D-2M	Fujisoku
SW103, SW108	2	Push Switch		FP1F-2M	Fujisoku
JP207, JP210, JP301	3	Pin Header	3 Pins	FFC-3AMEP1	Honda
JP103	1	Pin Header	10 Pins	FFC-10AMEP1	Honda
JP001, JP208, JP209, JP211, JP212	5	Pin Header	2 Pins	FFC-2BMEP1	Honda
JP003, JP206	2	Pin Header	4 Pins	FFC-4BMEP1	Honda
JP102, JP204, JP205	3	Pin Header	6 Pins	FFC-6BMEP1	Honda
JP002, JP101	2	Pin Header	8 Pins	FFC-8BMEP1	Honda
JP201	1	Pin Header	12 Pins	FFC-12BMEP1	Honda
JP202, JP203	2	Pin Header	20 Pins	FFC-20BMEP1	Honda
CN001	1	Banana Jack	Orange		
CN002, CN005, CN007	3	Banana Jack	Black		
CN003	1	Banana Jack	Blue		
CN004	1	Banana Jack	Red		
CN006	1	Banana Jack	Yellow		
CN008	1	USB Connector	Type-B Receptacle		
CN009	1	Pin Header	14 Pins	FFC-14BMEP1	Honda
CN101, CN102	2	RCA Connector	Yellow	LPR6520-0804	SMK
CN103	1	BNC Connector	Right Angle	BNC-LR-PC4	
CN201, CN202	2	Pin Header	20 Pins	XB-3-7-20	Mac8
CN203, CN205	2	RCA Connector	White	LPR6520-0803	SMK
CN204, CN206	2	RCA Connector	Red	LPR6520-0802	SMK
TP001, TP002, TP101, TP102, TP201, TP202, TP301	7	Test Terminal		LC-2-G	Mac8
	3	IC Socket ,DIP 8 Pins			
	12	Socket Pin		PX-1	Mac8
	32	Short Plug		DIC-130	Honda

2.3 DEM-DAI3060 Printed-Circuit Board

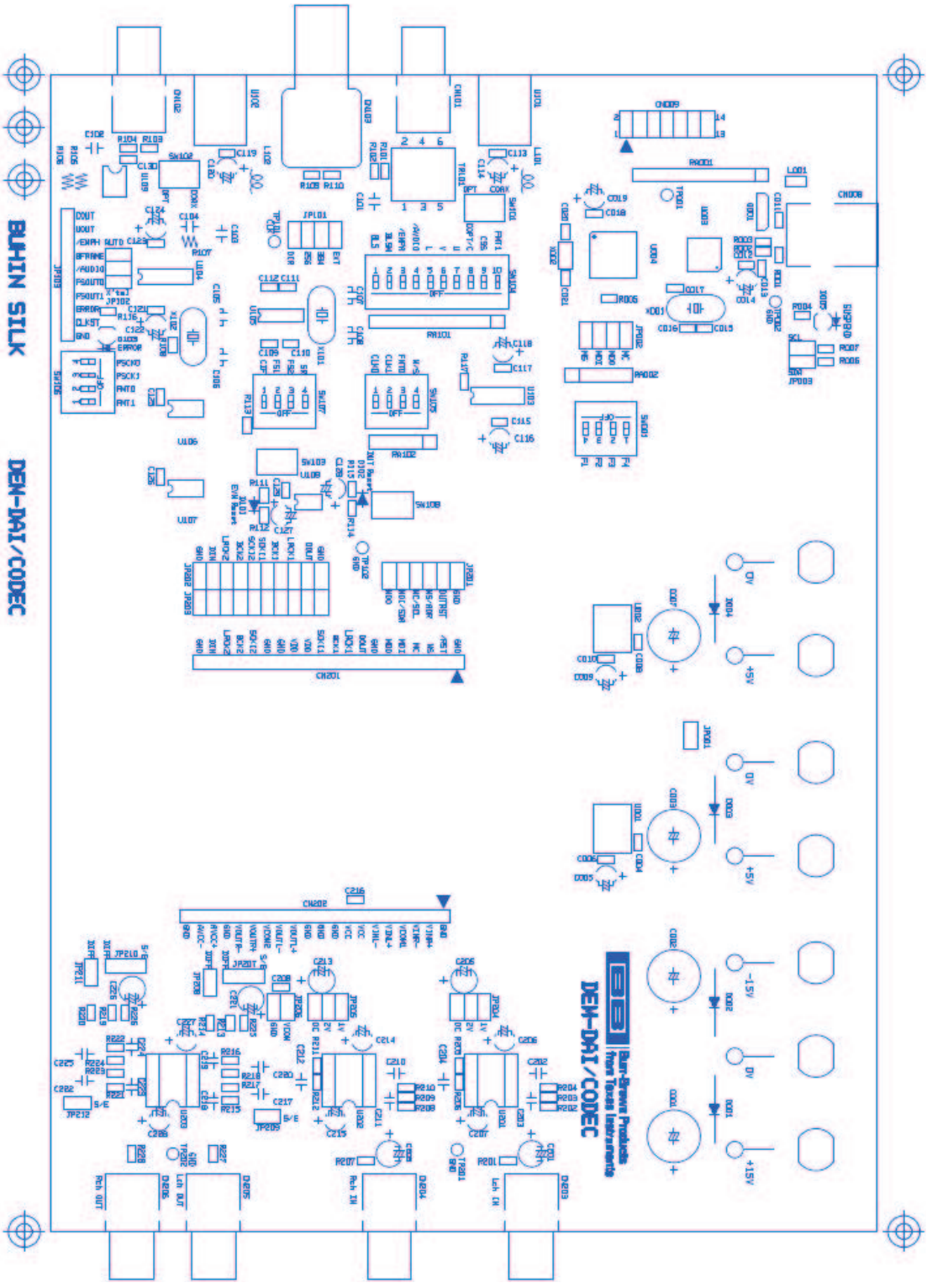


Figure 15. DEM-DAI3060 Silkscreen

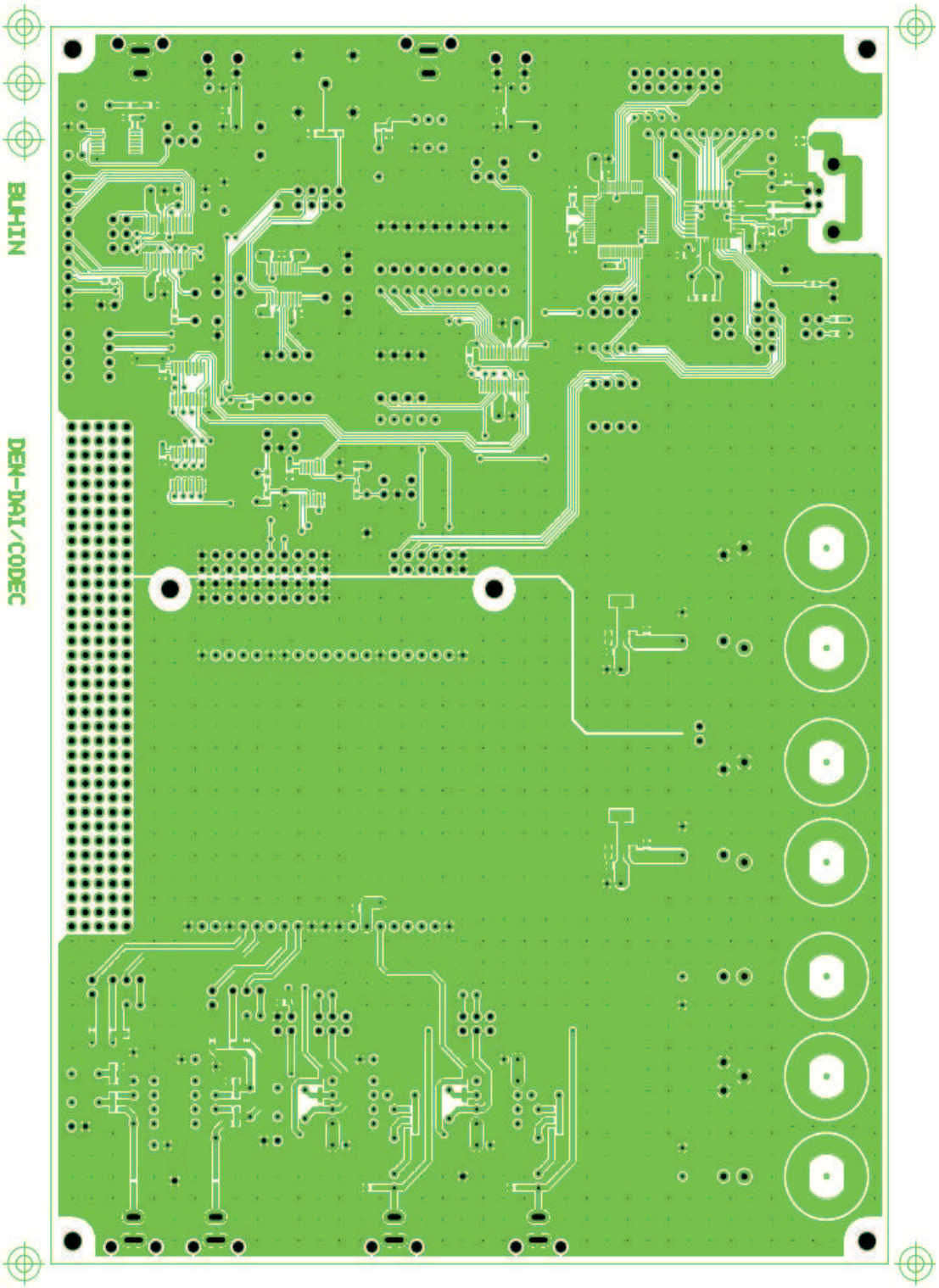


Figure 16. DEM-DAI3060 – Top View

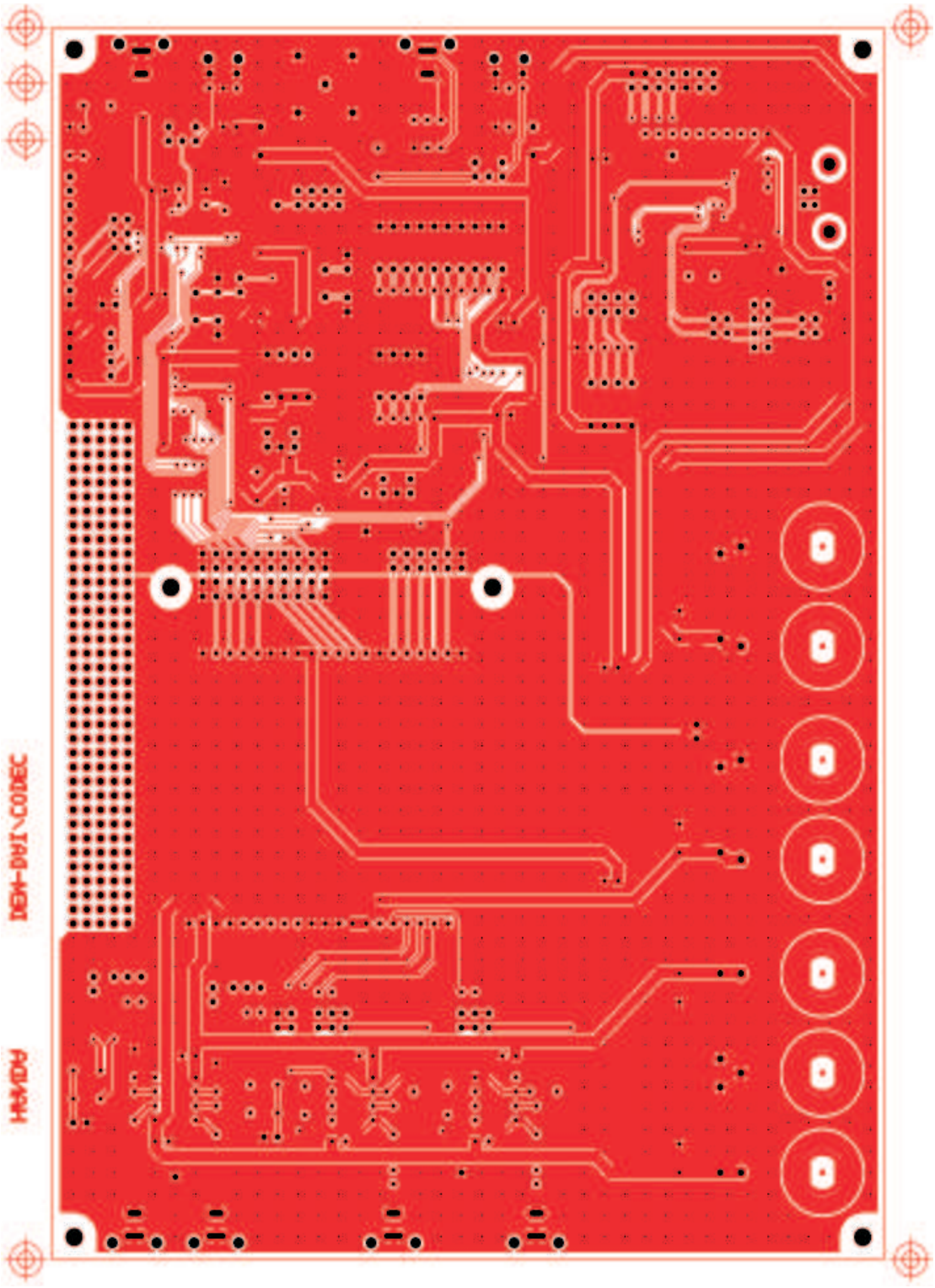


Figure 17. DEM-DAI3060 – Bottom View

2.4 DEM-DAI3060 Daughterboard Printed-Circuit Board

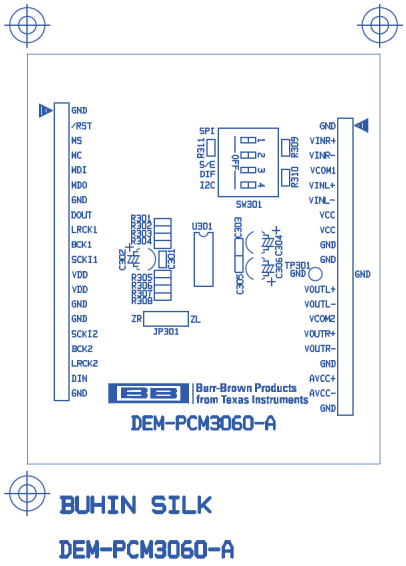


Figure 18. DEM-PCM3060 Silkscreen

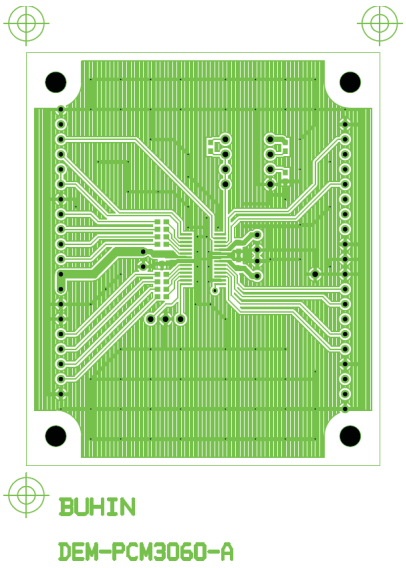


Figure 19. DEM-PCM3060 – Top View

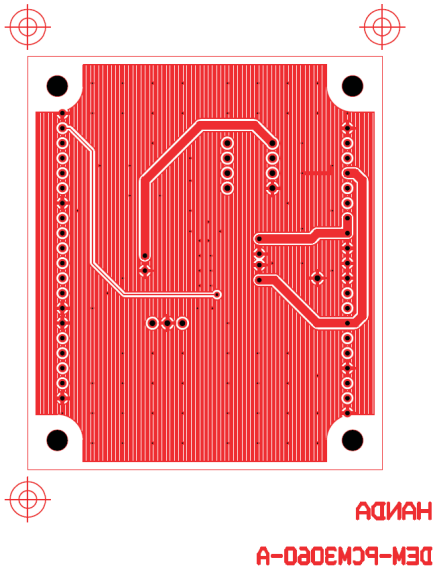


Figure 20. DEM-PCM3060 – Bottom View

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -4 V to +4 V and the output voltage range of -4 V to +4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 50° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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