ADS58C28 EVM

This is the user's guide for the ADS58C28 EVM Rev B. The ADS58C28 is a dual channel, 11-bit, 200MSPS analog-to-digital converter. This EVM is specifically suited for interfacing with TI's TSW1200 EVM to capture and display waveforms from the ADC. The EVM schematic, BOM, and layout files can be found in the design package in the ADS58C28 EVM product folder on www.ti.com.

1   Software Control

1.1   Installation Instructions

- Open folder named: ADS58C28_ADS42xx_Installer_vxpx (where xpx represents the latest version)
- Double-click: **setup.exe**
- Follow on-screen instructions to complete GUI installation
  - Wait for "ADS58C28/ADS42xx_ Installer" initializing screen to complete
  - Click "Next" to install files in the default destination directory
  - Select "I accept the License Agreement" and click "Next"
  - Select "Next" on the summary page
  - Wait for files to load and then click "Next"
  - Once all files are installed click "Next"
- If Windows Logo Message window appears, click "Continue Anyway"
- Once installed, launch by clicking on the ADS58C28_ADS42xx_GUI_vxpx program in Start>Texas Instruments ADCs
- When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
  - On the Welcome to the Found New Hardware Wizard window select "No, not at this time"
  - Select "Install the software automatically" button on the next window
  - Select "Continue Anyway" on the Windows Logo Message window
  - If computer can not find the drivers automatically then you can access them directly in the install directory: C:\Program Files\Texas \Instruments\ADS58C28_ADS42xx\data
  - Click "Finish" once completed

1.2   Software Operation

The software allows full programming control of the ADC device. Figure 1 shows the GUI front panel that has two register tabs: Top Level and Advanced. The Top Level tab provides an interface to the most used registers. The Advanced tab includes less used registers and provides an option to manually input address and data values.

1.2.1 Top Level

Figure 1 shows the Top Level tab of the register user interface. Below is a brief explanation of the controls. Please refer to the ADS58C28 datasheet for more detailed explanations of the register functions as needed.

- Reset: Device reset, click this switch to reset the device.
- PND Global: Device power down, click this switch on to power down the device.
- Data format: Device output data format, click it to set 2's complement.
- LVDS_CMOS Ctrl: Select this box for LVDS or CMOS output format.
- Digital Funct Ctrl: Enable or disable three digital functions:

    SNRb/Gain Disable – SNRBoost, gain, test patterns, and offset correction are disabled.

    SNRb Enable Only – SNRBoost is enabled; gain, test patterns and offset correction are disabled.

    SNRb/Gain Enable – SNRBoost, gain, test patterns, offset correction are enabled.

- Gain_chA: Set this box for gain of channel A.
- Gain_chB: Set this box for gain of channel B.
- Test Pattern: Select device test pattern.
- High Perf Mode: High performance mode enable or disable.
- High Freq Mode ChA: High frequency Mode enable for channel A.
- High Freq Mode ChB: High frequency Mode enable for channel B.
- Low Speed Mode En: Low speed mode enable or disable.
- Low Speed Mode ChA: Low speed mode for channel A.
- Low Speed Mode ChB: Low speed mode for channel B.
- LVDS Data Strength: Set the data strength from this switch.
- LVDS Clkout Strength: Set the output clock strength from this switch.
- CMOS Clk Strength: Set CMOS output clock strength from this switch.
- SNRBoost ChA: SNRBoost enable or disable for channel A.
- SNRBoost ChB: SNRBoost enable or disable for channel B.
- SNRBoost Filter ChA: Select SNRBoost filter for channel A.
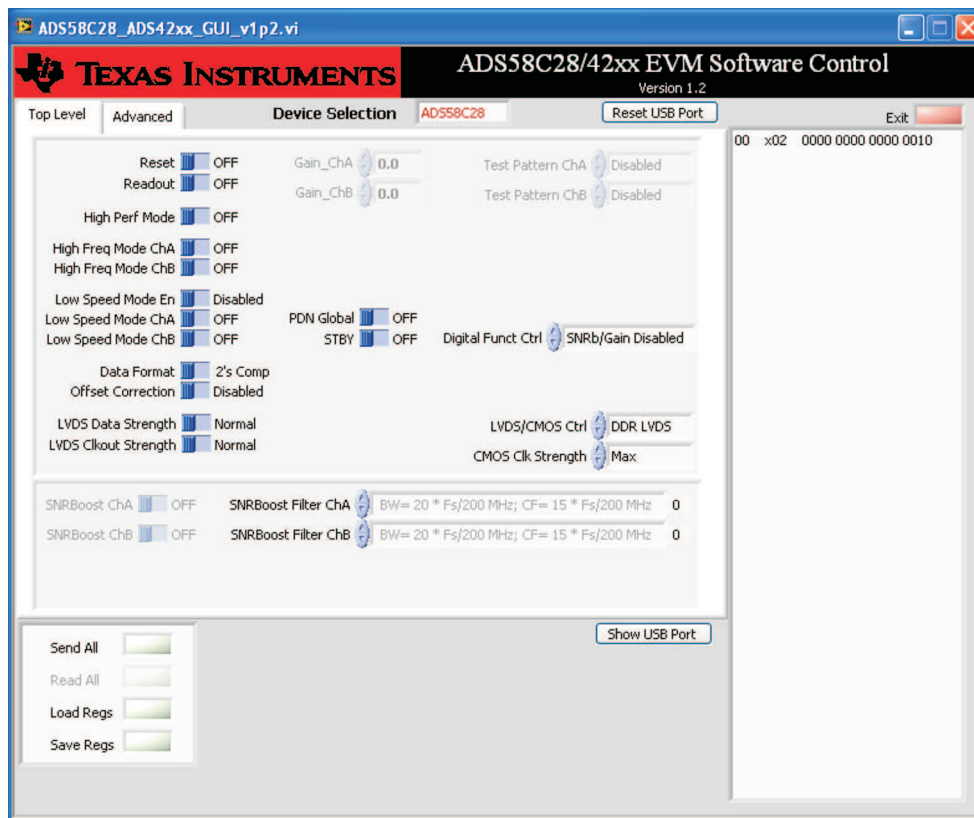- SNRBoost Filter ChB: Select SNRBoost filter for channel B.

Figure 1. ADS58C28_ADS42xx_GUI Front Panel – Top Level

1.2.2   Advanced Level

Click on "Advanced" tab on the GUI to bring the advanced panel to the front. On this panel user can write address and data of any register into the address/data boxes (as shown in Figure 2, "45" is address and "4" is data). Press Enter on the key board once data is entered or click "Send All" button on the GUI to send address and data from the boxes to ADC. The address and data are shown in the display box located at right side of the panel. In addition, there is group of switches used for output offset functions, SNRBoost pin overwrite, and a group of LEDs used to designate a custom test pattern.
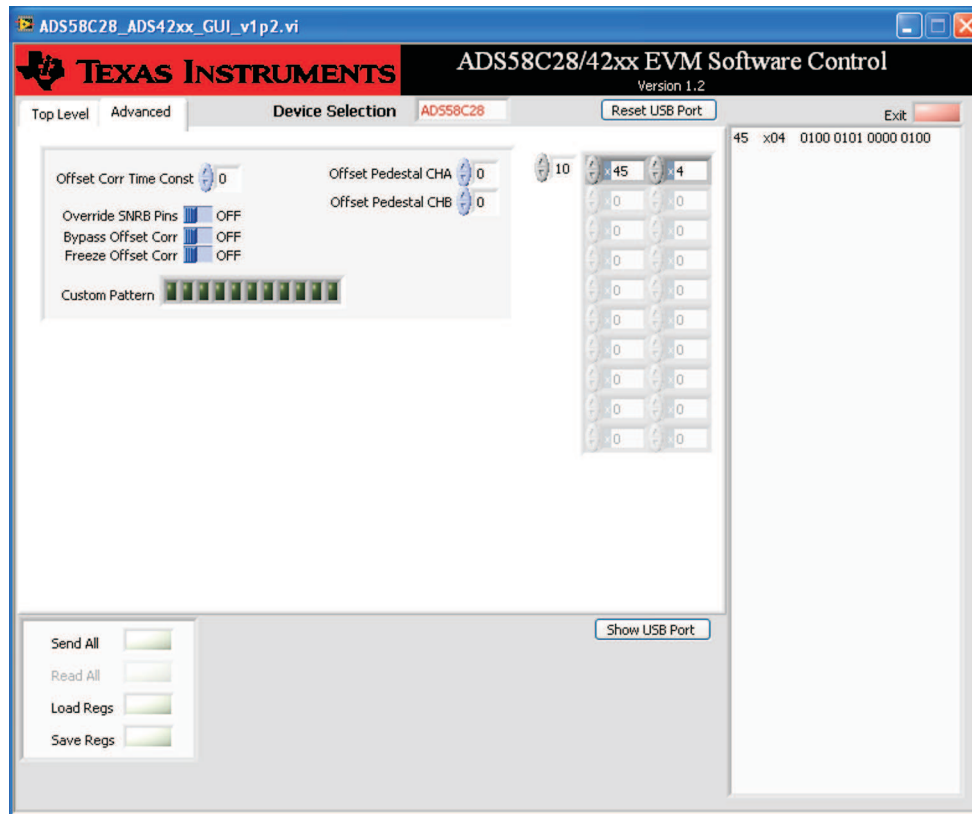
Figure 2. ADS58C28_ADS42xx_GUI – Advanced Level

1.2.3 Register Control

- Send All: Sends all the register configurations on the panel to the device
- Read All: Not active
- Save Regs: Saves the register configuration to text file
- Load Regs: Loads a register file from a text file. After load register the relative switches and selecting boxes are automatically updated.
  — Select Load Regs button.
  — Double click on the desired register file.
  — Click on Send All to ensure all of the values are loaded properly.

1.2.4 Misc Settings

- Device Selection: Select ADS58C28 for proper operation
- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address.
- Show USB Port: Allows user to change USB port configuration. Default setting is appropriate for the EVM RevB.
- Exit: Stops the program

2 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

2.1 Test Block Diagram

The test set-up for general testing of the ADS58C28 with the TSW1200 capture card is shown in Figure 3.
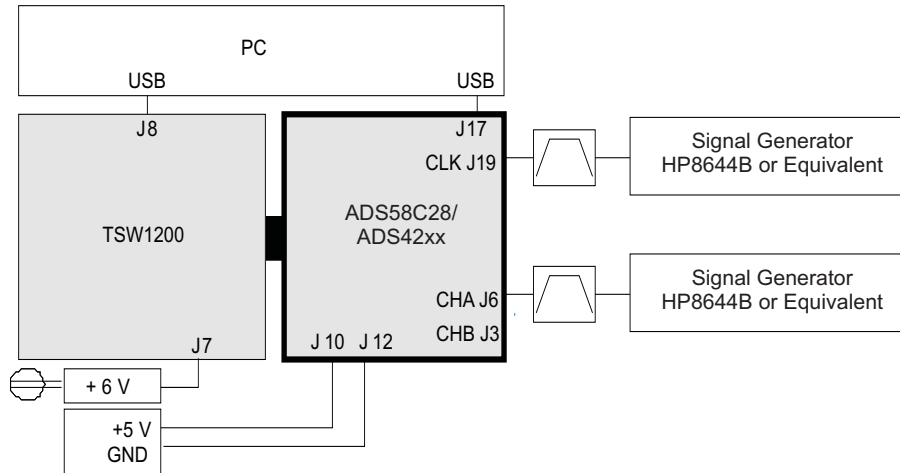
Figure 3. Test Set-up Block Diagram

2.2 Verify Board Set-up

Verify jumper settings are in the correct position as outlined in Table 1.

Table 1. Default ADS58C28/42xx EVM Rev B Jumper setting for serial interface

Jumper	Default position	Function
JP15	Short 1–2	DC supply
JP16	Short 1–2	DC supply
JP17	Short 2–3	DC supply, LDO
JP19	Short 2–3	DC supply, LDO
JP28	Short 2–3	DC supply, LDO
JP29	Short 2–3	DC supply, LDO
JP26	Open	DC supply for ext buffer
JP27	Open	DC supply for ext buffer
JP3	Short 2–3	OPA power down
JP4	Short 2–3	OPA power down
JP22	Open	SDOUT to FPGA
JP20	Short 1–2	CDC
JP21	Short 1–2	CDC
J14	Short 1–2	CDC power down
J18	Open	CDC, VCXO
JP8	Short 2–3	ADC SCLK for SPI
JP9	Short 2–3	ADC SDATA for SPI
JP10	Short 2–3	ADC SEN for SPI
JP11	Short 2–3	ADC for SPI, also reset
JP12	Short 1–2	ADC Low speed mode disable
JP13	Open	
JP14	Short 7 - 8	ADC 2's complement, DDR LVDS

Table 1. Default ADS58C28/42xx EVM Rev B Jumper setting for serial interface (continued)

Jumper	Default position	Function
JP5	Short 1 - 2	ADC CTRL3, normal operation
JP6	Short 1 - 2	ADC CTRL2, normal operation
JP7	Short 1 - 2	ADC CTRL1, normal operation
JP 18	Short 1 - 2	Ext Buffer
JP 23	Short 1 - 2	Ext Buffer
JP 24	Short 1 - 2	Ext Buffer
JP 25	Short 1 - 2	Ext Buffer

Table 2. Parallel interface with Pin Control of ADS58C28/42xx EVM Rev B Jumper Setting

| Jumper	Position	Function
JP8	Short 1 - 2	ADC SCLK for parallel control
JP9	Short 1 - 2	ADC SDATA for parallel control
JP10	Short 1 - 2	ADC SEN for parallel control
JP11	Short 1 - 2	ADC parallel control

2.3 Test Set-up Connections

- Connect ADS58C28 EVM to TSW1200 EVM
- Connect 5V power to banana jack at J10; connect ground to J12
- Connect USB cable to programming computer at J17
- Connect USB and power supply jack to TSW1200
- Connect Clock signal through appropriate BPF to J19
- Connect input signal through appropriate BPF to J6 or J3

2.4 TSW1200 Quick Start Operation

Reference the TSW1200 User's Guide for more detailed explanation of the TSW1200 set-up and operation. This document assumes the TSW1200 software is installed and functioning properly. The front panel of the TSW1200 is shown in Figure 4. The following configuration needs to be changed from the default settings

- Jumper setting on TSW1200 board
  Set J11 (2-3) High, J10 (1-2) Low for LVDS DDR data input (default)
  Set J11 (2-1) Low, J10 (1-2) Low for 1-wire serial data input
- Select ADS58C28 device name from the TI ADC Selection pull-down menu
  - If this option is not available then download the latest ADS58C28.ini file from the product folder of the TSW1200 at www.ti.com
  - Place updated *.ini files in the TSW1200 product directory located at C:\Program Files\Texas Instruments\TSW1200\ADC Files
- Select Single Tone FFT from the Test pull-down menu
- Select Data Capture Option>Capture Options>Two's Complement Mode to set data format
- Select the desired channel (i.e., Channel A or B) from the Channel Display pull-down menu
- Change ADC sampling rate to desired value (i.e., 200 MHz)
- Change input frequency to desired value (i.e., 140 MHz or other)
- Press Ctrl-Shift-I to reset the software as needed
- Verify status display in lower left has no errors
- Press Capture button to initiate a data capture
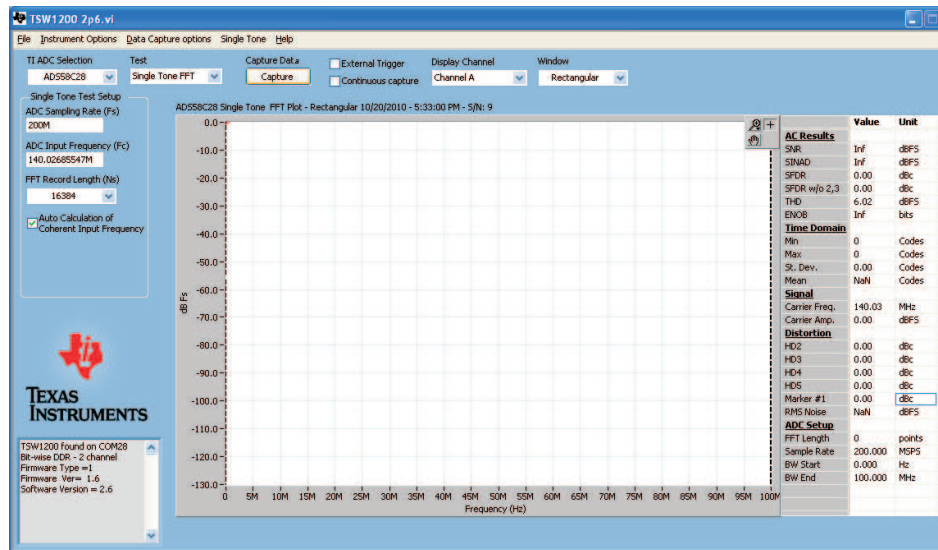
Figure 4. TSW1200 GUI

2.5 ADS58C28 Test Procedure

- Switch on 5V power supply on ADC EVM. Verify source current is about 310 mA ± 20 mA with clock and TSW1200 connected at EVM default (i.e., connected at 200MHz).
- Connect clock signal at J19 through an appropriate BPF.
  - Adjust the signal generator amplitude output 0.6Vrms to provide approximately 0.8 Vpp at J19 through a BPF with about 5 dB attenuation plus cable losses.
  - Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Connect input signal through an appropriate BPF at either J6 or J3 (Channel A or B, i.e., 140MHz).
  - Adjust frequency of generator to match the coherent frequency displayed in the TSW1200 GUI.
  - Select the proper Display Channel on the TSW1200 GUI software that corresponds to the input connection.
  - Adjust the signal generator amplitude output to achieve −1 dBFS on FFT plot at the "Carrier Amp" indicator.
  - Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Enable SNR Boost (if desired) through either hardware or software.
  - Hardware enable by CTRL pins JP5, JP6 and JP7
    - Set Digital Funct Ctrl to "SNRb/Gain Disable"
    - Select desired SNRBoost Filter Chx register
    - Set Digital Funct Ctrl to "SNRb Enable Only"
    - Set hardware pins at jumper JP5 and JP6 to High (short 2–3), set JP7 to LOW (short 1–2) to enable SNRBoost.
    - See table 8 in SBAS509 datasheet for other hardware control options
  - Software enable by setting the GUI registers only
    - Set Digital Funct Ctrl to "SNRb/Gain Disable"
    - Set desired SNRBoost filter for Chx
    - Set Digital Funct Ctrl to "SNRb Enable Only"
    - Set Override SNRb Pins to "On" in Advanced panel
    - Set SNRBoost ChA and ChB to "On" in Top Level panel
- Initiate a capture by pressing the Capture button on the TSW1200 GUI

2.6 ADS58C28 Performance Results

Figure 5 shows the performance results with the SNR Boost disabled at 200 MSPS clock frequency and with a 140 MHz input tone. Figure 6 shows the same set-up with SNR Boost enabled using a filter register setting of 40 (BW = 60 × Fs/184 MHz; CF = 46 × Fs/184 MHz) corresponding roughly to 60 MHz of BW for the given clocking rate. ADC calculations related to SNR and SFDR are completed over this specified bandwidth by adjusting the cursor bandwidth on the TSW1200 GUI.
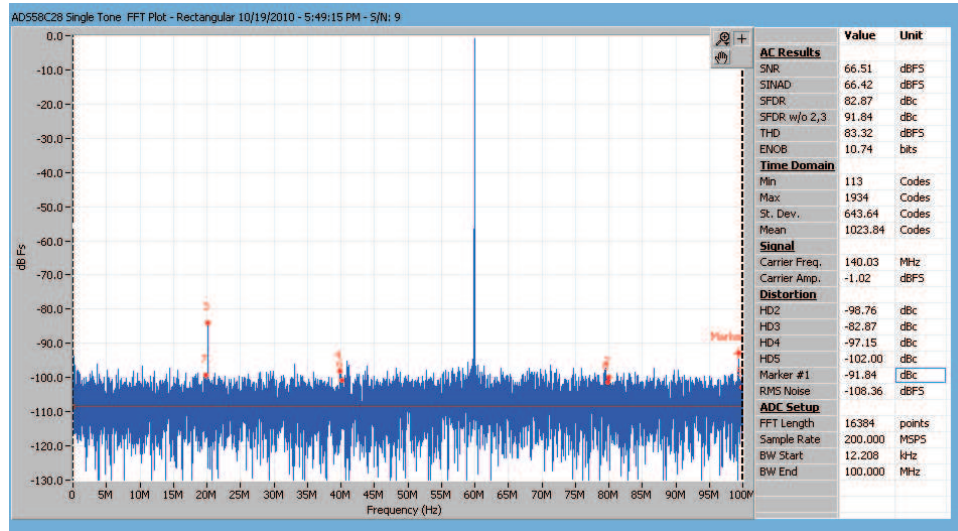

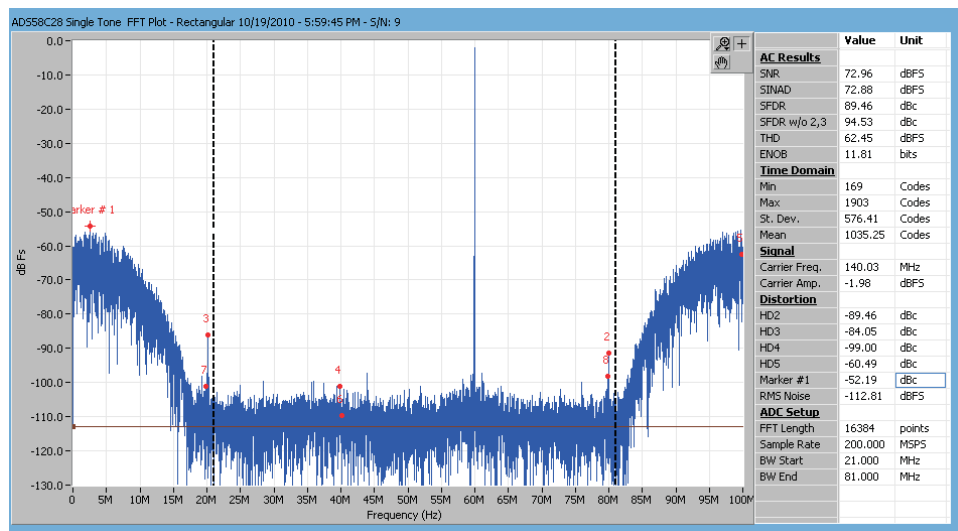**Figure 5. FFT Plot: 200 MHz Clock, 140 MHz input; SNRBOOST Disable**

Figure 6. FFT Plot: 200 MHz clock, 140 MHz input; SNRBOOST Enabled with Filter #40 (BW 60MHz)

3 Optional Configurations

3.1 THS4509 Input Op-Amp Configuration

The default analog input configuration is transformer coupling through T1 and T2 for channel A, and T3 and T4 for channel B. The optional configuration for analog input is through an Op-Amp THS4509. The changes required to modify the transformer coupled input to the OPA-driven input are shown in Table 3.

Table 3. Jumper Setting for Transformer-Coupled or OPA-Driven Input

Jumpers or 0 Ω	Transformer-coupled input (default)	OPA-driven input
R119	Install	Do not install
R123	Install	Do not install
R120	Do not install	install
R129	Do not install	install
R143	Install	Do not install
R141	Install	Do not install
R131	Do not install	Install
R132	Do not install	Install
R93	Install	Do not install
R94	Install	Do not install
R95	Do not install	Install
R96	Do not install	Install
R97	Install	Do not install
R98	Install	Do not install
R99	Do not install	Install
R114	Do not install	Install
SJP3	Shunt 2 - 3, default	Shunt 1-2
SJP4	Shunt 2 - 3, default	Shunt 1-2

J11 and J13 are the power supply for THS4509. An on-board layout option for a LPF or BPF is available between the amplifier and the ADC. By default the filter is bypassed to allow the user flexibility to design according to desired specifications.

3.2 On-board CDC72010 Clock

The default clock input configuration is 1:4 transformer coupling through T6. The optional configuration is through clock driver CDC72010. The changes required to modify the transformer coupled clock input to clock driver input are shown in Table 4.

Table 4. Jumper Setting for Transformer-Coupled or CDC72010 Input

Jumper	Transformer-coupled (Default)	CDC72010
J14	shunt	open
JP20	Shunt 1-2	Shunt 1-2
JP21	Shunt 1-2	Shunt 1-2
J18	open	open
R121	0 ohm	DNI
R122	DNI	0 ohm
SJP7	Short 1-2	Short 3-4
SJP6	Short 3-4	Short 5-6

The on-board layout is available for the option of VCXO and crystal BPF. The CDCE72010 comes with a default configuration (please see CDCE72010 data sheet for details about device default configuration). With a 10MHz primary reference at J19 and a 983.04 MHz VCXO on-board the CDC outputs a LVCMOS clock at U0P (pin7) at 245.76MHz. With a 491.52 MHz VCXO the CDC outputs a LVCMOS clock at U0P at 122.88MHz. The clock goes through an on-board crystal BPF (Y0) and is used as the input clock to the ADC through SJP6.

3.3 Parallel CMOS Output

The default ADC output is configured as DDR LVDS output on the EVM. The layout provides an option of 1.8V parallel CMOS output from the ADC. The changes required to modify from DDR LVDS output to parallel CMOS output are shown in Table 5.

Table 5. Jumper/Component Setting for DDR LVDS Output and Parallel CMOS Output

Jumper/Component	DDR LVDS output	Parallel CMOS
U12 (SN74AVC16T245)	DNI	Installed
U13 (SN74AVC16T245)	DNI	Installed
RN5 to RN8	Installed	DNI
RN9 to RN12	Installed	DNI
JP26	Open	Shunt
JP27	Open	Shunt

The CMOS output data is output from the EVM board at 40-pin connectors J1 (ch A) and J2 (ch B).

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 25° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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3.1.2   *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2   *Canada*

3.2.1   *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの

措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。 上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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