

# TI Precision Designs: Reference Design

## 10 $\mu$ A-10 mA, Single-Supply, Low-Side, Current Sensing Solution



### TI Precision Designs

TI Precision Designs are analog solutions created by TI's analog experts. Reference Designs offer the theory, component selection, and simulation of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

### Design Resources

[Design Archive](#)

[TINA-TI™](#)

[INA326](#)

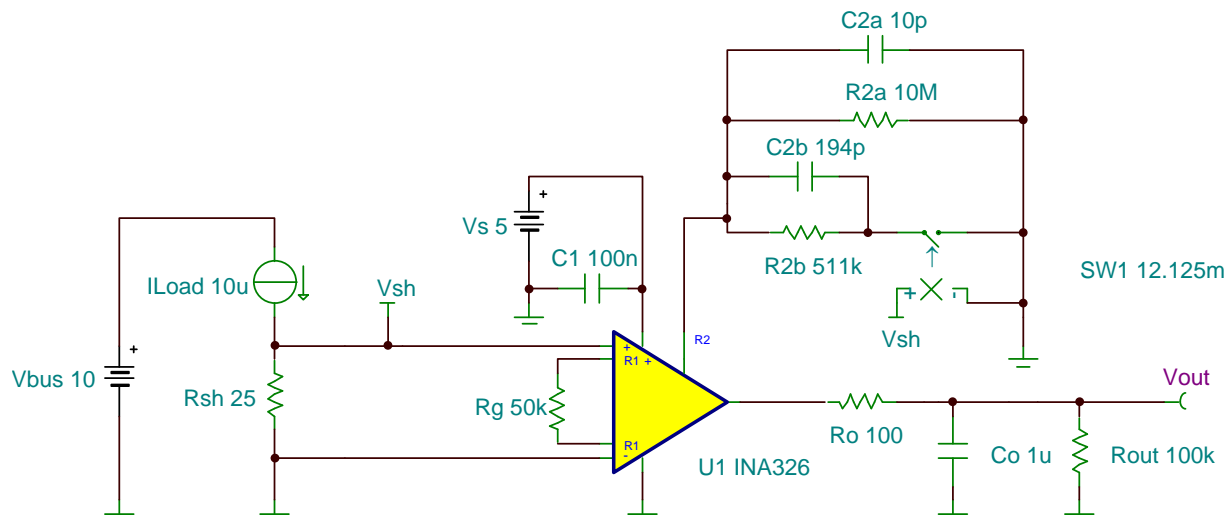
All Design Files  
SPICE Simulator  
Product Folder

### Circuit Description

This single-supply low-side current sensing solution can accurately detect load currents from 10  $\mu$ A to 10 mA. The linear range of the output is from 100 mV to 4.9 V. A unique yet simple gain switching network was implemented in order to accurately measure the three-decade load current range.



[Ask The Analog Experts](#)  
[WEBENCH® Design Center](#)  
[TI Precision Designs Library](#)



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

TINA-TI is a trademark of Texas Instruments.  
WEBENCH is a registered trademark of Texas Instruments.

## 1 Design Summary

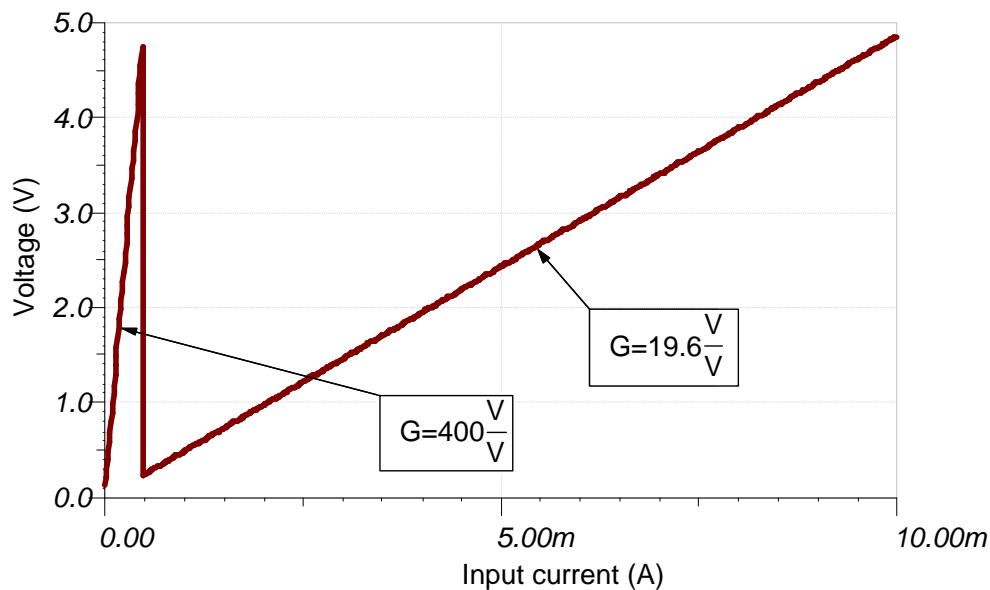
The design requirements are as follows:

- Supply Voltage: 5 V
- Input: 10  $\mu\text{A}$  – 10 mA
- Output: 100 mV – 4.9 V
- Maximum Shunt Voltage: 250 mV

The design goals and performance are summarized in Table 1. Figure 1 depicts the simulated transfer function of the design.

**Table 1. Comparison of Design Goals and Simulated Performance**

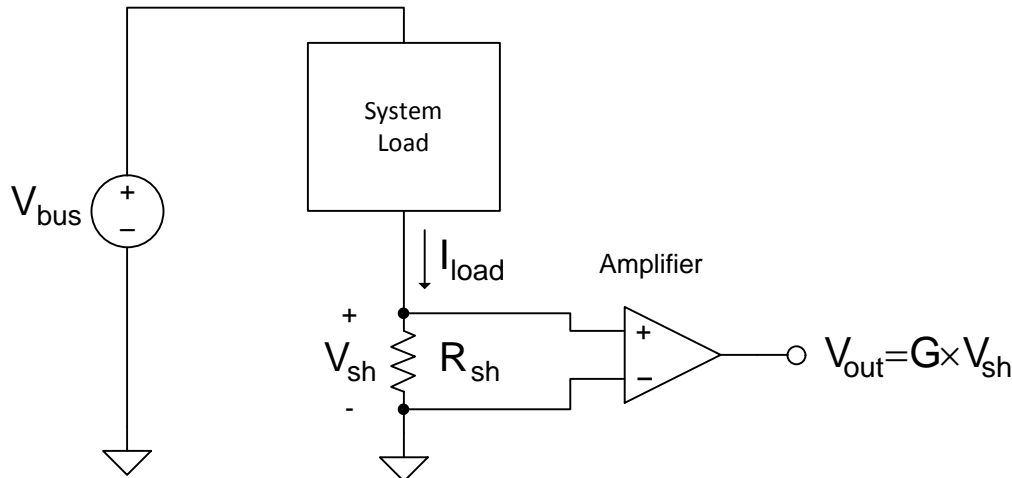
	Goal	Simulated
Error (%FSR <sub>error</sub> )	0.1%	0.088%
Relative Error ( $I_{load}=10 \mu\text{A}$ )	40%	29.6%
Relative Error ( $I_{load}=100 \mu\text{A}$ )	4%	4.04%
Relative Error ( $I_{load}=1 \text{ mA}$ )	0.4%	0.4%



**Figure 1. Simulated Transfer Function**

## 2 Theory of Operation

Low-side sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of bus voltage ( $V_{bus}$ ), which allows for the use of single-supply, rail-to-rail input/output (RRIO) amplifiers. Low-side current sensing places a shunt resistor ( $R_{sh}$ ) between the system load and ground. The current drawn by the load ( $I_{load}$ ) generates a voltage across the shunt resistor ( $V_{sh}$ ) that is proportional to  $R_{sh}$ . As shown in Figure 2, the output voltage ( $V_{out}$ ) of the circuit is equal to the product of  $V_{sh}$  and the gain of the amplifier ( $G$ ).



**Figure 2. Low-Side Current Sensing Topology**

As shown in Figure 2, the value of  $V_{sh}$  is the ground potential for the system load. If the value of  $V_{sh}$  is too large it may cause issues when interfacing with systems whose ground potential is truly 0 V. Therefore it is important to limit the voltage drop across the shunt resistor. Equation 1 can be used to calculate the maximum value of  $R_{sh}$ .

$$R_{sh(max)} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{250mV}{10mA} = 25\Omega \quad (1)$$

It is recommended to use the maximum shunt resistance to minimize relative error at minimum load current. Relative error is discussed in Section 4.3.

The gain(s) required for this design depend on the maximum output swing of the amplifier, shunt resistor, and the load current range. It is recommended to use the maximum gain to ensure full utilization of the linear operating range of the device. Equation 2 shows how to calculate the maximum gain for the maximum load current.

$$G_{load(max)} = \frac{V_{out(max)}}{V_{sh(max)}} = \frac{V_{out(max)}}{R_{sh} \times I_{load(max)}} = \frac{4.9V}{25\Omega \times 10mA} = 19.6 \frac{V}{V} \quad (2)$$

To determine if the design requires more than one gain, the minimum load current that can be measured given  $G_{load(max)}$  and  $V_{out(min)}$  must be calculated as shown in Equation 3 and Equation 4.

$$V_{sh(min)} = \frac{V_{out(min)}}{G_{load(max)}} \quad (3)$$

$$I_{load(min)} = \frac{V_{sh(min)}}{R_{sh}} = \frac{V_{out(min)}}{G_{load(max)} \times R_{sh}} = \frac{100mV}{19.6 \frac{V}{V} \times 25\Omega} = 204.08\mu A \quad (4)$$

Since  $I_{load(min)}$  does not meet the minimum load current specification of 10  $\mu A$ , a second gain is required. It is recommended to now calculate the maximum gain for the minimum load current ( $G_{load(min)}$ ) as shown in Equation 5.

$$G_{load(min)} = \frac{V_{out(min)}}{V_{sh(min)}} = \frac{V_{out(min)}}{R_{sh} \times I_{load(min)}} = \frac{100mV}{25\Omega \times 10\mu A} = 400 \frac{V}{V} \quad (5)$$

Equation 6 and Equation 7 show how to calculate the maximum load current that can be measured given  $G_{\text{load(min)}}$ .

$$V_{\text{sh(max)}} = \frac{V_{\text{out(max)}}}{G_{\text{load(min)}}} \quad (6)$$

$$I_{\text{load(max)}} = \frac{V_{\text{sh(max)}}}{R_{\text{sh}}} = \frac{V_{\text{out(max)}}}{G_{\text{load(min)}} \times R_{\text{sh}}} = \frac{4.9\text{V}}{400 \frac{\text{V}}{\text{V}} \times 25\Omega} = 490\mu\text{A} \quad (7)$$

Since the minimum load current that can be measured when  $G=19.6 \text{ V/V}$  overlaps with the maximum load current for  $G=400 \text{ V/V}$ , only two gains are required to measure the entire load current range.

If more than two gains are required, the design of the switching network may become overly complicated. For such applications it is recommended to investigate the use of alternate topologies and/or devices, such as programmable gain amplifiers (PGAs).

### 3 Component Selection

#### 3.1 Amplifier

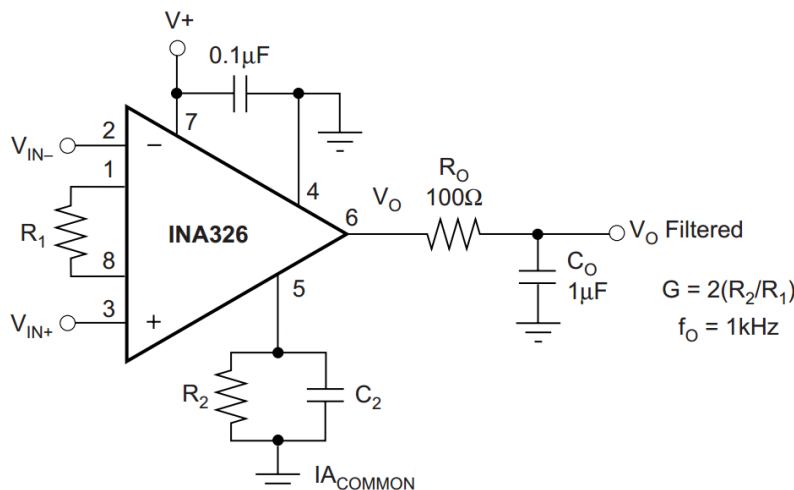
When selecting an amplifier for a low-side current sensing solution it is desirable to have a RRIO device with low offset voltage relative to the minimum value of  $V_{sh}$ . In addition, ensure that the input bias current is insignificant with respect to the load current and that the bandwidth of the device is sufficient for the application. While it is common to utilize op amps in low-side current sensing solutions, error can be introduced due to any parasitic impedance between the shunt resistor and ground. Implementing a low-side current sensing solution using an instrumentation amplifier, however, addresses this issue because the measurement is differential. Most instrumentation amplifiers utilize traditional 3-op amp or 2-op amp architectures. Such architectures typically have input common-mode voltage and output swing limitations that are not suited for low-side current sensing, especially when powered with a single-supply. The INA326, however, utilizes a unique current-mirroring topology that allows for true rail-to-rail input voltage swing even with a single supply. The linear input voltage range of the INA326 is from  $(V_-)-20$  mV to  $(V_+)+100$  mV. The output stage is also considered rail-to-rail for it can swing to within 75 mV of the supplies. The offset voltage is 100  $\mu$ V (max) and the input bias current is  $\pm 2$  nA. If the application is dc, the INA326's 1 kHz of bandwidth is sufficient. Therefore the INA326 is well suited for this application.

#### 3.2 Shunt Resistor

The ideal shunt resistor was calculated in [Equation 1](#) to be 25  $\Omega$ . This value is a standard value and is available with a tolerance of 0.1%. As previously mentioned it is recommended to use the maximum shunt resistor to minimize relative error at minimum load current.

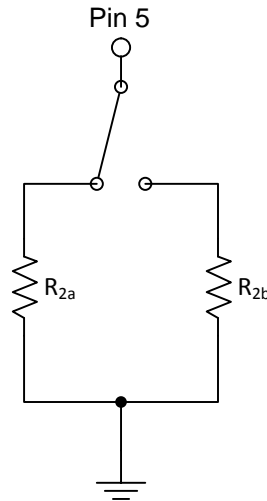
#### 3.3 Gain-Setting Resistors

The INA326 utilizes two resistors ( $R_1$  and  $R_2$ ) to set the gain as shown in [Figure 3](#).



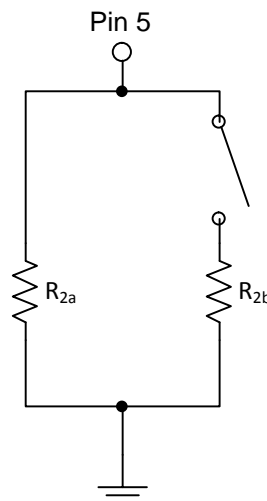
**Figure 3. Setting the Gain of the INA326**

A switch can be used to change the value of either  $R_1$  or  $R_2$ . Since  $R_1$  is connected to pins that are sensitive to parasitic capacitance, this design will change the value of  $R_2$ . One approach to changing the value of  $R_2$  is shown in [Figure 4](#).



**Figure 4. Changing the Gain Using SPDT Switch**

Using a single-pole double-throw (SPDT) switch, however, can cause inaccurate results during the switch's transition time. Therefore an alternate approach that utilizes a single-pole single-throw (SPST) switch was implemented as shown in [Figure 5](#).



**Figure 5. Changing the Gain Using SPST Switch**

This approach ensures that pin 5 of the INA326 is always connected to ground through a known impedance. While the gain calculation for  $R_1$  and  $R_{2a}$  is straightforward, the second gain calculation will utilize the parallel combination of  $R_{2a}$  and  $R_{2b}$ .

Setting  $R_1=50\text{ k}\Omega$  we can calculate the value for  $R_{2a}$  for  $G=400\text{ V/V}$  as shown in [Equation 8](#).

$$R_{2a} = \frac{R_1 \times G}{2} = \frac{50\text{ k}\Omega \times 400 \frac{\text{V}}{\text{V}}}{2} = 10\text{ M}\Omega \quad (8)$$

To calculate the value of  $R_{2b}$  the parallel combination of  $R_{2a}$  and  $R_{2b}$  must be used in the calculation.

$$R_{2a} \parallel R_{2b} = \frac{R_1 \times G}{2} = \frac{50\text{ k}\Omega \times 19.6 \frac{\text{V}}{\text{V}}}{2} = 490\text{ k}\Omega \quad (9)$$

Where

$$R_{2a} \parallel R_{2b} = \frac{R_{2a} \times R_{2b}}{R_{2a} + R_{2b}} = 490\text{k}\Omega \quad (10)$$

Finally,  $R_{2b}$  can be calculated as shown in Equation 11.

$$R_{2b} = \frac{490\text{k}\Omega \times R_{2a}}{R_{2a} - 490\text{k}\Omega} = 515.25\text{k}\Omega \quad (11)$$

Since gain and the value of  $R_2$  are directly related, a standard resistor value less than 515.25 k $\Omega$  must be selected to ensure the maximum gain of 19.6 V/V is not exceeded. Therefore  $R_{2b}$  was selected to be 511 k $\Omega$  and the ideal gain now becomes 19.4463 V/V.

### 3.4 Filtering

The INA326 datasheet values for  $R_o$  and  $C_o$  were used to create a low-pass filter on the output at a -3 dB point of 1.59 kHz.

$$f_{-3\text{dB}} = \frac{1}{2 \times \pi \times R_o \times C_o} = \frac{1}{2 \times \pi \times 100\Omega \times 1\mu\text{F}} = 1.59\text{kHz} \quad (12)$$

Figure 6 shows the gain and filtering network.

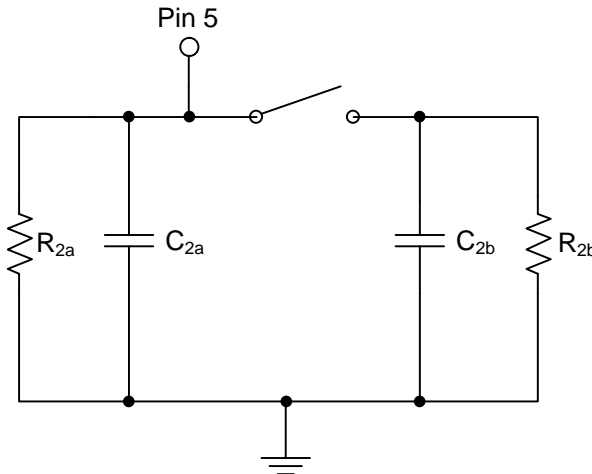


Figure 6. Gain and Filtering Network

When the switch is open,  $C_{2a}$  can be calculated using Equation 13.

$$C_{2a} = \frac{1}{2 \times \pi \times R_{2a} \times f_{-3\text{dB}}} = \frac{1}{2 \times \pi \times 10\text{M}\Omega \times 1.59\text{kHz}} = 10\text{pF} \quad (13)$$

After the switch closes,  $R_{2a}$ ,  $R_{2b}$ ,  $C_{2a}$ , and  $C_{2b}$  will be in parallel. The effective capacitance of  $C_{2a}$  in parallel with  $C_{2b}$  is the sum of the two capacitances. Therefore  $C_{2b}$  can be calculated as shown in Equation 14.

$$C_{2b} = \frac{1}{2 \times \pi \times (R_{2a} \parallel R_{2b}) \times f_{-3\text{dB}}} - C_{2a} = \frac{1}{2 \times \pi \times (10\text{M}\Omega \parallel 511\text{k}\Omega) \times 1.59\text{kHz}} - 10\text{pF} = 196\text{pF} \rightarrow 194\text{pF} \quad (14)$$

The closest standard capacitor value to 196 pF is 194 pF.

### 3.5 Passive Components

The critical passive components for this design are  $R_{sh}$ ,  $R_1$ ,  $R_{2a}$ , and  $R_{2b}$ . In order to meet the design objective of 0.1%  $\text{FSR}_{\text{error}}$ , 0.1% tolerance was selected for these components. Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function or add significant error to this design.

#### 4 Simulation

The TINA-TI™ schematic shown in Figure 7 includes the circuit values obtained in the design process.

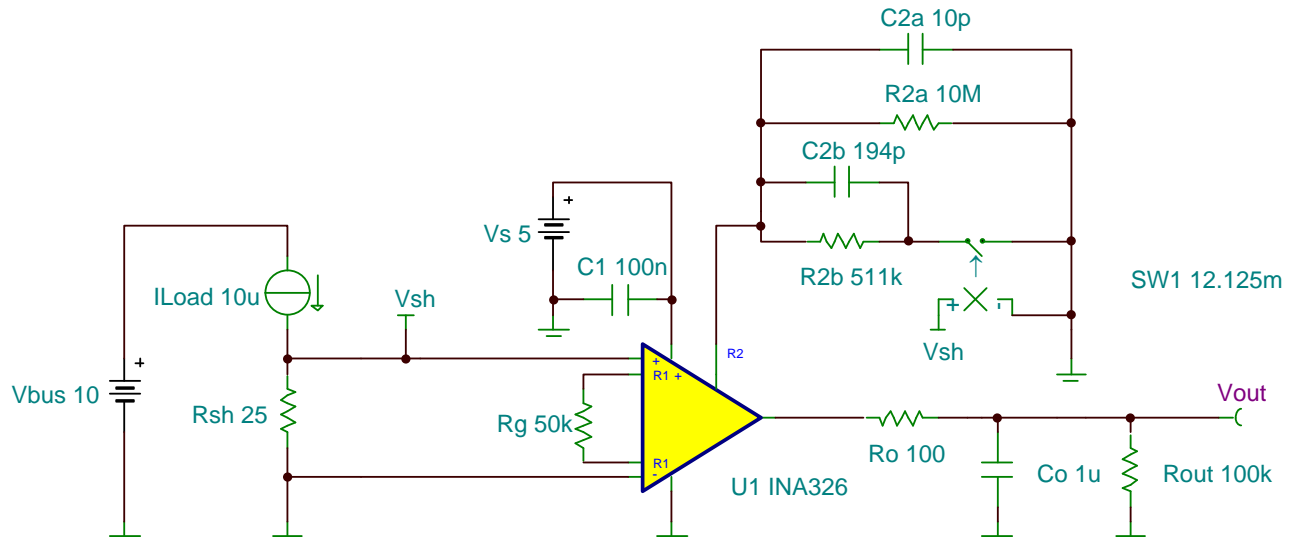


Figure 7. TINA-TI™ Schematic

Notice that a voltage-controlled switch (SW1) was inserted to control the gain of the circuit. By default, the switch is open, which equates to an ideal gain of 400 V/V. The set point of the switch can be calculated as shown in Equation 15. Note that 485 μA was used instead of 490 μA (the maximum load current before the output saturates when G=400 V/V) to allow for design margin and that the set point is referred to the input.

$$V_{SW1} = 485\mu A \times 25\Omega = 12.125mV \tag{15}$$

While an ideal switch was used in this design, it represents a real-world control system. This most likely solution would include measuring  $V_{out}$  using an analog-to-digital converter (ADC) of a microcontroller. Once the threshold is reached, the microcontroller would use a general purpose input/output (GPIO) pin to control the switch. It is recommended to use a switch with low on-resistance ( $R_{on}$ ) so as to preserve accuracy. The [TS5A3166](#) would work well for this application.



### 4.1 Transfer Function

The result of the dc transfer function simulation is shown in [Figure 8](#).

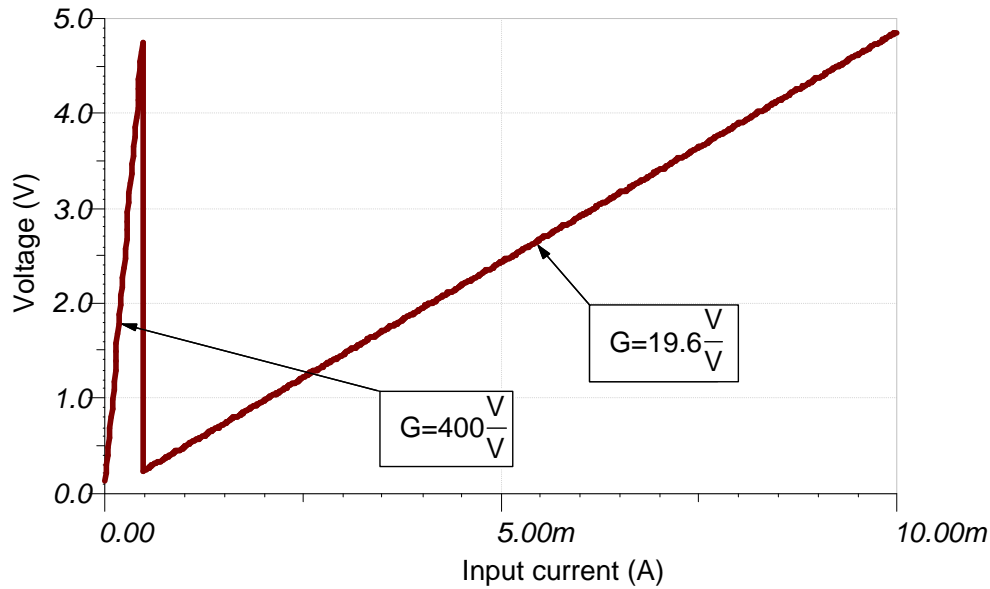


Figure 8. Transfer Function

### 4.2 Frequency Response

The circuit shown in [Figure 9](#) was utilized to perform an ac analysis for each gain of the circuit depending on whether the switch was open or closed. The simulation results are shown in [Figure 10](#).

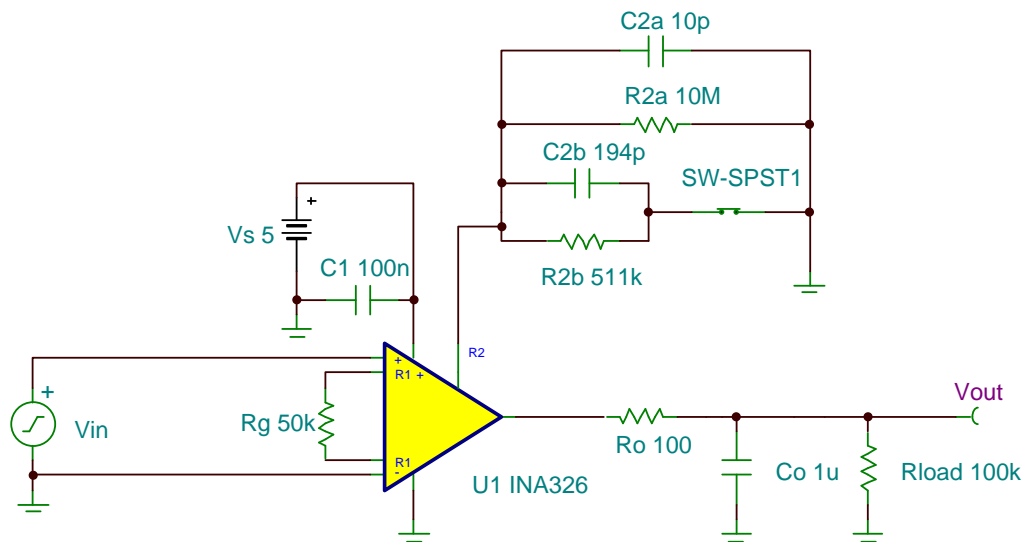
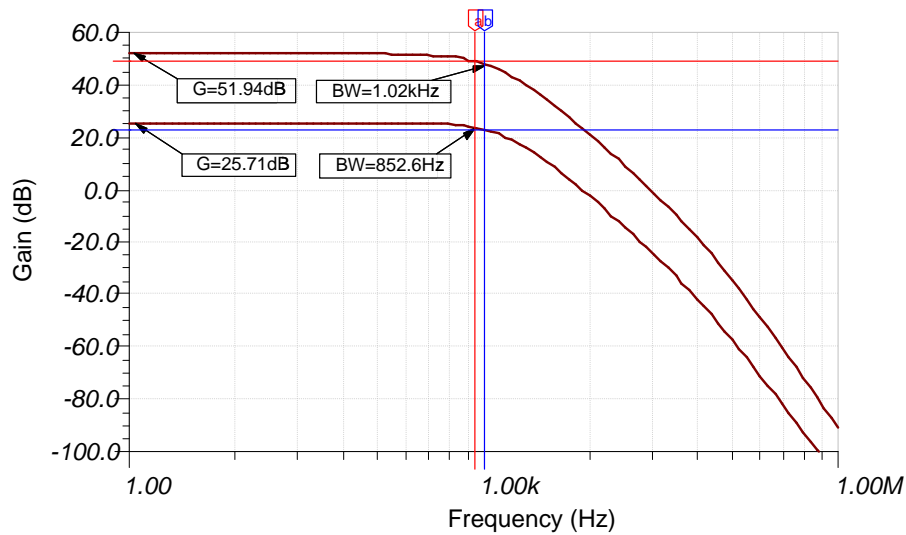


Figure 9. AC Analysis Schematic


**Figure 10. AC Analysis**

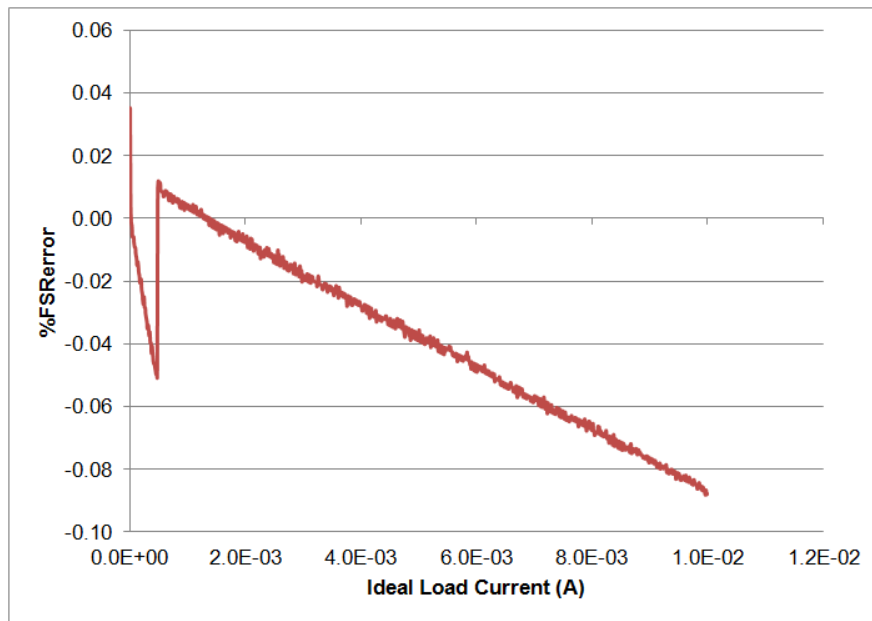
The dc gains of the simulation were found to be 51.94 dB and 25.71 dB, which equate to 395.37 V/V and 19.3 V/V, respectively. The bandwidth of each gain configuration was 852.6 Hz and 1.02 kHz, respectively.

### 4.3 Error Analysis

The data from [Figure 8](#) was exported to a spreadsheet in order to calculate the error as a percent of the full-scale range (%FSR<sub>error</sub>). [Equation 16](#) was used to calculate %FSR<sub>error</sub>.

$$\%FSR_{error} = 100 \times \frac{I_{load(sim)} - I_{load(ideal)}}{I_{load(max)} - I_{load(min)}} = 100 \times \frac{\left[ \frac{V_{out}}{G} \times \frac{1}{25\Omega} \right] - I_{load(ideal)}}{10mA - 10\mu A} = 100 \times \frac{\left[ \frac{V_{out}}{G} \times \frac{1}{25\Omega} \right] - I_{load(ideal)}}{9.99mA} \quad (16)$$

In order to accurately calculate the error, the gain was switched from 400 V/V to 19.4463 V/V once the load current reached 485  $\mu$ A. [Figure 11](#) shows %FSR<sub>error</sub> as a function of ideal load current.



**Figure 11. Full Scale Error**

The maximum %FSR<sub>error</sub> was found to be 0.088%, which meets our design goal of 0.10%.

The error relative to the ideal load current (relative error) was also calculated for each load current decade. Equation 17 shows how to calculate relative error.

$$\%RelError = 100 \times \frac{V_{os(max)}}{V_{sh}} \tag{17}$$

The maximum offset voltage of the INA326 is 100 μV. The maximum relative error for each decade of load current will occur at the minimum load current for each range (10 μA, 100 μA, and 1 mA). For example, the maximum relative error for a load current of 10 μA is calculated in Equation 18.

$$\%RelError_{10\mu A} = 100 \times \frac{V_{os(max)}}{V_{sh}} = 100 \times \frac{100\mu V}{25\Omega \times 10\mu A} = 40\% \tag{18}$$

The maximum relative error for 100 μA and 1 mA can be calculated in a similar manner. Table 3 summarizes the results of the calculations.

Equation 19 calculates the simulated relative error using the data from Figure 8. The output voltage was referred to the input by dividing by the ideal gain (400 V/V or 19.4463 V/V).

$$\%RelError_{sim} = 100 \times \frac{V_{os(max)}}{V_{out}} \times G \tag{19}$$

Table 2 depicts the simulated output voltage at the minimum load current of each range.

**Table 2. Simulated Output Voltage for Various Load Currents**

Load Current	Simulated Output Voltage
10 μA	135.15 mV
100 μA	990.65 mV
1 mA	486.31 mV

The simulated relative error for a load current of 10  $\mu\text{A}$  can be calculated as shown in Equation 20.

$$\% \text{RelError}_{\text{sim-10}\mu\text{A}} = 100 \times \frac{100\mu\text{V}}{135.15\text{mV}} \times 400 \frac{\text{V}}{\text{V}} = 29.6\% \quad (20)$$

The simulated relative error for 100  $\mu\text{A}$  and 1 mA can be calculated in a similar manner. Table 3 summarizes the results of the calculations.

#### 4.4 Simulated Results Summary

Table 3 summarizes the simulated performance of the design.

**Table 3. Comparison of Design Goals and Simulated Performance**

	Goal	Simulated
Error (%FSR <sub>error</sub> )	0.1%	0.088%
Relative Error ( $I_{\text{load}}=10 \mu\text{A}$ )	40%	29.6%
Relative Error ( $I_{\text{load}}=100 \mu\text{A}$ )	4%	4.04%
Relative Error ( $I_{\text{load}}=1 \text{ mA}$ )	0.4%	0.4%

## 5 Modifications

The components selected for this design were based on the design goals outlined at the beginning of the design process. An instrumentation amplifier was selected because the input is differential, which reduces errors due to parasitic impedances associated with the shunt resistor's ground connection. The amplifier's input common-mode range must include ground, which limits our choice of instrumentation amplifiers. One alternative to the INA326 is the INA122. The INA122 is a 2-op amp instrumentation amplifier with a common-mode voltage range that includes V-. Table 4 is a brief comparison of the two instrumentation amplifiers.

**Table 4. Brief Comparison of Instrumentation Amplifiers**

Amplifier	Max Supply Voltage (V)	Max Offset Voltage ( $\mu\text{V}$ )	Max Offset Drift ( $\mu\text{V}/^\circ\text{C}$ )	Quiescent Current ( $\mu\text{A}$ )	Bandwidth (MHz, G=5)
INA326	5.5	100	0.4	3400	0.001
INA122	36	500	5	85	0.12

Traditional op amps are also used for low-side current sensing. They are especially useful for higher-frequency measurements because they can have significantly greater bandwidth than the INA326 and INA122. Table 5 is a brief comparison of op amps that may be considered for low-side current sensing.

**Table 5. Brief Comparison of Op Amps**

Amplifier	Max Supply Voltage (V)	Max Offset Voltage ( $\mu\text{V}$ )	Max Offset Drift ( $\mu\text{V}/^\circ\text{C}$ )	Quiescent Current ( $\mu\text{A}$ )	Bandwidth (MHz)
OPA333	5.5	10	0.05	25	0.35
OPA330	5.5	50	0.25	35	0.35
OPA378	5.5	50	0.25	150	0.90
OPA320	5.5	150	5	1750	20
OPA365	5.5	200	1	5000	50
OPA376	5.5	25	1	950	5.5
OPA188	36	25	0.085	510	2

## 6 About the Author

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments' difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University's Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

## IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.