TAS3202 Data Sheet Errata

This errata document describes corrections to the TAS3202 data sheet, literature number SLES197.

1 Erratum: I²C Data Setup Time Violation

1.1 Problem Description

The TAS3202 slave I²C interface does not meet the minimum set up time for the Data ($t_{SU;DAT}$) of the *I²C Bus Specification* in between payload bytes while transmitting to the I²C Bus master.

Figure 1 shows a view of the time window between any two sequential payload byes of an I²C Read Transaction. The time window where the violation occurs is highlighted in red. Figure 2 shows the same violation in a much smaller time window

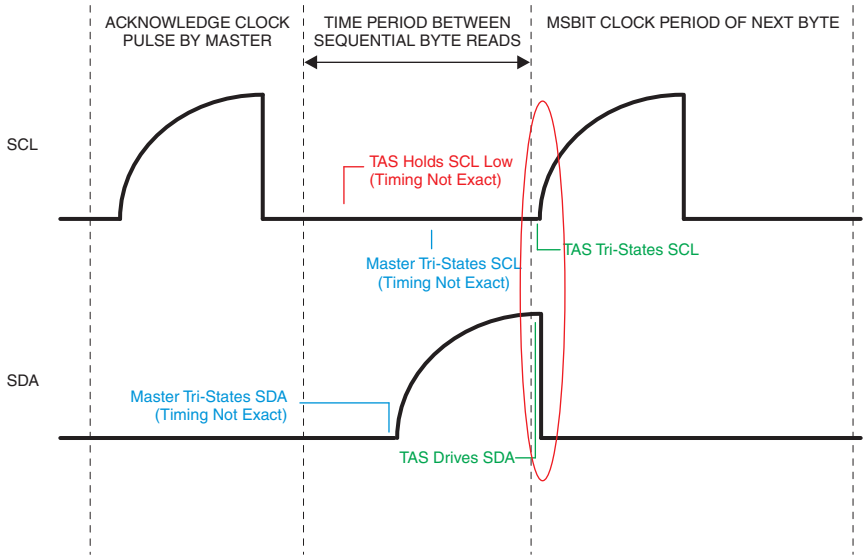

Figure 1. Problem Description: Timing Diagram

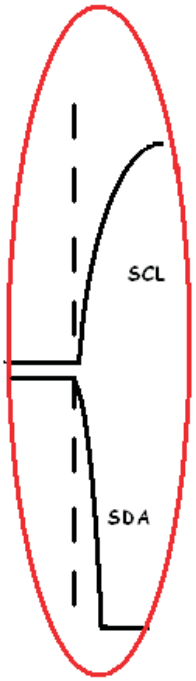

Figure 2. Overlap of Falling SDA/Rising SCL

1.2 System Impact

The rising edge of the Serial Clock (SCL) overlaps with the falling edge of the Serial Data (SDA). This overlap may cause conflicts with other integrated circuits on the same I²C bus, resulting in a hung bus.

1.3 Workarounds

Two possible workarounds for this errata have been identified: I²C Master Serial Clock Holdoff and I²C Bus Isolation.

1.3.1 I²C Master Serial Clock Holdoff

The I²C bus Master may insert an artificial clock stretch (hold SCL at logic 0) between every sequential set of the nine SCL clock pulses (for each byte) for a fixed time period of no less than $\frac{1}{2f_{SCL}}$ + 250 ns immediately after the falling edge of the 'Acknowledge' clock pulse.

This clock stretch by the master results in added time for the SDA to be driven low by the TAS3202 before the I²C bus sees the rising edge of the serial clock to meet the minimum $t_{SU;DAT}$ specification

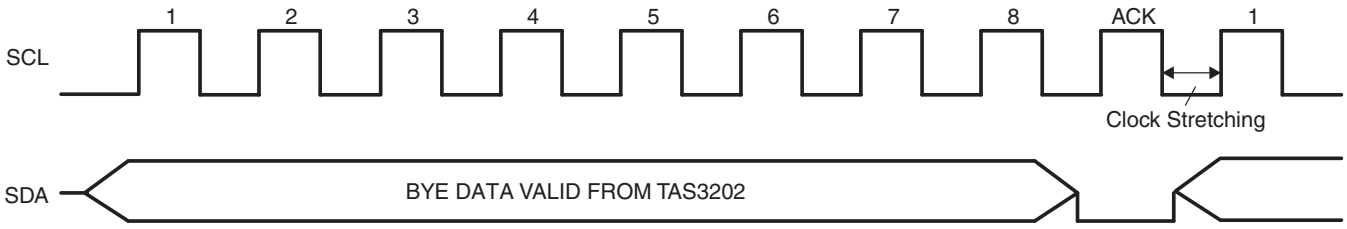

Figure 3. Clock Stretch Period by I²C Master

1.3.2 I²C Bus Isolation

The TAS3202PAG may be the only slave device placed on any given I²C Bus to prevent bus conflicts with other devices in the system

2 Erratum: ADC Multiplexer Polarity Inversion

2.1 Problem Description

The TAS3202 Analog-to-Digital Converter Multiplexer inverts the polarity of the selected analog differential pair.

2.2 System Impact

The positive/negative analog output differential pair will be a polarity flipped version of the input.

2.3 Workarounds

Two possible workarounds for this erratum have been identified: PCB Signal Swap and External Polarity Correction.

2.3.1 PCB Signal Swap

The corresponding AIN+/- differential signals can be swapped on the Printed Circuit Board.

2.3.2 External Polarity Correction

The analog signals may be reversed external to the device through an inverting amplifier.

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