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Interface Circuits for TIA/EIA-644 (LVDS)

Design Notes

September 2002

Mixed-Signal Products

SLLA038B

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Interface Circuits for TIA/EIA-644 (LVDS)

ABSTRACT

This design note provides information concerning the designing of TIA/EIA-644 interface circuits. The TIA/EIA-644 standard is discussed including electrical characteristics, interconnections, line termination, and noise immunity. Finally, eye patterns are used to measure the effects of signal distortion, noise, signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system.

General Information

TIA/EIA-644, otherwise known as LVDS, is a signaling method used for high-speed, low-power transmission of binary data over copper. This signaling technique uses lower output-voltage levels than the 5-V differential standards (such as TIA/EIA-422) to reduce power consumption, increase switching speed, and allow operation with a 3.3-V supply rail. The LVDS current-mode drivers create a differential voltage (247 mV to 454 mV) across a 100-Ω load. The LVDS receivers detect signals as low as ±100 mV with as much as ±1-V ground noise. TI offers LVDS receivers capable of recovering data over a common mode range from –4 V to 5 V, which allows up to 3 V of ground noise. These receivers are designated SN65LVDS33 and SN65LVDS34. The standard specifies a theoretical maximum of 1.923 Gbit/s.

The intended application of this signaling technique is for baseband data transmission over controlled impedance media of approximately 100 Ω, where the transmission media may be printed-circuit board (PCB) traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling from the environment.

Figure 1 shows a typical connection with LVDS drivers and receivers. The data inputs to the quad driver are received at the interface of the PCB traces from the host controller. The data inputs consist of up to n+1 bits of information and a transmit (Tx) clock. The data and clock signals are then transmitted differentially to the interface of the quad driver outputs, to the interconnecting traces, and to the host PCB connector. The signals then propagate from the interface of the host PCB connector to the cable connector to the balanced interconnecting media. At the plug on the other end of the cable, the signals pass through the cable plug, the target connector interface, and then to the target PCB traces. The LVDS signal path ends at the interface of the target PCB traces and the termination circuit. An additional interface is located at the points where the PCB traces to the quad receiver inputs are connected. The outputs of the receiver interface to the target PCB traces and then on to the receiving controller.

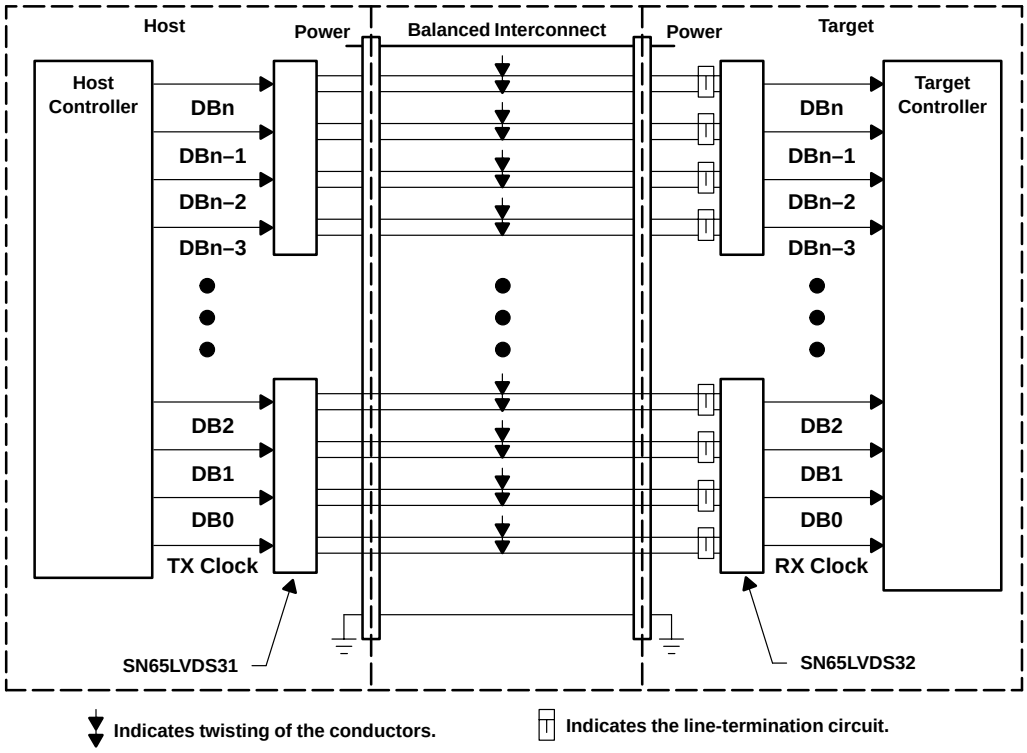


Figure 1. Typical Connection With LVDS Drivers and Receivers

Electrical Characteristics

Driver

The LVDS driver produces a differential voltage across a 100-Ω load in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground (see Figure 2). Most drivers are commonly implemented as current-mode devices, which allow power consumption to be virtually independent of frequency. These two characteristics, low voltage swings and constant current, allow LVDS drivers to operate at higher data rates and lower power dissipation.

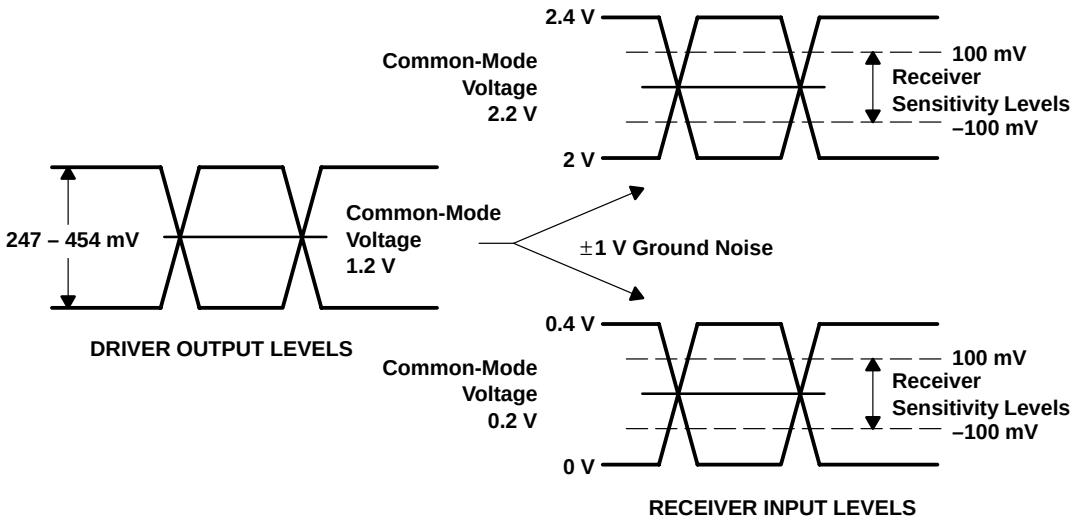
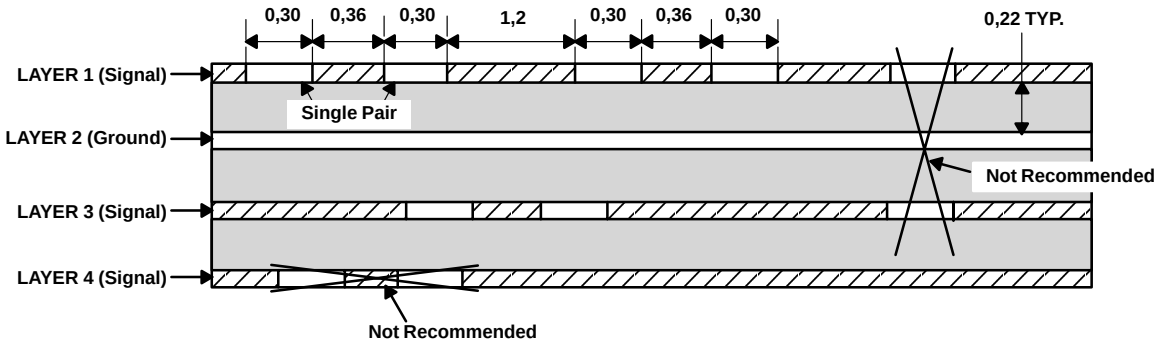


Figure 2. Driver and Receiver Electrical Characteristics

Unused Pins — Unused data input pins to the LVDS driver should be left open circuited, with the exception of the enabling pins. All inputs to the LVDS driver are internally pulled down to ground with approximately 300-kΩ resistance. If the enable pins are not driven, they can be connected directly to V_{CC} or GND. If there is a need for a pullup or pulldown resistor, then a resistance of no more than 10 kΩ is recommended.

Board Traces — All board traces from the host controller to the driver and from the driver to the connector should be as short as possible and matched in length. The overall length of any trace between the controller and driver should be kept to less than 5 cm and the lengths of all the traces to the controller should be matched to within 1 cm of each other with a 4-mA output buffer on the controller. Longer lengths are possible with higher current output buffers. The length of each trace between the driver outputs and the connector should be matched to within 5 mm of each other. Usually, this requires mitering the traces. If the PCB trace is more than 2 cm in length between the driver output pins and the connector, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω (see Figure 3).



NOTES: A. All fabrication items must meet or exceed best industry practice.
B. Laminate material: copper-clad FR-4
C. Copper weight: 1 oz. start
D. Finished board thickness: 0.032 (±0.010) inch
E. Dielectric thickness to be symmetrical between all layers (±0.005 inch)
F. Maximum warp and twist: 0.001 inch per inch
G. Circuitry on outer layers to be tin-lead plated (60/40), plated to 300 µin (minimum)
H. Soldermask both sides per artwork: green enthone
I. Copper plating to be 0.001 inch (minimum) in plated-through holes
J. Soldermask over bare copper with tin-lead hot-air leveling
K. Dimensions are shown in millimeters

Figure 3. Typical PCB Construction

Receiver

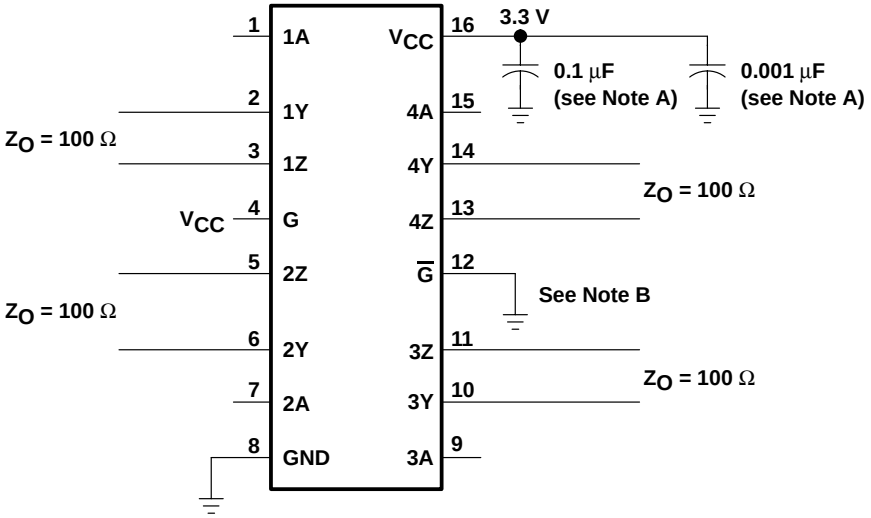
The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.05 V to 2.35 V. The receiver has a sensitivity level of ±100 mV to correctly assume the intended binary state (see Figure 2). The LVDS interconnecting media must be matched with the 100-Ω termination resistor located at the inputs of the receiver. Please see the *Line Termination* section of this document.

Unused Pins — The receiver data input pins should be left open if not being used. The receiver has a fail-safe feature that takes the outputs to a known state when the receiver inputs are left open (more on the fail-safe feature later in this document). The enable pins must be actively driven or connected directly to V_{CC} or GND through no more than a 10-kΩ resistance. There is no internal pullup or pulldown or resistance provided at the enable pins.

Board Traces — All board traces from the connector to the receiver and from the receiver to the controller should be as short as possible and matched in length. The length of each trace between the connector and the receiver input should be matched to within 5 mm of each other; this may require mitering the traces. If the distance between the connector and the receiver input pins is more than 2 cm, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω (see Figure 3). No run between the receiver outputs and the receiving controller should be more than 5 cm long, and runs should not be more than 1 cm from each other.

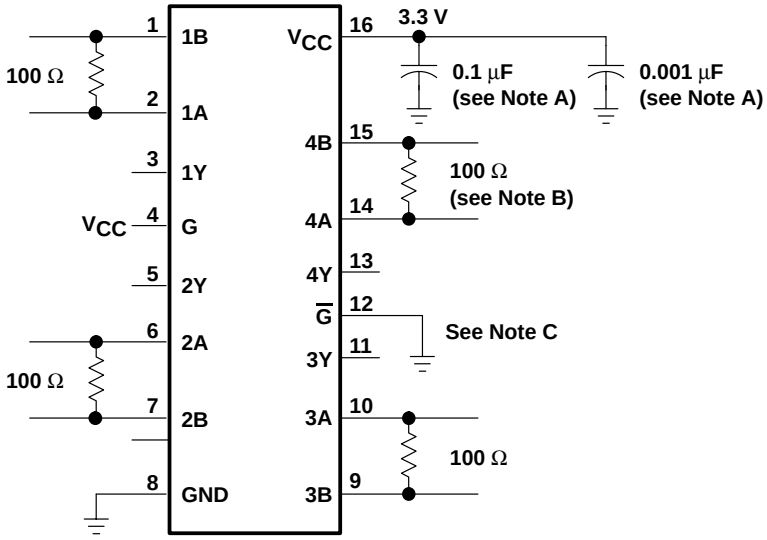
Supply Voltage

Since the standard does not specify power-supply voltages and the driver output characteristics are independent of power supply, the supply voltage may be 5 V, 3.3 V or even lower. It is recommended that two Z5U ceramic, mica, or polystyrene dielectric chip capacitors be placed between V_{CC} and the ground plane for the driver and the receiver. The capacitor should be as close as possible to the device pin. Refer to Figure 4 and Figure 5.



NOTES: A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 4. Typical Application Circuit Schematic for the SN65LVDS31 and SN65LVDS3487 Driver



NOTES: A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 5. Typical Application Circuit Schematic for the SN65LVDS32 and SN65LVDS3486 Receiver

A ground plane is highly recommended, if not mandatory. A power plane is recommended, but if not used, sharing of supply traces with other components should be held to a minimum. A power or ground plane can further reduce possible feedback at very high data rates if used to separate input signal traces and output signal traces.

Interconnections

Configurations

Point-to-point is the most common configuration for LVDS since signal quality is superior and it is the easiest to implement (see Figure 6).

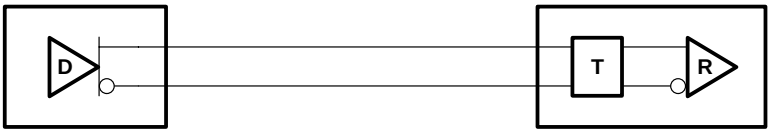


Figure 6. Point-to-Point Configuration

Multidrop configuration is attainable with LVDS, but many things must be taken into consideration, such as the stub length, the location of the receivers, and the terminating resistor. In a multidrop configuration, the stub lengths must be as short as possible and the terminating resistor must be connected only at the receiver located on the furthest end of the interconnect (see Figure 7).

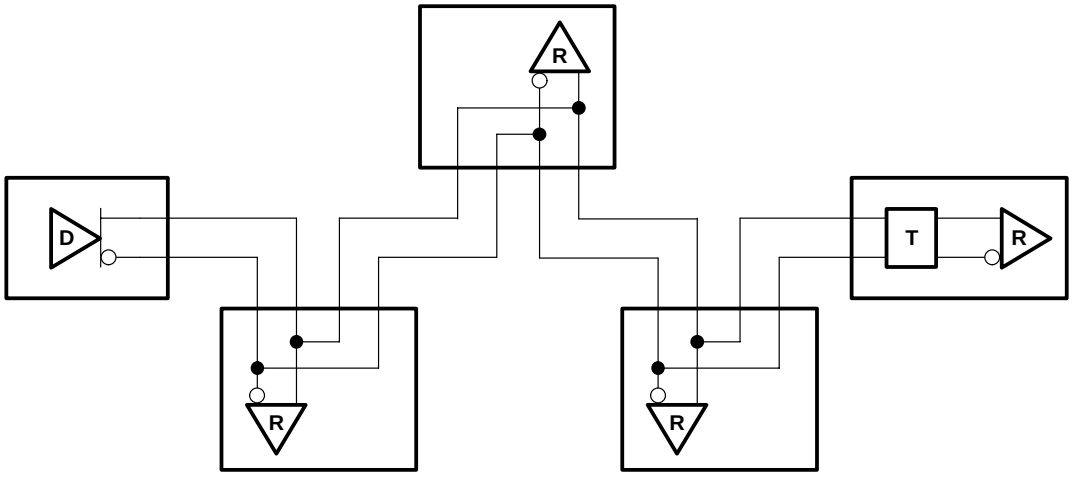


Figure 7. Multidrop Configuration

NOTE: Multipoint configuration can be achieved in LVDS with M-LVDS devices. TIA/EIA-644 interface circuits do not support a multipoint configuration, where more than one driver resides on a bus segment. These buses require the use of M-LVDS as specified in TIA/EIA-899.

Characteristic Impedance of Media

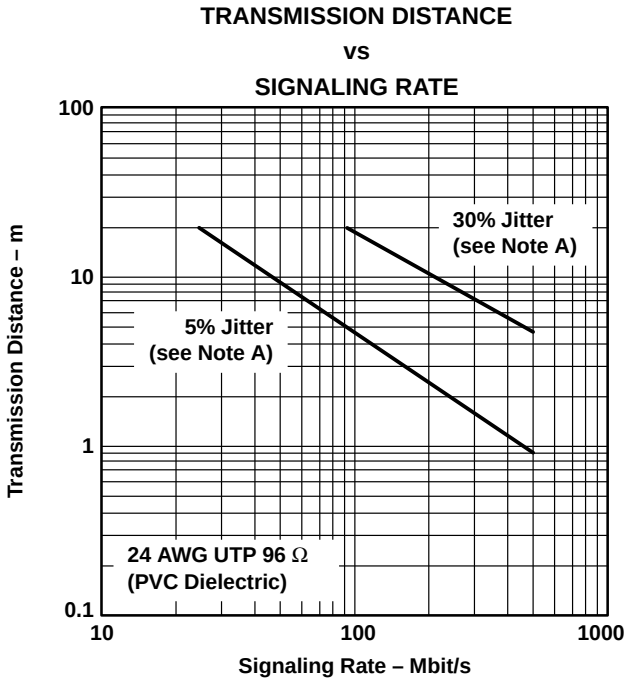
The balanced interconnecting media of LVDS is not specified in the standard and therefore may be PCB traces, backplanes, or cables. At any cut point in the interconnect, the differential characteristic impedance must be 90 Ω to 132 Ω.

For cables, it is recommended to use polyethylene, polypropylene, or Teflon™ insulation in either round or flat cables and uniform distance between the conductors in a signal pair. Belden #9807 is an example of round cable and Belden #9V28010 is an example of flat cable. The twisting of the signal pairs is recommended but not mandatory.

Transmission Distance vs Signaling Rates

LVDS surpasses the signaling rates of existing standards like TIA/EIA-422, -485 and -232. To attain high speed, LVDS uses very low voltage swings, typically 350 mV. This low voltage swing allows data to be switched very quickly at signaling rates up to 1.923 Gbit/s. Excluding very short distances, the restriction of the maximum signaling rate is the transmission media.

Figure 8 shows a typical plot of the transmission distance vs. signaling rates. The simplest way to determine the affects of random noise, jitter, attenuation, and dispersion on a transmission line is with the use of eye patterns. Eye patterns are useful in measuring the amount of jitter versus the unit interval to establish the data-rate versus cable-length curves. The *Eye Patterns* section of this document explains how to use eye patterns.



NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 8. Typical Transmission Distance vs Signaling Rates

Teflon is a trademark of E.I. Du Pont.

Line Termination

Termination at the far end of the interconnect from the transmitter is mandatory. The termination resistor should be located within 2 cm of the LVDS receiver. Choose a termination resistor that best matches the differential impedance of the transmission line; ideally, it would be between 90 Ω to 132 Ω . A thick-film leadless (0603 or 0805) chip resistor is recommended. The termination schematic diagram is shown in Figure 8.

Texas Instruments also offers LVDS receivers with integrated termination. The devices designated by LVDT (T denotes termination) offer an integrated termination on the receiver inputs. They have improved signal quality and lower bit error rates because the integrated termination is closer to the receivers inputs than what is possible with discrete solutions. In addition, the integrated termination feature allows designers to save board space by eliminating the need for a terminating resistor.

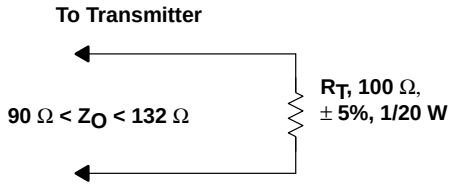


Figure 9. Differential Termination

Skew, Balance, and ISI

Skew in differential signaling is the phase difference between the signals. Skew can be reduced by matching the electrical lengths between traces and using a good quality manufactured cable. The propagation delay difference between signal pairs in good quality manufactured cables can range from 40 ps/m to 120 ps/m (specified by the vendor). A lower number is better.

To keep the transmission media balanced, the distance and insulation between the signal and return conductors in a pair should be uniform, and any parasitic loading (capacitance) must be applied in equal amounts to each line.

Intersymbol interference (ISI) in a data transmission system is the effect of neighboring pulses in a pulse train spilling over into adjacent pulses. This forces a reduction in the allowable permitted pulse rate for a given line length in order to maintain adequate distinction between adjacent pulses. To determine the effects of signal distortion, noise, and signal attenuation on ISI in a data transmission system, the eye pattern is used. The eye pattern is obtained by applying a random nonreturn-to-zero (NRZ) code down the transmission line under test. In LVDS, the maximum recommended cable length for non-encoded NRZ signaling is when the 10%-to-90% rise time of the signal at the termination is $t_R < \frac{t_{ui}}{2}$. For information on how to set up eye patterns refer to the *Eye Patterns* section of this document.

Noise Immunity

Fail-Safe Operation

One of the most common problems with differential signaling applications is how the system responds when the differential input voltage is between –100 mV and 100 mV within its input common-mode voltage, meaning there is little or no differential voltage present at the signal pair. This situation occurs when there is little or no input current to the receiver from the data line itself, known as an open circuit. This is due to the driver being in a high-impedance state or the cable being disconnected. The output logic state of most differential receivers is indeterminate when this condition exists.

TI's LVDS receivers handle the open-input circuit situation differently. For example, when the system is in open-circuit, the SN65LVDS32 receiver pulls each line of the signal pair to a high-level (near V_{CC}), through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage threshold at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage. It is under this condition that the output of the SN65LVDS32 is forced high with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 10. Other termination schemes may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

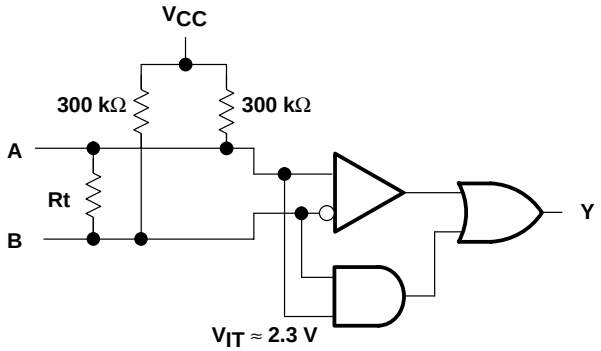


Figure 10. Open-Circuit Fail Safe of the LVDS Receiver

Radiated Emissions and Susceptibility

LVDS uses differential signaling, which is less susceptible to noise than single-ended transmission. A differential transmission involves using two signal-carrying wires between the driver and the receiver. Any noise induced on one of the lines is also induced on the other. The receiver is concerned only with the difference between these two signals. Therefore, noise coupled onto the two wires appears as common-mode noise and is rejected by the receiver.

LVDS low-voltage signaling and differential data-transmission scheme reduces electromagnetic interference (EMI). Since LVDS uses low-voltage signaling, the switching currents are much lower than CMOS/TTL and there is less radiation of EMI. Of greater importance, the balanced differential lines have equal but opposite currents, so most of the concentric magnetic field lines tend to cancel and most of the electric fields tend to couple.

To further reduce EMI it is suggested that the signal traces be as close to each other as possible and matched in length. Furthermore, only one path should exist for return current between the host controller and the target controller PCBs.

Shielding also is an effective way to reduce EMI. If an overall shield is desired, use a short pigtail crimped to the shield end at each connector and then brought through a separate connector pin to a ground, located as close to the connector as possible. If individual shielding of the signal pairs is needed, use the same terminating technique as for the overall shield.

To reduce noise, unused pins in connectors as well as unused wires in cables should be single-point grounded at the connector. Unused wires should be grounded at alternate ends. Galvanic isolation is another technique used to reduce noise in interface systems. Galvanic isolation is provided by means of optocoupler/optoisolators. For LVDS applications, the use of any optocoupler reduces the bandwidth and, therefore, the corresponding maximum data rate.

Electrostatic Discharge

Like many electronic parts, LVDS is sensitive to electrostatic discharge (ESD) and some precautions must be taken when handling them. To avoid ESD, it is advisable that exposed connectors have pins recessed from the shell to prevent casual contact and discharges. It also is a good idea to have the ground pins longer than the signal pins in order to make the ground connection first and equalize the ground potentials before signal connections.

Eye Patterns

To measure the effects of signal distortion, noise, and signal attenuation, and the resultant intersymbol interference (ISI) in a data transmission system, the eye pattern is used. ISI is the effect of neighboring pulses in a pulse train interfering with preceding or succeeding pulses. It forces a reduction in the signaling rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope, with the term *eye* coming from the appearance of the trace on the CRT.

Setting Up the Eye Pattern

The eye pattern is obtained by applying a pseudo-random nonreturn-to-zero (NRZ) code down the transmission line under test. This represents nearly all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the scope triggered using the synchronization clock to the NRZ code generator on a separate trace (see Figure 11).

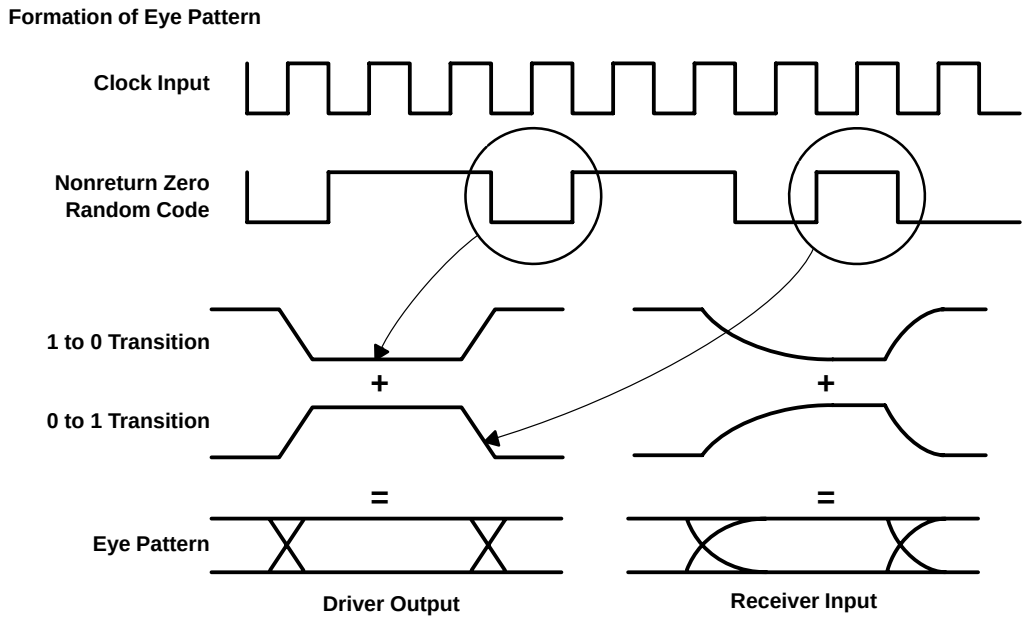


Figure 11. Signal Distortion Using Eye Patterns

Over any one unit interval, the pseudo-random code generator should produce a combination of signals. The resulting signals then can be viewed on the oscilloscope over a one-unit interval; each unit interval should resemble an eye similar to that shown in Figure 12. For differential transmission, both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

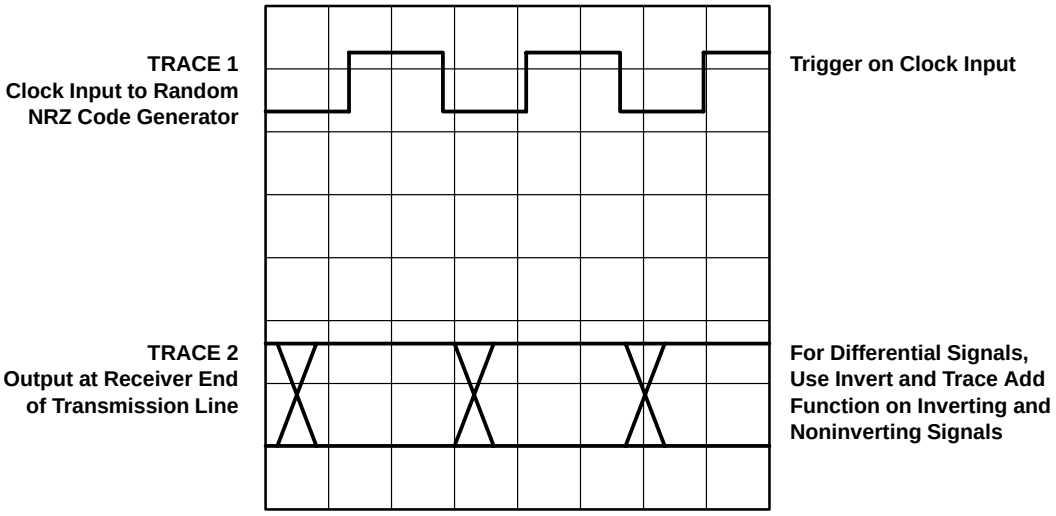
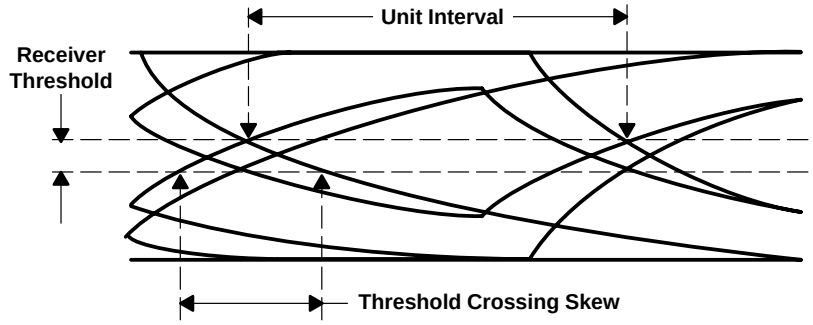


Figure 12. Eye Pattern Oscilloscope Trace

Taking Measurements From Eye Patterns

Before considering actual measurements, the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The openness of the eye is an indication of the quality of the transmitted signal and an indication of the noise and distortion tolerance of the system.

For actual measurements, the decision points of the transceiver should be superimposed on the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum time jitter of the system. The maximum allowable jitter is dependent on the timing accuracy of the receiving circuitry. A conservative guide used by cable manufacturers to determine signaling rate versus line-length curves is no more than 5% jitter. Where percent jitter is defined as the ratio of threshold crossing skew to unit interval as shown in Figure 13. Jitter is caused by a number of factors, including signal frequency, noise, and crosstalk. Noise frequency can modulate the transmitted signal, for example 50-Hz hum or noise from other low-frequency sources. It also should be noted that threshold misalignment can cause severe problems with the received signal, reducing the detected pulse width considerably.



$$\text{\% Jitter} = \frac{\text{Threshold Crossing Skew}}{\text{Unit Interval}} \times 100\%$$

Figure 13. Measuring Signal Transmission Quality

References

1. Introduction to M-LVDS (TIA/EIA-899), literature number SLLA108
2. Performance of LVDS With Different Cables, literature number SLLA053
3. Low-Voltage Differential Signaling (LVDS) Design Notes, literature number SLLA014