Capturing 1394 Events on the Twisted-Pair Lines

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ABSTRACT

This application report gives step-by-step guidelines for capturing events on the twisted-pair lines in an IEEE Standard 1394 system. It provides lab setup and capture information. The captured plots allow the customer to identify and illustrate 1394 signaling events on the twisted-pair lines and debug hardware problems on the cable termination.

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Introduction

The physical layer (PHY) generates all IEEE Standard 1394 (1394) bus-signaling events. The PHY operates between the link and the external interface, and comprises both digital and analog signals. The digital portion of the PHY is an I/O connected to the link. On the analog portion, there are a predetermined number of ports on each PHY. Each cable port incorporates two differential line transceivers. The transceivers include circuitry that monitors the line conditions needed to determine connection status, initialization and arbitration, and packet reception and transmission. The PHY provides cycle timing functions and communicates the packet to and from the link layer.

Setup Configuration

TI recommends a two-node network, one used as a transmitter and the other as an echo server. The echo server node echoes all received data to the transmitter node. To capture a good signal, the monitoring equipment is connected to the signal lines through a header that can be installed on the PHY-connector interface, or directly on the cable wires. A scope with sufficient bandwidth is required to capture a good plot. TI recommends using a 4-channel scope with 1-GHz bandwidth on each channel. Given the high frequency and low voltage of the signals, the high bandwidth helps verify timings on events such as bit periods on 400-Mbps signals.

One way to capture cable signals is to bring them out to a test card as shown in Figure 1. This test card, an extension of the cable, brings the signals on etch and enables headers to be installed for probe attachment. Figure 1 shows the final setup.

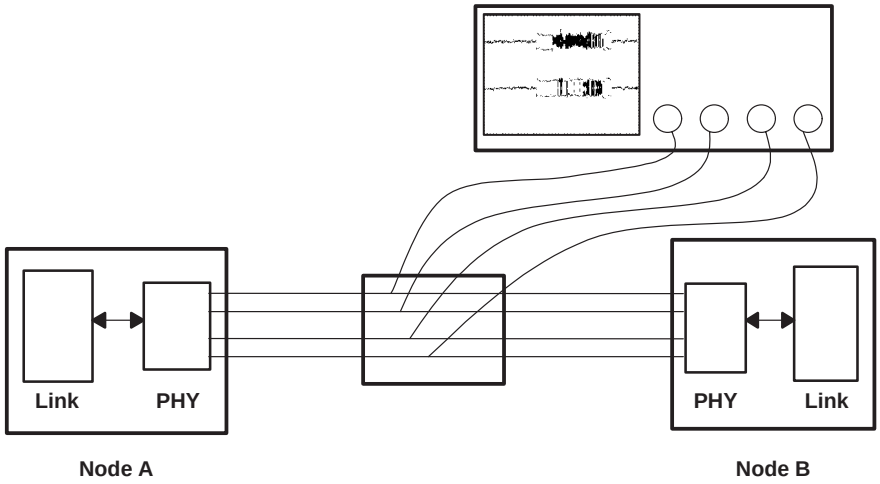

Figure 1. Final Setup

The 1394 signals have a bias voltage of 1.86 V. To capture these plots, the signals must have an offset of 1.86 V.

Table 1 shows the initial scope settings. When an event is captured, the user can change the settings depending on the event they capture.

Table 1. Initial Scope Settings

Channel X vertical scale	200 mV/ Div
Channel X horizontal Scale	1 Gs/s
Channel offset	1.86 V
Trigger setting(dependent on event)	1.86 V

Cycle Start

Figure 2 shows a capture of cycle-start packets. The cycle-start packet is sent out by the cycle master. These cycle-start packets occur every 125 μsec and indicate the beginning of an isochronous (ISO) cycle. Asynchronous (ASYNC) data, unlike ISO data, is not dependent on cycle start. The cycle-start packet notifies all nodes on the network that they should start arbitrating for the bus if they have any ISO data to transmit. This packet is a quadlet payload packet with special values that can be interpreted as a write request to the CYCLE TIME register. The packet-specific information field of this packet type specifies the destination offset for the request. The packet-specific quadlet-data field specifies the data quadlet to be written as a result of this request.

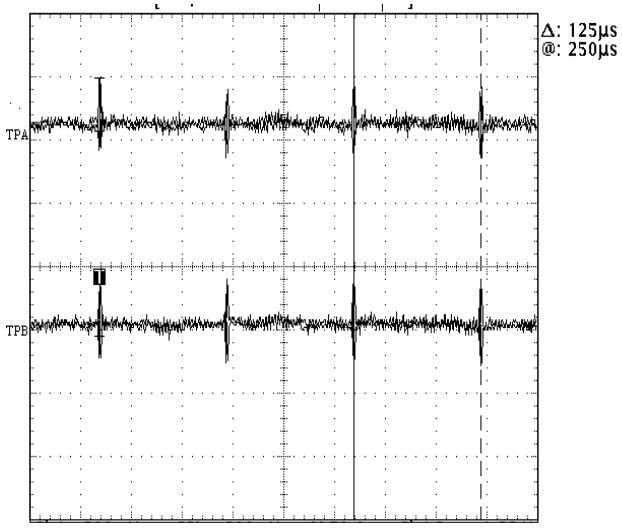

Figure 2. Cycle Start

Figure 3 shows a closeup view of the cycle-start packet. It is transmitted at the base rate of 100 Mbps, thus there are no speed signals. Even when ISO data at speeds of s200 and s400 are transmitted, the cycle-start packets maintain their s100 speed. To capture this on the scope, power up both boards, issue a bus reset, and set the trigger around 1.86 V on any of the 4 channels.

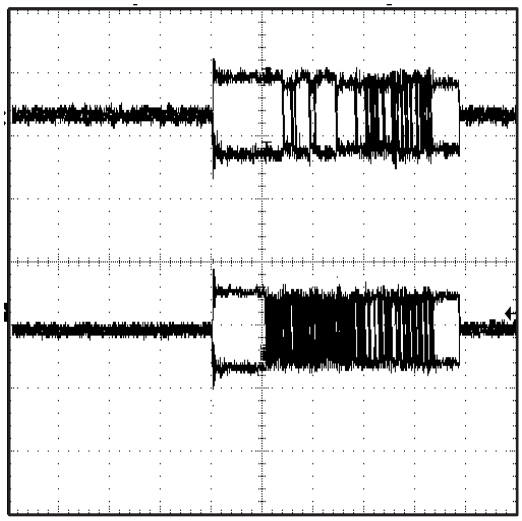

Figure 3. Cycle-Start Packet Closeup View

Bus Reset

Figure 4 shows a plot capture of a bus reset. This lasts for approximately 166 µs depending on the bus topology. During the bus reset both TP lines are driving; this causes a double high, which is easily seen in the plots. Following the bus reset, the cycle start packets continue every 125 µs.

Figure 4. Bus Reset

Figure 5 shows the end of the bus-reset, tree-ID, and self-ID process. On each twisted pair, a voltage drop occurs in the signals. This drop is the s400 speed signal. If a s200 PHY is used, a drop of a lesser magnitude is seen. For PHY of speed s100, the speed signal voltage has a value of 0 and is not identifiable.

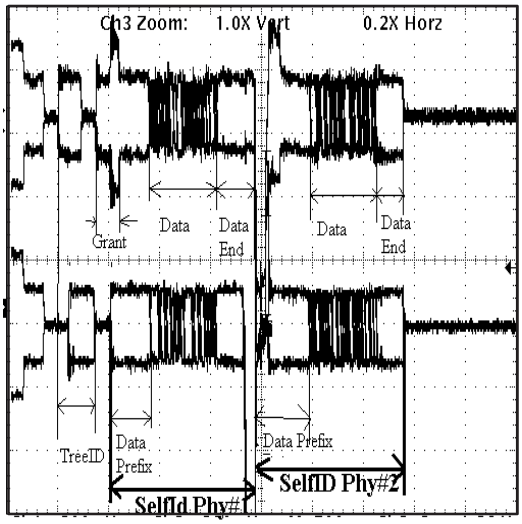

Figure 5. End-of-Bus Reset, Tree-ID, and Self-ID Process

Figure 6 shows the end of the bus reset. During the bus-reset process, both TP lines are driving to produce a double high at the end of the reset; one line stops driving before the other, so the reset comes down to a single high from a double high and eventually to the Hi-Z state. This indicates the end of the bus reset. After a short period of Hi-Z state, a single high occurs on the TP lines. This is the tree-ID process; here the two PHYs talk to each other and determine which is the parent and which is the child node.

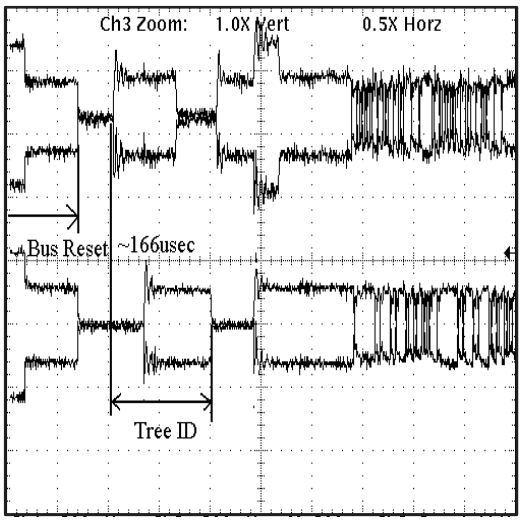

Figure 6. End-of-Bus Reset

Figure 7 shows the complete self-ID process. The plot shows the self-ID packet sent by the first PHY, the handshake between the two PHYs. During this handshake, the TP lines swing low; this is the speed signal. Following the speed signal, the second PHY self-ID packet occurs. All of this is determined immediately following a bus reset.

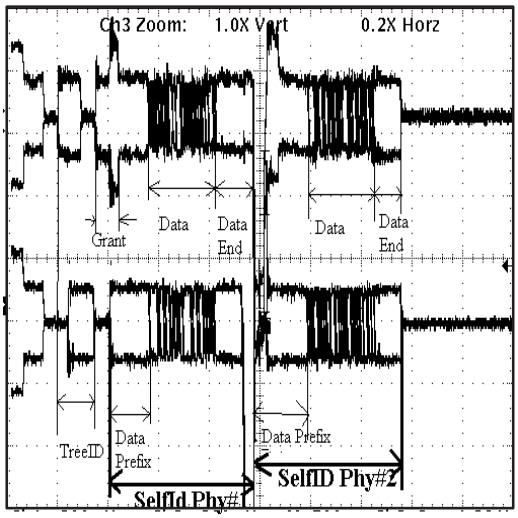

Figure 7. Self-ID Process

Figure 8 shows a closeup of the self-ID packet sent by the first PHY. Following the tree ID, the nodes go through a grant state during which the nodes on the network decide which specific node has been granted the bud—thus becoming the root node.

Following the grant, the first self-ID packet occurs. The self-ID packet is composed of three blocks: data prefix, data, and data end. The timings of the date prefix and grant overlap for a short interval, during which both lines are driving, causing a double high. This is seen in the TP lines of the root node.

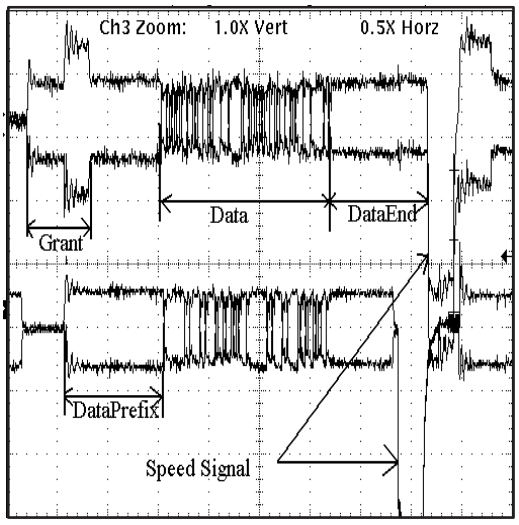

Figure 8. Self-ID Packet

Following the data end in Figure 9, a handshake occurs that is called the speed-signal exchange. The speed-signal exchange is where the PHY communicates with the other PHY on the node and decides their respective maximum speeds. In this case, both are of s400, thus 400 Mbps is the maximum speed at which they can communicate. If a s200 PHY is connected to a s400 PHY, during the speed-signal exchange they determine that for a valid transmission the s400 PHY must transmit no faster than the s200 PHY for the s200 device to receive the data.

In a system with an s200 link layer and an s400 PHY, the link layer can not transmit or receive s400 data; the PHY is limited to acting as a repeater when it receives any s400 data.

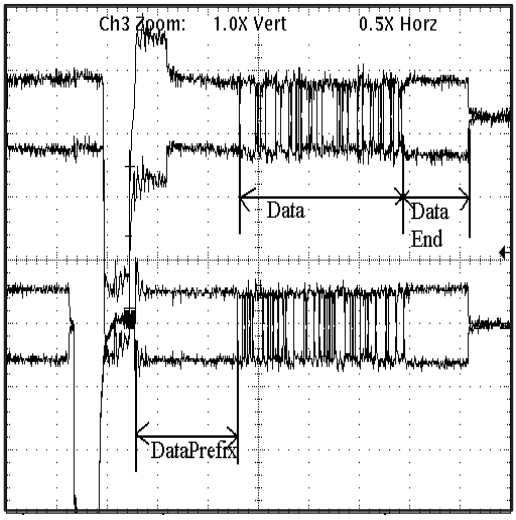

Figure 9. Speed Signal Exchange

In the 1394 standards, the number of self-ID packets transmitted by a PHY is dependent on the number of ports on the device. Per the standards, a PHY with 1–3 port PHYs has one self-ID packet; 4–11 port PHYs have two self-ID packets; 12–19 port PHYs have three self-ID packets and 20–27port PHYs have four self-ID packets. Currently the maximum ports available on a PHY is a six-port s400.

Figure 10 shows a capture of the self-ID packets that are transmitted by a six-port PHY. The six-port devices fall within the boundary of the 4–11 port devices, delivering two self-ID packets. As before, each self ID consists of the data prefix, data, and data end.

In Figure 10, the data prefix follows the speed-signal exchange. Following the data prefix is the data. This makes up the first self-ID packet. Then, instead of a data end as was the case with the three-port PHYs, there is another data prefix, then the data, and the data end. This makes up the second self-ID packet.

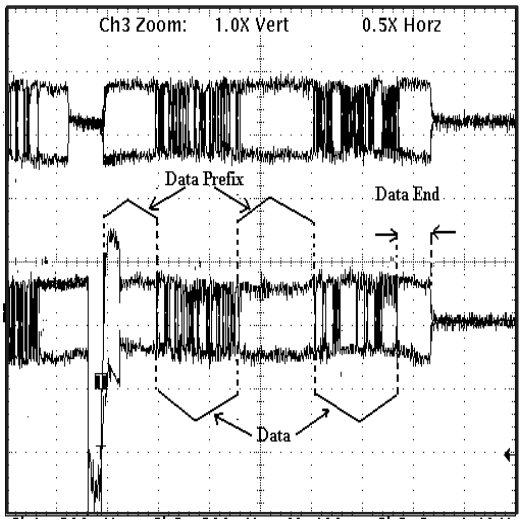

Figure 10. Self-ID Packets for a Six-Port PHY

Data Transfer – ASYNC and ISO

In 1394 there are two types of data transfer: ASYNC and ISO. ASYNC ensures delivery through an acknowledgement exchange. In ASYNC transfer, when the data is sent addressed to a specific node, the node responds back with an acknowledge (ACK) packet indicating that it has received the data.

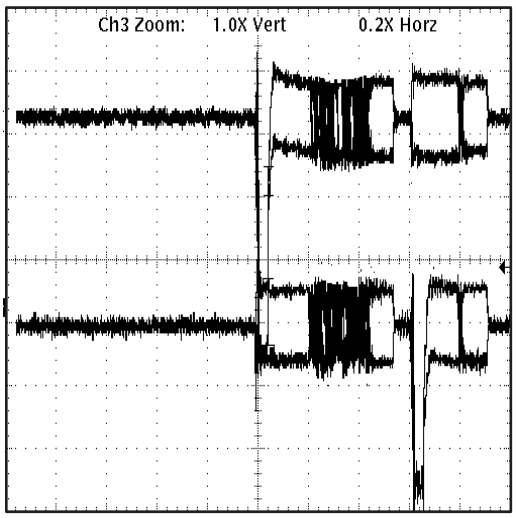

Figure 11. ASYNC Packet

Figure 11 shows an example of an ASYNC packet on the TP lines. The long speed signal on the TPA line shows it is transmitting at 400 Mbps. On the second set of TP lines, the speed signal occurs again; this is the ACK signal that is sent back by the second PHY. The ACK notifies the first node that the second node has received the ASYNC packet.

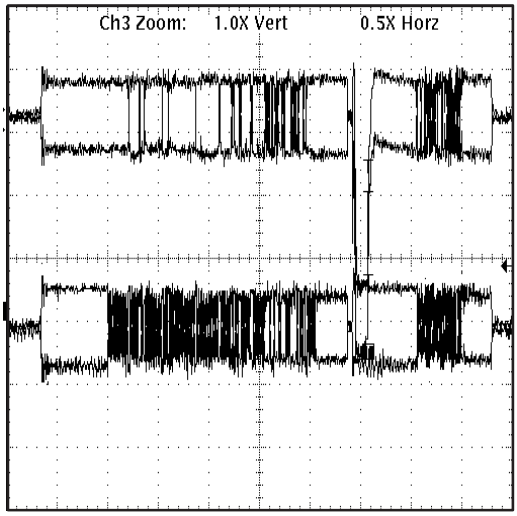

Figure 12. ISO Packet

Figure 12 shows an ISO packet on the twisted-pair lines. ISO data transfer ensures the bandwidth on the bus. On a typical 1394 bus, 80% of the available bandwidth is allocated to ISO and the rest to ASYNC. The ISO data is sent immediately following the cycle-start packet. In an ISO transmission there is no acknowledgment by the receiving node.

The captured plot shows that a packet is sent as s400 following the cycle-start packet. But unlike the ASYNC packets, there is no speed signal on the other twisted line. This indicates that there is no ACK (acknowledge) being sent back to the other node. The first node receives the data, the other node sees the data coming into it, but never sends an acknowledge back.

In a situation where the second node does not receive the data, the first node will never know about it and will keep transmitting; this results in dropped packets.

Reference

1. IEEE Std 1394–1995
   P1394a Draft 2.0

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