Application Report

eUSB2 Repeater Design Guide

ABSTRACT

This document provides information on the Embedded Universal Serial Bus 2.0 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, as well as schematic and layout guidelines for designing an eUSB2 repeater application.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction to the Embedded USB2 (eUSB2) Physical Layer Supplement

The embedded USB2 (eUSB2) Physical Layer Supplement to the USB 2.0 Specification was created to address the need for a low voltage, power efficient USB 2.0 Phy solution. It eliminates the need for 3.3-V IO signaling in small process technologies. eUSB2 is capable of supporting USB high-speed, full-speed, and low-speed operation, as well as the USB 2.0 L1/L2 link power management requirements. In addition, eUSB2 requires no change to the existing USB 2.0 software programming model. eUSB2 applications can be implemented in native mode or repeater mode as described below. This document focus on eUSB2 applications that use repeater mode.

- **Native mode** is used for permanent chip-to-chip communications with direct eUSB2 signal connections which can support long trace lengths. Standard USB 2.0 hosts or devices cannot directly connect to a native eUSB2 application.

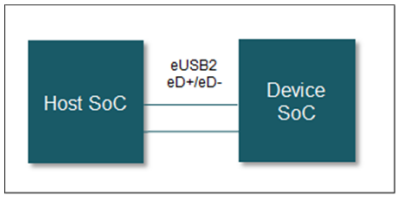

Figure 1-1. eUSB2 Native Mode Use Case

- **Repeater mode** enables chips implementing eUSB2 to connect to standard USB hosts or devices through a separate eUSB2 repeater. An eUSB2 repeater can also be routed to external connectors for complete traditional USB 2.0 interoperability.

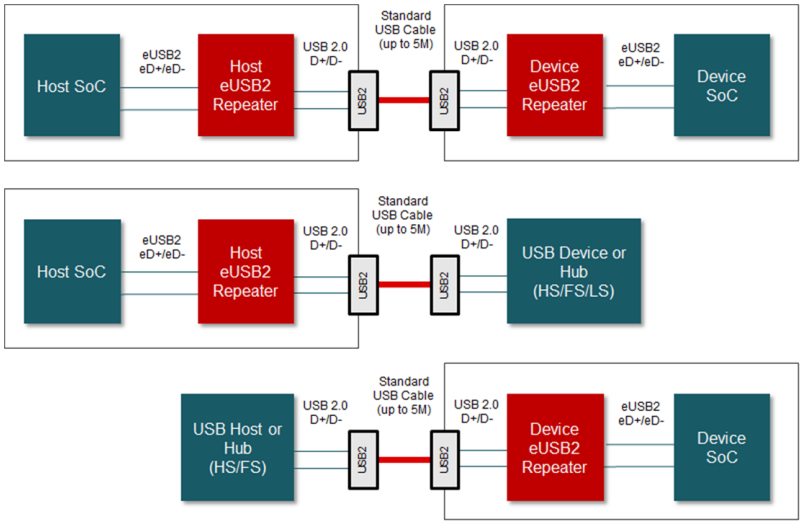

Figure 1-2. eUSB2 Repeater Mode Use Cases

2 eUSB2 Electrical Specifications

While designing an eUSB2 repeater application has many similarities to a USB 2.0 application, there are some notable differences. Instead of the 3.3-V differential signaling used for USB 2.0 full-speed and low-speed applications, eUSB2 uses 1.2-V or 1.0-V supply voltage (VCC) single-ended signaling. In addition, in eUSB2 high-speed the differential signaling has low swing (200 mV nominal); about half that of USB 2.0 high-speed signaling.

To support the low differential voltage swing, the eUSB2 SoC transmitter and the eUSB2 repeater transmitter (eUSB2 side only) must be source series terminated for good signal integrity. The source impedance mismatch on the eUSB2 transmitter is also limited to 4 Ω to prevent common-mode voltage variation. This mismatch can come from process variation or layout. In addition, an eUSB2 repeater application is required to have its eUSB2 receiver differentially terminated to minimize jitter in the system.

Due to the much lower IO voltage, there are also strict requirements in the eUSB2 Supplement around system power to reduce common-mode noise.

- VCC of two connected eUSB2 applications (SoC and repeater) must be within (15%) of each other at all times.
- GND of two connected eUSB2 applications (SoC and repeater) must be within (4%) of each other at all times.

Another difference from USB 2.0 is that the transmit impedance for eUSB2 is 40 Ω with a differential termination impedance of 80 Ω, instead of the 45-Ω and 90-Ω impedances respectively required by USB 2.0. To enable easier routing on PCBs with both eUSB2 and USB 2.0 traces, the recommended trace differential impedance for a eUSB2 design (native or repeater) is 85 Ω. Table 2-1 and Table 2-1 outline the various eUSB2 and USB 2.0 impedance requirements.

Table 2-1. Electrical Specifications From the eUSB2 Physical Layer Supplement

Parameter	Min	Typical	Max	Units
eUSB2 transmit source termination impedance	32	40	48	Ω
eUSB2 differential receiver termination (repeater mode)	72	80	88	Ω
eUSB2 trace differential impedance		85		Ω
eUSB2 trace differential impedance tolerance			15	%

Table 2-2. Electrical Specifications From the USB 2.0 Specification

Parameter	Min	Typical	Max	Units
USB 2.0 trace differential impedance		90		Ω
USB 2.0 trace differential impedance tolerance			15	%

3 eUSB2 Trace Routing

Similar to USB 2.0, eUSB2 data lines, eD+ and eD–, should be routed as a pair with differential impedance over a solid reference plane to provide a good return path for current. The nominal circuit board trace length for eUSB2 connections is 10 inches. This provides more routing flexibility than other similar low-voltage inter-chip interfaces.

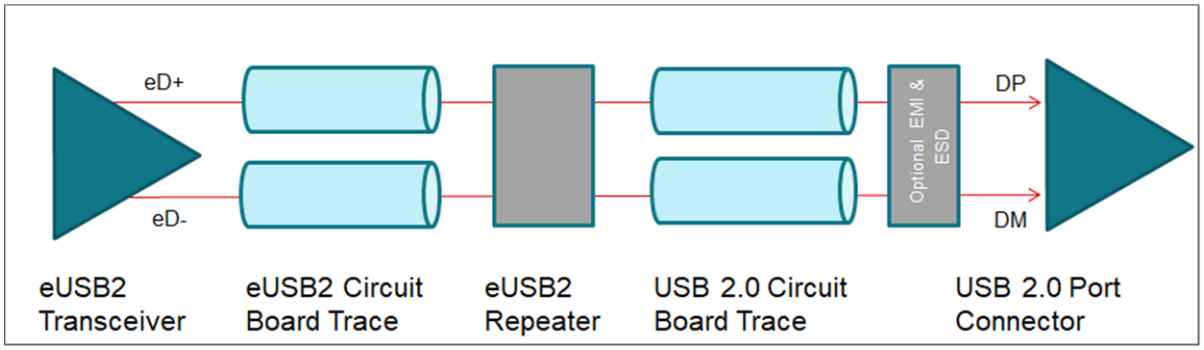

Figure 3-1. Repeater Mode Channel Topology

As previously noted, when routing the eUSB2 data lines, eD+ and eD–, as a differential pair the recommended trace differential impedance is 85 Ω. This allows for matching within the maximum 15% variation to the eUSB2 transmitter and the eUSB2 receiver, while also allowing the same impedance to be used for any USB 2.0 differential traces on the same eUSB2 repeater, simplifying the routing and fabrication.

The eUSB2 data lines can be routed as microstrips over a solid reference plane or as striplines on an inner layer. Routing the eUSB2 data signal pair as microstrips allows for direct routing with no vias in the path, and is the preferred solution if a direct routing path with 5 W distances (5 times the width of the eUSB2 data line trace) from possible noisy signals can be maintained.

A stripline approach will reduce the impact of system noise on the differential lines and allow for better impedance control of the traces; however it does add at least two sets of vias into the signal path that can act as discontinuities. The impact of vias can be minimized by keeping routing symmetric, adding ground vias nearby to act as returns paths and adjusting the anti-pad to control parasitic impedance. Via stub lengths have minimal impact at eUSB2 signaling speeds.

For both stripline or microstrip implementations, the eUSB2 data line traces should be kept as short as possible and routed over a solid reference plane, preferably a ground plane.

4 Matched Trace Length and Skew for eUSB2

In eUSB2, intra-pair skew can result in distortion to a single-ended 1 (SE1) line state that can result in false bus conditions seen at the eUSB2 repeater. While the eUSB2 repeater implements mechanisms to help filter these conditions, eUSB2 differential traces lengths should be matched to help minimize this skew. The transmit differential skew of the eUSB2 data lines should not exceed 500 ps.

Assuming a maximum budget of 270 ps skew for the driver and a guard band of 160 ps, that leaves a budget of up to 70 ps of interconnect skew. Referencing the AC specifications from the eUSB2 Physical Layer Supplement in Table 4-1 and using typical propagation delay numbers for a microstrip in FR4 of 150 ps/in (a stripline of 180 ps/in), it is recommend to keep skew to less than one tenth of the fastest possible rise time, so ideally the maximum routing skew would be 10 ps or 66 mils (55 mils). TI recommends that eUSB2 traces be matched within 50 mils using serpentine routing if necessary.

Table 4-1. eUSB2 AC Specifications

Parameter	Min	Typ	Max	Units
High-speed transmit rise and fall time (20%-80%)(1) (3)	100			ps
Full-speed / low-speed transmit rise and fall time (10%-90%)(4)	2		6	ns
Transmit rise/fall mismatch (1) (2)			25	%

(1) Defined under an ideal 80-Ω RX differential termination with maximum supply voltage variation.
(2) Rise/fall mismatch = absolute delta of (rise-fall time) / (average of rise and fall time).
(3) This parameter is informative, not normative.
(4) Measured with 2.5-pF test load at eUSB2 device or eUSB2 repeater end and assuming 10-inch channel trace in between eUSB2 Host and eUSB2 repeater or eUSB device.

5 PCB Stackup for eUSB2 Applications

Since eUSB2 supports the same maximum signaling speed as USB 2.0 at 480 Mbps, the PCB stackup requirements are similar. To maintain signal integrity and reduce EMI, a 4-layer PCB or greater is recommended. FR4 is a suitable and affordable material for both eUSB2 and USB 2.0 PCBs with low insertion loss at the Nyquist frequency of 240 MHz of less than 0.1 dB per inch.

Figure 5-1 shows an example PCB stackup with trace routing on layer 1, ground on layer 2, power on layer 3 and trace routing on layer 4. This stack-up assumes eUSB2 and USB differential microstrip routing on the outer layers.

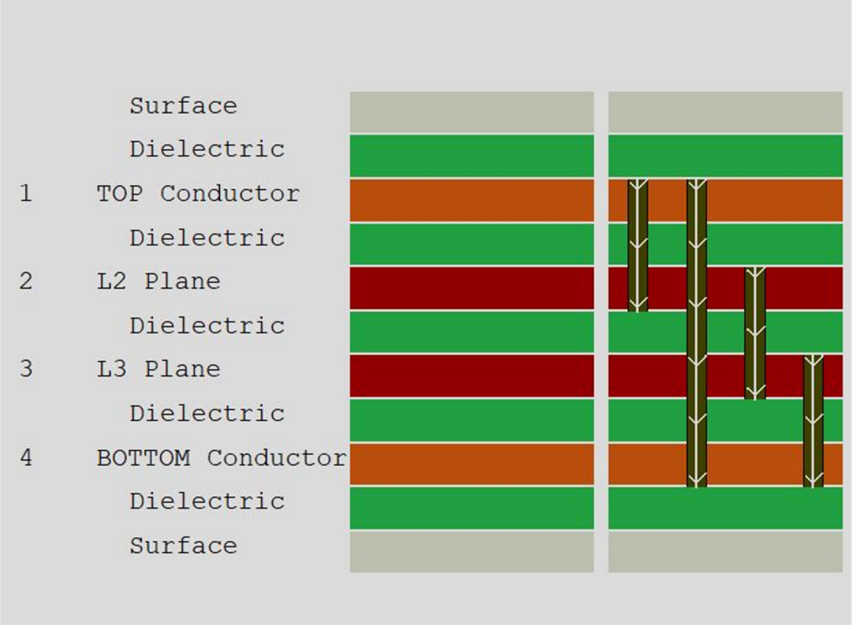

Figure 5-1. Sample 4-Layer PCB Stackup

Referencing the channel specifications from *Table 7-6* in the eUSB2 Physical Layer Supplement, duplicated in Table 5-1, FR4 is adequate for most eUSB2 applications.

Table 5-1. eUSB2 Channel Specification (Informative)

Parameter	Max	Units
Host-to-repeater insertion loss(1) (2)	–1.2	dB
Repeater-to-connector insertion loss	–2	dB

(1) The number is specified at 240 MHz frequency.
(2) See Figure 3-1: *Repeater Mode Channel Topology* for the topology setup.

6 Environmental Concerns and eUSB2

Since eUSB2 is intended as an interchip protocol, ESD (Electrostatic Discharge) protection devices are not recommended on the eUSB2 lines since no exposed connections are expected. eUSB2 repeaters and eUSB2 SoCs should have integrated ESD protections sufficient for most designs. Likewise, EMI (Electromagnetic Interference) protection devices such as common-mode chokes and ferrite beads are not recommend on the eUSB2 lines since they will negatively impact signal quality on the low voltage signal.

For EMC (Electromagnetic Compatibility), ferrite beads can be used to isolate the power to the eUSB2 devices and eUSB2 repeaters and any cable shields terminated to ground should include a capacitor option to decouple the chassis or cable ground and signal ground.

7 References

- *Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification,* Revision 1.1., July 24, 2019
- *Universal Serial Bus Specification*, Revision 2.0, April 27, 2000.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265