Application Note

Using THVD80x0 Devices to Communicate on Lower Voltage (<=36V) AC Power Lines

Parker Dodson

ABSTRACT

The THVD80x0 Family of TI's PowerBus Transceivers can be used to transmit Modulated RS-485 Signals on the same line as a power signal – eliminating the need for separate cables for power and data. The primary design focuses on DC power applications – however with slight modifications to the standard DC power system approach, the THVD80x0 Family of devices can be used in low voltage (<=36 V) applications and lower frequency (<=60 Hz). This document explains the modifications and motivations behind these changes so that the THVD80x0 can be adapted to these types of systems.

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Trademarks

1 Standard THVD80x0 Design Process and Assumptions

The standard architecture of a Power Bus application is shown in Figure 1-1. Please note that the termination resistor between A and B is not shown but is a recommended and common addition to help mitigate potential EMI/EMC issues due to reflections.

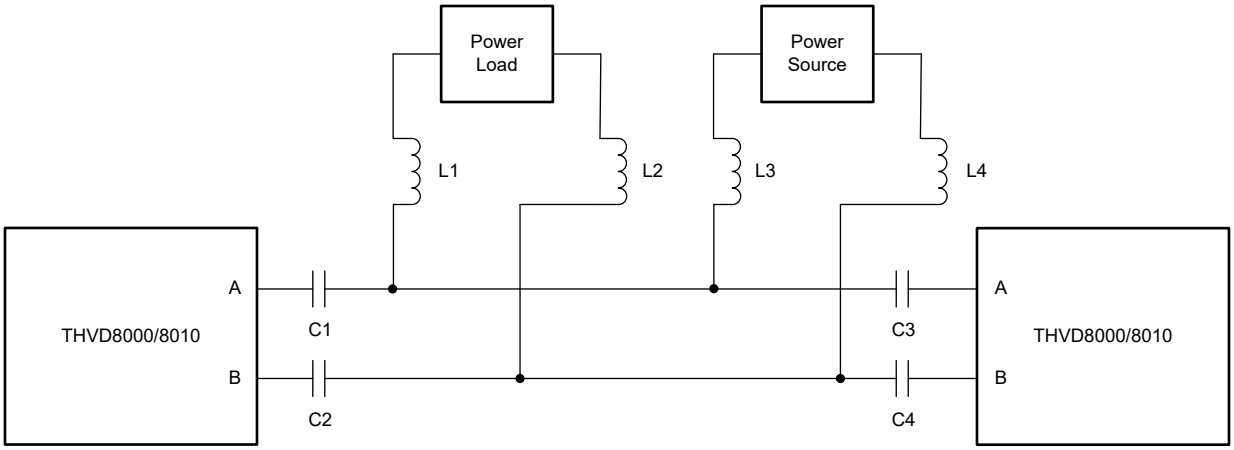

Figure 1-1. THVD80x0 Standard Approach with Two Nodes Shown

In the standard design process the THVD80x0 is assumed to see the power load and the power source as AC ground – this assumption is valid in DC power systems as most DC power sources have output bulk capacitance that filter the high frequency data signal from the THVD80x0 Device. An amended diagram with the *AC Ground* shown in Figure 1-2.

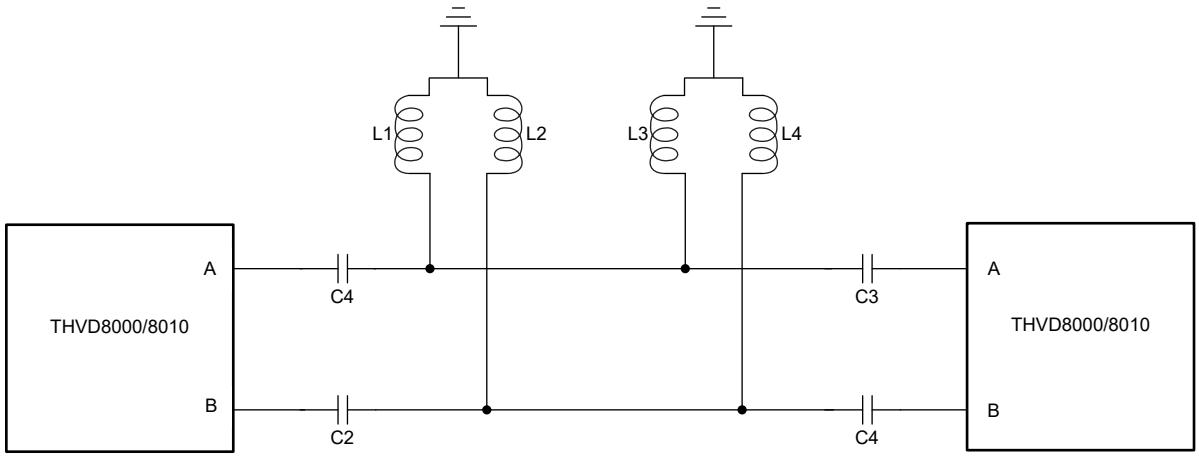

Figure 1-2. THVD80x0 Standard Approach, Including AC Ground, with Two Nodes Shown

Since PowerBus still relies on the RS-485 standard the impedance from either the *A* or *B* line to ground can be calculated with Equation 1 for terminated systems (assuming two 120 Ω terminations in the system) and Equation 2 for unterminated systems.

$$\frac{1}{\Sigma_2^N \frac{1}{Z_{in_i} + Z_{Ci}} + \Sigma_1^N \frac{1}{Z_{Li}}} + Z_{C1} \geq 375\Omega \tag{1}$$

$$\frac{1}{\Sigma_2^N \frac{1}{Z_{in_i} + Z_{Ci}} + \Sigma_1^N \frac{1}{Z_{Li}}} + Z_{C1} \geq 60\Omega \tag{2}$$

The first summation on the bottom left side is the input impedance plus series capacitance inductance on the either the A or B line. It starts at node 2, as node 1 is the transmitting node and can be excluded in this calculation, and counts all other nodes on the line (from 2 to N). The second summation is the effective

impedance of the inductors on the A or B line. The final term is the first series capacitance the transmitter sends its signal through and can be added to the rest of the impedance calculation. The input impedance for the THVD80x0 Family of Devices can be approximated to 96 KΩ and the capacitor impedance and inductor impedance are shown in Equation 3 and Equation 4 respectively.

$$Z_L = 2 \times \pi \times f_{mod} \times L \tag{3}$$

$$Z_C = \frac{1}{2 \times \pi \times f_{mod} \times C} \tag{4}$$

Where the modulation frequency is the frequency of the data signal set through a setting resistor on the THVD80x0 Family of Devices. It is easiest to have all inductors be the same value as well as all the capacitors having the same value. This simplifies the equations Equation 1 and Equation 2 to what is seen in Equation 5 and Equation 6 respectively

$$\frac{1}{\frac{N-1}{Z_C + Z_{in}} + \frac{N}{Z_L}} + Z_C \geq 375\Omega \tag{5}$$

$$\frac{1}{\frac{N-1}{Z_C + Z_{in}} + \frac{N}{Z_L}} + Z_C \geq 60\Omega \tag{6}$$

Capacitors should be designed to have a max impedance at the modulation frequency of 5 Ω whereas the inductors need to be designed around Equation 5 for terminated systems and Equation 6 for unterminated systems. The capacitor and inductor conditions are shown in equations Equation 7, Equation 8, and Equation 9 respectively.

$$C \geq \frac{1}{2 \times \pi \times f_{mod} \times 5} \tag{7}$$

$$L > \; = \frac{N}{2 \times \pi \times f_{mod} \times \left(\frac{1}{375 - Z_C} - \frac{N-1}{Z_C + Z_{in}}\right)} \tag{8}$$

$$L > \; = \frac{N}{2 \times \pi \times f_{mod} \times \left(\frac{1}{60 - Z_C} - \frac{N-1}{Z_C + Z_{in}}\right)} \tag{9}$$

The impact of the input impedance can be neglected in many applications – regardless of frequency as its impact is relatively small in low node count systems. The simplified equations are shown in Equation 10 and Equation 11 respectively.

$$L > \; = \frac{N}{2 \times \pi \times f_{mod} \times \left(\frac{1}{375 - Z_C}\right)} \tag{10}$$

$$L > \; = \frac{N}{2 \times \pi \times f_{mod} \times \left(\frac{1}{60 - Z_C}\right)} \tag{11}$$

Where the error between simplified equations in Equation 10 and Equation 11 and the full equations in Equation 8 and Equation 9 are given by Equation 12 and Equation 13 respectively.

$$Error = \left(\frac{1}{375 - Z_C} - \frac{N-1}{Z_C + Z_{in}}\right) \times \left((375 - Z_C) - \frac{1}{\frac{1}{375 - Z_C} - \frac{N-1}{Z_C + Z_{in}}}\right) \tag{12}$$

$$Error = \left(\frac{1}{60 - Z_C} - \frac{N-1}{Z_C + Z_{in}}\right) \times \left((60 - Z_C) - \frac{1}{\frac{1}{60 - Z_C} - \frac{N-1}{Z_C + Z_{in}}}\right) \tag{13}$$

A summary of percentage error when using the simplified equations compared the more correct equations are shown in Table 1-1. This is assuming capacitor impedance is 5 Ω and input impedance is 96 KΩ.

Table 1-1. Summary of Percentage Error with Simplified Equations

|Error Percentage|	Number of Nodes (Terminated)	Number of Nodes (Unterminated)
<0.1%	Not Possible	2
<0.5%	2	9
<1%	3	18
<5%	13	88
<10%	26	175

With a basic understanding of the design process and the assumptions (along with their justification) for DC power systems – how to modify the system to support AC power can now be explained.

2 Modifying THVD80x0 Design Process for Lower Voltage (≦36 V) AC Systems

In the standard design process, it is assumed that the power source/loads have bulk capacitance associated with them so that the THVD80x0 Family of devices will see the inductor connect to ground instead of the power tree. In AC systems this bulk capacitance is often not included and if the standard design process is followed without modification there will be the potential for a high frequency signal on the power line or the power load – with the fundamental frequency of this signal being *fmod.* This violates one of the intentions of the use case by not blocking the modulated data signal from the power source and power loads. Luckily this can be fixed by adding a single capacitor at each power node from the sources output to ground or have a parallel capacitor w.r.t. to the power load. This capacitor has two key care abouts when implementing it into the system: Loading on AC power source and reduction in THVD80x0 Signal at power nodes.

The first care about is stress to the AC power source – as adding a capacitor on the source could potentially attenuate the power signal too much for power delivery to occur effectively. What this implies is that the capacitor across the power load/power source needs to be high impedance at the power line frequency (typically 50 Hz - 60 Hz) but low impedance at the modulation frequency of the data stream from the THVD80x0 device. To illustrate the design process the following is an example of how to determine the maximum capacitance.

Example 2.1: *10 Node System, 1 Source and 9 Loads with each load requiring 500 mA of current, VAC = 36 V at 60 Hz with a max current of 5 A possible.*

1. Calculate additional current budget by subtracting the summation of currents from all power loads from the max current. In this example that would be 5 A – 9 loads × 500 mA each – so there is an additional 500 mA possible out of the source.
2. Calculate the current per node by dividing the additional current budget by the total number of nodes. In this example that would 500 mA/ 10 Nodes so each node can sink an extra 50 mA through a filtering capacitor.
3. Use the source's peak voltage and divide by the calculated current in step 2 to determine the minimum impedance that will be required to prevent the AC source from sagging due to overcurrent. In this example the minimum impedance that can be added to the power nodes would be 36 V divided by 50 mA which equals 720 Ω (in parallel with the source or load).
4. Convert the minimum impedance to the maximum capacitance by finding the capacitor value that has an impedance value equal to what is found in step 3. For this example, it would be 1 divided by 2 × π × 60 Hz × 720 Ω which give the max capacitance value of approximately 3.68 uF.

With a boundary on capacitance decided on the next step is to implement that capacitor – as the maximum allowable value will provide the most attenuation to the data signal at the power nodes. This step is best done with a Spice based simulation program as systems with many nodes can end up being very time consuming if calculating by hand. Simulation setup and an example is detailed in the next section: *Simulating the New System*.

With the main modification out of the way – there are a couple other considerations that are added on when using an AC source. The first being that in DC systems the inductor is seen as a small resistance (DCR) and doesn't have an active reactant term essentially creating a low impedance path at DC. With an AC signal – there is going to be reactant added to the impedance of the inductor as seen by the power source. So, when determining needed power source and load voltages – the attenuation of the power path cannot just include the DCR and trace impedance for its attenuation calculations, but must also include the reactant term based on the power source frequency. The best inductor value to choose is the minimum inductance value per node – as anything higher is unnecessary and would attenuate the power sources signal. The second consideration is the coupling capacitor between the THVD80x0 and the shared power/data bus. In DC systems the power source sees this as an open circuit – but with an AC source it is no longer high impedance. The minimum capacitance is the capacitance that has an impedance magnitude value of 5 Ω at modulation frequency will attenuate the power signal the most while still abiding by the requirements of the data bus. Since there is going to be AC leakage on the data node the need for a protection diode between A and B pins of every THVD80x0 device is present as anything out of the 12 V to -7 V range can cause damage to the THVD80x0 device. This protection diode is common, and often suggested, in most Powerbus and RS-485 application but it is even more so with an AC source as the capacitors between the communication node and the shared bus will not fully block the power signal.

3 Simulating the New System

To show how the simulation file should be set up two different examples are going to be shown to clarify the process as well as show results. A list of assumptions that are used through the simulation process are shown below.

1. Assumption 1: The system is very linear under normal operating conditions so superposition is used to remove the power source from the analysis – since it the noise on power nodes is independent of the source. This is valid as during normal operating conditions the THVD80x0 Device Family operates in a very linear manner.
2. Assumption 2: The THVD80x0 device is replaced with a differential source of value 1V so it easy to scale up to what the actual output voltage is in the specific system. This assumes the parasitics of the THVD80x0 output circuit doesn't greatly affect the noise on the power nodes.
3. The negative terminal of the source is grounded as Simulations tend to have issues with floating nodes. However, the Output differential voltage remains the same.
4. Assumption 4: The AC power source has contact resistance of 50 mΩ on both the positive and negative terminals. This could be smaller or larger so a small resistance was used to model the contact resistance.
5. Assumption 5: The THVD80x0 Devices have an input impedance, when in receive mode, of a constant 96 KΩ. This will vary based on input voltage but 96 KΩ is a common stand-in for 1/8 Unit Load Devices Input Impedance.
6. Assumption 6: Transmission Line and High Frequency Circuit Considerations are neglected in the simulation as through proper design it should only add a small amount of attenuation to the signal depending on distance.

Example 3.1: *2 Node System; 36VAC @ 60Hz that can provide 4A of current, Power load is requesting 3.6A, Modulation Frequency = 125KHz, 120 Terminations Used.*

1. Assume capacitor between communication node and shared power/data bus has an impedance at the modulation frequency of 5 Ohms. Using Equation 7 yields C ~ 255nF.
2. Since this is a low node count system (2 Nodes) Equation 10 can be used and it yields a minimum inductance value of ~942uH per node.
3. Calculate extra current budget by subtracting requested current from max current possible from source. For this example, that would be 4 – 3.6 = 400 mA of extra current available for filter caps.
   a. As a note all 400 mA need to be consumed by the filtering capacitor – but this will provide the lowest impedance possible for the THVD80x0 Device.
4. Calculate extra current per load by dividing available current by the number of nodes – so in the example it would be 400 mA / 2 which yields 200 mA per node.
5. The minimum impedance that this filter capacitor can be is the source voltage peak divided by the maximum current for the filtering capacitor in each node – so it would be 36 V/200 mA which yields 180 Ω
6. Find the capacitance that has an impedance magnitude of 180 Ω at power source frequency – for this example that would be approximately 14.7 4uF.:

Figure 3-1 is the simulation profile to see system impact without the AC filtering caps added.

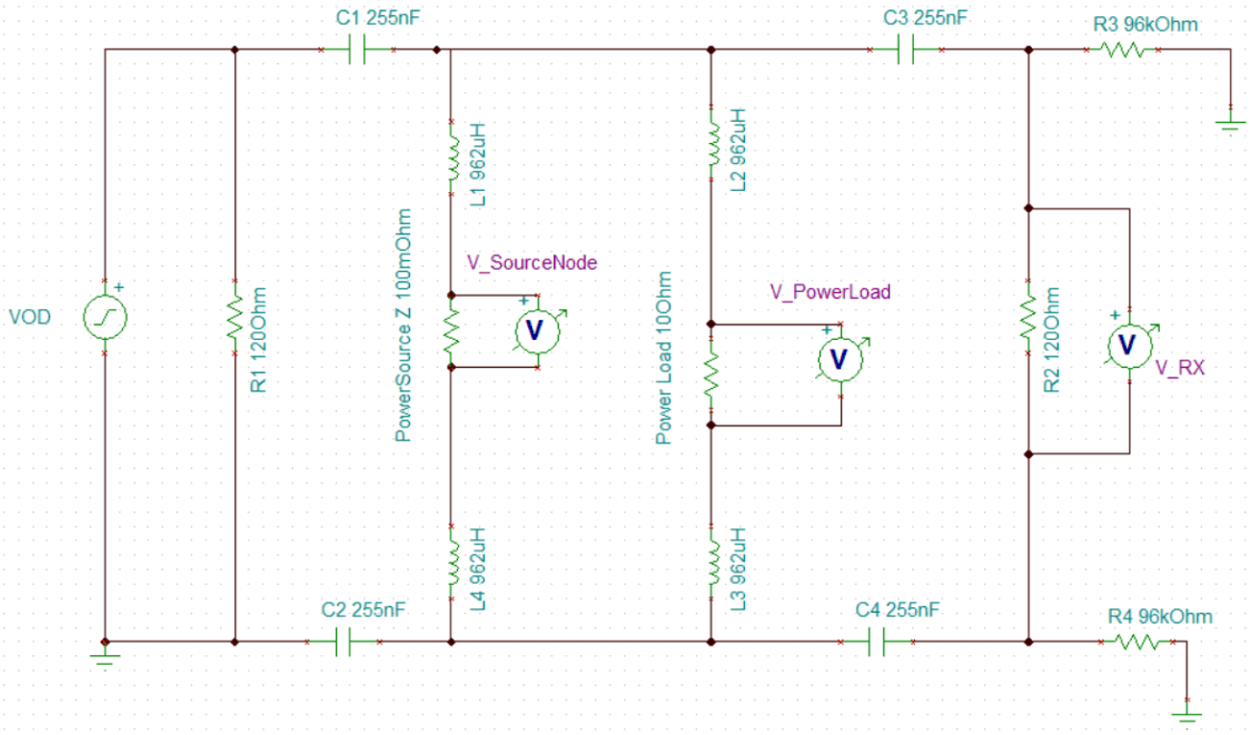

Figure 3-1. Simulation Profile, Without Filtering Capacitors

Without adding the filtering capacitor, the power nodes have more data signal leaking into them.

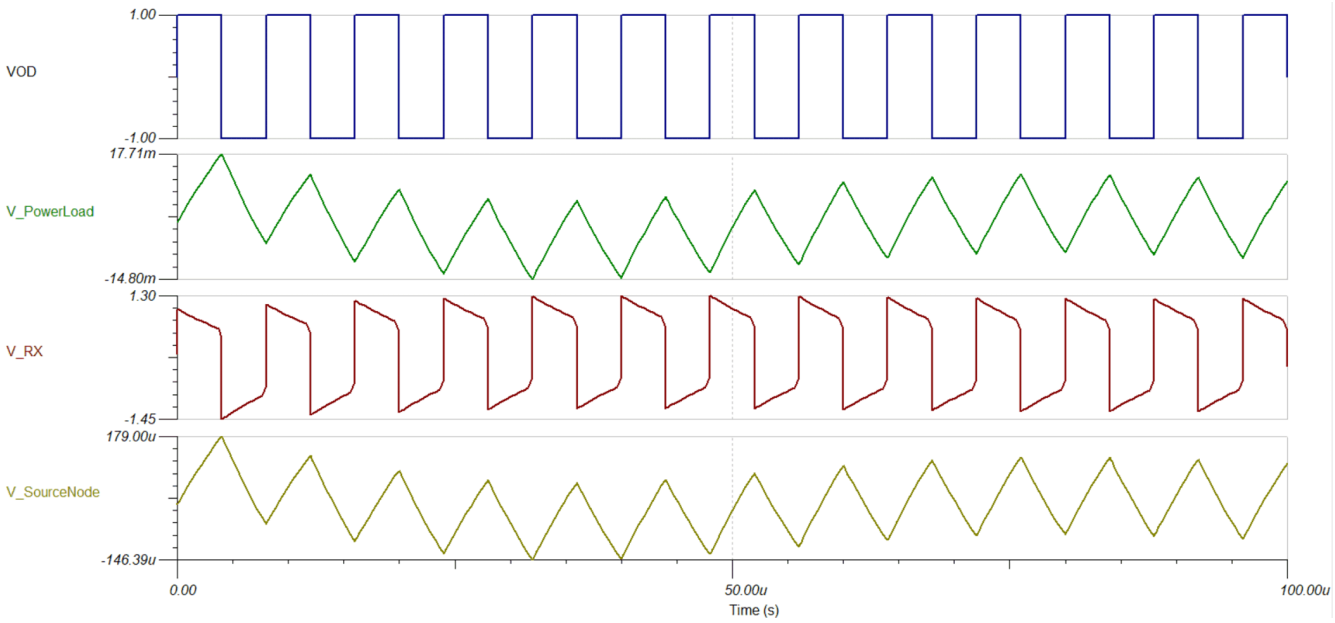

Figure 3-2. Simulation Results, Without Filtering Capacitors

The green signal is the modulated data stream present at the power node. It steadies out at a ripple magnitude of approximately 12 mV – or 1.2% of the data signal is present at the power node. Since the VAC source was shorted for the simulation only the contact impedance remained and shown with the yellow signal, however, since this was very small, the noise on the source node is also small by about a factor of 100 lower than seen on the power load. The received voltage is not being attenuated but has a small gain due to the passive network at 125 KHz.

Figure 3-3 is the simulation profile with the filtering capacitor added.

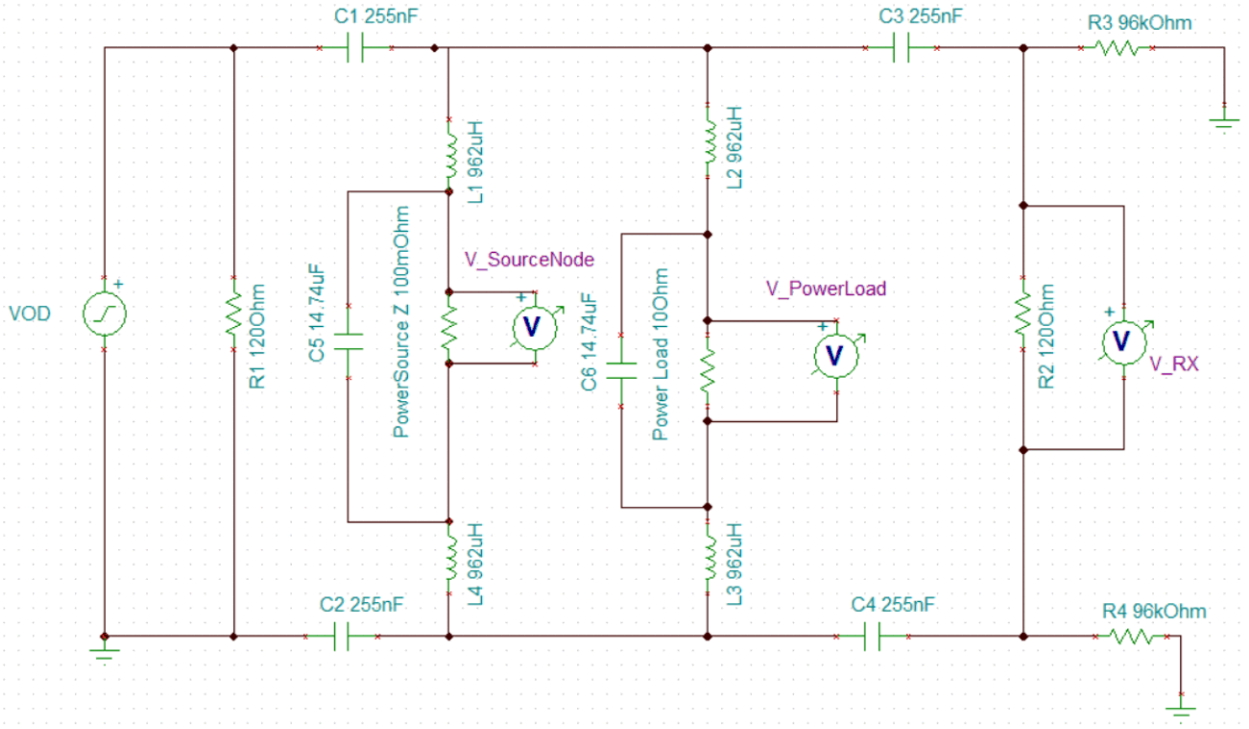

Figure 3-3. Simulation Profile, With Filtering Capacitors

Due to the additional capacitance the settling time has increased so a 500 us simulation was used compared to the 100 us of the first case.

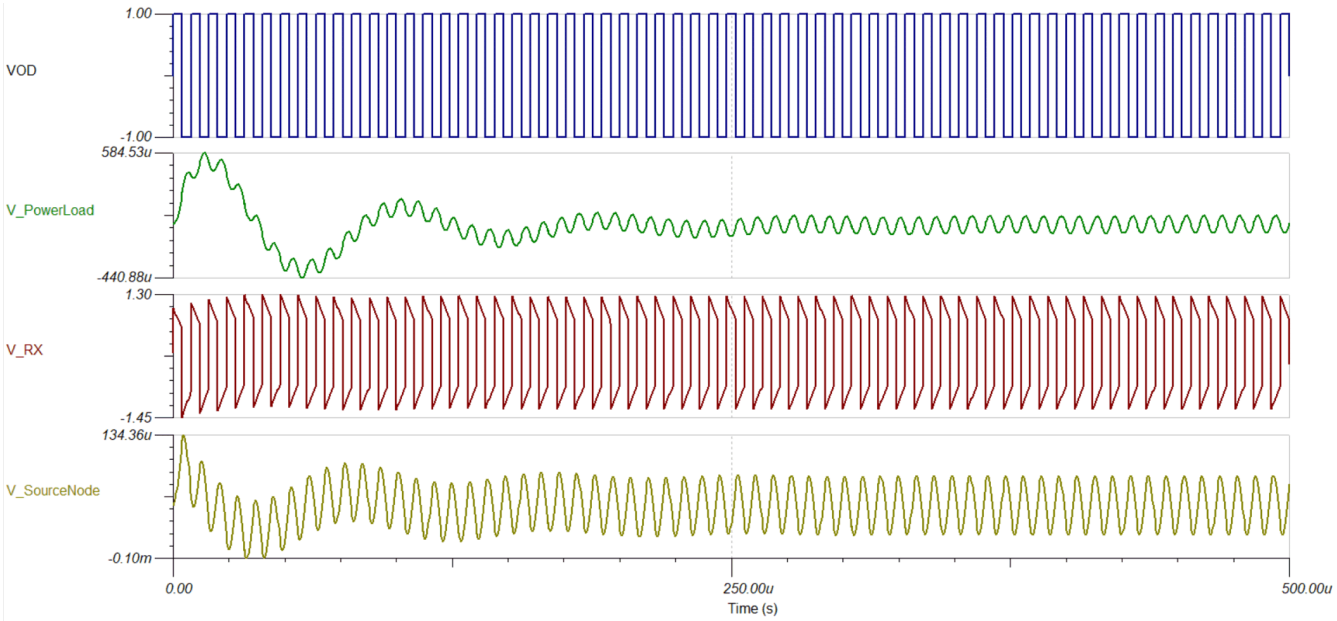

Figure 3-4. Simulation Results, With Filtering Capacitors

The peak signal on the power load is now ~585 uV or 0.0585% of the differential signal. It does take longer to steady out but when it reaches steady state the voltage on this node is about 70 uV or 0.07% of the differential signal. The source node also sees a slight improvement, but this was already small to begin with due to the analysis using superposition to short the AC source.

Example 3.2: *4 Node System; 24VAC at 50 Hz that can provide 5A of current, Power load 1 is requesting 3.6 A, Power load 2 is requesting 0.75 A, and Power load 3 is requesting 0.55 A, Modulation Frequency = 500 KHz, 120 Ohm Terminations Used.*

Using the same process as Example 3.1:

1. Equation 7 yields a capacitor value of ~64nF.
2. To keep error low since this system has > 3 nodes equation 1.8 is used for the inductor value which yields a value of approximately 119 uH.
3. There is a total current possible of 5A with 3 sources requesting a total of 4.9 A which leaves 100 mA left over.
4. Since there are 5 nodes each node can sink another 20 mA without overstressing the AC source.
5. The minimum impedance is the source voltage divided by the extra current per node so 24 V/0.02 A which yields 2.4 KΩ.
6. Converting that impedance to a capacitance value yields approximately 1.33 uF
7. Setup the simulation as shown in Figure 3-5.

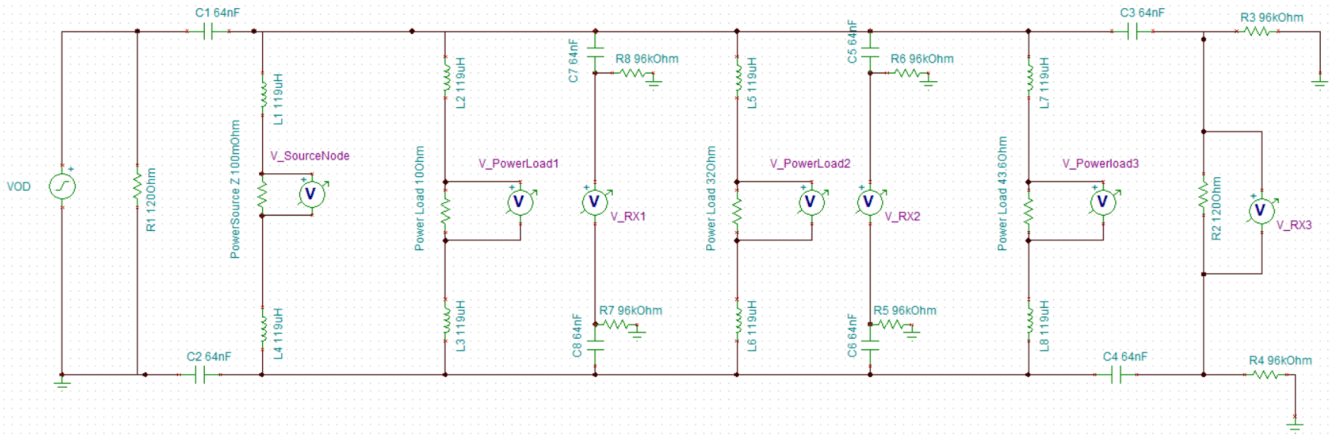

Figure 3-5. Simulation Profile, Without Filtering Capacitors

If there are difficulties running as a transient simulation try to run as a steady state simulation.

Since only two nodes are terminated the other device are essentially CR filters to ground. The simulation results without the capacitor are shown in Figure 3-6.

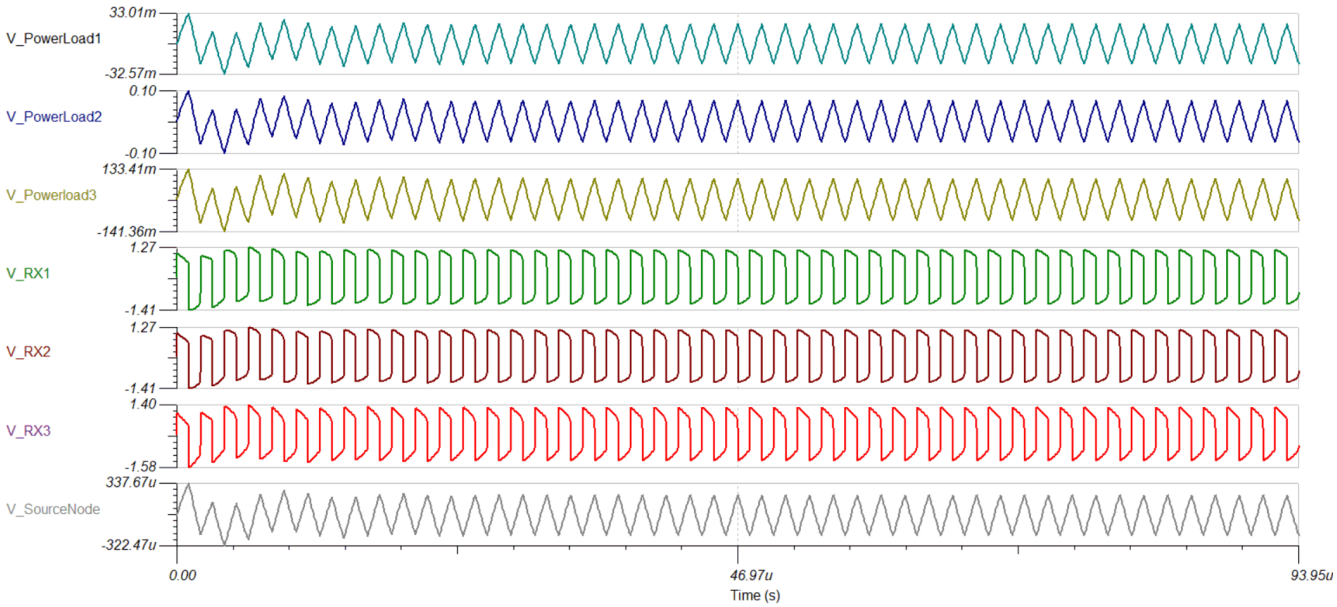

Figure 3-6. Simulation Results, Without Filtering Capacitors

The data stream leaks into the power load nodes depending on how resistive the load is. In this system power node 1 peaks around a magnitude of 3.3% of the differential voltage signal at this node and approaches a steady state magnitude of 1.8% to 2% of the differential voltage signal. Power node 2 peaks at 10% of the data signal and approaches a steady state magnitude of 6.4% to 6.6%. Power node 3 peaks at approximately 13% of the data signal and approaches a steady state magnitude of 8.3% to 9% of the differential voltage signal.

With the baseline approximated – the improvement can also be approximated by adding a 1.33 uF capacitor across each power load and the power source. Which yields the following simulation profile and results.

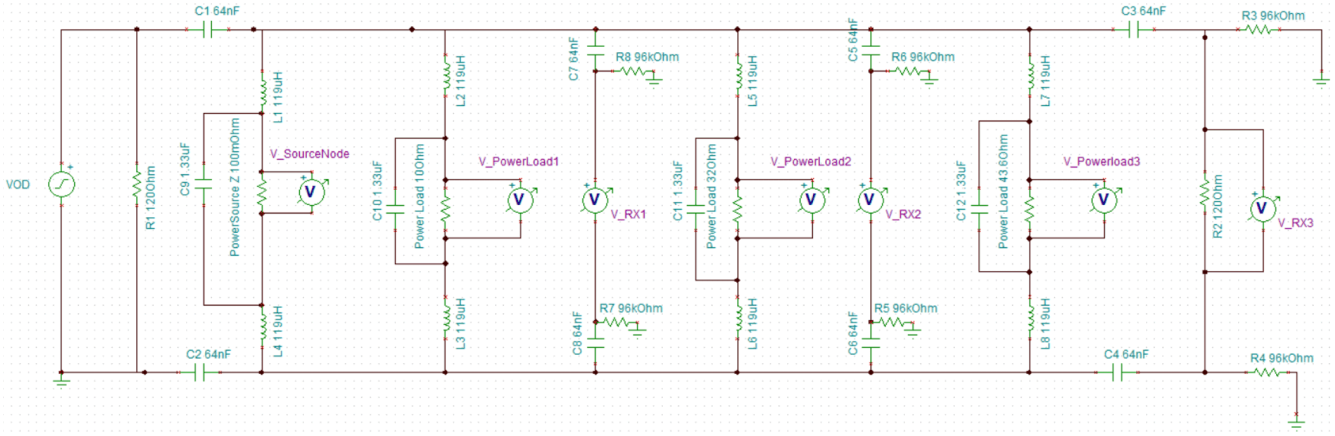

Figure 3-7. Simulation Profile, With Filtering Capacitors

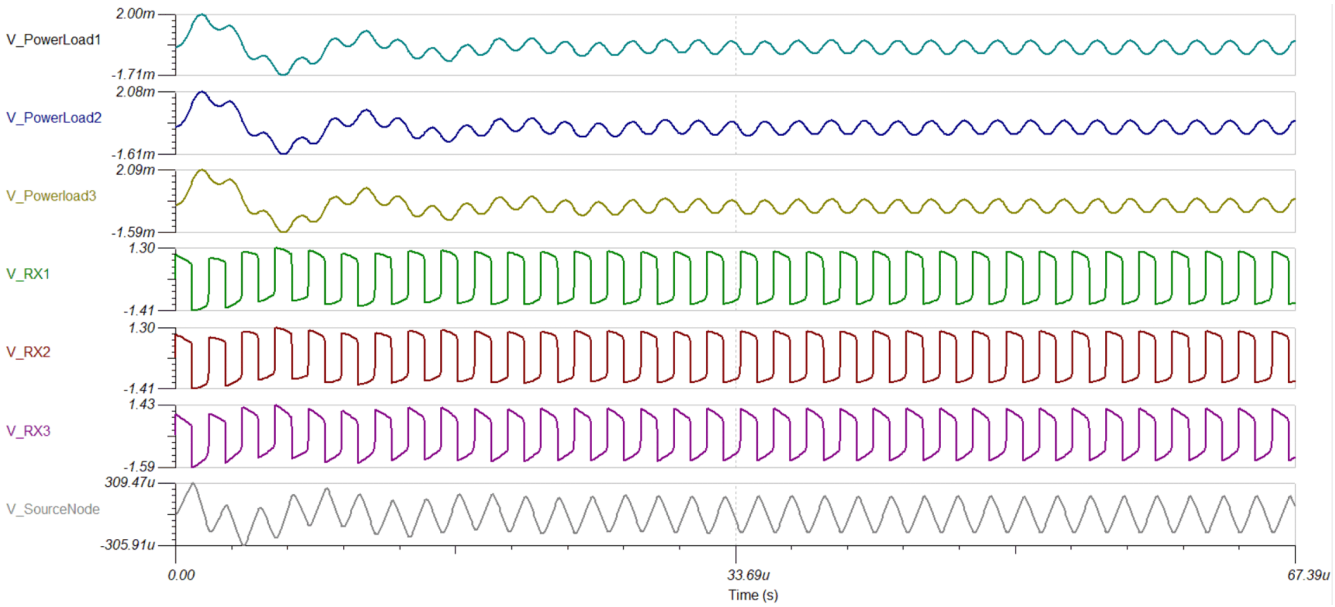

Figure 3-8. Simulation Results, With Filtering Capacitors

Where power load 1 now peaks at ~0.2% of the incoming differential signal and approaches a steady state magnitude of 0.04%. Power load 2 peaks at 0.208% of the incoming signal and approaches a steady state magnitude of 0.04% - the same as power load 1. Finally, power load 3 peaks at 0.209% of the incoming signal and approaches a steady state of ~0.04% the same as the first two loads.

4 Conclusion

Using the same process any low voltage (<=36 V), low frequency (<=60 Hz), AC supply can be modified to support a shared data and power bus by using a filtering capacitor on all power nodes. This will create the condition in which the THVD80x0 devices assumes to be true – the inductors are AC grounded – with this filtering capacitor the inductors are essentially AC grounded as the voltage will be attenuated by the inductors not over the power source or load. Once this filtering capacitor is added the design process is the same as one would use for DC power systems.

5 References

- Texas Instruments, *THVD8000 Design Guide* application note.
- Texas Instruments, *THVD8000 EVM User's Guide* user's guide.
- Texas Instruments, *THVD8000 RS-485 Transceiver with OOK Modulation for Power Line Communication* data sheet.
- Texas Instruments, *THVD8010 RS-485 Transceiver with OOK Modulation for Power Line Communication* data sheet.
- Texas Instruments, *Using THVD80x0 Devices to Communicate Over an AC Outlet* application note

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