User's Guide

ISO672x Dual-Channel Digital Isolator Evaluation Module

ABSTRACT

This user's guide describes the ISO672x dual-digital isolator evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the TI dual-channel digital isolators in an 8-pin SOIC package.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0-V to 5.5-V recommended operating range.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

This user's guide describes EVM operation with respect to the ISO672x dual-channel digital isolators. However, the EVM may be reconfigured for evaluation of any of TI's dual-channel digital isolators in an 8-pin SOIC package. This guide also describes the available channel configurations within the ISO6721 family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2 Overview

The ISO672x is TI's new digital isolator family capable of galvanic isolations up to 3000 V_{RMS}. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO672x digital isolators have logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3 Pin Configurations of the ISO672x Dual-Channel Digital Isolators

Figure 3-1 shows the ISO672x dual-channel digital isolator pin configurations.

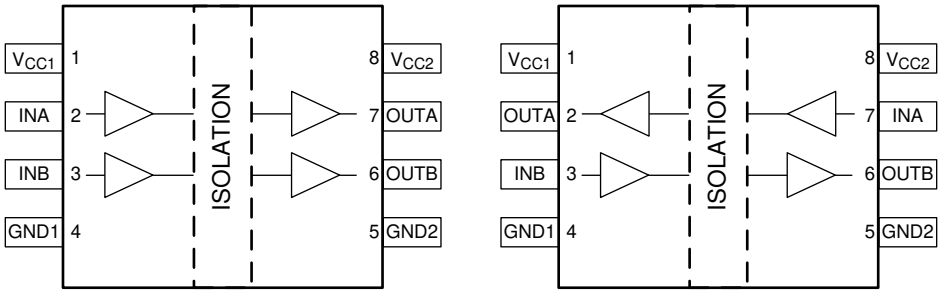

Figure 3-1. Dual-Channel Digital Isolator Pin Configurations

4 ISO6721 Board Block Diagram and Image

Figure 4-1 shows the board configuration for evaluation of the ISO6721 dual-channel digital isolator.

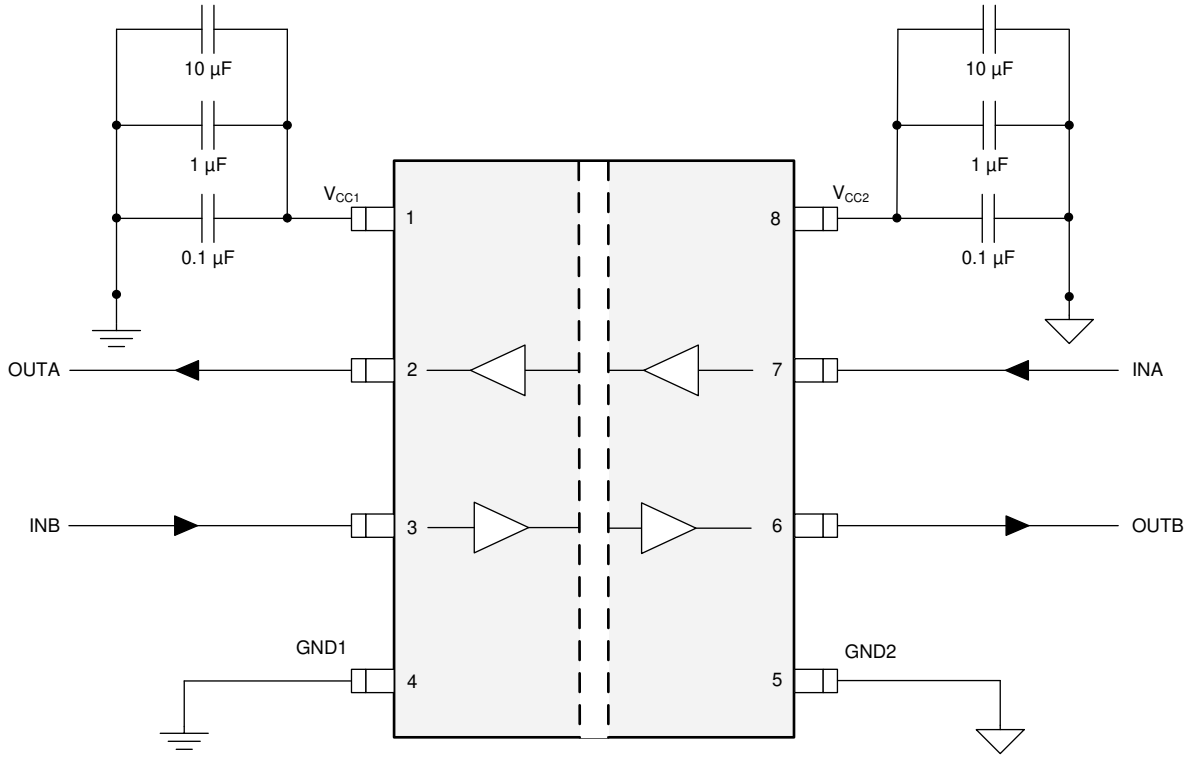

Figure 4-1. ISO6721 EVM Configuration

Figure 4-2 shows the 3D diagram of the EVM.

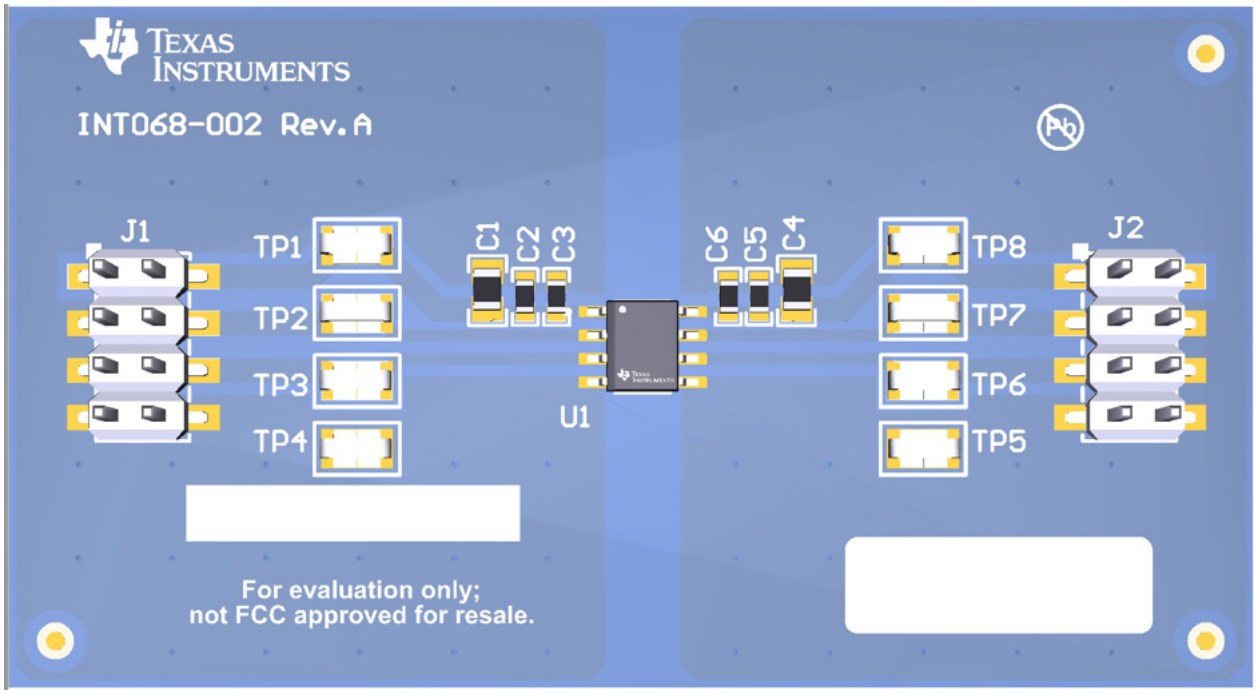

Figure 4-2. ISO6721DEVM 3D Diagram

5 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5-1 shows the configuration for operating the ISO6721 dual-digital isolator EVM using two power supplies.

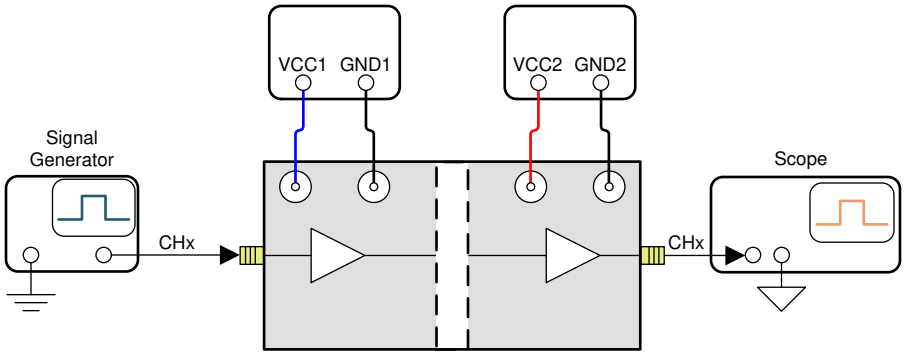

Figure 5-1. Basic EVM Operation

Figure 5-2 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

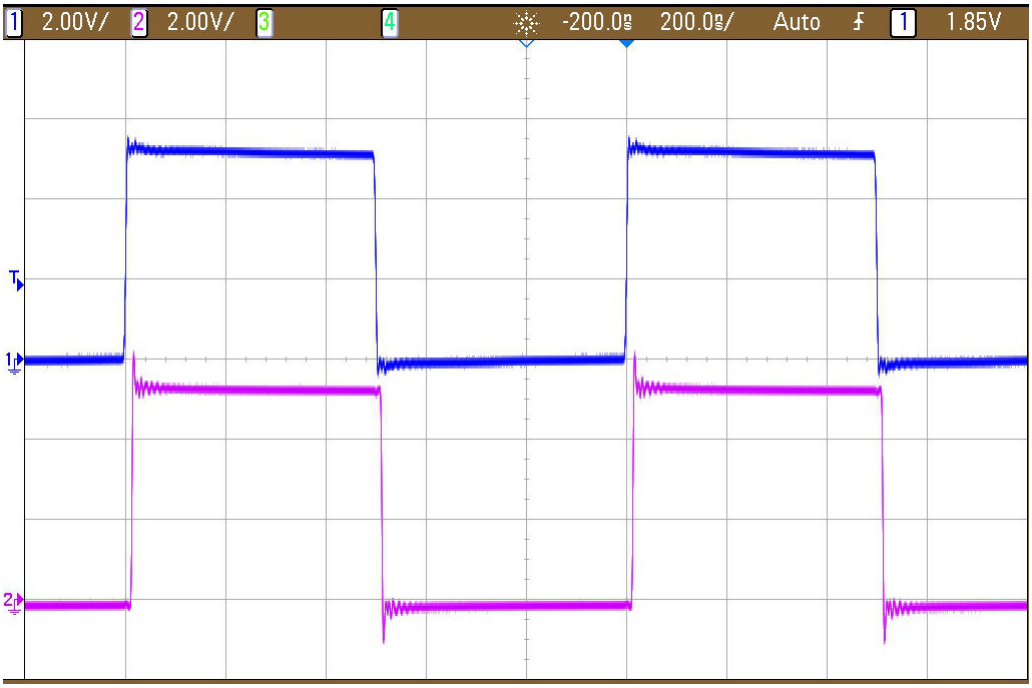

Figure 5-2. Typical Input and Output Waveform

6 Bill of Materials

Table 6-1 shows the bill of materials (BOM) for this EVM.

Table 6-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Quantity
1	C1, C4	CAP, CERM, 10 µF, 35 V, ± 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	2
2	C2, C5	CAP, CERM, 1 µF, 50 V, ± 10%, X5R, 0603	MuRata	GRM188R61H105KAALD	2
3	C3, C6	CAP, CERM, 0.1 µF, 25 V, ± 5%, X7R, 0603	AVX	06033C104JAT2A	2
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
5	J1, J2	Header, 100mil, 4x2, Gold, SMT	Molex	15910080	2
6	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test Point, Miniature, SMT	Keystone	5019	8
7	U1	Robust EMC, Low Power, Dual-Channel Digital Isolators, D0008B (SOIC-8)	Texas Instruments	ISO6721BQDRQ1	1

7 EVM Schematics and Layout

The ISO6721DEVM is designed to accommodate any of the ISO672x dual-channel devices in an 8-pin package. To evaluate any of the ISO672x dual-channel devices in an 8-pin package, replace ISO672x with the device of interest on the ISO6721DEVM PCB. No other component requires any modification. Figure 7-1 shows the ISO672x EVM schematic and Figure 7-2 shows the printed-circuit board (PCB) layout.

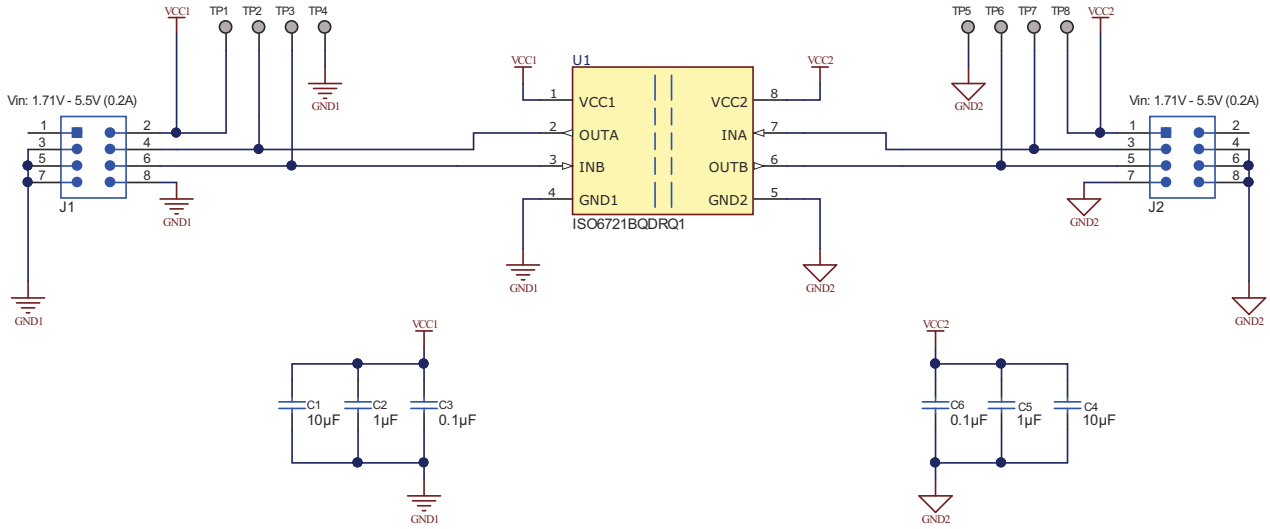

Figure 7-1. ISO6721DEVM EVM Schematic

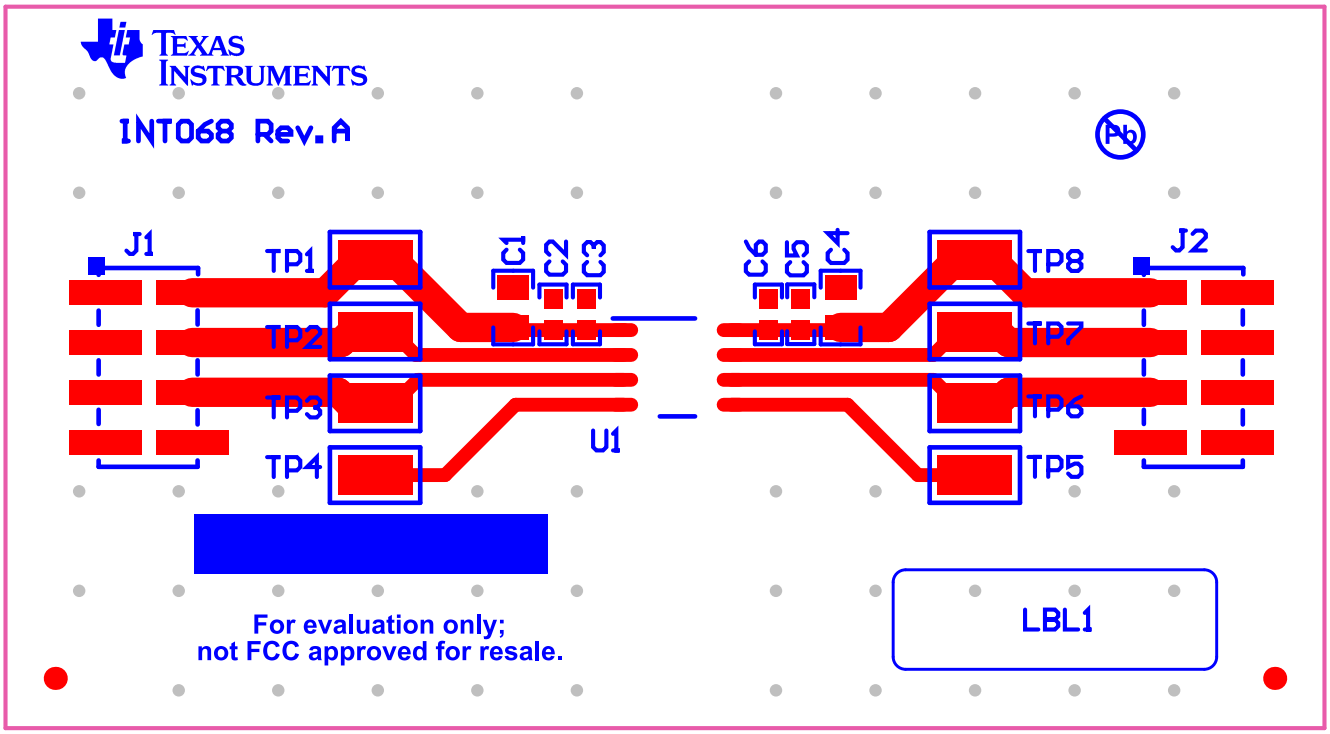

Figure 7-2. PCB Layout

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265