ERRATA FOR THE 1394 PHYSICAL LAYER DEVICES

(TEXAS INSTRUMENTS' DISCRETE PHY DEVICES AND INTEGRATED DEVICES)

Problem:

There is a slight potential for PHY lock-up in a receiving node (this includes a node that is repeating) when a peer node is powered off or unplugged while transmitting data to the receiving node.

Description:

If node B is unplugged or powered down while it is transmitting, its peer node A could see corrupted data on its port's twisted pair lines during the unplug or powerdown sequence. A rare condition has been discovered in which the node A PHY has the potential to enter a lock-up state after receiving a particular sequence of corrupted signals on the twisted pairs during unplug or powerdown of node B as node B is transmitting. Node A does see the bus reset event caused by the unplug or powerdown of node B but does not complete the collection of valid SelfID's.

When in this state, the node A PHY is unaware of and does not respond to the bus reset caused by the plug-in of a new node C (or to the power-up of node B), this causes the just-connected node B or C to continuously issue bus resets. This causes the entire network to cease to function until the node A PHY is hard reset or disconnected from the network.

This condition has never been reported in normal use; rather, it was observed in rigorous lab testing. All future releases of these devices shall have this issue fixed.

Software Workaround:

The lock-up state in node A is cleared only by a hard reset of the PHY. Software may detect and recover from this condition by issuing a hard reset to the PHY device through a register write. Software normally handles all 1394 bus resets. When a bus reset interrupt occurs, software should check for a "SelfID complete" interrupt to signal normal completion of the bus reset. If a "SelfID complete" interrupt does not occur within 1.5 ms (worst case time), an error condition is signaled, and software should reset the PHY via the software hard reset bit (SWR, register page 7, address 1110, bit 0) described in the datasheet. This will completely reset the device, which clears the lock-up condition, causes a bus reset, and results in normal operation. If additional bus resets are received during the 1.5 ms timer, the PHY has not entered the lock-up state.

If external nodes suspect that node A has entered a lock-up state, there is no software workaround for these other nodes to perform to reset the PHY in node A. The node whose port is connected to a locked-up PHY port may disable it's connected port to isolate the locked-up PHY from the rest of the bus.

TI shall provide example code for implementation of this workaround upon request.

Hardware Workaround:

The lock-up state is cleared only by a hard reset of the PHY. This can be done electrically by asserting the /RESET pin and releasing it, or by asserting the PowerDown (PD) pin and releasing it. On a system with only a passive reset circuit on the /RESET pin and a fixed input to the PD pin, power cycling of the device is required to electrically reset the PHY.

This document contains corrections and additions to the following device datasheets: TSB41AB1 (TI Literature Number SLLS425), TSB41AB2 (Lit. #SLLS424B), TSB41AB3 (Lit. #SLLS418D), TSB41LV04A (Lit. #SLLS379A), TSB41LV06A (Lit. #SLLS363A), TSB43AA22 (Lit. #SLLS358B), TSB43AA82 (Lit. #SLLS461B), TSB43AA82A (Lit. #SLLS512), TSB43AB21 (Lit. #SLLS503), TSB43AB22 (Lit. #SLLS436).

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